

Article

Impact of Busbar Resistance and Series–Parallel Topology on Current Inhomogeneity and Safety Limits in Battery Packs

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Highlights

1. A matrix model built from the pack topology gives the current in every cell of a pack of arbitrary size.
2. Identical parallel cells reach 1.64 times the mean current through the interconnection alone.
3. The current-supplying busbars dominate the imbalance; internal connections are secondary.
4. Pack-level voltage monitoring cannot detect the overcharge of the most loaded cell.
5. Design maps give the busbar resistance a given pack layout can tolerate.

Abstract

Current distribution in serial–parallel battery packs is commonly assumed to be uniform in the absence of cell-to-cell variations. However, in practical systems, the electrical topology and finite resistance of current-collecting busbars can introduce significant inhomogeneities even when all cells are identical. In this work, a matrix-based modeling framework is developed to analyze the current and voltage distribution in large battery packs with arbitrary serial–parallel configurations. The results reveal that the resistance of current-supplying busbars plays a dominant role in shaping current distribution, leading to pronounced current imbalance that increases with both resistance and operating C-rate. To quantify this effect, a current non-uniformity factor is introduced and used to define an illustrative criterion for acceptable operation. Based on this metric, together with a maximum-cell-voltage constraint, design maps are constructed to identify operating regions that are acceptable or critical with respect to current overload and localized overvoltage as a function of busbar resistance and charging rate. The analysis further demonstrates that topology-induced current inhomogeneity can lead to cell-level voltage divergence and localized overcharge under high-current operation. Such local effects may remain hidden when only the pack voltage or the voltage of a series-connected cell group is monitored, because conventional battery management systems (BMSs) typically do not resolve individual cell currents or local voltage drops within parallel-connected cell groups. The proposed approach enables the derivation of design-oriented constraints linking electrical performance to physical parameters such as busbar resistance and cell spacing. The resulting design maps



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provide a practical tool for battery pack engineering, enabling the determination of the maximum allowable busbar resistance or operating current to ensure safe, homogeneous pack operation.

Keywords: battery pack; serial-parallel configuration; design map; safety analysis; current inhomogeneity; busbar resistance

1. Introduction

Battery packs used in electric vehicles and stationary applications consist of a large number of cells connected in series and in parallel to meet the required voltage, capacity, and power [1–4]. While such configurations enable high energy and power, they also introduce complex internal current and voltage distributions that are not directly observable at the pack level [5].

Non-uniform current distribution within a battery pack can lead to significant safety and performance issues, including local cell overloading, accelerated degradation, and operation closer to voltage or electrode-potential limits [6]. In practical BMS architectures, the voltage of each series-connected cell group is often monitored [7,8]. However, this measurement typically represents the equivalent terminal voltage of a parallel cell group or module and does not provide direct information on the current carried by each individual cell within that group [9]. Therefore, intra-parallel current redistribution caused by finite interconnection and busbar resistances may remain unresolved, even when the measured series-cell-group voltage and pack current are within their nominal limits [10]. In a real pack, current enters and leaves the parallel group through finite-resistance busbars and connectors, so cells at different positions within the same group experience different local potentials, polarization voltages, and currents despite being nominally connected in parallel [11]. These local differences can accumulate into SoC deviations and may drive individual cells closer to overcharge, overdischarge, or lithium plating conditions than suggested by the group-level voltage measurement [1,12,13].

The risks associated with overcharge, over-discharge, and lithium plating arise from distinct degradation processes. A cell at a higher terminal voltage and a higher local current has a more negative anode potential, which enables lithium plating [14]; the deposit consumes cyclable lithium and can compromise separator integrity [15]. Sustained local overcharge also accelerates electrolyte oxidation and gas generation, and fire risk rises with the state of charge a cell actually reaches [16,17]. On discharge, cells taken to low potentials risk current-collector dissolution and subsequent internal short circuits. All of these processes release heat locally, so an electrically non-uniform pack becomes thermally non-uniform [18,19].

Temperature is the established indicator for these hazards and has been studied extensively. The present work approaches the same question from the electrical side. Divergence in current and voltage between nominally parallel cells precedes the thermal signature: it is the cause rather than the consequence, it is set by the interconnection design, and it can be evaluated for a candidate layout before a module is built [20,21]. The framework therefore provides a complementary, design-stage safety indicator, identifying the conditions under which the above mechanisms become relevant rather than resolving the mechanisms themselves.

Cell-to-cell variability in battery packs arises from manufacturing tolerances, aging, temperature gradients, and interconnection resistance. Manufacturing tolerances introduce initial variations in capacity and internal resistance, which may evolve during aging because

cells carrying higher currents degrade more rapidly [22,23]. Marlow et al. reported that cycling cells with deliberately induced start-of-life deviations shows total capacity fade and impedance growth converge due to different cell currents, with cells experiencing higher current undergoing accelerated degradation [24]. Temperature gradients further modify cell resistance and current sharing [25,26]. Unlike these cell-specific and time-dependent variations, interconnection resistance is design-dependent and determined by the busbar and connector geometry. It cannot be eliminated through cell sorting or balancing and systematically biases the current towards cells closer to the current feed. Previous studies have shown that interconnection resistance and the number of parallel-connected cells affect current non-uniformity more strongly than capacity variation. The present work therefore isolates the contribution of interconnection resistance and quantifies its effect on cell-level current distribution.

Although the electrical behavior of series–parallel systems is governed by well-established circuit laws, existing studies often focus on cell-level modeling or assume idealized, homogeneous pack configurations [26–28]. Bruen et al. studied parallel-connected lithium-ion cells. They found that a 30% impedance difference can cause a 60% difference in peak cell current, leading to pronounced energy imbalance and non-uniform aging within the module [29]. Liu et al. studied the combined effects of cell-to-cell variations, thermal gradients, and interconnects, and reported that cells located closer to load points experience systematically higher currents and accelerated degradation, demonstrating that pack-level layout and resistances strongly shape internal current distributions [30]. Hosseinzadeh et al. studied a generic 1S–15P module. They showed that the number of parallel cells and interconnection resistances are the dominant factors in current inhomogeneity, whereas capacity variation has a comparatively minor effect [12]. Yu et al. reported that different pack configurations and module collector positions lead to different equivalent connection resistances and found that symmetric, multiple collectors significantly improve current homogeneity in edge modules [31]. Kim et al. studied various module topologies and showed that cross-contacting terminals and cross-connectors markedly reduce the impact of connection resistance on cell-to-cell variation, increasing cycle life by more than a factor of four and suppressing overdischarge in individual cells [32]. Ren et al. reported that practical busbar geometries, including finite-resistance current collectors, asymmetric current-feeding locations, and non-uniform interconnection paths, can create cells with locally higher current and lower anode potential during fast charging, thereby increasing the risk of lithium plating and underscoring the safety relevance of interconnection design [20]. Despite these advances, it remains unclear, in a general quantitative sense, which specific interconnection resistances in large series–parallel packs play a dominant role and which have only a minor impact.

The main contributions of this work are as follows: (1) the development of a generalized matrix-based modeling framework for efficiently computing current and voltage distributions in series–parallel battery packs of arbitrary size; (2) the identification of the current-supplying busbar resistance as the interconnection parameter that governs current inhomogeneity, quantified across its design range, the internal interconnections alone leaving the distribution uniform; (3) the derivation of actionable design guidelines that reveal a trade-off between safety and charging performance, enabling targeted optimization of battery pack architectures.

The framework is applied to an industrially relevant case study based on a commercially available 36-cell cylindrical battery module. To focus on this dominant distributed-parallel-connection effect, the model is parameterized using a representative 9-cell parallel subgroup, while retaining the option to connect multiple modules in series at the pack level. The case study serves as a realistic demonstrator for assessing how finite busbar and inter-

connection resistances affect current distribution, local cell voltage, and design limits, and for identifying the dominant and secondary pathways that govern current inhomogeneity.

The remainder of the paper is organized as follows. Section 2 describes the commercial cell and the module used as the case study, together with the resistances that define its interconnection. Section 3 derives the matrix formulation of the network, its assembly from the pack topology, and its numerical solution. Section 4 reports the current and voltage distributions, the design maps that follow from them, and the associated ohmic losses. Section 5 states the conclusions and the limits of a purely electrical model.

2. Case-Study Battery Module and Pack Configuration

2.1. Commercial Cell and Case-Study Module

The module is built from commercially available 21700-type cylindrical lithium-ion cells (INR-21700-P45B, Molicel, Taipei, Taiwan) with a nickel-cobalt-aluminum oxide (NCA) cathode and a graphite/silicon-oxide (SiO_x) anode. Each cell has a typical capacity of 4.5 Ah, a charge cut-off voltage of 4.2 V and a discharge cut-off voltage of 2.5 V. The standard charge current is 4.5 A (1 C) and the maximum charge current is 13.5 A (3 C, specified with a 70 °C cell-temperature cut-off); the maximum continuous discharge current is 45 A (10 C). The 4.2 V and 13.5 A ceilings used as design criteria in Section 4 are therefore manufacturer limits rather than values chosen for this study. The cell and its principal dimensions are shown in Figure 1a. The EMF–SoC relationship in Figure 1b was obtained by quasi-equilibrium cycling of a single cell between 2.5 and 4.2 V at 0.05C and 25 °C. Charging followed a constant-current–constant-voltage (CCCV) protocol, while discharging was performed at constant current. At this low rate, ohmic and polarization overpotentials are small, and the concentration gradients within the electrodes remain close to equilibrium. The terminal voltage therefore provides a practical approximation of the open-circuit voltage without prolonged relaxation at each SoC. The charge and discharge voltage profiles were averaged at each SoC to minimize residual polarization and hysteresis, and the resulting curve was used as the EMF–SoC relationship. Figure 1c shows the module used as the basic building block of the pack, in which 36 cells are connected in parallel at a single series level, denoted 1S36P.

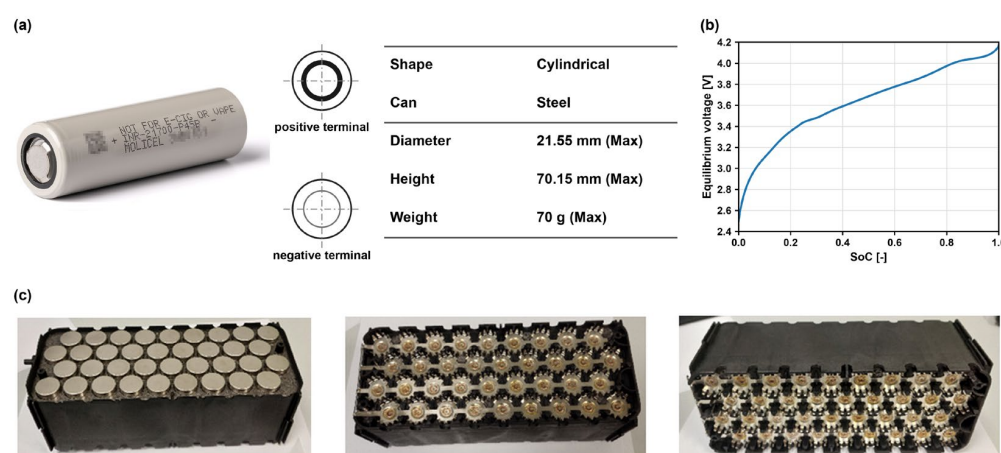


Figure 1. (a) The commercial 21700-type lithium-ion cell used in the case study, its two end views and its principal physical characteristics taken from the manufacturer’s data sheet [33]; the two-dimensional code and the batch identifier printed on the cell have been obscured; (b) Measured equilibrium voltage (or electromotive force, EMF) as a function of state of charge (SoC) at 25 °C; (c) Photographs of the 1S36P battery module developed within the collaborative project and used as the industrial case-study module for parameterizing the generalized pack model.

2.2. Electrical Interconnection Layout of the Module

Within a module the cells are not joined at a common node. The thirty-six cells are strung nine at a time along four flat conductors, their positive terminals welded at successive points along each conductor, whereas their negative terminals are not connected to one another inside the module and are joined instead through the corresponding conductor of the neighboring module. A pack of M modules therefore contains $M + 1$ such conductors, each acting simultaneously as the negative collector of one module and the positive collector of the next; the first and the last of them are the positive and negative current-supplying busbars of the pack. Following the convention used throughout this paper, the generalized network is denoted by NPMS, standing for N cells in parallel and M modules in series: N counts the cells along one finite-resistance conductor within the module and M the modules along the series connection.

The topology of the battery module is represented by the electrical layout shown in Figure 2a. The resistances R_s , R_c , and R_l represent different levels of interconnection within the module and collectively govern the current distribution across cells and parallel strings. In this configuration, R_s denotes the electrical resistance between adjacent cells within a parallel string, R_c represents the resistance of connectors between parallel strings, and R_l corresponds to the resistance between each string and the common busbar. The nominal value of R_s was determined from four-wire (Kelvin) DC measurements at room temperature, using a 10 A current source and a laboratory multimeter with about 1% accuracy. Approximately 50 measurements across several modules gave a mean of 0.37 m Ω and a range of 0.35–0.45 m Ω ; therefore the rounded value of 0.4 m Ω was adopted in all simulations. Other connection resistances were characterized separately. The bridge resistance between adjacent subgroups was measured as 0.4 m Ω but does not enter the reduced single-subgroup model. The series-connection resistance was approximately 0.1 m Ω , with measured values ranging from 0.05 to 0.2 m Ω . This resistance belongs to the cell branch rather than to the connection between parallel cells. Variations in the contact geometry prevent reliable separation of its bulk, interfacial-contact, and current-spreading contributions. Because their combined contribution is small relative to the cell internal resistance, the series-connection resistance is neglected in the model.

It should be noted that this parallel connection does not realize an ideal zero-resistance common node. Within each subgroup, the cells are attached to a flat conductor with a finite resistance R_s between neighboring cell connection points. As a result, cells located closer to the current-feeding side have a shorter current path than cells located farther away, although all cells are nominally connected in parallel. In addition, the practical module and pack-level boundary conditions are not electrically fully uniform. The positive and negative sides differ mainly in their connection technology: the positive busbar is welded, whereas the negative side is connected through spring-loaded contacts, which may lead to different contact resistances. In addition, the first and last modules of the series-connected pack are connected to solid copper planes that provide a low-resistance connection between the four 9-cell parallel subgroups within the module. These position-dependent boundary conditions modify the local current paths and can therefore influence the current distribution within the pack.

To describe the pack topology, indices are introduced as follows: the four subgroups are counted from the left to the right, and the cell position within each subgroup is counted from the bottom to the top in Figure 2a. Within a subgroup the cells are numbered $j = 1, \dots, N$ from the current-feeding end, and the modules are numbered $k = 1, \dots, M$ along the series connection, as depicted in Figure 2b.

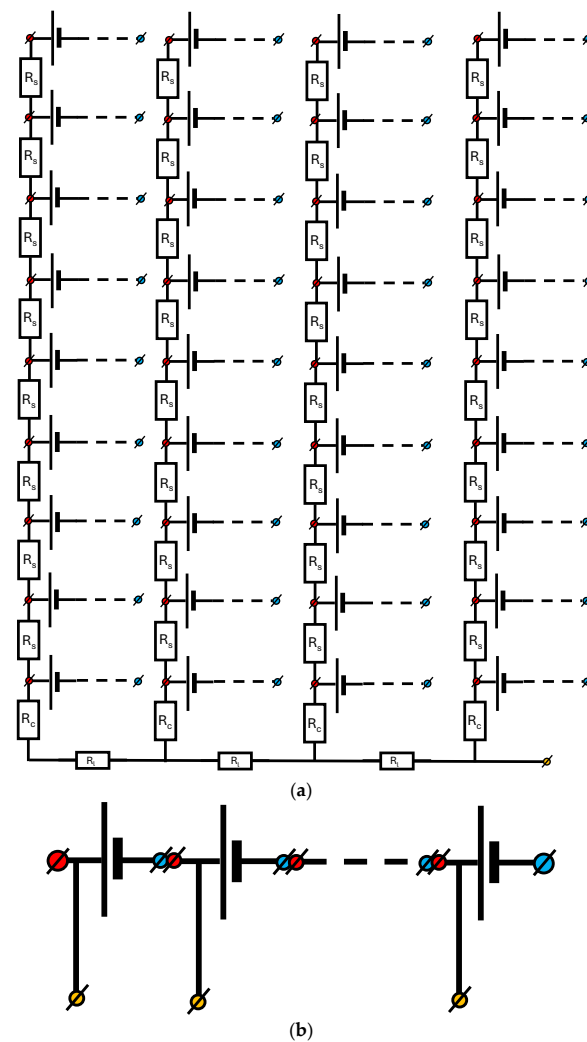


Figure 2. (a) Parallel connection within one module: electrical interconnection layout of the commercial 1S36P module. Within each subgroup, R_s denotes the resistance of the flat-conductor segment between neighboring cell connection points. R_c denotes the lateral coupling resistance between neighboring parallel subgroups, and R_l denotes the resistance linking a subgroup to the common current-collecting path or busbar. (b) Series connection at pack level: schematic representation of multiple modules connected in series at the pack level. The representative-subgroup model used in the following derivation retains the finite-resistance connection along one 9-cell parallel subgroup and allows the number of cells N and the number of series-connected modules M to be varied. The red crossed dots mark the connections to the positive current collectors, the blue dots those to the negative current collectors, and the yellow dots the external voltage-sensing taps connected to the corresponding nodes.

3. Generalized Matrix-Based Network Model

The model derivation is defined for the generalized NPMS-network, all the notation used in the electrical-network formulation is summarized in Table 1. Lowercase r is used for cell-internal resistance, whereas uppercase R denotes external interconnection, contact, or busbar resistance. The same notation is used consistently in the following sections to map the case-study module onto the generalized network. Each cell branch is represented by an equilibrium voltage source ε_j^k in series with an internal resistance r_j^k , where $j = 1, \dots, N$ denotes the cell position within the representative parallel subgroup and $k = 1, \dots, M$ denotes the module index along the series-connected pack.

Table 1. Notation used in the electrical-network model.

Symbol	Description	Unit/Range
k	Series-module index	$k = 1, \dots, M$
j	Parallel cell-branch index within module k	$j = 1, \dots, N$
N	Number of parallel cell branches represented in each module	case study: $N = 9$, if one subgroup is represented
M	Number of modules connected in series at pack level	user-defined
I_{app}	Applied pack current	A
i_j^k	Current through cell j in module k	A
I_j^k	Current through an interconnection/redistribution branch ()	A
ε_j^k	Equilibrium voltage/electromotive force of cell n in module k	V
SOC_j^k	State of charge of cell j in module k	-
Q_j^k	Capacity of cell j in module k	Ah
r_j^k	Internal resistance of cell j in module k	Ω
r_{cell}	Identical cell internal resistance used in the baseline simulations	Ω
R_s	Longitudinal inter-cell connection resistance along one subgroup of the case-study module	Ω
R_c	Lateral coupling resistance between neighboring subgroups in the case-study module	Ω
R_l	Resistance linking each path/row to the common current-collecting busbar	Ω
R_j^p	Segment resistance of the positive (p) current-supplying busbar	Ω
R_j^n	Segment resistance of the negative (n) current-supplying busbar	Ω
R_j^k	Interconnection resistance between neighboring modules (k) associated with parallel position j	Ω
A_i	Current-conservation matrix assembled from Kirchhoff's current law	-
A_v	Voltage-loop matrix assembled from Kirchhoff's voltage law	Ω or dimension-dependent
A	Combined system matrix containing current-conservation and voltage-loop equations	dimension-dependent
g_i	Right-hand-side vector of the current-conservation equations	A
g_v	Right-hand-side vector of the voltage-loop equations	V
g	Combined right-hand-side vector	dimension-dependent
δ_l	Current non-uniformity factor/maximum current overload factor	-
P_{bus}	Ohmic loss in current-supplying and busbar paths	W
P_{int}	Ohmic loss in the interconnection branches	W
P_{ext}	Total external ohmic loss, $P_{ext} = P_{bus} + P_{int}$	W

The full module consists of four 9-cell parallel subgroups coupled through lateral interconnections. One subgroup is selected as the basic unit for the model formulation, as presented in Figure 2a. The number that enters the model is therefore nine and not thirty-six. The thirty-six cells of the module do not share one conductor: they are strung nine at a time along four separate flat conductors that meet only at the module collectors. What governs position-dependent current sharing, and hence the whole subject of this work, is the number of cells along one finite-resistance conductor, and for this module that number is nine; a formulation at thirty-six would describe different hardware, in which every cell hangs from a single conductor. This first-order electrical description of the cell is sufficient to capture topology- and busbar-resistance-induced current redistribution. Electrochemical dynamics beyond this level are intentionally neglected, since the redistribution mechanism under study is governed by the resistive topology rather than by cell kinetics. Physics-based descriptions resolving electrochemical transport and high-frequency electrical dynamics have been developed separately [34] and are not required here.

The governing equations follow from current conservation at the network nodes and Kirchhoff's voltage law, which relates the loop voltage drops to differences in cell equilibrium voltages. Both sets of equations are assembled on the network shown in Figure 3, whose horizontal branches are the cell branches and whose vertical branches are the terminal busbars and the interconnections between neighboring modules. Figure 3a is used for the current law and Figure 3b, which repeats the same network with the closed contours, for the voltage law.

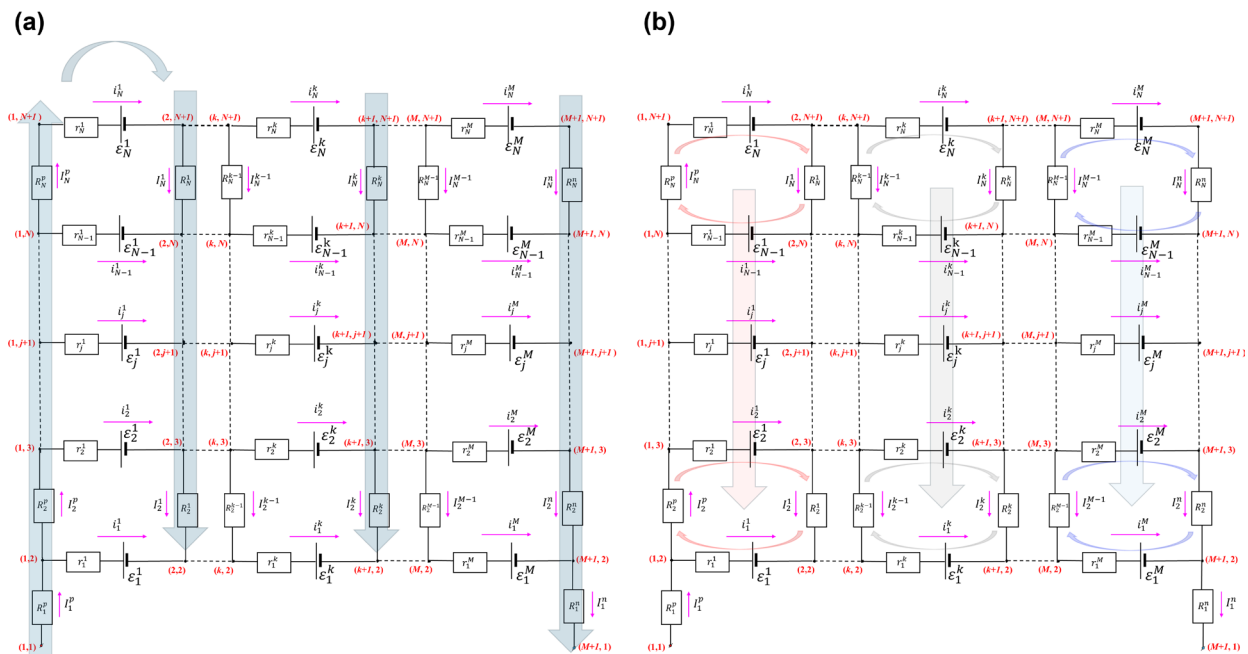


Figure 3. Electrical-network representation of the generalized NPMS battery-pack model. Each cell branch is represented by an equilibrium voltage source and an internal resistance, while the vertical branches represent the terminal busbar and interconnection paths used for current supply, collection, and redistribution. The red labels denote node indices and the pink arrows the predefined branch-current directions; both are common to (a,b). (a) Assembly of the current-conservation equations. The grey semi-transparent arrows give the order in which the node equations are collected, the thin arrow running upward along the positive busbar and the thick arrows downward along each subsequent module string, the curved arrow linking the two. (b) Assembly of the voltage-loop equations on the same network. The curved arrows indicate the selected closed-contour directions and the vertical semi-transparent arrows the order in which the contours are assembled; a separate color is used for each module, so that the curved arrows and the vertical arrow drawn in one color belong to the same module. Only selected contours are shown for clarity. In total, $(N - 1)M$ independent contours are used, each corresponding to a voltage balance between two neighboring parallel cell branches.

Figure 3a fixes three conventions on the network. Node numbering: a node is a point at which several branches meet, and the numbering, given by the red labels, starts at the bottom-left node (1,1), the positive terminal of the pack, and runs from bottom to top along the leftmost vertical string as (1,1), (1,2), (1,3), ..., (1, $N + 1$), each of these nodes being the connection point of one cell branch. Along the bottom series string it runs as (1,2), (2,2), (3,2), ..., ($M + 1$,2), so that the first index counts the module and the second the parallel position, and the equilibrium voltages of that string are $\varepsilon_1^1, \varepsilon_1^2, \dots, \varepsilon_1^M$, all sharing the same lower subindex; the same rule applies to every row and every column of the layout for N cells in parallel and M modules in series. The segment resistances R_j^p and R_j^q of the leftmost and the rightmost strings are the positive and the negative current-supplying busbars, kept distinct from the internal interconnection resistances R_j^k ($k = 1, \dots, M - 1$) because thicker connectors are used at the pack terminals. Reference directions: the pink arrows

give the direction of every branch current. This direction is from bottom to top in the leftmost vertical string, i.e., string defined by $(1, 1), \dots, (1, N + 1)$ nodes, and in the opposite direction in all other vertical strings. In the horizontal direction currents are defined from left to right. Currents in the vertical branches are written with capital letters I and currents through the cells with lowercase letters i . Assembly order: applying conservation of charge at each node gives the first set of equations, and the grey semi-transparent arrows give the order in which they are collected. The first equation is written at node $(1, 1)$ and sets the busbar current I_1^p equal to the applied pack current I . The numbering then moves up the leftmost vertical string along the thin arrow, passing over nodes $(1, 1), \dots, (1, N + 1)$, and down over nodes $(2, N + 1), \dots, (2, 2)$ along the thick arrow, the same rule applying module by module up to nodes $(M + 1, N + 1), \dots, (M + 1, 2)$.

The unknown branch currents are collected into the column vector i in the order shown in Figure S9 of the Supplementary Information. Within each module containing N parallel cells, there will be $2N - 1$ currents. N ‘horizontal’, flowing across the parallel cells, and $N - 1$ ‘vertical’, corresponding to parallel (rebalancing) connections. The rightmost module is closed by the ‘vertical’ string, which contains current-carrying connectors that lead toward the negative terminal of the overall pack. Note that for the leftmost and rightmost modules, there are 2 additional currents, i.e., I_1^p and I_1^n which correspond to the input/output currents of the whole battery pack. The total number of currents (variables to be solved for) is, therefore, $(2N - 1)M + (N - 1) + 2 = (2N - 1)M + N + 1$.

Then the system of equations for currents can be written in the following way:

$$A_i i = g_i \quad (1)$$

where g_i is defined as a column vector of $N(M + 1) + 2$ elements having all zeros except for the first and the last elements, which are equal to I (current applied to the pack); i is the column vector of dimension $(2N - 1)M + N + 1$, containing unknown currents to be solved. The system matrix A_i determining equations has the following block structure

$$A_i = \begin{pmatrix} C_B & O & O & O \\ B_i & O & O & O \\ O & T_i & O & O \\ & \ddots & & \\ O & O & T_i & O \\ O & O & O & F_i \\ O & O & O & C_F \end{pmatrix} \quad (2)$$

where submatrix T_i is repeated $M - 1$ times on the diagonal. Symbols O represent zero submatrices of the suitable dimensions, and

$$C_B = \begin{pmatrix} 1 & 0 & \dots & 0 & 0 \end{pmatrix} \quad (3)$$

$$C_F = \begin{pmatrix} 0 & 0 & \dots & 0 & 1 \end{pmatrix} \quad (4)$$

Each row of A_i is one current-conservation equation written at a single node, the rows following the node order of Figure 3a, and each column corresponds to one unknown branch current, in the order in which the currents are collected into i . An entry is +1 when the reference arrow of that branch points into the node, −1 when it points away from it, and zero when the branch does not touch the node. The matrix therefore contains only the integers 0, +1 and −1 and is fixed by the topology of the pack alone, so it is assembled once; the resistances and the states of charge enter the system only through the voltage-law part

derived below. The two single-row blocks C_B and C_F carry the boundary conditions at the pack terminals. C_B selects the first unknown and C_F the last one so that, with the first and the last entries of g_i equal to I , the current entering the positive terminal and the current leaving the negative terminal are both set to the applied pack current. Every other entry of g_i is zero, because current conservation at an internal node has no source term.

Three different blocks are needed because a node is touched only by the branches of its own module and of the modules adjacent to it. The nodes of the first module are reached by the positive-busbar currents and by the cell currents of that module alone, and the nodes of the last module by its own cell currents and by the negative-busbar currents, so that B_i and F_i are both N by $2N$. An interior node is reached in addition by the vertical interconnection currents at the module boundary, so that T_i is N by $3N - 1$ and straddles two neighboring column blocks. Reading a single row recovers the corresponding node equation: the first row of B_i states that the busbar current arriving at node (1, 2) from below leaves that node partly along the busbar and partly through the first cell branch. The structural submatrices B_i , T_i , and F_i within A_i are given by Equations (5) to (7), written out for $N = 4$ so that the pattern of the entries stays legible; the case study of Section 4 uses $N = 9$, where the same blocks measure 9 by 18 and 9 by 26.

$$B_i = \begin{pmatrix} 1 & -1 & 0 & 0 & 0 & 0 & 0 & -1 \\ 0 & 1 & -1 & 0 & 0 & 0 & -1 & 0 \\ & & \ddots & \ddots & & \ddots & & \\ 0 & 0 & 1 & -1 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \end{pmatrix} \quad (5)$$

$$T_i = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & -1 & -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & -1 & 1 & 0 & -1 & 0 & 0 \\ & & \ddots & \ddots & \ddots & & & & & \ddots & \\ 0 & 0 & 1 & 0 & -1 & 1 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & -1 \end{pmatrix} \quad (6)$$

$$F_i = \begin{pmatrix} 1 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 & -1 & 0 & 0 \\ & & \ddots & & & \ddots & \ddots & \\ 0 & 0 & 1 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 1 & -1 \end{pmatrix} \quad (7)$$

The diagonal structure of these blocks shows how they can be written down for arbitrary N and M without listing their entries: the diagonals are the inflow and outflow currents encountered on moving from one node to the next.

To obtain the second part of the system of equations, the second Kirchhoff's voltage law is applied to independent closed contours in the pack network. These equations introduce the cell electromotive forces, cell internal resistances, and external interconnection resistances into the system matrix and determine how the applied current is distributed among the parallel branches. Figure 3b shows the same network with representative contours used for applying Kirchhoff's voltage law. The curved arrows give the direction in which each contour is traversed and the vertical semi-transparent arrows the order in which the contours of one module are taken, a separate color being used for each module. Each contour is formed by two neighboring parallel cell branches within one module, closed through the corresponding interconnection resistances, so that $(N - 1)M$ independent contours are obtained. Only a subset of them is shown for illustrative purposes.

The system of equations corresponding to the second Kirchhoff's law has the form

$$A_v i = g_v \quad (8)$$

where

$$A_v = \begin{pmatrix} O & B_v & O & O & O & O \\ O & O & T_v^1 & O & O & O \\ & & & \ddots & & \\ O & O & O & T_v^{M-2} & O & O \\ O & O & O & O & F_v & O \end{pmatrix}. \quad (9)$$

The corresponding submatrices are given by Equations (10) to (12)

$$B_v = \begin{pmatrix} 0 & 0 & 0 & R_N^p & r_N^1 & -r_{N-1}^1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & R_N^1 \\ 0 & 0 & R_{N-1}^p & 0 & 0 & r_{N-1}^1 & -r_{N-2}^1 & 0 & 0 & 0 & 0 & 0 & R_{N-1}^1 & 0 \\ & & \ddots & & & \ddots & \ddots & & & & & \ddots & \\ 0 & R_3^p & 0 & 0 & 0 & 0 & 0 & r_3^1 & -r_2^1 & 0 & 0 & R_3^1 & 0 & 0 \\ R_2^p & 0 & 0 & 0 & 0 & 0 & 0 & 0 & r_2^1 & -r_1^1 & R_2^1 & 0 & 0 & 0 \end{pmatrix} \quad (10)$$

$$T_v^s = \begin{pmatrix} 0 & 0 & 0 & -R_N^s & r_N^{s+1} & -r_{N-1}^{s+1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & R_N^{s+1} \\ 0 & 0 & -R_{N-1}^s & 0 & 0 & r_{N-1}^{s+1} & -r_{N-2}^{s+1} & 0 & 0 & 0 & 0 & 0 & R_{N-1}^{s+1} & 0 \\ & & \ddots & & & \ddots & \ddots & & & & & \ddots & \\ 0 & -R_3^s & 0 & 0 & 0 & 0 & 0 & r_3^{s+1} & -r_2^{s+1} & 0 & 0 & R_3^{s+1} & 0 & 0 \\ -R_2^s & 0 & 0 & 0 & 0 & 0 & 0 & 0 & r_2^{s+1} & -r_1^{s+1} & R_2^{s+1} & 0 & 0 & 0 \end{pmatrix} \quad (11)$$

$$F_v = \begin{pmatrix} 0 & 0 & 0 & -R_N^{M-1} & r_N^M & -r_{N-1}^M & 0 & 0 & 0 & 0 & R_N^n & 0 & 0 & 0 \\ 0 & 0 & -R_{N-1}^{M-1} & 0 & 0 & r_{N-1}^M & -r_{N-2}^M & 0 & 0 & 0 & 0 & R_{N-1}^n & 0 & 0 \\ & & \ddots & & & \ddots & \ddots & & & & & \ddots & \\ 0 & -R_3^{M-1} & 0 & 0 & 0 & 0 & 0 & r_3^M & -r_2^M & 0 & 0 & 0 & R_3^n & 0 \\ -R_2^{M-1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & r_2^M & -r_1^M & 0 & 0 & 0 & R_2^n \end{pmatrix} \quad (12)$$

where $s = 1, \dots, M - 2$. The three blocks differ in which vertical conductor segments close their contours: the positive busbar and the first interconnection in B_v , two neighbouring interconnections in T_v , and the last interconnection and the negative busbar in F_v . This is why T_v , in contrast to T_i in Equation (6), depends on its place in A_v . Also, the right-hand side of Equation (8), each entry of which is the difference of the two equilibrium voltages driving the corresponding contour, is defined as

$$\mathbf{g}_v = \begin{pmatrix} \varepsilon_2^1 - \varepsilon_1^1 \\ \varepsilon_3^1 - \varepsilon_2^1 \\ \vdots \\ \varepsilon_N^1 - \varepsilon_{N-1}^1 \\ \varepsilon_2^2 - \varepsilon_1^2 \\ \varepsilon_3^2 - \varepsilon_2^2 \\ \vdots \\ \varepsilon_N^2 - \varepsilon_{N-1}^2 \\ \vdots \\ \varepsilon_2^M - \varepsilon_1^M \\ \varepsilon_3^M - \varepsilon_2^M \\ \vdots \\ \varepsilon_N^M - \varepsilon_{N-1}^M \end{pmatrix} \quad (13)$$

Each row of A_v corresponds to one Kirchhoff voltage-law equation obtained from a single independent closed contour. The two cell branches of that contour contribute their internal resistances with opposite signs, and the two vertical conductor segments closing

the loop contribute their resistances, so that only four entries of the row are non-zero. The number of rows in each voltage-loop block of Equation (9) is $(N - 1)$, corresponding to the number of independent loops between neighboring parallel branches. The number of voltage-loop block submatrices in A_v is equal to the number of series-connected modules, M . In contrast to A_i , whose entries are determined only by topology, A_v contains resistance values and may therefore change when cell or interconnection parameters vary.

It is worth noting that, in a real battery system, resistances r_j^k are not constant but are implicit functions of current across the cell, cell parameters, and time. In the present work, these resistances are treated as constant parameters over the simulated time window; coupling the network model to detailed electrochemical or electro-thermal cell models is left for future work.

Equations (1) and (8) jointly can be written as

$$Ai = g \quad (14)$$

where

$$A = \begin{pmatrix} A_i \\ A_v \end{pmatrix}, \quad g = \begin{pmatrix} g_i \\ g_v \end{pmatrix} \quad (15)$$

Note that Equation (14) contains one equation more than the number of unknowns. This redundancy amounts to exactly one equation for any N and M , and it corresponds to global charge conservation: the final current-conservation row is implied by the remaining rows. The system is therefore consistent rather than genuinely overdetermined, and it possesses a unique solution, which has been verified numerically for every pack size used in this work. Because the system is rectangular, the solution is obtained by sparse QR factorization, invoked through the backslash operator; forming the normal equations explicitly is avoided, since that squares the condition number of the problem. The numerical verification and the comparison of the two solution routes are given in Section S7 of the Supplementary Information. For completeness, in the explicit case the OLS solution $\hat{i}$ is written as

$$\hat{i} = (A'A)^{-1}A'g \quad (16)$$

All simulations reported in this work were carried out in MATLAB R2024b. The pack model is implemented directly from the matrix formulation given above, with no additional toolboxes required beyond core MATLAB; the linear system of Equation (14), with A and g composed as in Equation (15), is assembled in sparse form and solved with the built-in sparse QR factorization. The equilibrium-voltage curve is supplied as measured data and evaluated by linear interpolation. Figures showing current, voltage and state-of-charge distributions are generated directly from the solution vector of the same model. The complete parameter set is listed in Table S2 of the Supplementary Information, which also gives the assembly of A_v , A_i , g_i and g_v as pseudocode for arbitrary N and M , together with fully worked small-network examples that can be reproduced by hand.

The assembly was checked against an independent formulation of the same network. Modified nodal analysis uses node potentials rather than branch currents as unknowns and shares no part of the implementation above. For the case study at 3 C the two agree to a relative difference of 4.1×10^{-8} in the maximum cell current, at both 0.4 and 1 mΩ busbar segment resistance. This verifies the assembly and its solution, not the physical assumptions behind them.

4. Results and Discussion

Using the formalism introduced in the previous section, the system matrix can be assembled in a structured sparse form. The sparsity pattern for representative configurations

is illustrated in Figure 4, where Figure 4a corresponds to a small system ($M = 3$, $N = 4$) and Figure 4b to the case-study configuration ($N = 9$, $M = 13$), that is the nine-cell parallel subgroup of the 1S36P module with thirteen modules in series. White spaces represent entries with zero values, while colored dots correspond to non-zero elements. Throughout this section the modelled network is one of the four nine-cell subgroups of the module, carried through the thirteen series-connected modules. The complete module contains four such subgroups and therefore draws four times the applied current at the same C-rate.

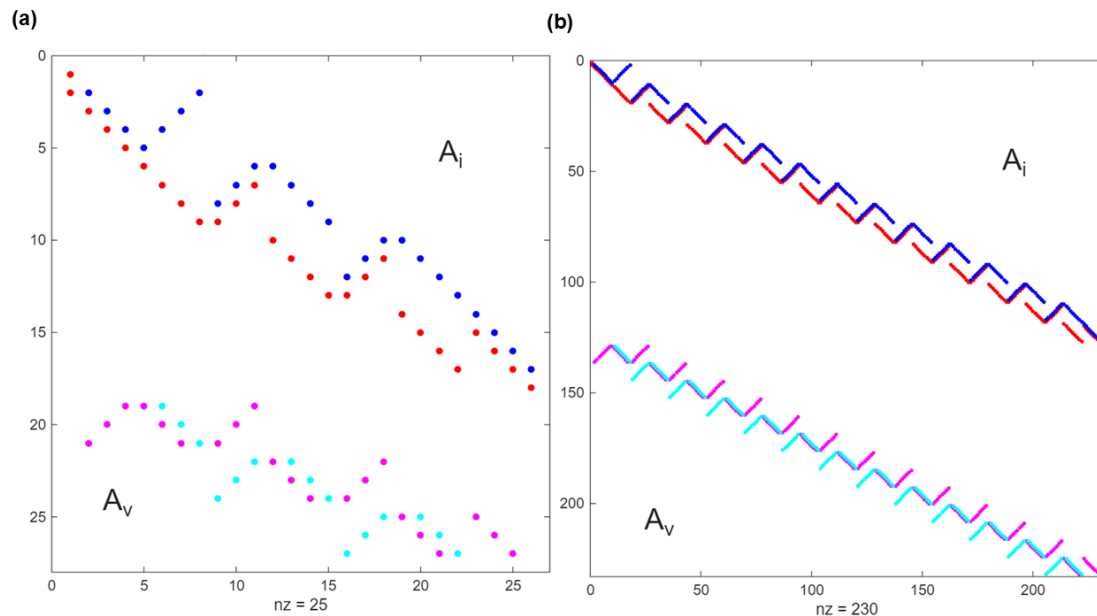


Figure 4. Sparsity pattern of the combined system matrix (A). (a) A small network, drawn only so that the sparsity pattern remains legible and not one of the configurations studied here, with ($M = 3$) and ($N = 4$). (b) The case-study network with ($N = 9$) and ($M = 13$). White regions denote zero entries, whereas colored markers denote non-zero entries. The upper block corresponds to the current-conservation matrix (A_i), and the lower block corresponds to the voltage-loop matrix (A_v). Red and blue mark entries equal to $+1$ and -1 , which occur only in the current-conservation block A_i ; magenta and cyan mark the positive and negative resistance coefficients of the voltage-loop block A_v .

The matrix can be decomposed into two distinct submatrices, A_i and A_v , corresponding to current conservation and voltage relations, respectively. The submatrix A_i contains only integer entries (± 1), reflecting the topology of current continuity across the network. In contrast, A_v incorporates the system's electrical parameters, with entries determined by the pack's resistive elements, resulting in both positive and negative values of varying magnitude.

4.1. Ideal Homogeneous Current Distribution

The current distribution in an ideal configuration is first considered as a reference case. In this case, the positive and negative terminal busbar resistances are set to zero, i.e., $R_i^p = R_i^n = 0$, while all cells are assumed to be identical. The cell internal resistances are set to $r_i^k = 10 \text{ m}\Omega$, and the local interconnection resistances are kept at $R_i^k = 0.4 \text{ m}\Omega$. It should be noted that, the manufacturer's data sheet specifies a DC internal resistance of $15 \text{ m}\Omega$ at 50% SoC [33], whereas our measurements yielded approximately $10 \text{ m}\Omega$. The measured value was adopted as a conservative choice because a lower cell resistance increases the relative influence of the interconnection network. Each cell is initialized at an SoC of 0.2, corresponding to an EMF of 3.3 V according to the measured EMF–SoC curve. The total applied current is 40.5 A. Since each module contains nine parallel-connected

cells with a capacity of 4.5 Ah, this corresponds to an ideal current of 4.5 A per cell, or a charge rate of 1C. As shown in Figure 5b, the current is uniformly distributed among the parallel cell branches under this symmetric condition, and the terminal busbars introduce no position-dependent current imbalance. In Figure 5a the two edges of the surface, at interconnection levels 1 and $M + 1$, carry much larger currents than the interior levels, because those two levels are the current-supplying busbars through which the whole pack current enters and leaves, whereas in this ideal case the interior levels carry essentially no current.

The total pack voltage, measured between nodes (1, 1) and (13, 1), is equal to 43.485 V. This corresponds to a total overvoltage of 0.585 V relative to the sum of the equilibrium cell voltages. Since the busbar resistances are zero in this reference case, this overvoltage originates from the internal resistance of the cells rather than from voltage gradients in the external interconnection network. This idealized configuration therefore provides a baseline against which the effect of finite busbar resistance can be isolated.

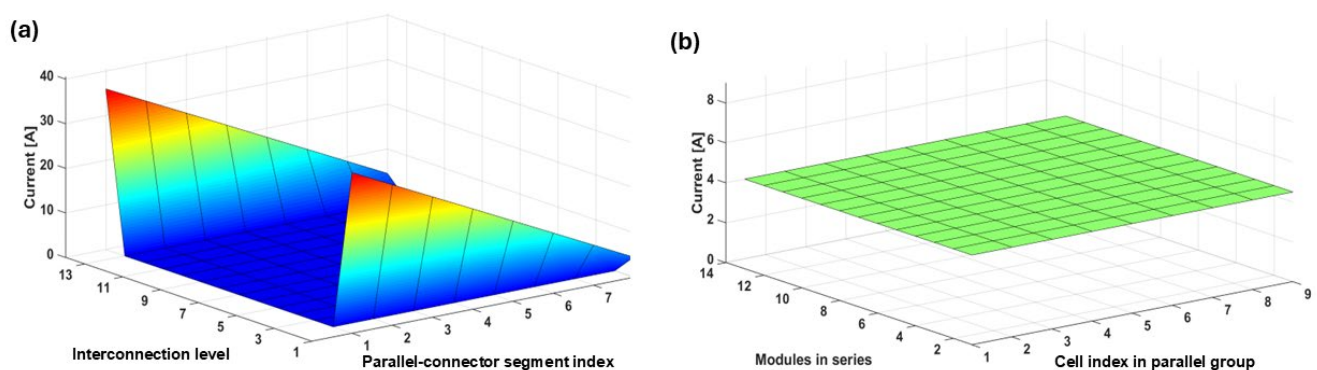


Figure 5. Current distribution in the ideal reference case, $R_i^p = R_i^n = 0$. (a) Currents in the parallel-connector network. (b) Cell-branch currents. The cell index $j = 1, \dots, N$ is the position within the nine-cell subgroup, counted from the current-feeding end; the segment index runs over the $N - 1$ connectors between neighboring cells; the interconnection level runs from 1 to $M + 1$, levels 1 and $M + 1$ being the positive and negative busbars. The same convention is used in Figures 6–8.

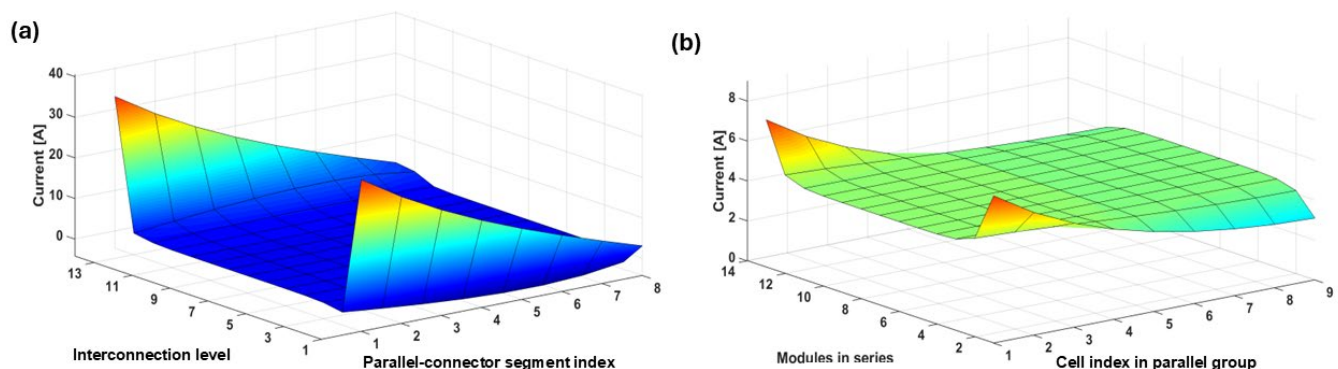


Figure 6. Current distribution with finite positive and negative busbar resistance, $R_i^p = R_i^n = 0.4\text{m}\Omega$. (a) Currents in the parallel-connector network. (b) Cell-branch currents. Axes as in Figure 5.

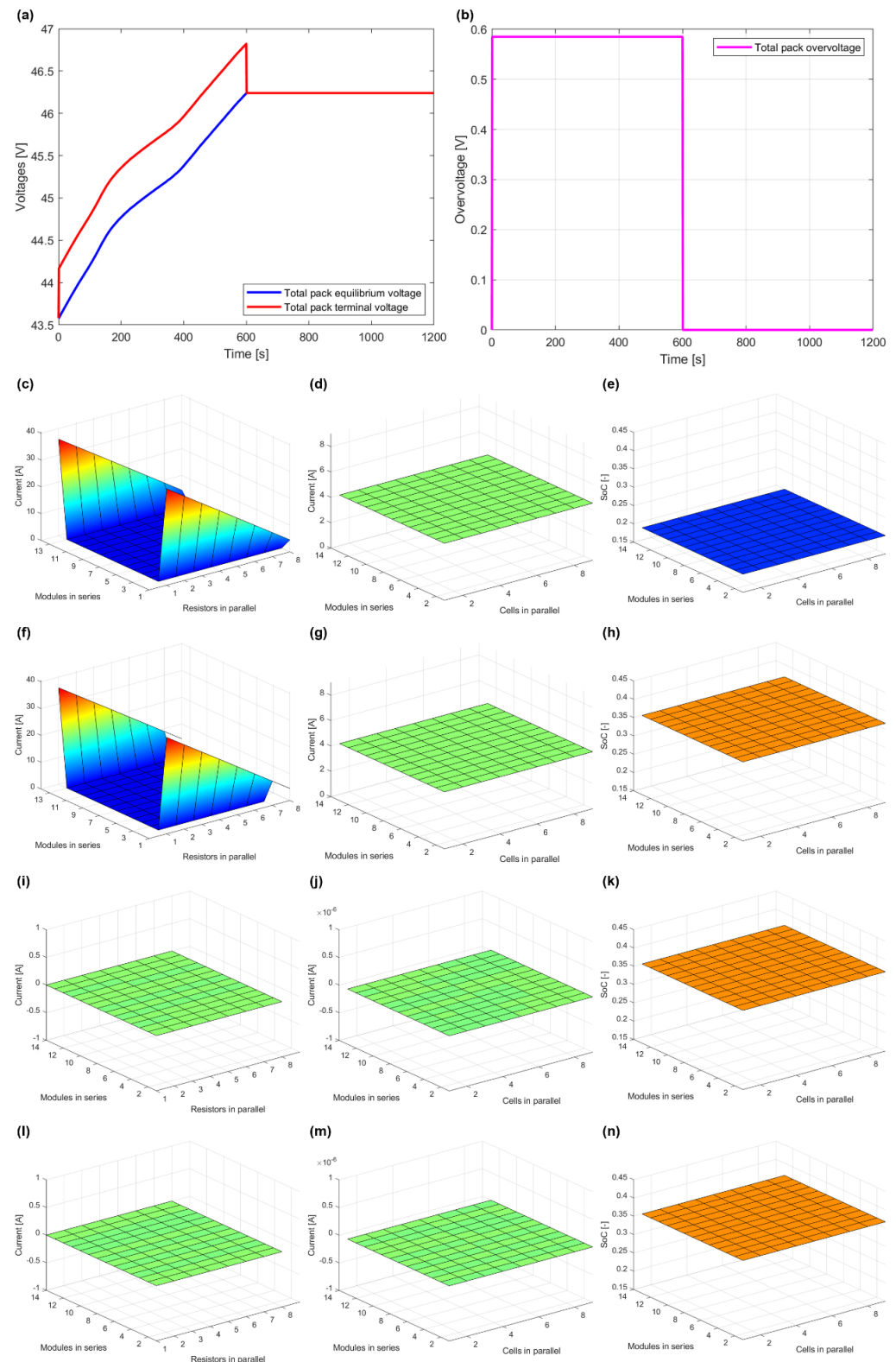


Figure 7. Dynamic evolution of voltage, current, and SoC distributions in the ideal reference case with zero positive and negative busbar resistance. (a) Total pack equilibrium voltage and terminal voltage. (b) Total pack overvoltage. (c–e) Current and SoC distributions at the beginning of charging. (f–h) Distributions at the end of the charging pulse. (i–k) Distributions immediately after current interruption. (l–n) Distributions at the end of the relaxation period. Within each group of three, (c,f,i,l) show the currents in the parallel-connector network, (d,g,j,m) the cell-branch currents, and (e,h,k,n) the SoC distribution.

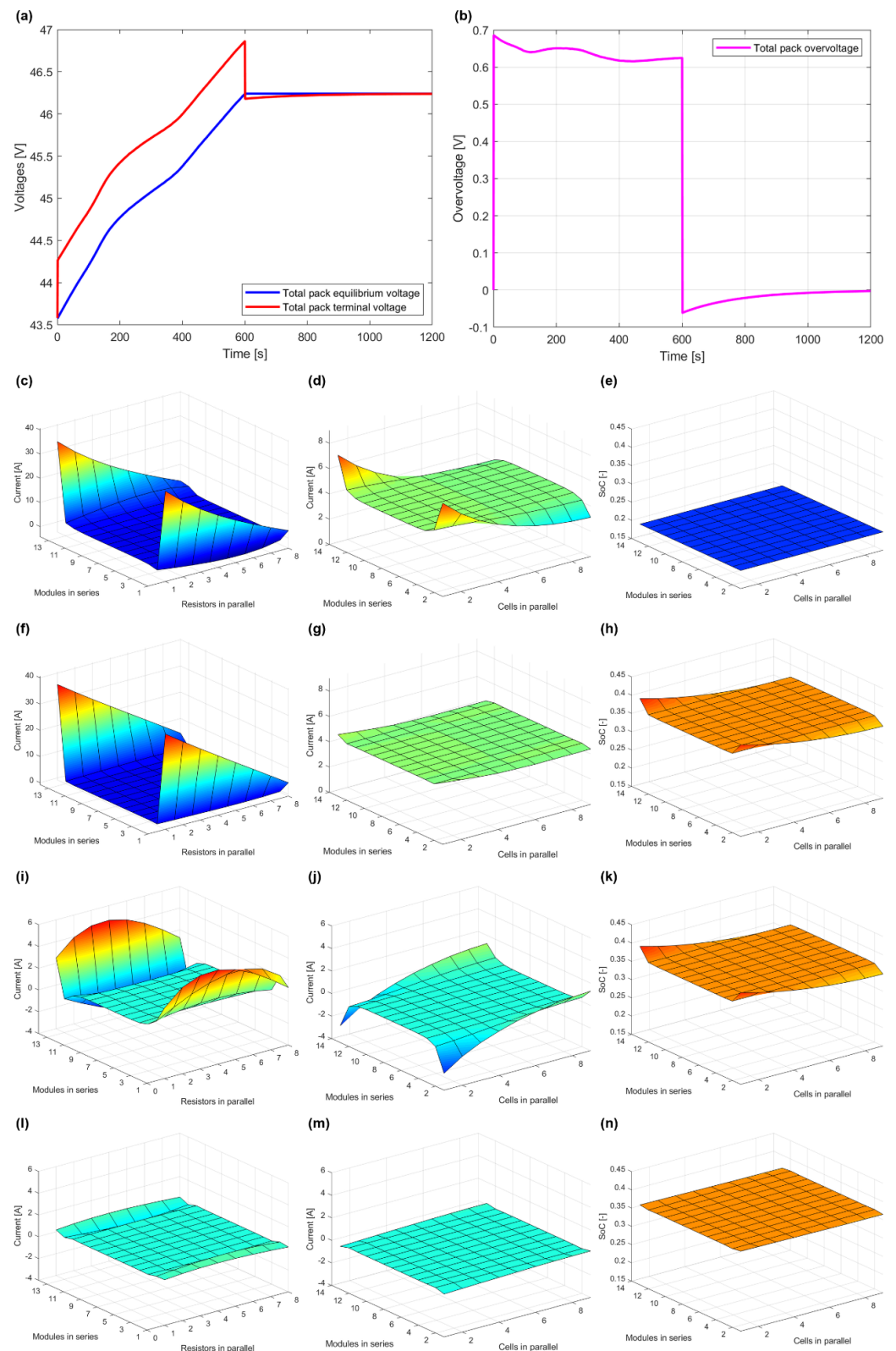


Figure 8. Dynamic evolution of voltage, current, and SoC distributions with finite positive and negative busbar resistance, $R_i^p = R_i^n = 0.4\text{m}\Omega$. (a) Total pack equilibrium voltage and terminal voltage. (b) Total pack overvoltage. (c–e) Current and SoC distributions at the beginning of charging. (f–h) Distributions at the end of the charging pulse. (i–k) Distributions immediately after the current interruption. (l–n) Distributions at the end of the relaxation period. Finite busbar resistance induces non-uniform current sharing during charging and drives redistribution currents during the subsequent relaxation period.

4.2. Impact of Busbar Resistance on Current Inhomogeneity

The effect of finite busbar resistance on the current distribution is examined in Figure 6. In this case, the resistances of the positive and negative busbars are no longer negligible and are set equal to the interconnection resistances, i.e., $R_i^p = R_i^n = 0.4 \text{ m}\Omega$ for all i . All other parameters remain identical to those of the ideal case.

Introducing finite busbar resistance breaks the symmetry of the electrical network and results in a clearly non-uniform current distribution. Although all cells have identical internal resistance and electromotive force, the cell-branch currents in Figure 6b are no longer evenly shared among the nine parallel cells. They range from 3.10 A to 7.38 A about a mean of 4.5 A, the largest occurring at $j = 1$ in the modules adjacent to the two current-supplying busbars. At the same time, pronounced redistribution currents appear in the external interconnection network of Figure 6a, indicating that the parallel branches are electrically coupled through the shared busbar structure.

The total pack voltage increases from 43.485 V in the ideal case to 43.586 V, corresponding to an overvoltage increase from 0.585 V to 0.685 V. This increase reflects the additional resistive losses introduced by the finite busbar resistance.

From a circuit perspective, this behavior originates from voltage drops along the busbar segments. These voltage gradients drive lateral redistribution currents between neighboring parallel branches, which in turn modify the cell-branch currents. Therefore, the current distribution is not determined solely by the cell properties, but also by the resistance and topology of the interconnection network.

4.3. Dynamic Evolution of Current and SoC Distribution

To investigate the temporal evolution of current and SoC distributions, the static network model is extended by updating the SoC of each cell according to the local cell current:

$$\text{SoC}_j^k(t + \Delta t) = \text{SoC}_j^k(t) + \frac{1}{3600 Q_j^k} \int_t^{t+\Delta t} i_j^k(\tau) d\tau, \quad (17)$$

where $\text{SoC}_j^k(t)$, in Equation (17), is the SoC of cell number j in the module k at the moment of time t ; $i_j^k(\tau)$ [A] is the current across the cell number j in the module k at the moment of time τ ; Q_j^k [Ah] is the maximal capacity of cell number j in the module k , and Δt is the time step. A charging pulse of 40.5 A is applied for 600 s, followed by a zero-current relaxation period.

The equilibrium voltage is obtained by linear interpolation of the measured EMF–SoC data of Figure 1b. The measurement covers SoC = 0 to 1, with an upper equilibrium voltage of 4.169 V, and the interpolant is clamped at these limits. Charging is terminated when the pack-average cell voltage, that is the pack terminal voltage divided by the number of series-connected modules, reaches 4.2 V. This criterion reproduces the information available to a battery-management system, which monitors the voltage of a series-connected group but not the individual cells within a parallel group; the maximum individual cell voltage is evaluated at that same instant, which makes the cell-level overcharge that is invisible at pack level directly quantifiable. Since the time to reach this cutoff scales inversely with the applied current, the simulated interval is matched in charge throughput across the investigated rates rather than fixed in duration. All reported design and loss quantities are evaluated over this interval.

Figure 7 shows the dynamic response of the ideal reference case, in which the positive and negative busbar resistances are neglected. The total pack equilibrium voltage and terminal voltage are shown in Figure 7a, while the corresponding total overvoltage is shown in Figure 7b. During the charging pulse, the overvoltage remains constant because

the current distribution is uniform and the resistance network does not introduce additional voltage gradients. Once the applied current is interrupted, the overvoltage immediately drops to zero, indicating the absence of relaxation currents in the ideal case. Figure 7c–n show the current and SoC distributions at selected times. Figure 7c–e correspond to the beginning of charging, Figure 7f–h to the end of the charging pulse, Figure 7i–k to the moment immediately after the current interruption, and Figure 7l–n to the end of the relaxation period. Because of the symmetry of the ideal configuration, all cell branches carry the same current of 4.5 A during charging. As a result, the SoC increases uniformly in all cells. After the current interruption, both the cell currents and redistribution currents become negligible, and the homogeneous SoC distribution is maintained.

The situation changes when the busbars are modeled with finite resistance. Figure 8a and b show the voltage and overvoltage evolution of the pack with R_i^p and R_i^n equal to $0.4 \text{ m}\Omega$, the same as all other R_i^k . All other parameters are identical to those in the ideal reference case. Compared with Figure 7, the total overvoltage in Figure 8b is larger during the charging pulse and exhibits a relaxation transient after current interruption. This behavior indicates that finite busbar resistance not only increases the instantaneous resistive loss, but also generates non-uniform SoC distributions that drive self-balancing currents after the external current is removed. At the beginning of charging, the distribution in Figure 8c–e is consistent with the static result shown in Figure 6. Although all cells start from the same SoC and electromotive force, the finite busbar resistance introduces voltage gradients along the external interconnection network. These gradients lead to non-uniform cell-branch currents, particularly near the terminal modules. In these regions the individual branch currents range from 3.10 A to 7.38 A about a nominal mean of 4.5 A, so the most heavily loaded cell carries 1.64 times the mean, purely as a consequence of its position within the parallel group and with all cells otherwise identical. Such local current amplification may accelerate the SoC increase in selected cells and may not be directly observable from pack-level current measurements alone.

As charging proceeds, the non-uniform current distribution results in a non-uniform SoC distribution, as shown in Figure 8f–h. The SoC inhomogeneity reaches its largest value near the end of the charging pulse. Immediately after the applied current is switched off, pronounced redistribution currents appear in the interconnection network and through the cell branches, as shown in Figure 8i–k. Their magnitude is substantial: individual cell branches carry between -2.50 A and $+1.28 \text{ A}$ while the net pack current is zero, so that some cells are actively discharging into others through the interconnection network. These currents are driven by the SoC-dependent voltage differences accumulated during charging. During the subsequent relaxation period, the redistribution currents gradually decay and the SoC differences are partially reduced, as shown in Figure 8l–n. By the end of the relaxation period the branch currents have decayed to between -0.18 A and $+0.12 \text{ A}$ and the state-of-charge spread has narrowed from 0.054 to 0.005. Since the cells are identical here, the relaxation continues until the state of charge is uniform again, so the topology-induced imbalance is transient once the current is removed; it is the imbalance while current flows that determines the peak cell loading. Therefore, finite busbar resistance affects not only the instantaneous current sharing during operation, but also the post-pulse relaxation behavior of the pack.

4.4. Cell-Level Voltage Divergence and Hidden Safety Risks

A direct consequence of non-uniform current distribution is the emergence of cell-level voltage divergence during high-rate operation. Figure 9 compares the cell-branch voltage evolution and the corresponding pack-level voltage response during high-rate charging and discharging. This normalized pack voltage corresponds to the voltage that

would be inferred from a pack-level measurement, whereas the gray curves reveal the internal voltage spread among individual cell branches. Figure 9a illustrates the evolution of individual cell voltages during 3 C charging in the non-ideal configuration. A substantial spread in cell voltages develops during charging, becoming most pronounced toward the end of charge.

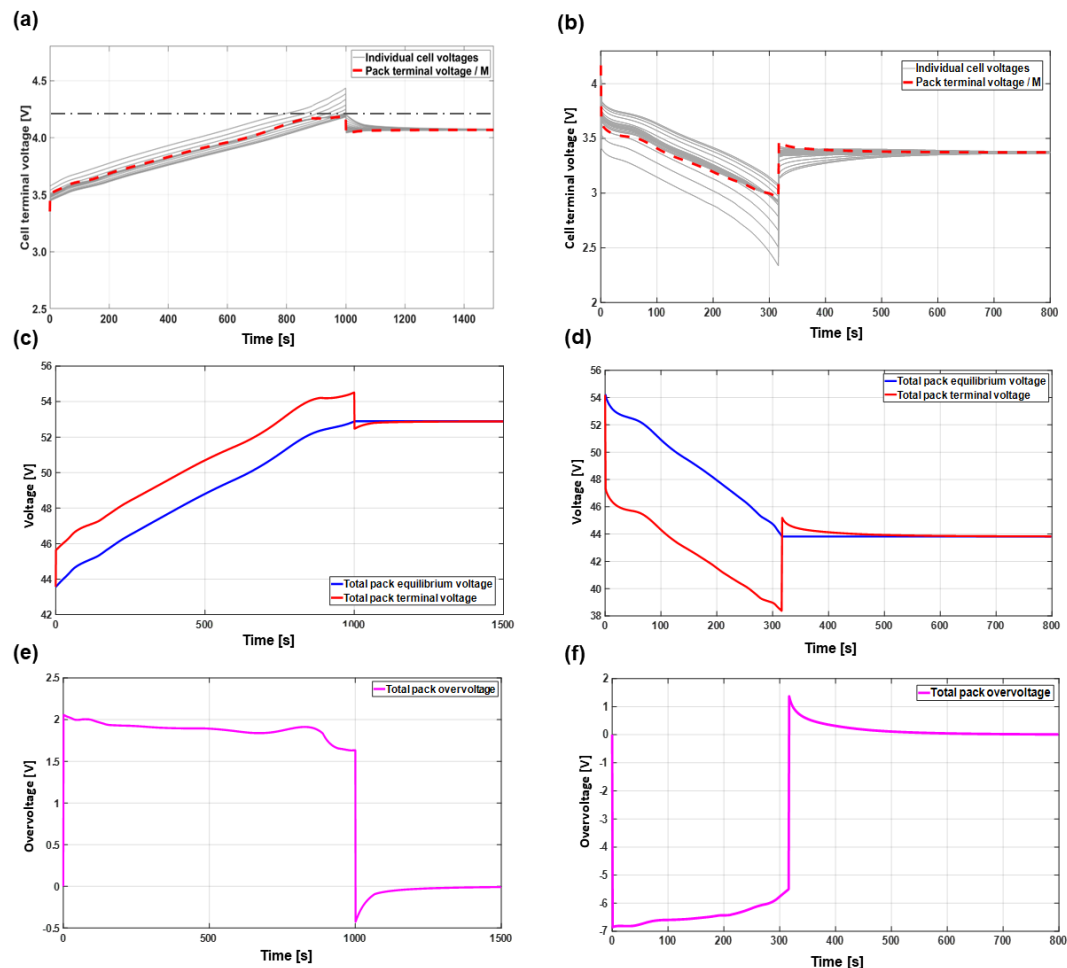


Figure 9. Cell-level voltage evolution and pack-level voltage response under high C-rate operation: (a,b) individual cell voltages during charging and discharging, respectively. The gray solid lines represent individual cell-branch voltages, and the red dashed line represents the total pack terminal voltage normalized by the number of series-connected modules. The black dash-dotted line in (a) indicates the upper cell-voltage limit. (c,d) Total pack equilibrium voltage and terminal voltage during charging and discharging. (e,f) Corresponding total pack overvoltage. The comparison shows that pack-level voltage measurements may not capture the maximum or minimum local cell-branch voltage under non-uniform current distribution.

At 874 s the charging process is terminated, because the average cell voltage has reached the manufacturer's charge cut-off of 4.2 V. At that instant the most heavily loaded cell has reached 4.324 V, exceeding the cut-off by 124 mV while the pack-level measurement reads exactly its nominal limit. This discrepancy reveals a critical limitation of pack-level monitoring: although the average voltage remains within the prescribed limit, individual cells may already be operating in an overcharge regime.

This behavior originates from the non-uniform current distribution induced by finite busbar resistance. Cells carrying higher currents experience larger polarization and reach higher terminal voltages, while others remain below the average level. As a result, cells con-

nected in parallel do not necessarily operate at the same voltage under dynamic conditions, despite their electrical configuration.

A similar effect is observed during discharge, as shown in Figure 9b. In this case, certain cells exhibit significantly lower voltages than the pack average, indicating localized over-discharge. This further confirms that voltage divergence is a general consequence of current inhomogeneity, affecting both charging and discharging regimes. The corresponding evolution of pack-level voltage and overvoltage is shown in Figure 9c–f. In contrast to the ideal case, the voltage profiles are no longer linear in time, reflecting the nonlinear dependence of the open-circuit voltage on SoC. More importantly, these pack-level quantities do not capture the internal voltage spread between cells and therefore fail to provide a complete picture of the system state.

Overall, current inhomogeneity causes substantial cell-level voltage divergence and may drive individual cells beyond their voltage limits even when the pack-level voltage remains acceptable. This risk becomes more pronounced at high C-rates. In the present case, the most heavily loaded cell exceeds the cut-off voltage by 124 mV. During charging, its higher voltage and local current shift the anode potential to more negative values, promoting lithium plating, loss of cyclable lithium and, potentially, dendritic growth and internal short circuits. During discharge, excessively low cell potentials may cause dissolution of the copper current collector. These local degradation processes can also intensify thermal non-uniformity. Safe operating limits and battery-management strategies should therefore account for internal current and voltage distributions rather than pack-average quantities alone. The present model identifies the electrical conditions associated with these risks; resolving the underlying degradation and thermal responses would require coupled electrochemical–thermal modeling and experimental validation.

4.5. Design-Oriented Analysis and Safety Limits

Beyond predicting current distribution, the proposed framework enables a quantitative assessment of battery pack safety from a design perspective. In particular, the non-uniform current distribution induced by finite busbar resistance leads to deviations between individual cell behavior and pack-level observable quantities. This effect becomes increasingly critical at high C-rates, where even small variations in resistance can result in substantial current and voltage non-uniformities across cells connected in parallel. To quantify the worst-case current non-uniformity during charging, a maximum relative current-deviation factor is introduced:

$$\eta_I^{\max} = \max_{t \in [0, t_I]} \left[\max_k \frac{\max_j |i_j^k(t) - i_{avg}^k(t)|}{|i_{avg}^k(t)|} \right], \quad (18)$$

where

$$i_{avg}^k(t) = \frac{1}{N} \sum_{j=1}^N i_j^k(t). \quad (19)$$

Here, $i_j^k(t)$ is the current of the cell j in module k , $i_{avg}^k(t)$ is the average cell current within the module k , and t_I is the duration of the constant-current charging interval. The maximum in Equation (18) is taken over all cells, all modules, and all time steps during the constant-current charging stage. Thus, $\eta_I^{\max}$ is a worst-case design metric rather than a time-average quantity.

Figure 10a compares the current non-uniformity factor as a function of busbar resistance under charging rates from 1 C to 5 C. The results show that the current non-uniformity is primarily governed by the pack's resistive topology, while the dependence on charging rate remains comparatively weak across a broad operating range. In particular, the 1 C–3 C

curves nearly overlap, indicating that the normalized current overload is largely insensitive to the absolute current level under moderate operating conditions. At higher charging rates (4 C–5 C), a somewhat greater deviation is evident, suggesting that current redistribution effects are more pronounced under aggressive high-power operation.

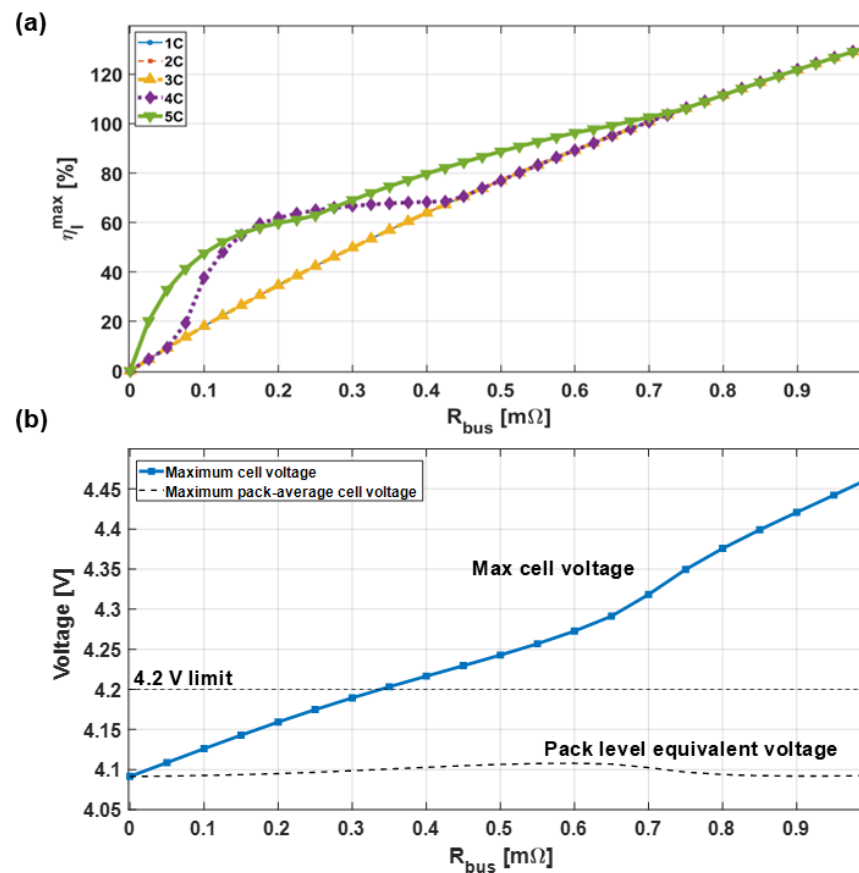


Figure 10. Design-oriented safety metrics as a function of current-supplying busbar resistance. (a) Maximum current non-uniformity factor under different charging rates, evaluated as the maximum over all cells, modules, and time steps during the constant-current charging interval; (b) Maximum cell voltage and pack-level equivalent cell voltage (V_{pack}/M), evaluated over the same simulation window.

For low busbar resistance values (below approximately 0.05–0.1 $m\Omega$), the pack operates in a quasi-homogeneous regime, where η_I^{max} remains below the adopted 10% criterion. As the busbar resistance increases, the system rapidly transitions into a strongly inhomogeneous regime, with peak current overload exceeding 20–30% and eventually becoming substantially larger at elevated resistance values. This transition defines a practical design boundary separating electrically acceptable and potentially unsafe operating conditions.

In contrast, the maximum cell voltage is strongly dependent on both busbar resistance and operating current. As shown in Figure 10b, even when the pack-level equivalent voltage remains within nominal limits, individual cells may exceed the upper voltage threshold (e.g., 4.2 V) under certain conditions. Here, the pack-level reference voltage is represented by the pack terminal voltage normalized by the number of series modules, V_{pack}/M , rather than the arithmetic average of individual cell voltages. The slight non-monotonic variation in this pack-level quantity at higher busbar resistance reflects the redistribution of internal voltage drops and current paths, rather than numerical inaccuracy. This effect becomes more pronounced at high C-rates and elevated busbar resistance, where localized overcharging occurs despite seemingly normal pack-level operation.

The model also determines the maximum allowable busbar resistance for a given operating condition. By imposing a constraint on the current non-uniformity factor (e.g., $\eta_I^{max} < 10\%$), an upper bound for the busbar resistance can be identified.

4.6. Design Maps for Combined Operating Conditions

The combined effects of busbar resistance and operating C-rate are summarized in two-dimensional design maps, as shown in Figure 11.

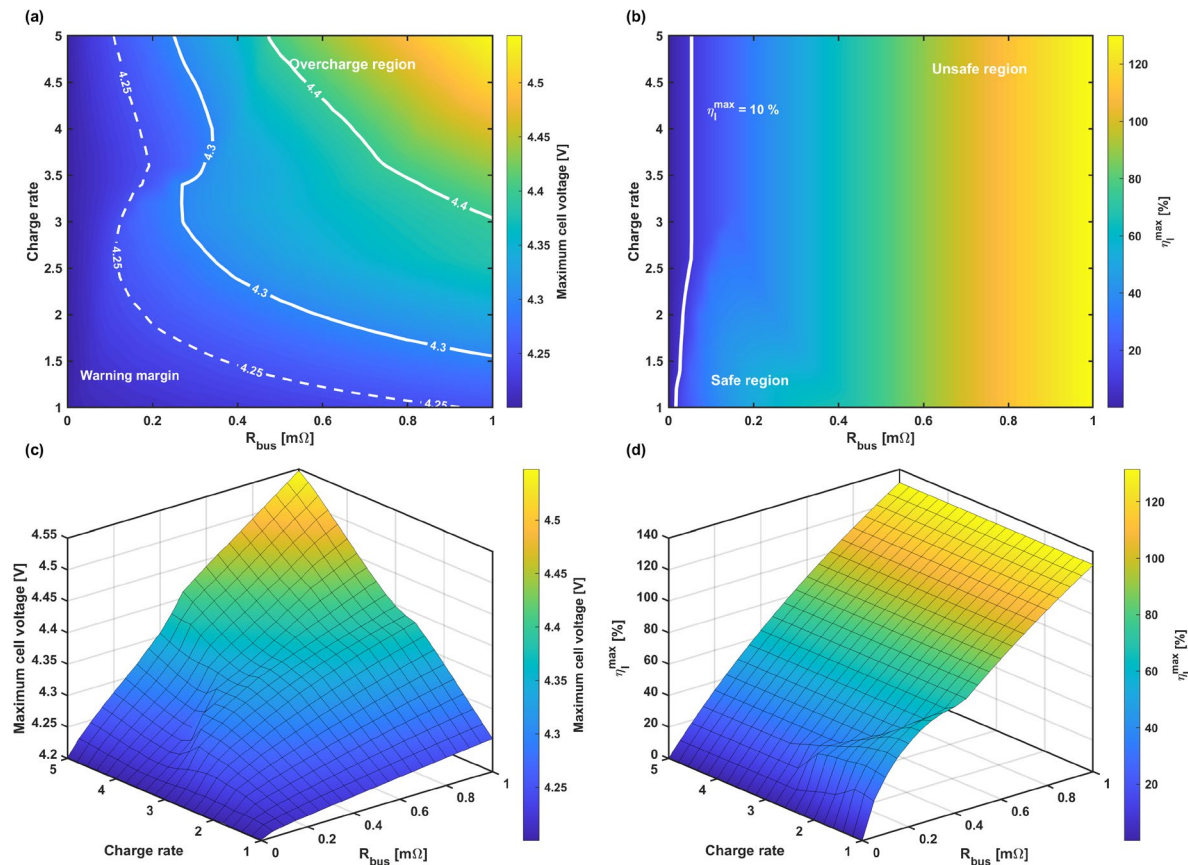


Figure 11. Design-oriented performance maps of the battery pack as functions of busbar resistance and charging rate: (a) maximum cell voltage, with contours 50, 100 and 200 mV above the 4.2 V limit delimiting the warning and overcharge regions; (b) current non-uniformity factor, indicating the transition between safe and unsafe operating regimes based on the 10% criterion; (c) surface representation of maximum cell voltage; and (d) surface representation of current non-uniformity factor.

Figure 11a presents the maximum cell voltage across the parameter space. Charging is terminated when the pack-average cell voltage reaches the 4.2 V limit, so the maximum individual cell voltage lies at or above that limit throughout the map, and the continuous contours mark where the most heavily loaded cell exceeds it by 100 and 200 mV. In contrast to the current non-uniformity behavior, these contours exhibit a strong dependence on the C-rate. At higher charging rates, the allowable busbar resistance is significantly reduced, indicating that even moderate resistance can lead to cell-level overvoltage during high-power operation. The additional dashed contour, 50 mV above the limit, defines a warning region that can serve as a conservative design margin. The margin is sized to cover cell-to-cell variation, which the model omits; this is quantified in Section S5 of the Supplementary Information.

Figure 11b shows the corresponding design map for the current non-uniformity factor. The boundary defined by the 10% criterion runs almost horizontally, so the transition

already seen in Figure 10a appears here as a limiting busbar resistance that hardly moves with C-rate.

The surface representations in Figure 11c,d make the difference between the two constraints explicit. The maximum-cell-voltage surface is curved in both directions and steepens as the charge rate rises, so the voltage margin is lost fastest where both busbar resistance and charge rate are high. The current-non-uniformity surface, by contrast, has almost no gradient along the charge-rate axis, and is therefore governed by the busbar resistance alone except at small resistance, where the lowest rate deviates from the others.

From a practical design perspective the two criteria have to be met at once, so the allowable busbar resistance lies in the intersection of the safe regions of Figure 11a,b. Neither criterion alone is sufficient, because the topology-induced inhomogeneity and the operation-dependent voltage constraint bind in different parts of the map; only their combination links the electrical limits to structural parameters such as busbar material, cross-section and cell spacing.

4.7. Power Loss and Efficiency Implications

Figure 12 further quantifies the energetic implication of the external interconnection network during constant-current charging. The applied pack current was defined as $I_{app} = 40.5 \times C_{rate}$ A, corresponding to 40.5, 81, 121.5, 162, and 202.5 A for 1 C, 2 C, 3 C, 4 C, and 5 C, respectively, that is 4.5 A per cell at 1C for the nine 4.5 Ah cells represented in the model. Since the instantaneous power losses vary during the dynamic simulation, all loss quantities shown in Figure 12 were averaged over the constant-current charging interval. This interval is matched in charge throughput rather than in wall-clock time, so that the different charging rates are compared on a physically equivalent basis. The total external ohmic loss is defined as $P_{ext} = P_{bus} + P_{int}$, where P_{bus} denotes the loss in the current-supplying and current-collecting busbar paths, and P_{int} denotes the loss in the interconnection branches. The normalized loss in Figure 12b is calculated as the ratio between the mean external loss and the mean absolute terminal input power over the same constant-current interval.

As shown in Figure 12a, the mean external loss increases monotonically with both current-supplying busbar resistance and C-rate. This behavior is consistent with the (I^2R) dependence of ohmic dissipation and confirms that finite busbar resistance affects not only current redistribution but also the power dissipated in the pack-level current paths. At low C-rate, the absolute loss remains small over the investigated resistance range. In contrast, at high C-rate and large busbar resistance, the external loss reaches approximately 224 W. Because a total dissipation does not by itself determine a local temperature, this value is reported here as an electrical and efficiency result, and its thermal consequences are discussed only qualitatively.

The normalized loss in Figure 12b shows the corresponding efficiency penalty relative to the mean absolute terminal input power during the constant-current charging interval. Although the applied current is constant during CC charging, the terminal power remains time-dependent because the terminal voltage changes with the cell state and polarization. Therefore, the normalized loss is calculated as $\langle P_{ext} \rangle_{CC} / \langle |P_{terminal}| \rangle_{CC}$, where $\langle \cdot \rangle_{CC}$ denotes time averaging over the constant-current charging interval. The normalized external loss increases with both C-rate and R_{bus} . Under the highest investigated C-rate and busbar-resistance conditions, the external loss accounts for 2.2% of the terminal input power. This result indicates that busbar resistance can become an efficiency-relevant design parameter, particularly under fast-charging operation.

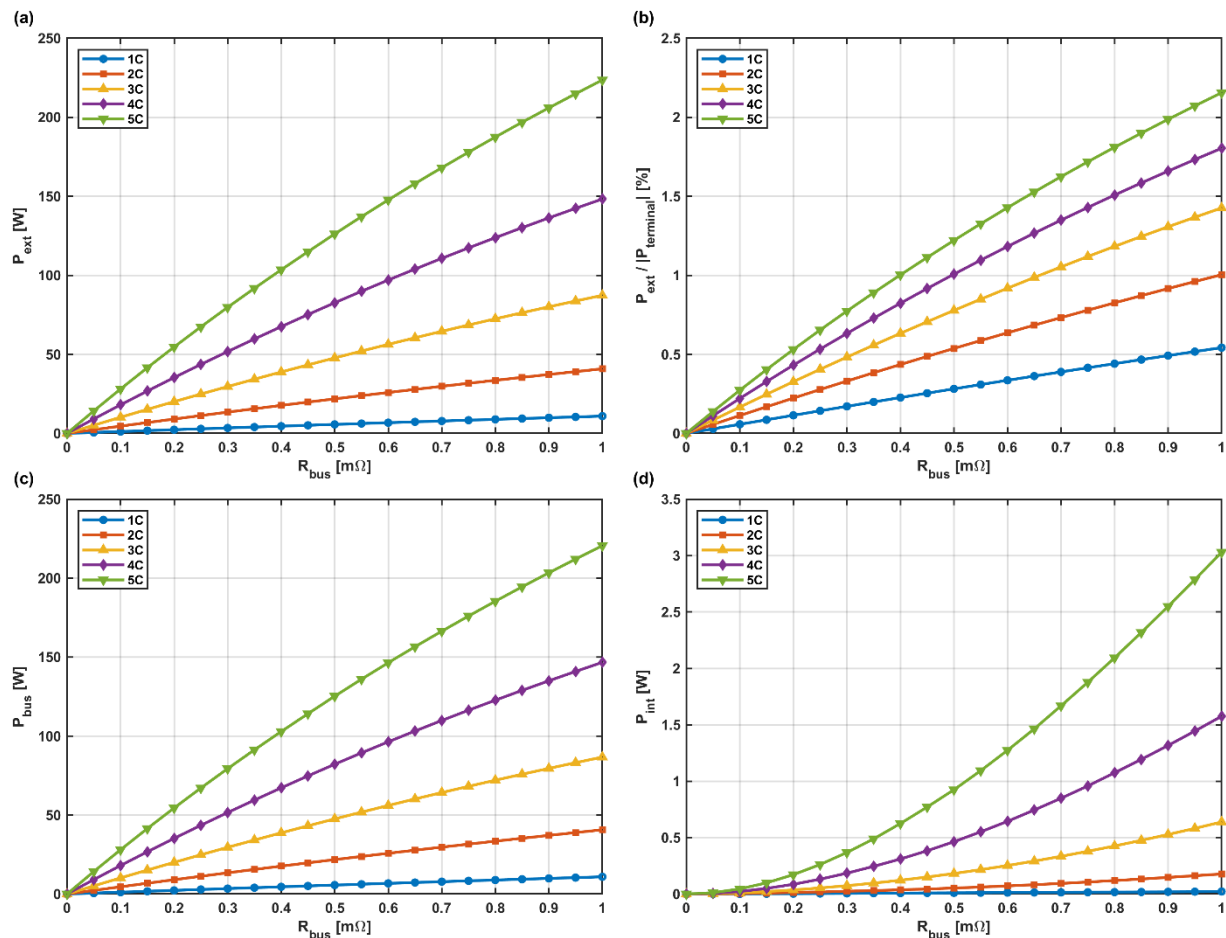


Figure 12. External ohmic losses during constant-current charging. (a) Total external loss, ($P_{ext} = P_{bus} + P_{int}$). (b) External loss normalized by terminal input power. (c) Busbar loss, (P_{bus}). (d) Interconnection loss, (P_{int}). All losses are averaged over the constant-current charging interval.

The loss decomposition in Figure 12c,d shows that the total external loss is dominated by the busbar contribution. The busbar loss in Figure 12c follows the same monotonic trend as the total external loss in Figure 12a, whereas the interconnection loss in Figure 12d is smaller by roughly two orders of magnitude, contributing 4 W of the 224 W total at 5C with a 1 $m\Omega$ busbar segment. Nevertheless, P_{int} also increases with C-rate and busbar resistance because finite busbar resistance modifies the branch-current distribution and redistribution currents. The loss is not uniformly distributed over the interconnection network. The busbar segment adjacent to the pack terminal carries the entire pack current by construction and therefore dissipates $I_{app}^2 R_{bus}$, which is 5.91 W at 3 C with $R_{bus} = 0.4 m\Omega$, whereas each segment further along carries only the current of the cells beyond it, so the loss falls monotonically to 0.06 W in the last of the nine segments. The two segments nearest each terminal account for 53.4% of the external loss and the four nearest each for 82.3%, while the interconnection segments account for the remaining 0.3% at this 3 C and 0.4 $m\Omega$. These results show that reducing current-supplying busbar resistance is beneficial not only for mitigating current inhomogeneity and cell-level voltage divergence but also for reducing external ohmic heating and improving pack-level charging efficiency.

5. Conclusions

This study developed a generalized matrix-based framework for analyzing current distribution, local cell voltage and interconnection losses in series–parallel battery packs. Kirchhoff current and voltage equations are assembled into a sparse linear system. The

model can represent different numbers of parallel cells and series modules, as well as finite resistances in individual branches. Topology constraints and resistance terms are assembled separately, which allows the pack geometry and resistance values to be varied without reformulating the model.

The framework was applied to an industrial cylindrical cell module. The current distribution proved to be controlled by the resistance of the current-supplying busbar. With negligible busbar resistance, identical parallel cells shared the current uniformly. Finite busbar resistance broke this symmetry and caused cells on shorter or less resistive paths to carry higher currents. At the start of charge, the local cell currents ranged from 3.10 to 7.38 A for a nominal current of 4.5 A per cell. The highest current was therefore 1.64 times the mean value. This imbalance arose even though all cells had identical capacity, internal resistance and equilibrium voltage.

The non-uniform current distribution also produced substantial differences in local cell voltage. Under high-rate operation, the most heavily loaded cell exceeded the 4.2 V cut-off by 124 mV, while the pack-level voltage remained within the nominal operating window. Pack-average quantities may therefore fail to identify the most stressed cell. This limitation becomes more important as the operating current increases.

A current non-uniformity factor and a maximum cell voltage criterion were used to construct design maps as functions of busbar resistance and charging rate. These maps identify operating conditions that satisfy both current and voltage limits. They can therefore support the selection of busbar resistance, conductor geometry and operating current. Interconnection resistance also caused external power losses of up to 224 W under the most severe conditions studied, 5 C with a busbar segment resistance of 1 m Ω , corresponding to 2.2% of the terminal input power. These losses occur almost entirely in the current-supplying busbars, which account for 220 of the 224 W. Their effect on temperature cannot be determined from the present electrical model and requires a coupled thermal analysis.

The model was verified numerically, but its local predictions have not yet been validated experimentally. The equilibrium voltage curve and interconnection resistance were obtained from measurements, and the numerical system was checked for uniqueness, conservation and conditioning. However, the predicted cell currents, redistribution currents and local busbar voltage drops were not measured. The results should therefore be used as design stage indicators for comparing interconnection layouts, rather than as direct evidence that a specific electrochemical or thermal hazard will occur.

The framework can be applied to other battery packs by changing the cell parameters, interconnection resistances and topology inputs. Candidate layouts can be evaluated over the required operating range and revised when the most stressed cell exceeds the selected limits, which makes explicit how much interconnection resistance, and therefore how much conductor material, can be tolerated before the weakest cell rather than the pack average sets the usable operating window. Future work should include experimental measurement of local currents, heterogeneous cell properties and coupling to a thermal network. Overall, the results show that busbar resistance is a key pack design parameter because it affects current sharing, local cell voltage and energy efficiency.

Supplementary Materials: The following supporting information can be downloaded at <https://www.mdpi.com/article/10.3390/batteries12090324/s1>, Figure S1: Kirchhoff's law for a single cell during charging; Figure S2. Kirchhoff's law for a single cell during discharging; Figure S3. Layout and first Kirchhoff's law for the 3PS1 assembly; Figure S4. The second Kirchhoff's law for the 3PS1 assembly; Figure S5. Layout and first Kirchhoff's law for the 3PS3 assembly; Figure S6. Layout and first Kirchhoff's law for the 3PS3 assembly; Figure S7. Layout and first Kirchhoff's law for the 4PS3 assembly; Figure S8. Layout for the second Kirchhoff's law, case of S3P4 assembly; Figure S9.

Definition and ordering of branch-current variables in the N-parallel, M-series battery-pack network; Table S1. Additional rise in the maximum cell voltage at charge termination when a cell-to-cell spread is superimposed on the identical-cell baseline of 4.324 V; Table S2. Complete parameter set of the simulations reported in the manuscript.

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