

The d-DotFET: MosFET based on locally strained silicon

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Introduction

In microelectronics the predictions of Moore's law were fulfilled by downscaling the device dimensions by almost three orders of magnitude: In 2005 the physical gate length was driven below the 50 nm boundary. In the first time this development was facilitated just by scaling, afterwards new materials for metallization, gate electrodes (metal gate) and gate oxides (high- κ) were introduced. In recent years also the material for the channel, the silicon itself, is under investigation: to enhance carrier mobility the material is strained, leading to higher mobility and hence to higher I_{on}/I_{off} ratio. To apply strain to silicon SiGe pseudosubstrates are widely used, which consists of relaxed SiGe-layers on Si substrates. In the d-DotFET approach we use ordered Ge dots to facilitate locally strained silicon layers. The growth sites of the Ge dots are defined by patterning of the substrate (template assisted self assembly): the Ge dots will grow on the prepatterned sites serving as local pseudosubstrate for the subsequently grown Si capping layer. By integrating the MOSFET on top of this locally strained layer the strain can be utilized to improve device performance. Besides the straightforward processing of the locally strained layer, the applied strain can be larger as in the planar case, because the Ge content in the dots is larger than possible in normal blanket epitaxy of SiGe-layers [1].

Device Processing

The dot sites were defined by e-beam lithography, given a lateral positioning accuracy of ± 5 nm. Ordered Ge dots were grown with 500 nm pitch. After epitaxial growth of the Ge dots and the in situ doped locally strained Si capping layer by MBE the source and drain wells were implanted. For the outdiffusion of Ge into the surrounding silicon at temperatures exceeding 600°C the activation of the dopants was done after Ge removal at the end of the process. A 100 nm thick field oxide was deposited by PECVD at temperatures of 350°C. After defining the active area by optical lithography and etching in diluted HF the gate stack was deposited: we used 5 nm of e-gun evaporated $GdScO_3$ as gate dielectric and 40 nm of AVD deposited TiN as gate metal. The gate definition itself was done by e-beam lithography and Reactive Ion Etching (RIE) using hydrogensilsesquioxane (HSQ) as negative tone e-beam resist. A self aligned shallow implantation is performed to form source and drain extensions. To adjust the gate width, again with e-beam lithography the source and drain extensions were patterned and etched by RIE: the shallow implantation was removed except of small bridges of silicon connecting the wells with the active area (Fig. 1). For devices with gate length and width smaller than 120 nm the etch pit touched the Ge dot below the channel. Therefore it was possible to remove the Ge dot itself by selective wet etch, while the strain in the channel was maintained by the gate stack itself. This disposal of the Ge dot forms a strained silicon on nothing transistor which is of benefit for the device performance, too.

Results and Conclusion

Transistors with gate length between 60 nm and 1 μ m were processed with different gate width ranging from 60 nm to 180 nm. In comparison to transistors fabricated on the same chip, but without Ge dot, the increase in drain current is up to 35% for transistors with 80 nm gate length and width. For gate dimension exceeding 120 nm there is no positive effect recognizable, because the active area becomes larger than the dot itself. Therefore the effect of strain is decreased. To investigate the influence of the disposal of the Ge dot the results were compared to devices proposed in [2]. Here also MOSFETs were integrated on a locally strained silicon layer on top of Ge dots, but the dot is not removed. The drain current increase for those devices is 22.5% showing that removing the Ge dot will further increase performance. In conclusion the d-DotFET concept of exploiting locally strained silicon in MOSFET channels offers an alternative to get higher strain and hence improved device performance by means of lower process complexity.

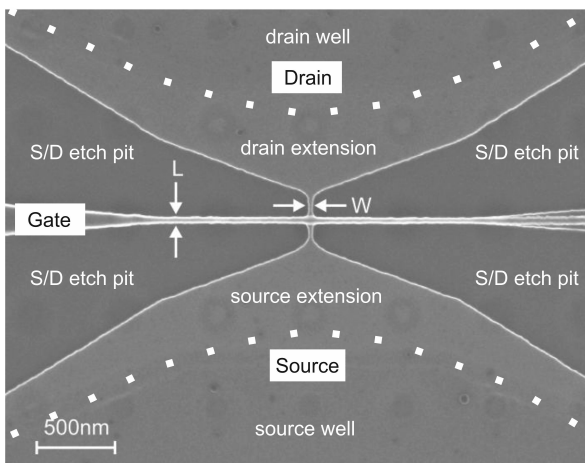


Fig. 1: Top view SEM micrograph of a d-DotFET.

[1] N. Hrauda et al.: Nano Lett. 2011, 11, 2875–2880

[2] V. Jovanović et al: IEEE ELECTRON DEVICE LETTERS, VOL. 31, NO. 10, OCTOBER 2010