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InAlN/GaN/Si heterostructures and field-effect transistors with lattice matched and tensely or compressively strained InAlN

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Properties of InAlN/GaN heterostructures and field-effect transistors with nearly lattice matched (InN=18%) and tensely (13%) or compressively (21%) strained InAlN barrier layer were evaluated. The sheet charge density increased from 1.1×10^{13} to 2.2×10^{13} cm^{-2} with decreased InN mole fraction. The saturation drain current as well as the peak extrinsic transconductance increased inversely proportional to the InN mole fraction—from 1 A/mm to 1.4 A/mm (V_G=2 V) and from 190 to 230 mS/mm. On the other hand, the threshold voltage shifted to higher values with increased InN mole fraction. The pulsed current-voltage measurements (1 μs pulse width) yielded relatively low and nearly identical gate lag for all devices investigated. These results show that InAlN/GaN heterostructures with tensely strained InAlN can be useful for high-frequency and high-power devices and with compressively strained InAlN might be useful for the preparation of enhancement mode GaN-based devices. © *2010 American Institute of Physics*. [doi:10.1063/1.3507885]

InAlN/GaN heterostructure field-effect transistors (HFETs) are since recently under systematic studies as an efficient alternative to AlGaN/GaN microwave transistors. Encouraging results on InAlN/GaN HFETs have been obtained recently, which can be documented by 205 GHz current gain cutoff frequency[1] and 10 W/mm output power at 10 GHz.[2] One of the main advantages of InAlN/GaN material structure is that InAlN can be grown lattice matched to GaN.[3] In such a case the piezoelectric polarization charge is eliminated which should led to reduced or eliminated surface related current collapse,[4] i.e., to better high-frequency performance. This expectation can be supported by recent observation that the gate lag of the HFETs with lattice-mismatched InAlN is higher than that of the counterpart with lattice-matched InAlN barrier.[5] Main part of published results on InAlN/GaN structures and devices is devoted to lattice-matched material and less is reported on lattice mismatched InAlN/GaN.

Commonly accepted composition of InAlN lattice-matched to GaN is with an InN mole fraction of $x=17\%-18\%$.[3,6] This composition follows from an assumption that the underlying GaN layer is strain free. However, it is well known that the GaN layers are not fully relaxed. They exhibit a residual strain which depends on various factors, such as the substrate used,[7,8] ohmic contacts deposition, and subsequent annealing,[9] passivation type,[10] and layer thickness.[11] A composition of 15.8% was evaluated for lattice-matched InAlN to GaN grown on sapphire.[5] The question of the "true" InAlN composition might be also the reason for significantly different band gap energy which follows from published results, e.g., 4.03 and 4.6 eV.[12,13] It should be also noted that the highest current gain cutoff frequency on GaN-based HFETs was obtained using "nearly lattice-matched (NLM) (x=14%)" InAlN.[1] On the other hand, this fact needs to be considered if a comparison of InAlN/GaN material structures and devices of different origin will be made.

In this letter, a comparative study of the InAlN/GaN/Si heterostructures and HFETs with NLM and tensely or compressively strained (CS) InAlN is presented. The sheet charge density evaluated was found to be in agreement with calculated one for spontaneous and piezoelectric polarization, i.e., it increased with decreased InN mole fraction in the InAlN. The saturation drain current and extrinsic transconductance of the HFETs increased proportionally to the sheet charge density. As expected, the threshold voltage increased with the InN mole fraction. The pulsed current-voltage (I-V) measurements show very low gate lag, which is nearly identical for all three types of devices investigated. These results show that material structures with tensely strained (TS) InAlN can be preferable for high power devices while CS InAlN might be suitable for the preparation of normally-off switching devices.

The InAlN/GaN heterostructures used in this study were grown by metal-organic vapor phase epitaxy on Si(111) substrate.[14] They consisted of ~2 μm GaN insulating buffer layer followed by a 1 nm AlN spacer layer and a 10 nm InAlN barrier layer. Heterostructures with three different compositions of the InAlN were prepared. The first one was with an InAlN NLM to GaN—designated as NLM in the next. The other two were with tensely and CS InAlN barrier layer—designated as TS and CS, respectively. Conventional transistor fabrication steps, known for AlGaN/GaN HFETs, were used for the device preparation. At first, a multilayered Ti/Al/Ni/Au sequence for the ohmic contacts was evaporated and patterned. Afterwards, mesa isolation by ion beam etching in an Ar plasma was made. The ohmic contacts were formed by rapid thermal annealing at 800 °C for 2 min in a

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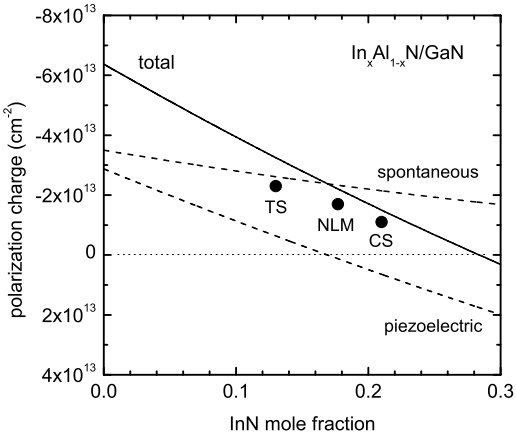

FIG. 1. Experimentally evaluated sheet charge density for three InAlN/GaN heterostructures used in this study (full dots) in comparison with calculated polarization charge as a function of InN mole fraction in InAlN.

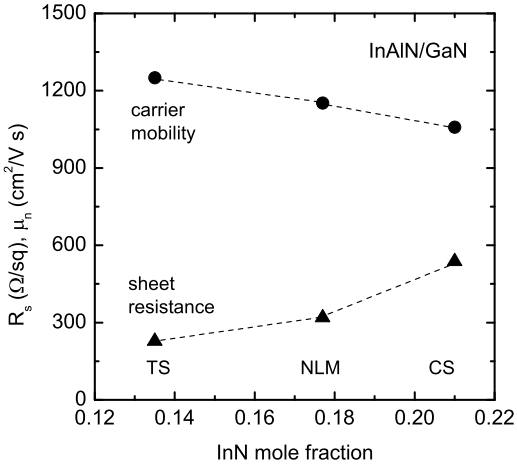

FIG. 2. Sheet resistance and carrier mobility of InAlN/GaN heterostructures with TS, NLM, and CS InAlN layer.

N_2/H_2 forming gas atmosphere. Finally, Ni/Au Schottky gate contacts were patterned by electron-beam lithography. Passivated devices (120 nm SiN) with a gate length ranging between 0.5 and 2.5 μm and a gate width of 2×50 and 2×100 μm were prepared.

The InAlN/GaN heterostructures were characterized at first. Composition of the InAlN barrier layer was evaluated by x-ray diffraction (XRD) and x-ray photoemission spectroscopy (XPS). The XRD measurements yielded $x=0.175$ for NLM structure and 0.13 and 0.21 for the TS and CS structure, respectively. The XPS evaluation showed similar data, the difference in the InN mole fraction was less that $\pm1\%$.[15] From both types of measurements it follows, beside the differences obtained that the three structures used in this study can be well described as NLM, TS, and CS structures. The sheet charge density evaluated increased with decreasing the InN mole fraction, from 1.1×10^{13} cm^{-2} for CS structure to 1.7×10^{13} cm^{-2} for NLM structure and to 2.2×10^{13} cm^{-2} for TS structure. These data can be well compared with calculated total polarization charge in InAlN of different composition, as shown in Fig. 1—the measured data are about 74% of the theoretical values. The sheet resistance was 530, 320, and 230 Ω/sq and the carrier mobility was 1060 cm^2/V s, 1150 cm^2/V s, and 1250 cm^2/V s for the CS, NLM, and TS structures, respectively, as shown in Fig. 2. One would expect a decrease in the carrier mobility with increased carrier density, i.e., with decreased In content. However, the difference in the mobility data is less than $\pm10\%$.

Performance of the InAlN/GaN HFETs was evaluated by static output and transfer measurements as well as by pulsed *I-V* and frequency dependent capacitance-voltage (*C-V*) measurements. The static characterization typically yielded the saturation drain current of 1.4 A/mm, 1.2 A/mm, and 1 A/mm at $V_G=+2$ V for TS, NLM, and CS devices, respectively. These data scale well with the sheet charge density dependence on the InAlN composition. The threshold voltage shifted to higher values with increased InN mole fraction, from -7.2 V (TS) and -5.5 V (NLM) to -3.5 V (CS structure). Transconductance measurements yielded similarly an improvement with decreased InN mole fraction in the InAlN barrier layer, as shown in Fig. 3. The peak extrinsic transconductance increased from 186 mS/mm for CS structure to 215 mS/mm for NLM and to 230 mS/mm for TS structure. The gate voltage at which the transconductance maximum occurred has shifted from -3.2 V for the tensile-strained InAlN to about zero voltage for the CS InAlN barrier layer.

The room temperature *C-V* measurements have shown similar shifts in the threshold voltage to higher values with increased InN content in the InAlN as obtained from the static characterization. The sheet charge densities evaluated from the 1 MHz measurements were nearly identical with those evaluated from the static measurements on all three types of devices. This indicates that low trapping effects might be expected at high-frequency operation. The thickness of the InAlN barrier was in the range of 10.1–10.8 nm as evaluated from the zero bias capacitances. This is in good agreement with the nominal thickness of 10 nm.

Pulsed *I-V* characteristics were measured to evaluate an effect of the lattice mismatch on the gate lag of the InAlN/GaN HFETs. Measurements were performed using a pulse width of 1 μs and a duty cycle of 0.1%. A comparison of the static *I-V* characteristics measured at $V_G=0$ V and pulsed characteristics in which the gate was pulsed from the threshold voltage to $V_G=0$ V is shown in Fig. 4. From this result it follows that the gate lag is relatively small and nearly identical for all three types of devices investigated. Thus, accord-

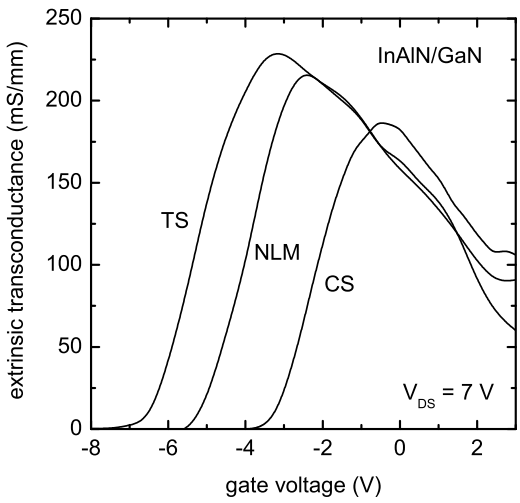

FIG. 3. Transconductance characteristics ($V_{DS}=7$ V) of InAlN/GaN HFETs with TS, NLM, and CS InAlN layer.

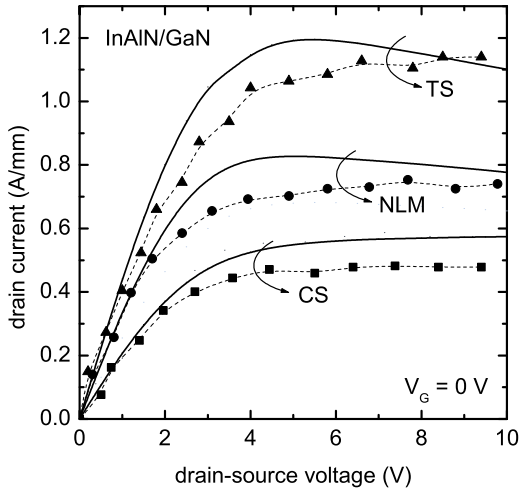

FIG. 4. Static (full lines) and pulsed (full marks) *I-V* characteristics for InAlN/GaN HFETs with TS, NLM, and CS InAlN layer.

ing our result, tensile or compressive strain in InAlN barrier layer has no significant influence on the gate lag of InAlN/GaN HFETs. This is in contradiction to previous reported data, however obtained on unpassivated devices.[5] Details on the pulsed behavior of the devices investigated, e.g., gate lag versus drain lag, different quiescent bias points, etc., will be published elsewhere.

In summary, properties of the InAlN/GaN heterostructures and field-effect transistors with nearly lattice matched and tensely or CS InAlN barrier layer were evaluated and the results can be described as follows:

(i) Structures with strained InAlN show higher sheet charge density and saturation drain current, i.e., they are preferable for high-frequency and high-power devices.

(ii) Structures with CS InAlN might be useful for the preparation of enhancement mode GaN-based devices (recently a positive threshold voltage has been reported on InAlN/GaN HFET with an InN mole fraction of 25% in InAlN).[16]

(iii) The gate lag of devices investigated was relatively low and nearly identical independent on the InAlN composition.

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