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Advanced high-k gate dielectric amorphous $LaGdO_3$ gated metal-oxide-semiconductor devices with sub-nanometer equivalent oxide thickness

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Careful selection of pulsed laser deposition conditions was executed to achieve sub-nanometer EOT (equivalent oxide thickness) in amorphous $LaGdO_3$ based high-k/metal gate stacks. The lowest EOTs attained were ~5.4 Å and 8.4 Å with and without quantum mechanical correction, respectively. The electrical measurements yielded a high permittivity of 20.5 ± 2.4, a thin bottom interfacial layer of thickness 4.5 ± 1 Å, and interface ($cm^{-2}eV^{-1}$) and fixed (cm^{-2}) charge densities of ~10^{12}. Analysis of temperature dependent leakage currents revealed that gate injection current was dominated by Schottky emission below 1.2 MV/cm and quantum mechanical tunneling above this field. The physical origin of substrate injection was found to be a combination of Schottky emission and trap assisted tunneling. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4805037]

According to the International Technology Roadmap for Semiconductors (ITRS)[1] Process Integration, Devices, and Structures 2 (PIDS2) table for future high performance logic technology devices (based on extended planar bulk), an equivalent oxide thickness (EOT) of 6.5 Å is required as early as 2013. Lanthanum oxide (La_2O_3) and Gadolinium oxide (Gd_2O_3) with the most stable configurations (trivalent with M_2O_3 formula) in the Lanthanide series are identified as two of the most promising candidates for advanced CMOS (complementary metal-oxide semiconductor) devices due to their high permittivities (~27 (Ref. 2) and ~15 (Ref. 3)), large band gaps (~5.7 and ~5.3 eV, between occupied oxygen p and unoccupied rare earth d levels), and compatibility with silicon even at elevated temperatures. A ternary oxide of La and Gd are expected to have the added advantage of higher moisture resistance without sacrificing permittivity and large band gaps. In their bixbyite cubic structures, La_2O_3 and Gd_2O_3 with lattice parameters ~1.1325 nm and 1.085 nm show ~+3.9% and −0.46% lattice mismatch, respectively, with Si ($2a_{Si}$ ~ 1.09 nm). So the epitaxial films of the resultant ternary oxide will have a lower strain when grown on Si. This aspect is attractive as the epitaxial growth of high-k oxides on silicon for an abrupt interface (with a low interface trap density) and minimized leakage currents is an intensive area of research. It is worth to mention that a ternary oxide composed of metal ions such as La and Gd from the first half of the lanthanide series is likely to have lower Si diffusivity; as the atomic number increases the ionic radii decreases (lanthanide contraction) and the diffusivity of Si from substrate into the metal-oxide layer increases.[4] This is beneficial for the bottom interfacial layer (IL) thickness control. The IL containing silicate with moderately higher k value (lower than that of oxide layer) will help in reducing the gate dielectric leakage (standby power) considering the observed inverse proportionality between permittivity (k) and band gap (E_g).[3] Taking all these aspects into account, we have identified[5] the ternary high-k material $LaGdO_3$ (LGO) based upon interlanthanide oxides with higher linear permittivity (~22),[6] larger band gap (~5.6 eV),[7] and sufficient electron- (~2.57 eV) and hole- (~1.91 eV) band offsets on silicon,[7] as a promising candidate for the future generations of CMOS devices. In this paper, we report the efficient way to achieve sub-nanometer EOT in Pt/LGO (mono-dielectric layer)/Si high-k/metal gate (HKMG) stacks (for gate last process flow with lower thermal budget to preserve the device performance) with a minimized bottom IL, reduced dielectric layer thickness, and lower top IL in order to enable the world wide effort for continued scaling (Moore's law)[8] of metal-oxide-semiconductor (MOS) structures in logic devices and metal-insulator-metal (MIM) structures in memory devices.

Amorphous thin films of LGO were fabricated on two types of p-Si substrates by using pulsed laser deposition (PLD). One of the substrates was (111) oriented with ~3–6 Ω cm resistivity and the other was (100) oriented with ~0.1–1 Ω cm resistivity. The silicon substrates were ultrasonicated in acetone and then in methanol and finally immersed in 2% HF:H_2O solution for 30 s to remove the native oxide before loading to the PLD chamber. The LGO ceramic target was prepared in-house by pelletizing multiple calcined mixture of predetermined amount of La_2O_3 and Gd_2O_3 powders

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which was sintered at 1500 °C in air for 4 h.[6] The target to substrate distance was kept at 5 cm. The substrates were heated up to 300 °C, and high purity (~99.99%) oxygen at a partial pressure of ~1-2 mTorr was introduced in to the chamber halfway during heating to minimize the duration of exposure of H-terminated Si wafer to oxygen ambient. The total number of shots from a KrF excimer laser (248 nm, 1 Hz) with a fluence of ~3 J/cm^2 on target was in the range of 15–300 to grow different layer thicknesses. Intentional efforts were made during film fabrication to reduce the thickness of the high-k layer and that of the inter-layer at the high-k/semiconductor interface to achieve sub-nanometer EOT. Even though LGO is found to have a better moisture resistance, the as-grown LGO/Si(100) ultrathin hetero-structures were preserved in inert environment of high purity argon for improved functionality. Details of film growth conditions, and characterization, have been reported elsewhere.[9] The important approaches implemented towards achieving sub-nanometer EOT with reduced defects (e.g., Oxygen vacancies) in LGO layer and subdued high-k/Si interfacial reaction include (i) optimization of deposition temperature to a low value of ~300 °C, (ii) time of oxygen introduction in to growth chamber and duration of exposure of bare Si wafer to oxygen ambient, (iii) control of oxygen partial pressure to ~1-2 mTorr during ablation, and (iv) preserving the ultra thin heterostructures in inert environment of high purity argon. The physical thickness of the LGO layers on Si was determined with glazing incidence X-ray reflectivity (XRR) measurements and was found to vary from ~3 to 49 nm under different conditions of depositions. About 50 nm thin Pt gate metal electrodes of area ~2.5×10^{-5} cm^2 were deposited using dc sputtering (power density ~1 W/cm^2) through square metal shadow mask to form Pt/LGO/Si n-MOS devices. These HKMG devices were passivated using forming gas annealing treatment (90% N_2 + 10% H_2) at 400 °C for 20 min in rapid thermal annealing (RTA) chamber to reduce the interface trap density. The elemental composition and crystalline structures at the LGO (~8 nm)/Si interfacial layer were investigated by x-ray photoelectron spectroscopy (XPS) (after sputtering etches) and high resolution transmission electron microscopy (HRTEM) equipped with selected area electron diffraction (SAED). The capacitance-voltage (C-V) sweep was carried out at 100 kHz (50 mV AC drive signal) using HP4294A impedance analyzer. C-V curves were modeled using Hauser CVC program.[10] Temperature-dependent gate oxide leakage measurements were carried out in the range of 300-450 K with Keithley electrometer (model# 6517A) and a programmable Joule Thompson thermal stage system (MMR model# K-20).

The C-V characteristics of Pt/LGO/p-Si MOS devices measured at a frequency of 100 kHz are depicted in Fig. 1. As can be seen, the C-V curves show a counter-clockwise hysteresis during sweeping from inversion to accumulation (forward) and back to inversion (reverse). The observed hysteresis was larger for thicker gate oxide layers compared to the thinner ones and may be attributed to the presence of rechargeable oxide traps in them. An inconsistency in accumulation capacitance (×1.21) scaling with physical thickness reduction (×2.7) was noted while going from 16 nm film to 6 nm film. Even though LGO is having a better

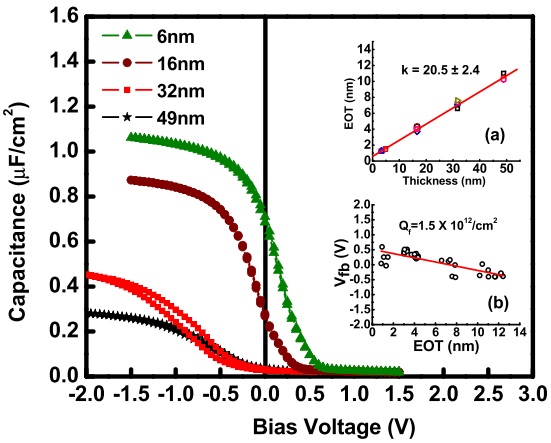

FIG. 1. High-frequency C-V curves of Pt/LGO/Si gate stacks with varying LGO thicknesses from 6 to 49 nm. (a) The XRR thickness plotted as a function of EOT of the MOS capacitors to estimate the k-value and interlayer thickness. (b) Flat band voltage versus EOT characteristics to extract the fixed charges.

moisture resistance than La_2O_3, the effect is not negligible. Also as the thickness reduces, the effect of lower k IL starts making effective contributions to the charge holding capability of the layer. The inconsistency can be attributed to these two facts. From Fig. 1, it is clear that the thinnest film (6 nm) is the worst affected (in terms of k-value) among the four as a result of ambient exposure. Experimental C-V plots with similar trend have already been reported elsewhere.[11] The dielectric constant (k) value was estimated to be 20.5 ± 2.4 from the accumulation capacitance density in terms of the EOT (without quantum mechanical correction) as a function of physical thickness of the LGO layer on both the types of substrates as shown in inset (a) of Fig. 1. It can also be concluded from the intercept on the EOT axis (in the same inset) that there exists an interfacial layer (perhaps of La-Gd silicate) having thickness 4.5 ± 1 Å with moderate high-k value (~8-14 for La silicate,[12] much higher than that of SiO_2) formed due to reaction between LGO and Si at the interface. In majority of the atmosphere/ambient-exposed thicker films with EOT more than 8 nm, we observed a negative flat-band voltage (V_{fb}) shift which is undesirable for CMOS applications and could be due to presence of positive oxide charges in the form of oxygen vacancies V_o^{2+} (Ref. 13) and/or due to incorporation of moisture [which replaces O_2^{-2} sites with $(OH)^-$ in amorphous ternary oxide].[14,15] On the other hand, the thinner films with EOT < 1.5 nm which were preserved in inert argon atmosphere generally exhibited the opposite trend, i.e., positive flat band voltage shift, indicating presence of negative charges in the form of interstitial oxygen (O_i^{2-}) in LGO. The overall flat band voltage shift in both the cases was in the range of ±0.5 V (roll-off and roll up). Despite the small uncertainties in the data points, the EOT versus V_{fb} plot as shown in the inset (b) of Fig. 1 was found to fit to a straight line indicating that dipoles at the high-k/Si interface are responsible for the observed V_{fb} shift and the fixed charge density Q_f estimated from slope of the linear fit was 1.5×10^{12}/cm^2

$$V_{FB} = \phi_{ms} - \frac{Q_f}{\varepsilon_0 \varepsilon_{SiO_2}} EOT = \phi_{ms} - \frac{Q_f}{C_{ox}}. \quad (1)$$

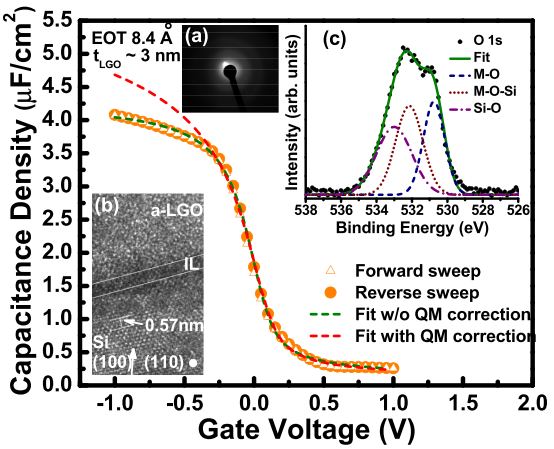

FIG. 2. C-V characteristics of Pt/LGO/p-Si n-MOS deices measured at 100 kHz including its Hauser fit with and without quantum mechanical correction (a) SAED image of a-LGO. (b) Cross-sectional TEM images of LGO thin film fabricated at 300 °C. (c) *Ex-situ* O1s XPS peak from ~8 nm thick LGO layer on Si after Ar+ sputtering etches.

Fig. 2 shows the C-V characteristics of Pt/LGO/p-Si n-MOS devices, with LGO physical thickness of ~3 nm (grown with better IL control and kept in Argon ambient), measured at 100 kHz. It can be seen that the C-V characteristics of the device are unsaturated (4.08 μF/cm^2 at −1 V) due to the extreme thinness of LGO layer and is close to ideal C-V curve with $V_{fb} \sim 37$ mV, threshold voltage V_t of ~1.11 V, a negligibly small hysteresis of ~2 mV (ΔV_{fb} between sweeps), and interface trap density D_{it} of $\sim 6 \times 10^{12}$ cm^{-2} eV^{-1}. The EOTs determined from the accumulation capacitance by fitting experimental C-V data to ideal simulation curve with and without quantum mechanical correction were ~5.4 Å and 8.4 Å, respectively. The reduced effect of Q_f on V_{fb} at lower EOT (and hence in higher capacitance density C_{ox}) plays a role in the observed very low V_{fb} which approaches the intrinsic value ϕ_{ms} as can be deduced from Eq. (1). The extrinsic frequency dispersion calculated using the relation $(C_{100kHz} - C_{1MHz})/C_{100kHz}$ was found to be ~14% which may be considered to have arisen due to several reasons such as parasitic effects (series resistance arising due to silicon bottom electrode imperfection and cable connection), quantum confinement, presence of interface traps, lossy interfacial layer, and gate leakage current density.[16] The cross-sectional image of one of the heterostructures with ~8 nm thick LGO layer studied using HRTEM as shown in Fig. 2(b) revealed a thin structure less IL of thickness ~6 Å between the LGO layer and Si substrate that was in good agreement with the deduced value from electrical measurements. The SAED pattern of the same LGO layer shown in Fig. 2(a) contains no sharp rings or bright spots indicating amorphous nature of the PLD-grown LGO layer. The observed non-direct-contact between LGO and Si substrate [due to formation of La-Gd silicates (dark layer) and/or silicon oxide (SiO_x) interlayer at the interface] was further investigated using XPS as shown in Fig. 2(c). The O1s spectra of LGO layer were found to be asymmetrical with much wider line width (FWHM) of ~3.2 eV compared to that of symmetrical O1s spectra of pure SiO_2 (narrower FWHM of ~1.8 eV)[17] indicating possible bonding of oxygen to La and Gd in addition to Si in the IL. Multiple oxygen bonding states were identified by Gaussian deconvolution of the O1s peak into three components corresponding to three different chemical compositions: viz. M (metal) –O-M (530.75 eV, FWHM ~1.4 eV), M-O-Si (532.15 eV, FWHM ~1.8 eV), and Si-O-Si (533 eV, FWHM ~2.3 eV)[18] and confirmed the findings from cross-sectional HRTEM measurements. The origin of the nonstoichiometric IL formation is due to the inter-diffusion of La and Gd in to SiO_x and/or Si in to LGO layer during the growth and is beneficial in two ways: (i) metal silicate has a higher permittivity[12] than SiO_x to boost the sub-nanometer EOT scaling and (ii) it produces less carrier (remote coulomb) scattering and mobility reduction.[19]

A key motivation in finding an alternative gate material is to reduce the gate-induced leakage current at sub-nanometer EOT regime. The non-linear I-V driven nano-capacitors form the basis for the future technology nodes. Temperature dependent J-E characteristics for n-MOS devices with 8.4 Å EOT were measured in the temperature range of ~27-177 °C in order to understand their charge transport mechanism(s) and device reliability and results are shown in Fig. 3. We observed moderate temperature dependence for the gate injection when negative voltage was applied to the Pt top electrode. At 300 K in the low oxide field regime (1.2 MV/cm $< q\Phi_B >$ 4kT ~ 0.1 V ~ 0.5 MV/cm), current grew faster with voltage and their dependence was plotted in Schottky coordinates (ln J versus $E^{1/2}$) as shown in Fig. 3(b). The linearity in the plot is suggestive of electrode/interface-limited Schottky conduction mechanism caused by field assisted thermionic emission of electrons over barrier Φ_B (~4 eV),[9] the energy offset between Pt Fermi level and LGO conduction band minima. Generally such plots are insufficient to discriminate unambiguously between Schottky and Poole-Frenkel mechanisms, since both give the same exponential field dependence, differing only by a factor of ×2 in the coefficient. Other tests are required, and often for high-dielectric oxides, it is necessary to use the Simmons modification[20] of the Schottky equation which has an "extra" factor of E in it and applies to systems in which the mean free path is shorter than the Schottky barrier width. However, the best check on this is the value fitted to the high frequency refractive index (n_∞) calculated using ln J versus $E^{1/2}$ plot; when the Simmons form is required, fits of the data to the ordinary Schottky equation usually give unrealistic values for refractive index n_∞. In our data fitting, n_∞ was within 50% of the values obtained from optical analysis of thicker films[7] and electrical studies on bulk ceramics,[21] so the Simmons correction is probably small. Based on these observations, we suggest that Schottky emission dominates the transport mechanism in low oxide field regime. In addition, the Mott plot (ln $IT^{0.5}$ vs $T^{-0.25}$, not shown here) followed a linear relationship indicating the contribution of trap assisted tunneling in the form of Mott hopping[22] due to the presence of interfacial and trap densities in the film. In the high oxide field regime (>1.2 Mv/cm, $< q\Phi_B \sim 4$ eV, in accumulation mode), current grew slowly with applied voltage and the voltage behavior was found to be nearly clamped. These features indicate that the major high-field conduction mechanism is direct quantum mechanical tunneling ($t_{LGO} \sim 3$ nm). A good linear fit of E × ln (J/E^2) vs $E^{3/2}$ plot[23] as shown in Fig. 3(c) confirmed this argument. One may note that the

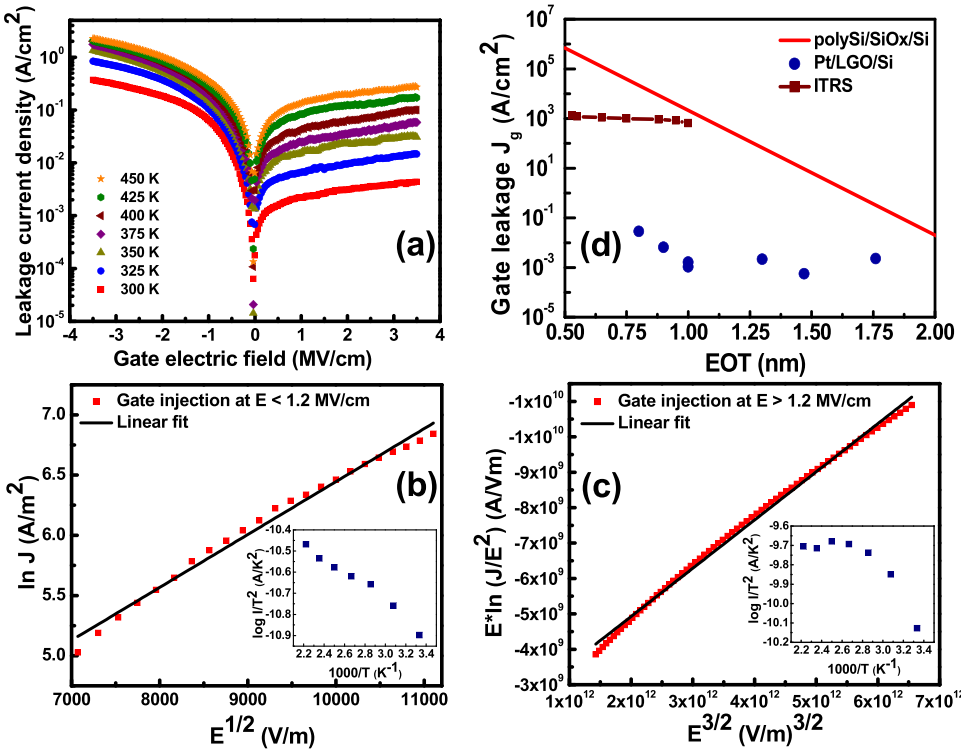

FIG. 3. DC current transport mechanism in Pt/LGO/p-Si devices after post deposition anneal in forming gas. (a) Temperature dependent J-E characteristics in the 300–450 K range. (b) Gate injection at low oxide filed ($E < 1.2$ MV/cm) in Schottky coordinates. The corresponding Arrhenius plot is given in inset. (c) Gate injection at high oxide filed ($E > 1.2$ MV/cm) fitted to direct tunneling with its deviation from Arrhenius relation shown in inset. (d) Comparison of leakage current densities of various LGO/Si ultra thin films with EOT ≤ 1.8 nm (without quantum corrections) with ITRS requirements and SiO_x/Si heterostructures at an applied gate voltage of 1 V below V_{fb}.

extent of deviation from linear of Arrhenius plots (log I/T^2 vs 1000/T), as shown in insets of Figs. 3(b) and 3(c), further validates the proposed physical origins of forward-bias conduction. For substrate injection with negative bias on Si, the reverse-bias leakage data showed greater temperature dependence than that for gate injection and it was found to fit linearly to Schottky expressions (plot not shown) in the entire field regime. The estimated slope was even smaller than that for low-field gate injection and is indicative of partial contributions from high-field emission of thermally activated carriers (linear Arrhenius plot, not shown here) from Si in to the conduction band of LGO in combination with trap assisted tunneling form one trap site to another (linear Mott plot, not shown) as explained in the case of low-field gate injection. One may note that, throughout our analysis, a linear voltage drop $\Delta V(t_{LGO})$ is assumed across the sample. In principle, there could be a non-linear drop at the interfaces, but the present data do not require or suggest that. Gate leakage current densities of various LGO ultra thin films on Si as a function of their respective EOTs and their comparison with ITRS limits[1] and classical SiO_x/Si heterostructures[24] are shown in Fig. 3(d). Leakage current densities (2.3×10^{-3} to 29×10^{-3} A/cm^2 for films with EOT 1.8 to 0.8 nm) of all the samples at an applied gate voltage (V_g) of $\sim$1 V below flat band voltage ($V_g = V_{fb} - 1$) are at least four or more orders lower than the stringent ITRS requirements and SiO_x films.

The interfacial layer thickness in LGO/Si ultra thin hetero-structures was minimized by controlling the pulsed laser deposition parameters and associated conditions to achieve sub-nanometer EOTs. The HKMGs exhibited high performance in terms of a close to ideal C-V characteristics, an electrical functional thickness of $\sim$5.4 Å and 8.4 Å with and without quantum mechanical corrections, and low leakage current density of $\sim 4.3 \times 10^{-3}$ A/cm^2, below the ITRS requirements and its SiO_x competitors. The composition of IL was analyzed by using HRTEM and XPS measurements, and it was found that the minimized metal silicate of high permittivity significantly facilitate the down-scaling of EOT. The physical origin of current transport during gate injection was found to be dominated by Schottky emission below 1.2 MV/cm and direct tunneling above this field. In summary, these studies revealed that LGO can be a promising candidate for the future sub-nanometer logic technology nodes, especially with gate last sequence, by incorporating highly conformal coating techniques such as atomic layer deposition (ALD) and high-aspect ratio geometries. Further efforts in this direction are underway.

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