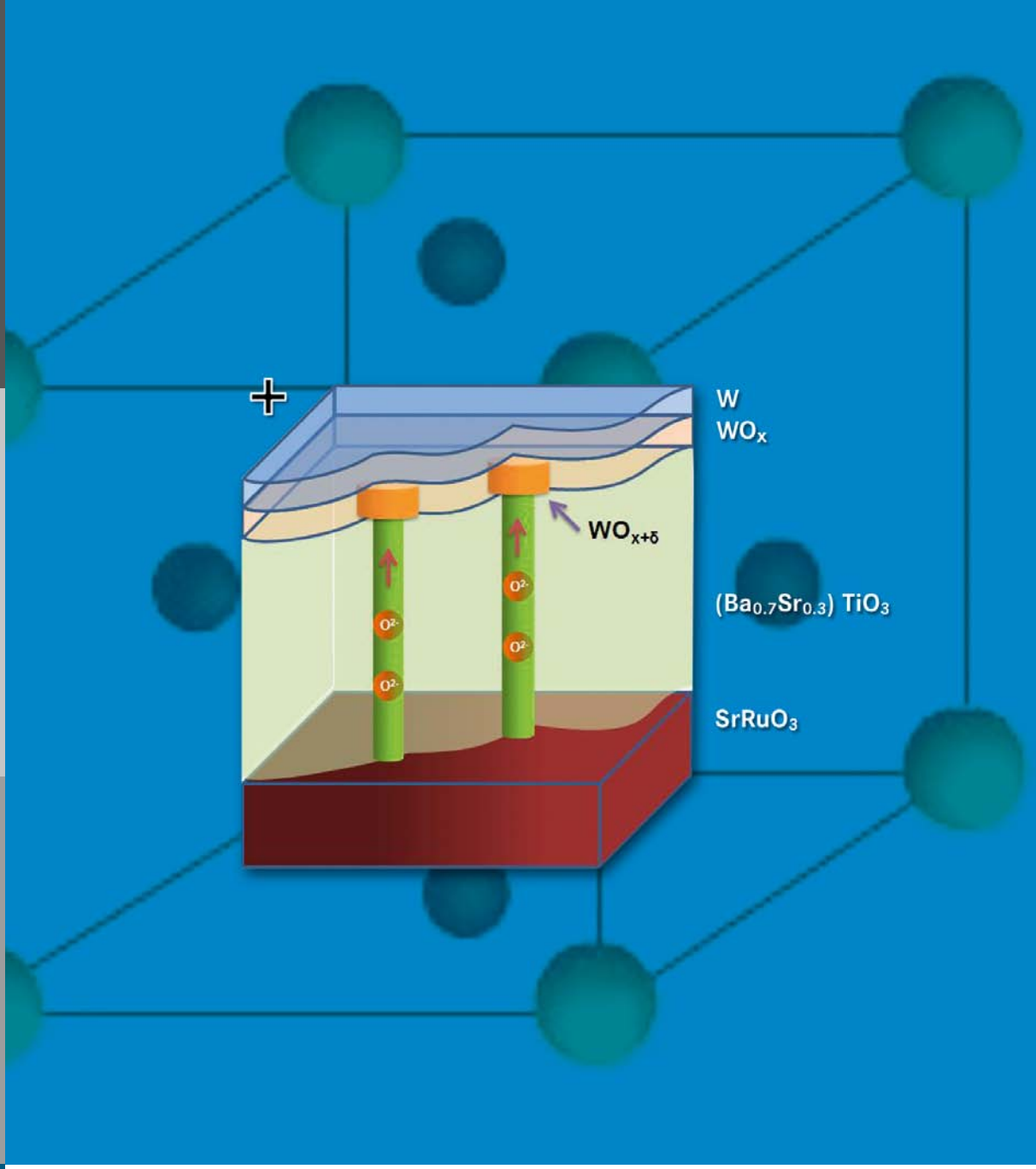

Investigation of resistive switching in barium strontium titanate thin films for memory applications

Wan Shen

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Kurzfassung

Das Konzept der „Resistive Random Access Memory“ (RRAM) hat wegen des niedrigen Stromverbrauchs, der hohen Schreib- und Lesegeschwindigkeit, der zerstörungsfreien Datenauslese und der potentiell hohen Integrationsdichte große Aufmerksamkeit auf sich gezogen und gilt als einer der vielversprechendsten Kandidaten für die nächste Generation nicht-flüchtigen Speicher.

Innerhalb dieser Dissertation wurde das resistive Schalten von dünnen BST Schichten mit unterschiedlichen kristallinen Eigenschaften untersucht. Die Qualität der dünnen Schichten und Dünnschichtbauelemente wurde durch eine Variation der Laser-Energiedichte optimiert. Obwohl die Kristallqualität durch die Verringerung der Laser-Energiedichte verbessert werden konnte, hat sich die Ausbeute der resitiv schaltenden Bauelemente auf diesen Proben von 67 % auf etwa 3% verringert. Das gibt einen Hinweis darauf, dass die beste Kristallqualität nicht zu den besten Schalteigenschaften führt, sondern das eine hohe Defektdichte vorteilhaft für die Beobachtung der Schaltphänomene in diesen Materialien ist.

Das bipolare resitive Schalten wurde an epitaktischen dünnen BST Schichten auf SRO / STO Substraten untersucht. Im Vergleich zu Proben mit Pt-Deckelektrode konnte die Ausbeute, die Ausdauer und die Zuverlässigkeit durch die Verwendung von W Deckelektroden stark verbessert werden. Während die Proben mit Pt-Elektrode nach wenigen Schaltzyclen eine schnelle Abnahme des Widerstandes beider resitiven Zustände zeigen, lassen sich proben mit W-Deckelektrode 10^4 mal ohne eine signifikante Widerstandänderung schalten. Der Widerstandabfall für die Proben mit Pt-Deckelektrode kann durch die Diffusion von Sauerstoff entlang der Pt Korngrenzen während des Schalten erklärt werden Für Proben mit W Deckelektrode führt möglicherweise die reversible Oxidation und Reduktion einer WO_X Schicht an der Grenzfläche zwischen W-Elektrode und BST Film zu einer Verbesserung der Ausdauer der resistiv schaltenden Bauelemente, indem ein irreversibler Verlust von Sauerstoff verhindert werden kann.

In polykristallinen BST Schichten wurde ein Übergang von bipolaren zu unipolaren resitiven Schalten beobachtet. Voraussetzung für die Beobachtung dieser Umwandlung ist, dass ein metallisch leitender niederohmiger Schaltzustand auftritt. Das Fehlen von unipolarem Schalten in einkristallinen Proben kann möglicherweise auf die Abwesenheit von Korngrenzen und den damit verbundenen Verarmungszonen oder auf den veränderten Wärmeübergang in polykristallinen Schichten zurückgeführt werden. Durch die Kontrolle der Schaltspannung kann man in polykristallinen BST Schichten reversibel zwischen bipolarem und unipolarem Schalten hin und her wechseln. Dieser reversible Wechsel kann möglicherweise auf die lokale Änderung der aufgeschmolzenen Filamente durch die Bewegung von Sauerstoffleerstellen zurückgeführt werden.

Abstract

Resistive random access memory (RRAM) has attracted much attention due to its low power consumption, high speed operation, non-readout disturbance and high density integration potential and is regarded as one of the most promising candidates for the next generation non-volatile memory.

The resistive switching behavior of Mn-doped $BaSrTiO_3$ (BST) thin films with different crystalline properties was investigated within this dissertation. The laser fluence dependence was checked in order to optimize the RRAM properties. Although the film epitaxial quality was improved by reducing the laser energy during deposition process, the yields fluctuated and only 3% RRAM devices with highest epitaxial quality of BST film shows resistive switching behavior instead of 67% for the samples with worse film quality. It gives a clue that the best thin film quality does not result in the best switching performance, and it is a clear evidence of the importance of the defects to obtain resistive switching phenomena.

The bipolar resistive switching behavior was studied with epitaxial BST thin films on SRO/STO. Compared to Pt top electrode, the yield, endurance and reliability were strongly improved for the samples with W top electrode. Whereas the samples with Pt top electrode show a fast drop of the resistance for both high and low resistance states, the devices with W top electrode can be switched for 10^4 times without any obvious degradation. The resistance degradation for devices with Pt top electrode may result from the diffusion of oxygen along the Pt grain boundaries during cycling whereas for W top electrode the reversible oxidation and reduction of a WO_x layer, present at the interface between W top electrode and BST film, attributes to the improved switching property.

The transition from bipolar to unipolar resistive switching in polycrystalline BST thin films was observed. A forming process which induces a metallic low resistance state is prerequisite for the observation of unipolar switching behavior. The absence of unipolar switching in single crystalline samples may relate to space charge depletion layers at grain boundaries and their impact on the electronic conduction properties as well as the different local heat transfer in thin films. By controlling the switching voltage, the bipolar and unipolar resistive switching can be alternated in polycrystalline BST thin films. The bipolar/unipolar alternation is dynamically repeatable and the alternation may relate to the local modification of broken filaments by breakdown or oxygen vacancy movement.

Acknowledgements

First and foremost, I owe my greatest thanks to my supervisor Professor Dr. Rainer Waser to give me the opportunity to do research in this group. I would like to thank Professor Dr. Georg Roth for his interest in this work and being my co-supervisor. I would like to thank Dr. Regina Dittmann for her support and guide in the last three years. I would like to thank Intel Inc., for the financial support they provided during my research in Juelich.

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Contents

Chapter 1

Introduction

1.1 Objectives

The ideal nonvolatile memory (NVM) should be excellent in terms of high density, low cost, low energy operation and high performance for potential applications. [1] Memories have constituted 20% of the semiconductor market for the last thirty years and the market share of memories is expected to continue increasing in the coming years. [2] Generally, the semiconductor memories can be divided into two categories, the volatile and the non-volatile memories using complementary metal–oxide–semiconductor (CMOS) technology. [3] Volatile memories are fast in writing and reading or can be integrated in very high density (DRAM) but once the power supply is turned off the data stored will be lost. In contrast, the nonvolatile memories can keep the data without power supply.

In 1988, Flash EEPROM consisting of a single EPROM cell was proposed.[4] The name Flash was given to emphasize the phenomenon that the whole memory array can be erased in a “Flash” involving a very short time.

According to Moore's law, the number of devices that can be integrated on a chip of fixed area would double every 18-24 months.[5] However, as predicted by International Technology Roadmap for Semiconductors (ITRS) [6, 7], the Flash cell reduction will face physical limits in the near future. Flash also suffers from general shortcomings like slow programming (from microseconds up to milliseconds), limited endurance (typically 10^5-10^6 write/erase cycles) as well as the need for high voltages (10-20V) during programming and erase. [8, 9]

In order to replace Flash, alternative technology has to be superior to it in scalability, cost per bit and device performance.[10] New materials that enable unique switching mechanisms have to be introduced and a variety of alternative memory concepts have been explored. Novel nonvolatile memories such as Ferroelectric Random Access

Memory (FeRAM), [11-15] Magnetic Random Access Memory (MRAM) [16-20] and Resistive Random Access Memory (RRAM) are being investigated.[21-27] FeRAM, MRAM and RRAM all store information by a resistance change caused by the ferroelectric polarization, magnetic field induced spin change or directly by electrical field stimulus. However, FeRAM and MRAM exhibit technological and inherent problems in the scalability. Among these novel nonvolatile memories, RRAM attracts more and more attention (Figure 1.1) for its nondestructive readout, low operation voltage, high operation speed, long retention time, and simple structures.

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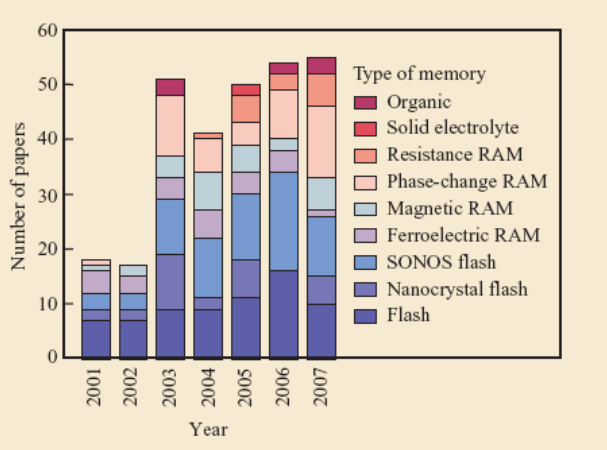


FIG. 1.1 Number of papers presented at the Symposium on VLSI Technology and the International Electron Devices Meeting (IEDM) from 2001 through 2007, categorized in terms of storage-class memory technology candidates.

1.2 Plan of Dissertation

There are still open questions about the physical origin of the resistance change in RRAM devices. The location of the resistance variation occurred at interface or in bulk film needs a further clarification. The role of defects during switching process is still not clear. Meanwhile, the reliability of RRAM devices needs to be improved as the fast fatigue observed in erase-write operations. For bipolar switching, the resistance ratio (R_{off}/R_{on}) is generally not high enough to easily read the memory states and there is also only bipolar switching observed in perovskite thin films.

In this dissertation the resistive switching behavior of BST this films was investigated in order to understand the resistive switching phenomena. In chapter 2 the experimental methods were introduced in fabricating RRAM devices. The SRO and BST thin films were deposited by pulsed laser deposition on STO single crystal. The metal thin films were sputtered or electron beam evaporated with followed lithography and dry etching to form top electrodes. For device structural characterization, AFM, XRD, SEM and ToF-SIMS were used. The quasi static electrical characterization was employed to measure the memory properties.

The thin film deposition by PLD was optimized by changing laser fluence which will be described in Chapter 3. Nano-imprint technology was also used to prepare nano electrodes in order to investigate the scaling and switching mechanism. Furthermore, the BST thin film based RRAM devices was prepared in cross-point structure to attest the scaling possibility and size dependence.

Chapter 4 mainly focuses on the bipolar resistive switching behavior of epitaxial BST thin films with Pt and W top electrodes. The characteristics of bipolar resistive switching phenomenon were introduced. For electrical characterization, Current-voltage (I-V) characteristics, pulse measurements were used. The endurance, retention behavior were investigated which shows BST thin film based RRAM device is promising to be used as non-volatile memory.

Chapter 5 will introduce both the bipolar and unipolar switching we observed in polycrystalline BST thin films. The bipolar to unipolar switching transition was firstly observed in perovskite thin films, which can be induced by a sufficient forming current. Moreover, by control the switching voltage, the bipolar switching and unipolar switching mode can be alternated.

1.3 Overview on the resistive switching

Since 1962 as firstly introduced by Hickmott, lots of reports have shown that varieties of oxide insulators in a Metal-Insulator-Metal sandwich structure exhibit resistance switching behavior. [28] The insulator material ranges from binary and multinary oxides to higher chalcogenides as well as organic materials. Here Metal stands for metal electrodes including metallic ceramic thin films. The current period for research in resistive switching behavior started in the late 1990s triggered by Kozicki *et al.*[29]and Beck *et al.*[30]

A working RRAM device generally consists of one resistor and one corresponding transistor or diode. [31] The resistor was prepared in the MIM structure and the resistance was used to store the data. The materials used in RRAM applications can be divided into perovskite oxide materials, binary metal oxide materials or organic materials.

1.3.1 Bipolar and unipolar resistive switching

There are two schemes related to the electrical polarity required for the resistive switching on the basis of I–V characteristics as seen in Figure 1.2 (a) and (b), respectively.[32] When the resistance change does not depend on the polarity of the voltage or current and the device can be switched between high resistance state (HRS) and low resistance state (LRS) with the same polarity, this polarity independent switching behavior is called unipolar switching. Another scheme is called bipolar switching which need opposite polarity of the applied voltage or current to switch the device between HRS and LRS.

Generally, the as-prepared memory cell is in a highly insulating state and then a high voltage stress was applied to trigger the device to a more conductive resistance state, which was called “forming”. After the forming process, the RRAM device can be switched from LRS to HRS (Reset) or from HRS to LRS (Set) by applying a voltage with current compliance to protect the device from permanent breakdown.

The unipolar switching and bipolar switching have been widely observed and researched in simple binary metal oxide such as NiO, [33] ZrO_2, [34] TiO_2, [35] while expect for the report by Choi et al., [36] generally only the bipolar switching is observed for complex perovskite type oxide (ABO_3) films, such as PCMO, [37] Cr-doped $SrZrO_3$, [38] and ($Ba_{0.7}Sr_{0.3}$) TiO_3. [39, 40]

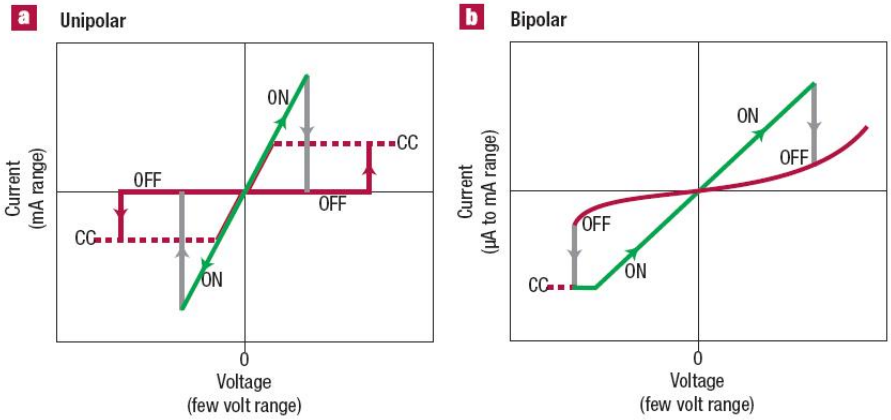


FIG. 1.2 Classification of the switching characteristics in a voltage sweeping experiment. (a) Unipolar switching. The set voltage is always higher than the voltage at which reset takes place, and the reset current is always higher than the current compliance during set operation. (b) Bipolar switching. The set operation takes place on one polarity of the voltage or current, and the reset operation requires the opposite polarity. [32]

Furthermore, there is only bipolar-unipolar transition observed in binary metal oxide. [41] The unipolar switching has much larger resistance change than the bipolar switching, and this makes it much easier to read the memory state. [42] In addition, devices using unipolar switching can be potentially integrated in higher density. [43]

1.3.2 Resistive switching mechanism

A large variety of physical phenomena can lead the resistive switching effects as shown in Figure 1.3.[28] In this dissertation only the valency change memory effect and thermo-chemical memory effect will be discussed. The valency change resistive switching effect

generally shows bipolar switching behavior. Even though the exact microscopic mechanisms for bipolar resistive switching are still under controversial discussion, [44-48] there exists a general agreement that the migration of oxygen ions under an applied electric field plays a key role. [49] Since oxygen vacancies work as the donors in oxide-based semiconductors, the field driven local accumulation or depletion of oxygen vacancies may be identified with the two resistance states. It has been proposed that the reduction or increase of oxygen vacancies may change the Schottky barrier height at the oxide-electrode interface and will thereby modulate the device resistance. [50, 51] The movement of oxygen vacancies may either occur homogeneously perpendicular to the whole electrode area as supported by the experimental data of Sawa *et al.* [50] or it may be restricted to defect-rich filaments within the bulk oxide matrix. [51, 52]

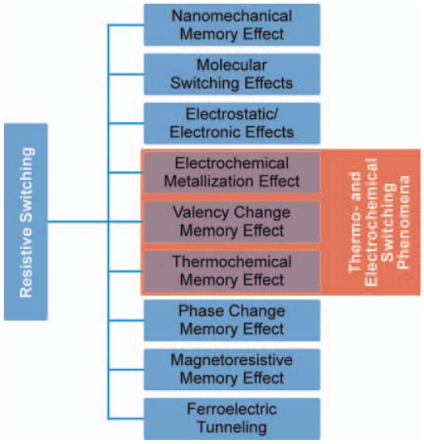


FIG. 1.3 Classification of the resistive switching effects which are considered for non-volatile memory applications. [28]

The thermo-chemical memory effect shows unipolar switching behavior. The unipolar resistive switching is thought to be the fuse/antifuse of conduction paths or filaments. For devices exhibit unipolar switching, forming is always necessary to transform thin film from highly insulating to a more conductive state to realize the unipolar resistive switching. During the electroforming process the device consumes large amount of electric power and the power dissipation in the cell is estimated to be high enough (Figure 1.4) to form the conduction paths between top and bottom electrode. [53]

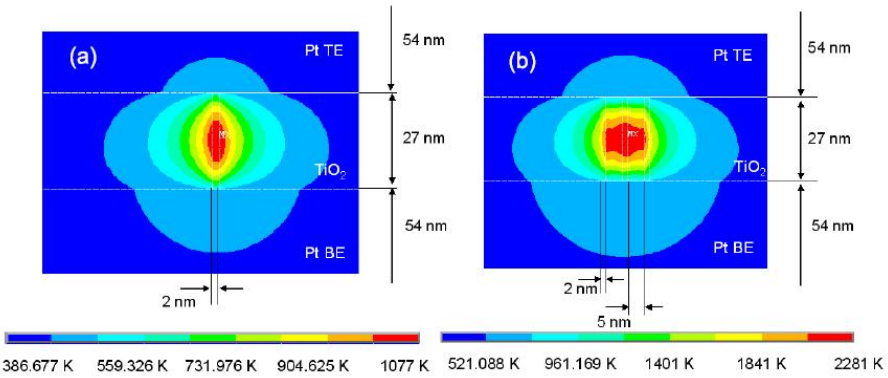


FIG. 1.4 Calculated temperature distributions under a constant voltage of 1 V using finite element analysis (a) for a single conduction path and (b) for three conduction paths neighboring with each other. [53]

1.4 Overview on the perovskite oxides

Perovskite is one of the most common structures among complex oxides. The ideal perovskite ABO_3 structure can be regarded as a cube with large A-cations and small B-cations as shown in Figure 1.5. Along the cubic <001> direction the repeating stacking sequence is AO/BO_2. The A-cation can be an alkaline, alkaline-earth or rare-earth element, while the B-cation is normally a transition metal element.

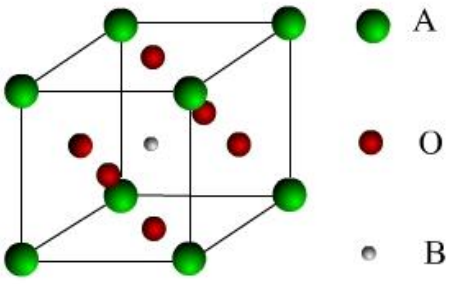


FIG. 1.5 The cubic unit cell of perovskite ABO_3 structure.

The perovskite ($Ba_{0.7}Sr_{0.3}$) TiO_3 (BST) has been widely used as high dielectric material for dynamic random access memory (DRAM) and tunable microwave phase shifters. BST is a solid solution of $BaTiO_3$ and $SrTiO_3$ and the Ba/Sr ratio strongly affects the physical properties. The Ba^{2+} and Sr^{2+} alternately occupy the A-sites according to the Ba/Sr ratio. For ($Ba_{0.7}Sr_{0.3}$) TiO_3 there are 70% Ba^{2+} and 30% Sr^{2+} in which the room temperature phase transition [54] and a maximum dielectric constant exceeding 5000 [55] has been observed.

For application as RRAM, the BST thin film based devices have been investigated by R. Oligschlaeger *et al.* [39]. The capacitor-like $SrRuO_3$/($Ba_{0.7}Sr_{0.3}$) TiO_3 /Pt structure was epitaxially grown on $SrTiO_3$ substrate and a weak but stable hysteresis in the current voltage curve was observed. The high or low resistive state as well as intermediate states can also be switched by applying short voltage pulses. However, the device endurance is facing big problems and the devices show fast resistance degradation, which will hinder its potential applications working as memories.

Chapter 2

Experimental methods

In this chapter, details of device fabrication techniques and experimental methods used to characterize the samples are presented. STO single crystal substrate were etched and annealed to induce step flow growth of thin films. The pulsed laser deposition was used to deposit SRO bottom electrode and BST working layer. Pt thin films were deposited by DC sputtering and W film was deposited by electron beam evaporation. Photo lithography and ion beam etching was applied to form top electrodes. The major analytical tools employed are atomic force microscopy (AFM), scanning electron microscopy (SEM), time of flight secondary ion mass spectroscopy (ToF-SIMS) and the current-voltage (I-V) measurements.

2.1 Device fabrication methods

2.1.1 RRAM device structure description

Sandwich Structure

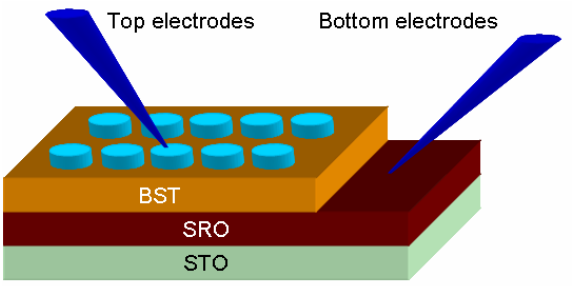


FIG. 2.1 Test TEL/BST/SRO/STO RRAM device structure.

In order to elucidate the mechanism of resistive switching in BST thin film and to clarify

the suitability for future RRAM devices, the test devices were fabricated and characterized in sandwich structures, which are shown in Figure 2.1. BST thin film was sandwiched between top and bottom electrodes with different size. Generally the fringe effect can be neglected because the top electrodes are much large (50-1000 μm in diameter) in comparison with the film thickness (45-200nm).

The device fabrication process of the test RRAM in sandwich structures can be divided into the following steps:

1) Deposition of SRO thin film to form bottom electrode (PLD).

2) Deposition of the BST working layer (PLD).

3) Deposition of top electrode film Pt (DC sputtering) or W (e-beam evaporation)

4) Pattern the top electrodes by photolithography.

5) Etch the patterned devices and form top electrodes.

Cross-point structure

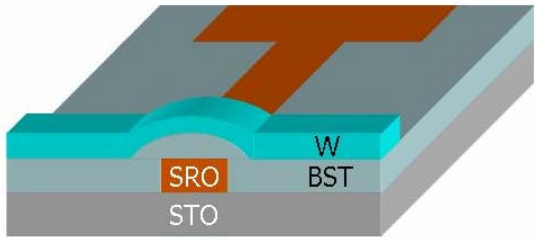


FIG. 2.2 Cross-point structures prepared on STO substrate.

For investigation of scaling and integration possibilities of RRAM devices, the cross-point structures were prepared on STO substrate as shown in Figure 2.2. The device fabrication process of the cross-point structures are as follows:

1) Deposition of SRO thin film (PLD).

2) Patterning of the SRO thin film by photolithography and etching to form bottom electrode.

3) Deposition of the BST working layer (PLD).

4) Deposition of top electrode film W (e-beam evaporation) or Pt (DC sputtering) .

5) Patterning of the top electrodes by photolithography and etching to form top electrodes and exposure the SRO bottom electrodes.

2.1.2 Substrate preparation

It is advantageous to grow thin films with a step-and-terrace surface. TiO_2 terminated terrace structure guarantees the step flow growth of SRO thin film bottom electrode and prevents the formation of pinholes in the subsequently deposited BST thin film. Figure 2.3 shows the surface of BST and SRO films directly deposited on an as-received STO substrate. It is clear that a lot of pinholes formed after deposition and the pinholes may lead to device failure and form short circuit between top and bottom electrodes. All step edges on the terrace surface should have equal height (single unit cell 0.4 nm) and the steps should be approximately parallel and equidistant. To achieve the terrace surface, we have to go through the following two steps:

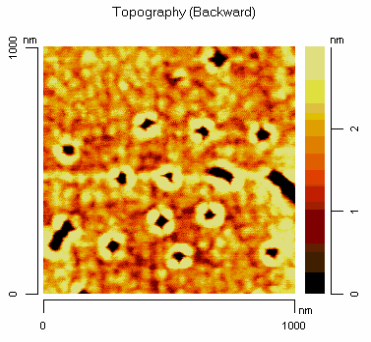


FIG. 2.3 Surface of BST and SRO films directly deposited on an as-received STO substrate. Lots of pinholes were formed after deposition.

1) Etching.

$SrTiO_3$ substrates can be etched in NH_4F-HF (buffered HF or BHF) at room temperature

to obtain a TiO_2 terminated terrace surface. Etching is a chemically selective process and the BHF preferentially removes Sr and ensure that the STO surface is purely TiO_2 terminated. The BHF etchant attacks the Sr at the step edges, dissolving it and then remove Ti by lift-off as shown in Figure 2.4. [56] The pH value should be carefully controlled because large numbers of etch pits could appear if the pH is too low, or residue remains on the surface if the pH is too high. In our experiment we choose BHF with pH 6.5 and the etching time varies from 100s to 210s.

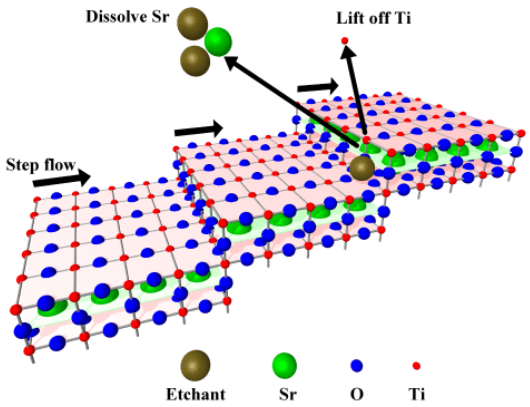


FIG. 2.4 The etching process of STO substrate. The BHF etchant attacks and dissolves the Sr at the step edges, and then remove Ti by lift-off. [56]

2) Annealing

Annealing process gives a near-perfect terrace surface, which is mostly Ti terminated. There are no Sr islands on the surface and all steps have single unit cell of 0.4 nm height. Steps are not bunched and the step direction is determined by the crystal miscut direction.

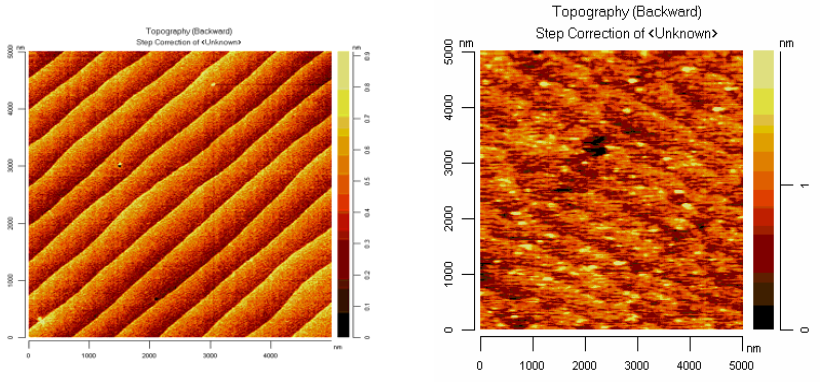


FIG. 2.5 (a) surface of the treated STO substrate and (b) surface after SRO and BST deposition. The pinholes were notably reduced.

Figure 2.5 (a) shows the surface of the treated STO substrate. The substrate was etched in BHF (pH 6.5) for 210s and annealed at 950°C for 2 hours. The surface is very smooth with RMS=0.15nm and the terraces were perfectly formed. The surface after SRO and BST deposition is shown in Figure 2.5 (b). The RMS increased a little to 0.28 nm and the pinholes were notably reduced compared to Figure 2.3.

2.1.3 Pulsed laser deposition (PLD)

Pulsed laser deposition technique is a popular method for deposition of multi-component materials because it generally could keep the stoichiometry from a given ceramic or single crystalline target to the deposited thin films.[57] The working principle of the PLD technique is displayed in Figure 2.6 (a). A short, ns range, pulse of an excimer laser beam is transferred through a optical system to the rotating target. Because of the high energy of the laser pulse, the target surface can be evaporated and immediately forms plasma, containing energetic neutral atoms, ions and molecules. The so-called “plume” reaches the substrate surface with an energy of 0.1 to > 10 eV, depending on the pressure of the background gas environment. As a result of the short, high energetic laser pulses, the evaporated material is not in the thermodynamic equilibrium and the relative amount of

different compounds in the plume corresponds to the target composition even for strongly-differing melting points. A chronological resolution of the evolution of the plume can be found in Figure 2.6 (b).

For substrate purposes, commercial STO single crystals [(100) orientation, Crystec GmbH] with an area of 1 x 1 cm^2 and about 1 mm thick are used. Thin films were deposited at substrate temperature of 700 °C with the working O_2 pressure of 0.25 mbar. The laser frequency is chosen as 10Hz. After one deposition, the target was replaced by turning the target carousel and positioning another target into the laser beam without breaking the low vacuum, thus allowing an in-situ deposition of the resistive switching thin films of interest.

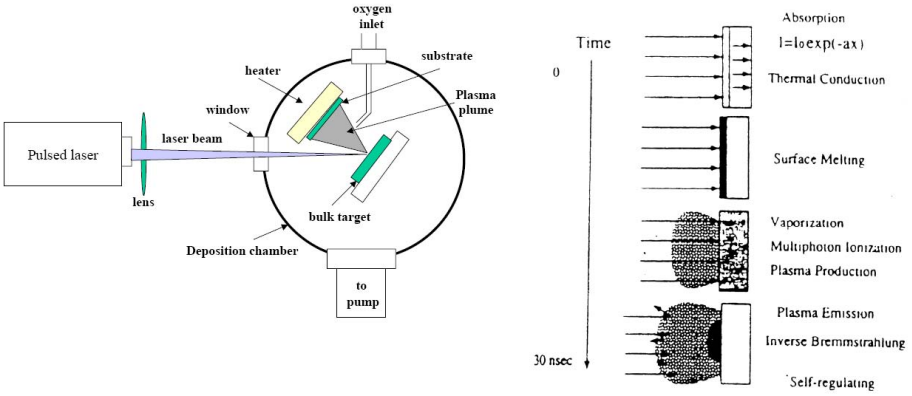


FIG. 2.6 (a) Set-up of a PLD chamber and (b) Time evolution of the plasma emission.

2.1.4 DC sputtering

Sputtering is a physical process and removes fractions of the material from the target which is subsequently deposited onto a substrate. Sputtering is achieved by bombarding the target surface with Ar ions which were accelerated in high electrical field. As a result of the ion impingement, atoms (or occasionally molecules) are ejected from the target

surface due to the momentum transfer by the impinging ions.[58] The bombarding ions are formed by a glow discharge process, where inert gas atoms are ionized by an electric discharge to form plasma. Plasma is usually created with argon gas which is fed into the sputtering chamber.

In our experiment, the Pt film was sputtered to form Pt top electrodes. In DC sputtering the Pt target is negatively biased (typically up to few hundred volts) to attract Ar^+ ions and make collisions on the target surface. These attracted Ar^+ ions also responsible for the production of secondary electrons which cause further ionization of the sputtering gas. A sufficient ionization rate is required to keep the plasma stable. One method to increase the ionization probability is to increase the partial pressure of the sputtering gas (i.e., increasing the gas pressure, more collisions result in the formation of more ions). Increased ion current to the target results in higher depositions rate. However, at very high pressures, sputtered target atoms get scattered before reaching the target and it reduces the deposition rate. Therefore a peak in the deposition rate versus pressure curve occurs. Schematic of a DC sputtering setup with Ar sputtering gas is shown in Figure 2.7.

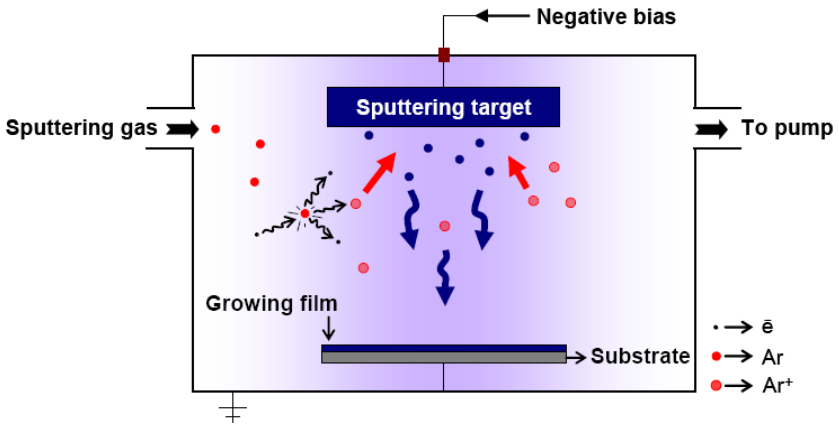


FIG. 2.7. Schematic of a simple sputtering setup with Ar as sputtering gas.[58]

2.1.5 Electron beam evaporation

The Electron Beam Evaporation (also know as e-beam evaporation) process was generally known as Physical Vapor Deposition (PVD). PVD processes are commonly used for the deposition of metals, because they can be performed at lower process risk and cheaper in regards to materials cost in Chemical Vapor Deposition (CVD), and also deposited materials witch are not easily be deposited like W.

In the evaporation process, W target was heated to the point (5555°C)[59] where it starts to boil and evaporate. Then it was deposited on BST/SRO/STO devices for 20nm, because for thicker W films there will be cracks induced by stress. The electron beam was used to heat the W target and cause evaporation. In order to protect the W layer from oxidation, we deposited in-situ a Pt protection layer on top of the sample.

2.1.6 Photolithography process

Photolithography is used in our experiment to transfer patterns from photomask (reticle) to the surface of RRAM devices. After this process, the top electrodes will be patterned through photoresist on the devices and be ready to be etched.

The photoresists can be classified into two groups, positive resists and negative resists. A positive resist is a type of photoresist in which the portion of the photoresist that is exposed to light becomes soluble to the photoresist developer and the portion of the photoresist that is unexposed remains insoluble to the photoresist developer. A negative resist is a type of photoresist in which the portion of the photoresist that is exposed to light becomes relatively insoluble to the photoresist developer. The unexposed portion of the photoresist is dissolved by the photoresist developer. AZ 5214 E is a special photoresist capable of image reversal. Exposed areas may be selectively cross-linked by a

bake cycle after exposure. A flood exposure before development converts unexposed areas soluble, resulting in a negative tone image. The profile generated by such processing has a negative side-wall allowing for use in lift-off techniques. For sandwich structures we only use AZ 5214E as positive resist.

Prior to the spinning of photoresist on samples all residuals need to be removed by appropriate cleaning steps. The sample was first cleaned in acetone and then heated up to 90 °C for 3 min to get rid of moisture. Then the sample was cooled down for another 3 min. AZ 5214E photoresist is spin-coated at 4000 rpm to reach a film thickness of 1.4 μm followed by a soft bake at 90 °C for 3 minutes to remove excess solvents. Then the sample was cooled down again for the exposure process.

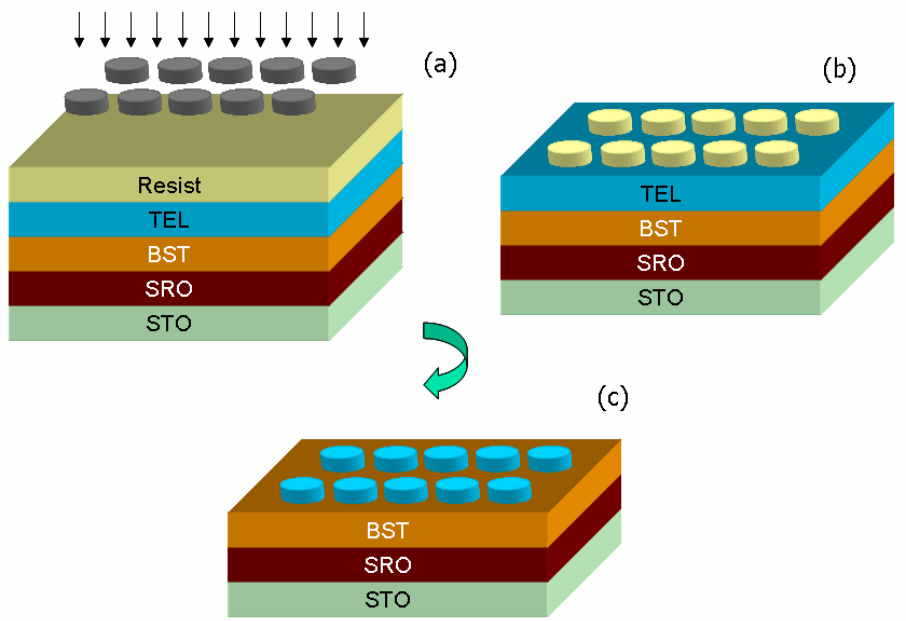


FIG. 2.8. Photolithography processes (a) sample was spin coated with AZ 5214E resist and exposed. (b) after developing, the pattern was transferred from mask to the sample. (c) when etch down, the top electrodes formed.

The sample with photoresist on top and the photomask are brought into contact by use of a mask aligner. The photomask is covered with chromium dots structures, which needs to be transferred to the sample. The assemble is then irradiated with UV light for 60s, whereby only the non-covered parts are exposed by the UV light.

To release the exposed structures, the sample was rinsed in a developer for 70s. Developers often contain sodium hydroxide (NaOH). By using the positive photoresist the developer will remove all exposed areas. The resulting sample is then "hard-baked", typically at 120 to 180 °C for 20 to 30 minutes. The hard bake solidifies the remaining photoresist, to make a more durable protecting layer in the following plasma etching process. Detailed illustration is shown in Figure 2.8.

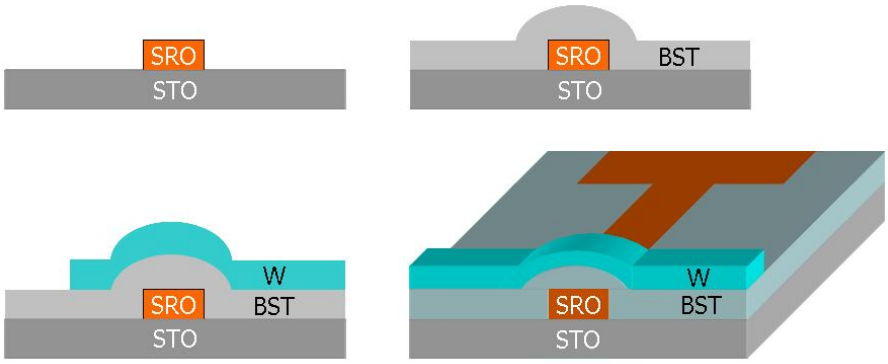


FIG. 2.9 Cross-point structures prepared on STO substrate.

For investigation of scaling and integration possibilities of RRAM devices, the cross-point structures were prepared on STO substrate. Figure 2.9 shows the detailed process. The 80 nm-thick SRO thin film was deposited by pulsed laser deposition (PLD). The deposition condition is described in § 2.1.3. The SRO film was patterned by lithography and reactive ion beam etching (RIBE) to form the bottom electrode. Then 45nm thick 0.2% Mn doped $Ba_{0.7}Sr_{0.3}TiO_3$ was deposited also by PLD in same condition.

For top electrode, 20nm W was e-beam evaporated and covered by 100 nm Pt in order to avoid the oxidation. The W film was patterned again by lithography and dry etching to form the cross-point structure.

2.1.7 Ion Beam Etching

Ion beam etching is a versatile etch process in which the substrate to be etched is placed in a vacuum chamber in front of the broad-beam ion source. Ions (typically argon) are generated inside the ion source and are accelerated into a broad beam, and to a defined energy, by the extraction grids on the front of the source.[60] As the ion beam etches the surface, the substrate is tilted to an angle in the beam and continuously rotated in order to optimize the uniformity. The wall angles in the resulting pattern being etched by the use of a photomask can be adjusted by tilting and rotating the sample during etching. Therefore, we use 45° tilt angle in our case.

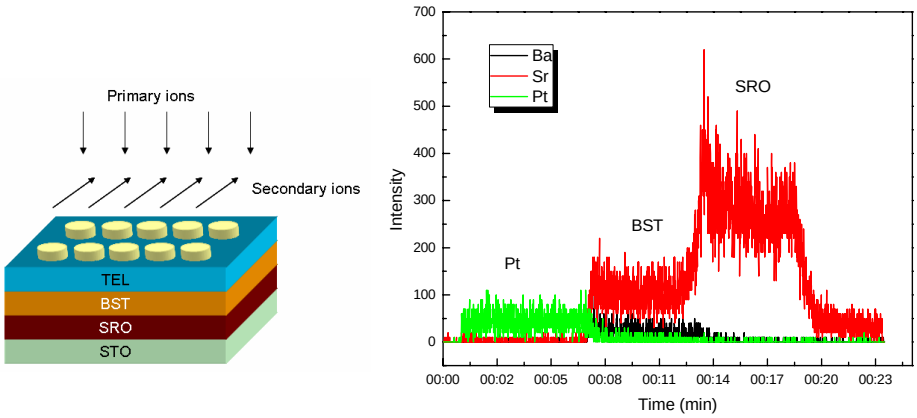


FIG. 2.10. (a) Illustration of the SIMS process during RIBE. (b) Secondary Ion Mass Spectrometry of Pt/BST/SRO/STO device.

Ion beam etching employs ion beam to physically sputter the sample surface. During sputtering, secondary ions are created at the surface with a mass to charge (m/z) ratio which is characteristic of the material at the surface. Secondary Ion Mass Spectrometry (SIMS) can be used to monitor the intensity of the secondary ion signal at specific m/z ratios, making it possible to detect which interface has been reached and which material was exposed [Figure 2.10 (a)]. Thus SIMS can be used to determine the end point of the etching process. Figure 2.10 (b) presents the SIMS result of the etching process for Pt/BST/SRO/STO and we could receive the ideal etching stop or etching depth.

2.2 RRAM device characterization methods

2.2.1 Atomic force microscopy (AFM)

Atomic force microscopy probes the sample and make measurements in three dimensions, x, y and z and enabling the presentation of three dimensional images of a sample surface. The principle behind the operation of an AFM in the contact mode is shown in Figure 2.11.[58] The AFM probe typically contains a sharp tip (made either of silicon or Si_3N_4) located at the free end of a cantilever. Forces between the tip and the sample surface can cause the cantilever bend, or deflect. A detector measures the cantilever deflections as the tip is scanned over the sample, or the sample is scanned under the tip. The measured cantilever deflections could be transferred by software to generate surface topography. To a large extent, the distance regime (i.e., the tip-sample spacing) determines the type of force that will be sensed. In our present investigation for surface topography only, we used non-contact mode to characterize the thin films. By replacing the silicon or silicon nitride probes to conductive tips, we could characterize the electrical conductivity or current distribution on the researched thin films. A DC bias is applied to the tip and the current passing through the BST thin film is measured to generate the conductive AFM

image. Obviously the contact mode was applied in this case.

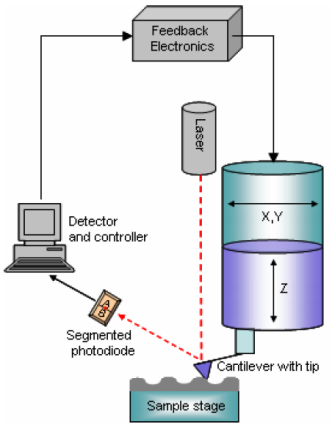


FIG. 2.11. Schematic diagram showing the operating principles of the AFM in the contact mode. [58]

2.2.2 X-Ray Diffraction (XRD)

X-ray diffraction (XRD) is a very powerful tool for materials science to identify crystalline and structural properties by recording and analyzing diffraction of x-rays by the closely spaced lattice of atoms in a crystal produces a pattern. [61, 62] In our experiment, mainly the (θ-2θ, ω) x-ray diffraction patterns of thin films were measured using the x-ray diffractometry.

θ-2θ scan

The θ-2θ scan provides information about the crystalline orientation of the crystal and the out-of-plane lattice parameters. A beam of x-rays, with wavelength λ, that reaches the crystal surface at angle θ is elastically scattered by electrons as shown in Figure 2.12 (a). The sample consists of rows of crystal planes that are separated by d, which is a distance between the atomic layers in a crystal. The constructive interference of the scattered

probe results in sharp diffraction peaks determined by the celebrated Bragg's law

$$n\lambda = 2d \sin\theta \qquad (2.1)$$

where n is integer.

ω-scan

The ω-scan, commonly known as a rocking curve measurement, gives the information on the texture and the crystalline quality of the films. For a (00*l*) oriented thin film, the ω-scan of a Bragg reflection, is performed to determine whether atomic layers are perfectly aligned with each other. To measure a ω-scan, the peak from the θ-2θ scan should be chosen and then the detector remains at a fixed position as displayed as black lines in Figure 2.12 (b), while the rocking curve is measured by rotating (or rocking) the sample around the ω circle. The ω-scan is defined as θ_0-θ as shown in Figure 2.12 (b). If the

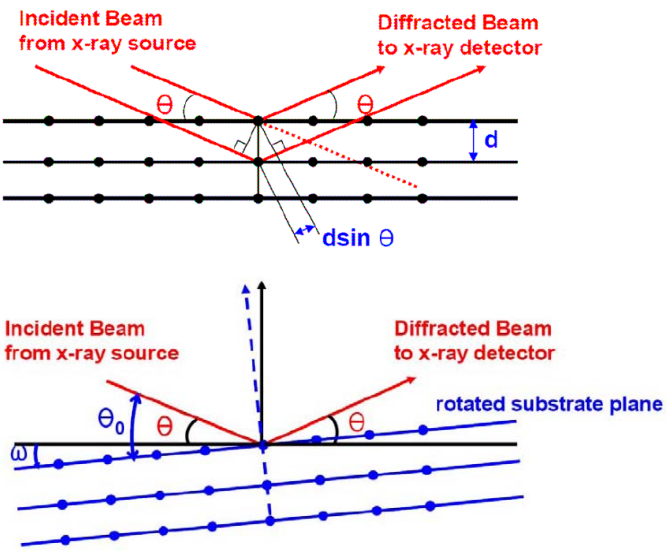


FIG. 2.12. Probing of the crystalline planes parallel to the surface. (a) Bragg diffraction of x-ray and (b) Schematic describing the ω-scan (Rocking curve).

sample is a single crystal or epitaxially grown thin film, the intensity of the reflected beam becomes zero because θ_0 does not satisfy the Bragg condition. On the other hand, if the sample is composed by atomic layers that are not perfectly aligned to each other, a finite intensity is measured. Therefore, the full width at half maximum (FWHM) in ω provides a measure of the spread in the orientation of the atomic layers aligned to each other.

2.2.3 Scanning electron microscopy (SEM)

Scanning electron microscopy (SEM) makes use of an energetically well-defined and highly focused beam of electrons to scan across a sample. The electrons interact with the atoms of the surface layers producing signals that contain information about the surface topography, elemental composition and other properties such as electrical conductivity. Two types of scattering will occur. Elastic scattering will induces back scattered electrons and inelastic interactions produce diverse effect including phonon excitation, cathode-luminescence, characteristic X-ray radiation, plasma production and Auger electron production.

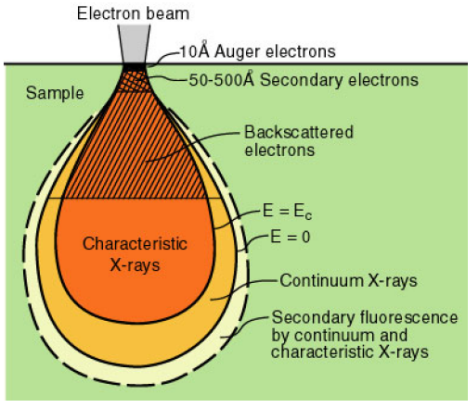


FIG. 2.13. Interaction volume showing the regions of various electron-specimen interactions. [58]

The primary electron beam interaction volume in the sample by SEM is a teardrop shaped volume. This volume extends from less than 100 nm to ~5 μm into the surface. The size of the interaction volume depends on the energy of the impinging primary electrons, the atomic number of the specimen and the specimen's density. Figure 2.13 schematically illustrates the interaction volume for various portions of electron-specimen interactions.

The common imaging mode collects the low energy secondary electrons (< 50 eV). The electrons originate from the top few nanometers below the sample surface. [63] These electrons are typically detected by an Everhart-Thornley detector [64] which is a type of scintillator photomultiplier device. The brightness of the signal depends on the number of secondary electrons reaching the detector. If the beam enters the sample perpendicular to the surface, then the activated region is uniform about the axis of the beam and a certain number of electrons escape from the sample. As the angle of incidence increases, the escape distance of one side of the beam will decrease, and more secondary electrons will be emitted. Thus steep surfaces and edges tend to be brighter than flat surfaces, which results in images with a well defined three dimensional appearance.

2.2.4 Time-of-flight secondary ion mass spectroscopy (ToF-SIMS)

To investigate the oxide layer between W top electrode and BST film, Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) was utilized. It uses a pulsed primary ion beam to desorb and ionize species from a sample surface.[65, 66] The resulting secondary ions are accelerated into a mass spectrometer, where they are mass analyzed by measuring their time-of-flight from the sample surface to the detector.

There are three different modes of analysis in TOF-SIMS. 1) mass spectra used to determine the elemental and molecular species on a surface; 2) images to visualize the

distribution of individual species on the surface; and 3) depth profiles to determine the distribution of different chemical species as a function of depth from the surface.

TOF-SIMS can provide information about depth profile by shallow sputtering. An ion gun is operated in the DC mode during the sputtering phase in order to remove material, and a second ion gun is operated in the pulsed mode for acquisition phase. Depth profiling by TOF-SIMS allows monitoring of all species of interest simultaneously, and with high mass resolution. Figure 2.14 shows a TOF-SIMS depth profile of a W/BST/SRO/STO RRAM device. We could distinguish different layers in the depth profile, and also by calculating the etch time and etch rate, the thickness of the WO_x layer exiting at the W/BST interface can be estimated.

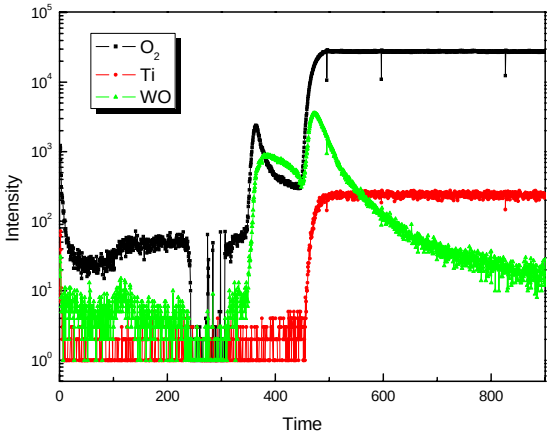


FIG. 2.14. A TOF-SIMS depth profile of a W/BST/SRO/STO RRAM device

2.2.5 RRAM device measurement setup

Besides the surface and structural analysis with SEM, XRD, AFM etc., the electrical characterization is also important to investigate the RRAM device properties.

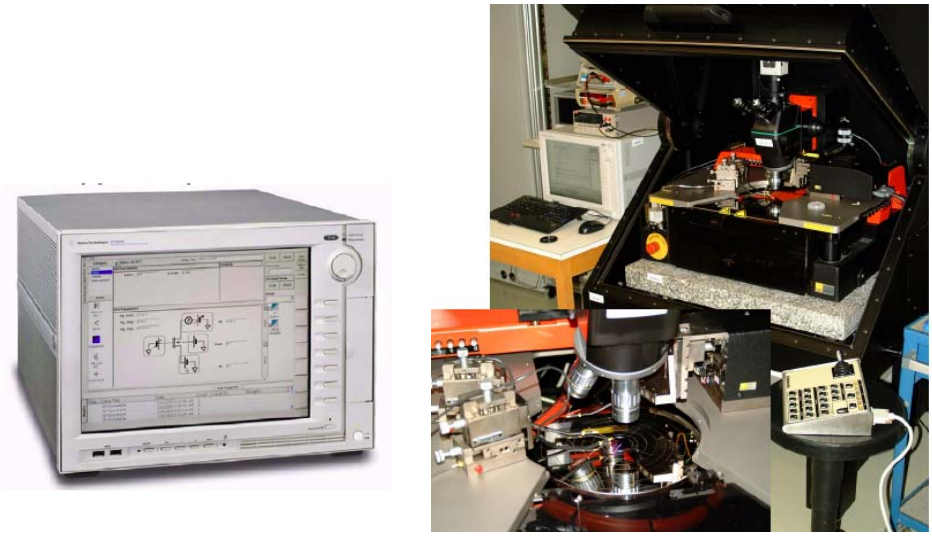


FIG. 2.15. RRAM device measurement setup (a) Agilent Semiconductor Device Analyzer B1500A. (b) Probe station.

The electrical measurements were performed using a Semiconductor Device Analyzer B1500A in combination with a probe station in order to achieve good connection and sufficient shielding against interferences from the environment which was shown in Figure 2.15. The Agilent B1500A is capable to provide DC voltage/current output, DC voltage/current measurement, and the AC signal output.

The most significant measurements in our experiments are I-V measurements. The RRAM device was operated by sweeping voltage with same/different polarities to obtain different resistances indicating “ON” or “OFF”. The B1500A analyzer has four source/monitor units (SMU), which can apply/measure DC voltage or current on the RRAM devices. The SMU could provide a compliance feature to limit output voltage or current to prevent the device failure during measurements.

A typical I-V curve measured by Semiconductor Device Analyzer B1500A is presented in Figure 2.16. By sweeping the voltage the sample switches between the high resistance state (HRS) and the low resistance state (LRS). The LRS and HRS can be defined as “1” and “0”, thus the data can be stored by means of resistance variation.

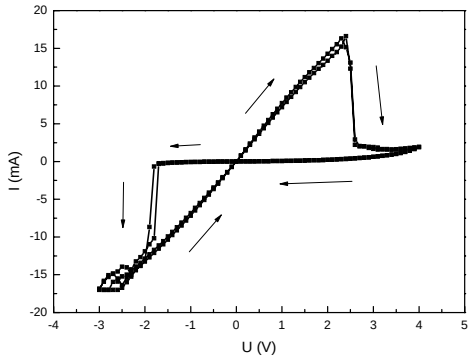


FIG. 2.16. A typical I-V curve indicating that the device resistance can be repeatably changed.

Chapter 3

Process development

3.1 Thin film deposition: Laser fluence dependence

During thin film deposition by PLD a wavelength of 248 nm laser was generated by a KrF excimer. The laser energy density on the target is a crucial point for the deposition of stoichiometric thin films. There are reports that the different laser energy density or so called laser fluences can result to the shift of stoichiometry, as researched in STO thin films by B. Dam *et al.* [67] The reduced laser fluences from 2.0 J/cm^2 to 0.4 J/cm^2 changes the Sr/Ti ratio in deposited film from ~1 to ~1.45. Therefore, the laser fluence has to be controlled and adjusted prior to deposition to optimize the RRAM properties. Figure 3.1 (a) shows the scheme of the optical path of the PLD system with a filter to adjust the laser fluence. Besides the mirror which serves to position the laser spot on the target, there exists a filter within the optical path, which is used to adjust the exact laser energy density by its tilt angle. Figure 3.1 (b) shows the energy at the chamber entrance in dependence of the tilt angle of the filter. The laser density is 133 mJ if do not apply the filter, and all tested tilting angles lead to the reduction of laser energy.

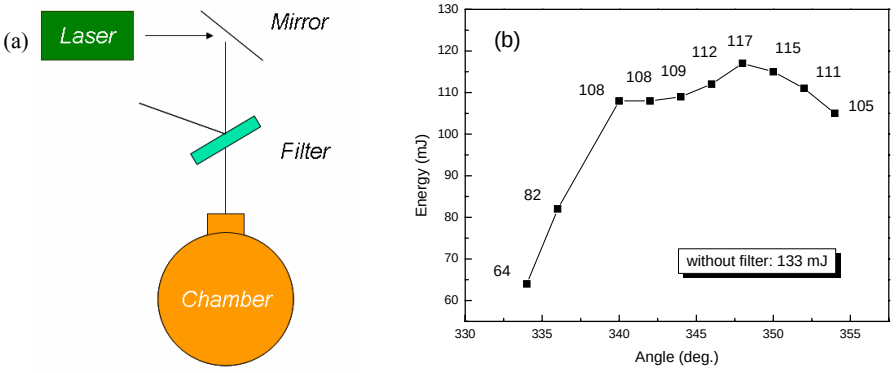


FIG. 3.1. (a) Scheme of the optical path; (b) Energy at the chamber entrance in dependence of the filter tilt angle.

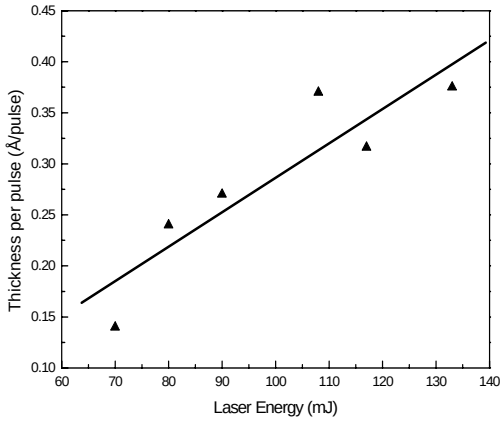


FIG. 3.2. Laser energy dependence of the deposition rate (film thickness per pulse).

For higher laser energy it is reasonable to deduce that the film deposition rate should be enhanced due to more materials were ablated from the BST target in a giving time. Figure 3.2 displays that the deposition rate or BST thin film thickness per pulse increased from about 0.15Å/pulse to 0.40Å/pulse when the laser energy increased from 70 mJ to 117 mJ, the highest laser energy we could reach with the optic filter, and 133 mJ without filter. Thus in order to obtain the same film thickness with varied laser energy, the deposition time was controlled.

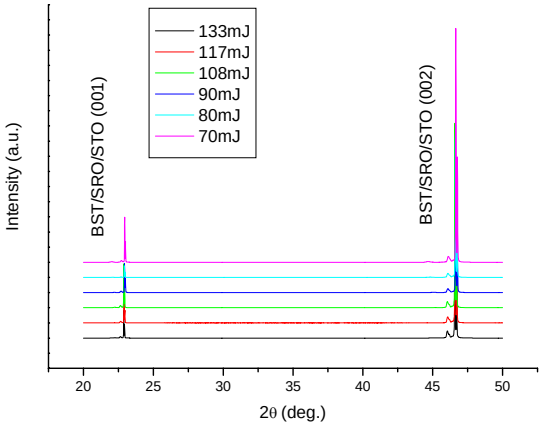


FIG. 3.3. X-ray diffraction of in-situ deposited BST/SRO thin films in different laser energy on STO substrate. BST and SRO films all exhibit (00*l*) oriented epitaxial growth.

The in-situ deposited BST / SRO thin films in different laser energy on STO substrate were all epitaxially grown as confirmed by X-ray diffraction as shown in Figure 3.3. The BST film is 45 nm thick and SRO is 80nm thick. Only the (00*l*) peaks of BST and SRO thin films were observed and the BST and SRO films all exhibit (00*l*) oriented epitaxial growth.

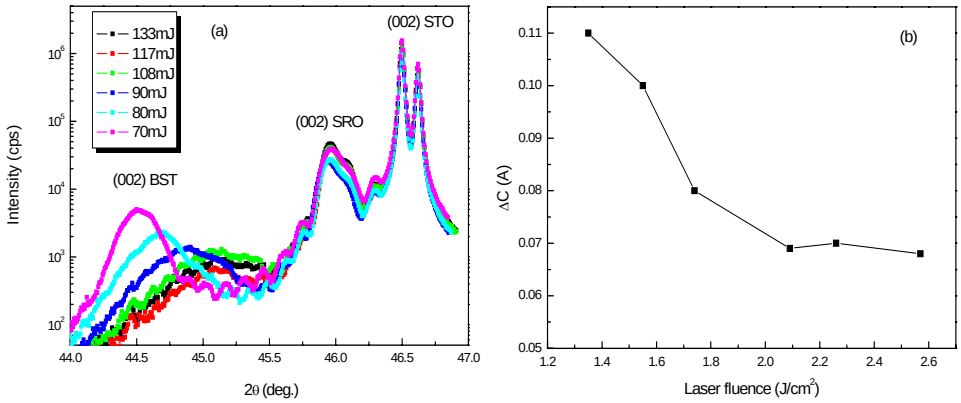


FIG. 3.4 (a) XRD pattern of the deposited BST thin films with different laser energy and (b) out-of-plane lattice constant variation.

A notable feature of the XRD pattern of the deposited BST thin films with different laser energy is the shifted (002) peak to lower angle with reduced laser energy as shown in Figure 3.4 (a). Using the position of (002) peak we can calculate the out-of-plane lattice constant (c axis) and the results is shown in Figure 3.4 (b). The laser spot size is measured as 5.17mm^2 and the laser spot size is supposed not be influenced by the titled filter. The Δc (c- c_{BST}, c_{BST}=3.95Å) increased with reduced laser energy or laser fluence. The lattice distortion may come from the the small thickness variation although the deposition time was controlled. However, for thicker films the Δc will decrease due to strain relaxation as approved by R. Dittmann *et al.*. [68] The full width at half maximum (FWHM) of BST (002) peak in ω-scan with laser energy variation is shown in Figure 3.5. It is clear that the film epitaxy was greatly improved with reduced laser energy.

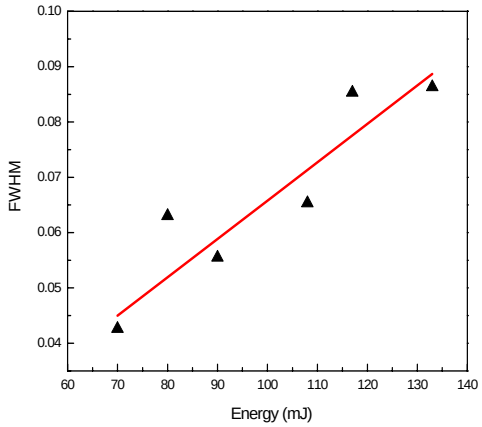


FIG. 3.5. The full width at half maximum (FWHM) in ω-scan with laser energy variation.

TABLE 3.1 Laser fluence dependence

Sample Name	S9	4.4	5.4	C9	C10	C11
TEL	Litho. & Etching	Litho. & Etching	Litho. & Etching	Litho. & Etching	Litho. & Etching	Shadow mask
Laser energy (mJ)	133	117	108	90	80	70
Laser fluence (J/cm2)	2.57	2.26	2.09	1.74	1.55	1.35
Out-of –plane lattice constant ΔC (A)	-	0.07	0.069	0.08	0.1	0.11
Film thickness (nm)	~80	43	55	48	48	32
FWHM	0.084	0.0853	0.0653	0.0555	0.063	0.0426
Measured pads	46	39	38	38	27	37
Switched pads:~	54%	67%	58%	68%	37%	3%

The statistics of the laser fluence dependence on out-of-plane lattice constant, film thickness, full width at half maximum and yields are shown in Table 3.1. Although the

film quality was improved by reducing the laser energy during film deposition, the yields fluctuated and only 3% RRAM devices with highest epitaxial quality of BST film shows resistive switching behavior. The defects such as dislocations or grain boundaries has great influence on the switching property and those defects may provide the conductive channels to alternate device resistance, thus the result shown in laser fluence dependence gives a clue that the best thin film quality does not result in the best switching performance, and it is a clear evidence of the importance of the defects to obtain resistive switching phenomena.

3.2 Nano-imprint Lithography

3.2.1 Introduction

Nano-imprint lithography is a novel method to fabricate nanometer scale patterns. It is a simple nano-lithography process with low cost, high throughput and high resolution. Nano-imprint lithography was first invented by Stephen Chou in 1996 [69] and later on it was further developed, and also has been added to the International Technology Roadmap for Semiconductors (ITRS) for the 32 and 22 nm nodes. Nanoimprint lithography has been widely used in fabricating device for electrical, optical, photonic and biological applications such as MOSFET, single electron memory, sub-wavelength resonant grating filter, integrated photonics circuit and sub-10 nm nanofluidic channels.[70]

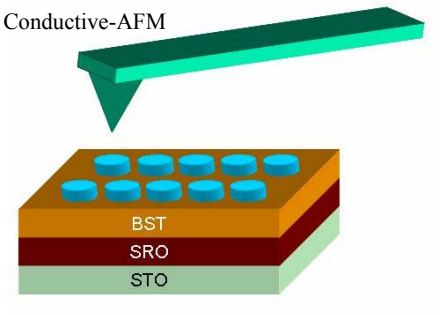


FIG. 3.6 Illustration of the nano top electrodes prepared by nano-imprint. The nano top electrodes will be contacted by conductive-AFM for characterization.

For resistive switching applications, M. Meier *et al.* have succeeded in fabricating crossbar structures with integrated methyl-silsesquioxane (MSQ) using nanoimprint lithography. [71] In our experiment, we intend to prepare nano top electrodes by nanoimprint lithography on STO single crystal, and contact the nano top electrodes with conductive-AFM to investigate the switching mechanism and the scaling possibilities (shown in Figure 3.6). This work is challenging because the yield of nanometer sized pattern transfer is very low and the dimension of the STO single crystal substrates is too small compared to the Si wafer.

There are mainly two types of nanoimprint lithography, photo nanoimprint lithography and thermo nanoimprint lithography. In photo nanoimprint lithography a UV curable liquid resist was spin coated on the substrate and the mold is normally made of transparent materials. Then the transparent mold and the substrate were pressed together and the resist was exposed in UV light and became solid. After the mold separation, the pattern was transferred onto the sample.

Thermo nanoimprint lithography was the earliest nanoimprint lithography technique developed by Chou's group. In a standard thermo nanoimprint lithography process, a thin layer of thermoplastic polymer was spin coated onto the substrate. The mold with predefined topological patterns was brought into contact with the sample and then was pressed together under a certain pressure. The pattern on the mold will be pressed into the softened polymer film when the thermoplastic polymer was heated up above the glass transition temperature. After cooling down the mold was separated from the sample and the patterned thermoplastic polymer was left on the sample. The detailed illustration of the thermo nanoimprint lithography is shown in Figure 3.7. In our investigation we only used the thermo nanoimprint lithography.

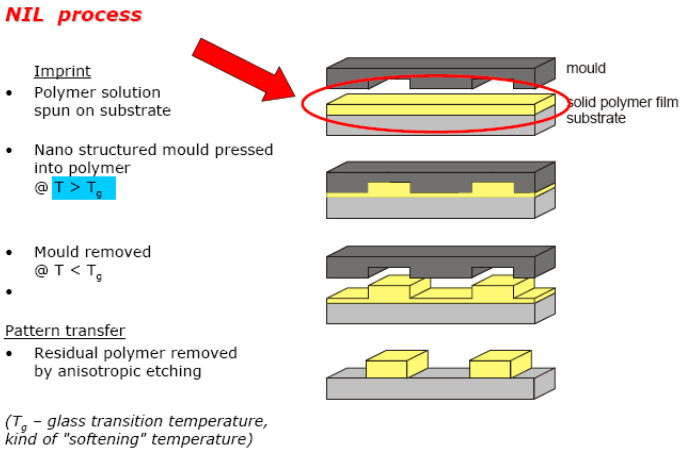


FIG. 3.7 Illustration of the thermo nanoimprint lithography process.

3.2.2 Mould design

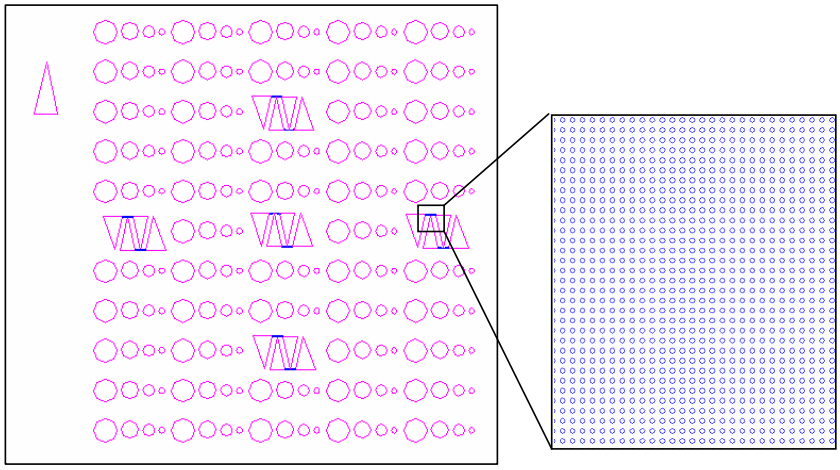


FIG. 3.8. The mould designed for nano top electrodes application. The nano dots arrays located between tips of three triangles

The mould used for nano top electrodes application through thermo nanoimprint lithography was designed by Auto CAD. The nano dots arrays located between tips of

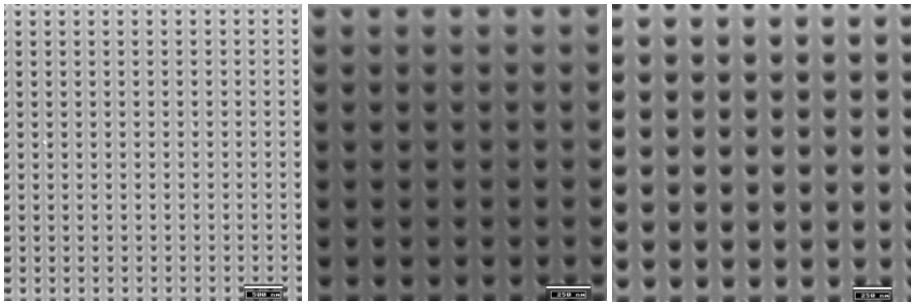


FIG. 3.9 SEM images of the mould after etching. The diameter of the nano dots are (a) 100nm (b) 90nm and (c) 80nm.

three triangles as shown in Figure 3.8, thus the nano dots arrays could be easily found by the microscopy affiliated on the conductive-AFM. The diameter of the designed nano dots ranged from 50 nm to 100nm for scaling test. The mould was then transferred on Si wafer by e-beam writing technique and RIBE.

Figure 3.9 shows the SEM images of the mould after etching. The patterned nano dots are well aligned and the spread is homogenous for diameter from 80 nm to 100 nm. For dots ranged from 50nm to 70nm the pattern was not well transferred.

3.2.3 Sample preparation

For sample preparation, the Pt coated Si was firstly used as substrate because of the high expenses of STO single crystal. The size of the Pt coated Si is also 10x10 mm_2, the same as the STO single crystal substrates. Once the process succeeds, we could simply transfer it on STO single crystal substrates. Prior to the imprint, the substrate was cleaned using standard clean, bake process as used in photo lithography. The cooling process was skipped because the resist is sensitive to moisture. The PR 1020 resist was used and spin coated on the sample at Recipe 9 (3000 rpm). The imprint was carried out on Nanonex

NX-2000 at 170C for 6 min with pressure of 300psi. After imprint the system was cooled down and checked with microscopy as displayed in Figure 3.10. The nano dots arrays were successfully transferred onto the substrate with diameter from 80nm (inner blocks) to 100nm (outer most blocks). Also in some areas the 70nm nano dots arrays can be observed.

FIG. 3.10. Nano dots arrays were transferred onto the substrate with diameter from 80nm (inner blocks) to 100nm (outer most blocks). Also in some areas the 70nm nano dots arrays can be observed.

For higher resolution the imprinted sample was also checked with SEM as shown in Figure 3.11. The nano dots are all well aligned and homogeneously spread for diameters from 80nm to 100nm [Figure 3.11 (a)-(c)]. For 70 nm nano dots array some parts are lost [Figure 3.11 (d)]. Although the nano dots are well transferred with diameters from 80nm to 100nm using PR 1020, the residual resist layer is too thick as confirmed by the following etching process and the patterned structure are all lost

.

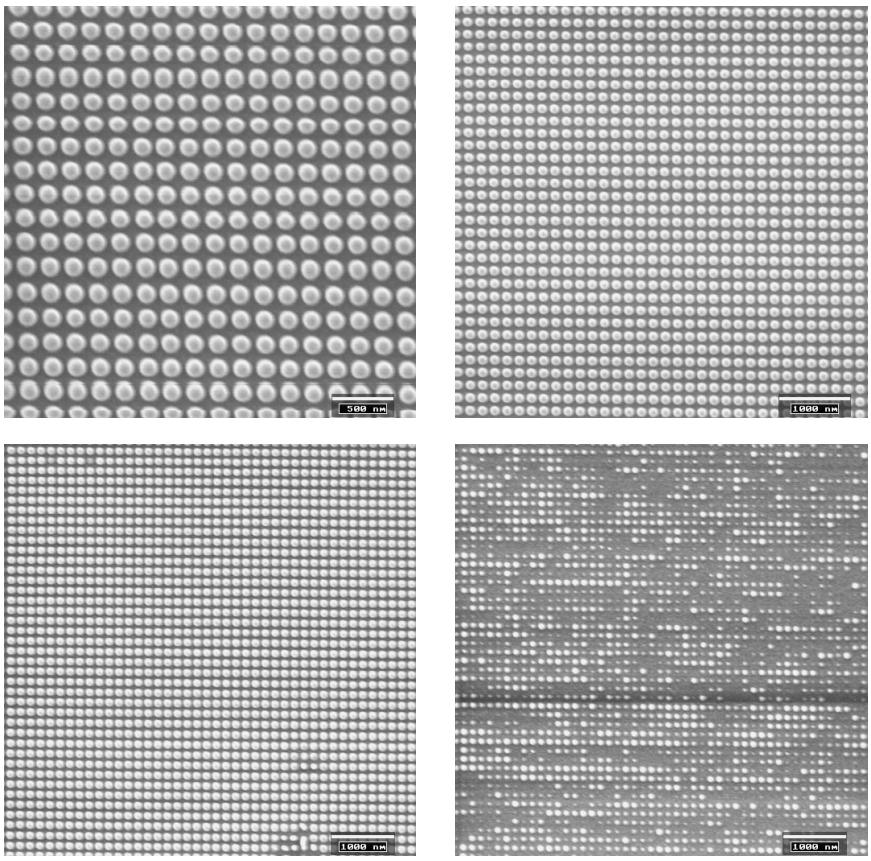


FIG. 3.11. SEM images of transferred nano-dots on Pt coated Si with diameter form 100nm (a), 90nm (b), 80nm (c) and 70nm (d) using PR 1020.

For thinner resist the Mr 7010e was used and spin coated with Recipe 9 (3000 rpm), and the sample was then post-baked at 140°C for 2min. The transferred structure is given in Figure 3.12. However, this process is not well repeatable. We could succeed in transferring in some cases but most of the attempts failed. This probably comes from the residual resist adsorbed on the mould. The resist will plug up the patterned nano-structures on mould and therefore makes the imprint failed. This was confirmed by check of traditionally cleaned mould in microscope. Thus the complete cleaning of the

mould is of great significance for successfully pattern transfer. A clean with acetone in mega-sonic basin for 30min is recommended.

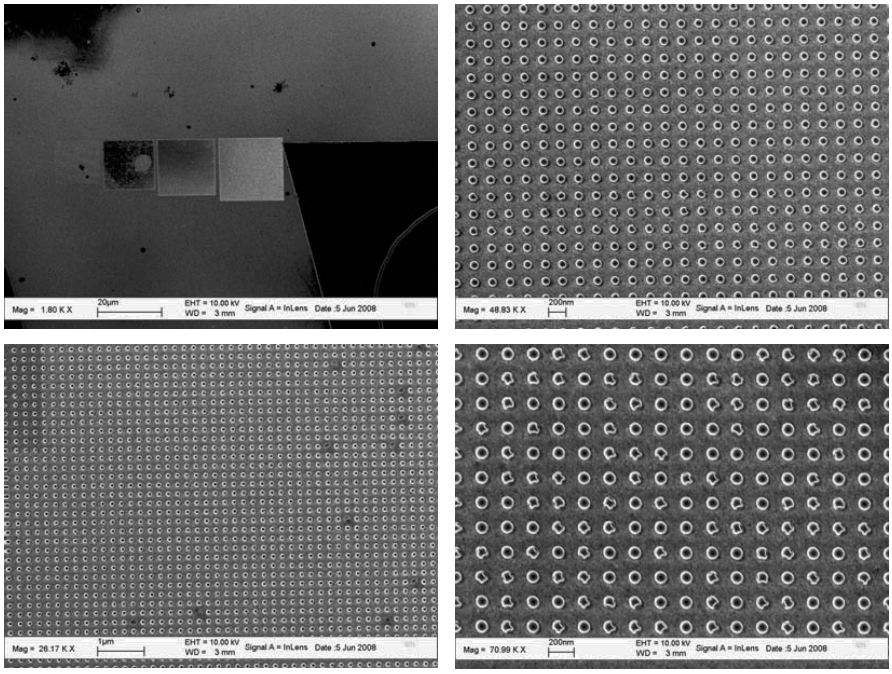


FIG. 3.12. SEM images of transferred nano-dots on Pt coated Si using Mr 7010e.

Outlook of imprint to prepare nano-dots top electrodes

The imprint mould plays a key role in imprint technology. As shown in § 3.2.2, although the designed nano dots are ranged from 50nm to 100nm in diameter, only nano dots with diameter from 80 nm to 100 nm were well aligned and homogenously transferred through e-beam writing and for dots ranged from 50nm to 70nm the pattern was not well transferred. The resist thickness is also very important to fill in the pattern in mould and leave not too thick residual layer. Thus the resist should be carefully chosen and spin speed should also be optimized.

3.3 Resistive switching in Cross-point structure

The cross-point structure was also prepared and the detailed preparation method is described in § 2.1.1 and § 2.1.6.

Figure 3.13 (a) is an optical microscope picture of cross-point junction. The designed junction size is 5um × 5um and the real size is shrunk to ~3um × 4um. The I-V curve switched at μA range is shown in Figure 3.13 (b). Different to the polarity change with increased current we observed in pad structure, the switching direction is the same in mA range. When the current compliance is gradually increased to 3mA, the resistance of the junction degraded and the resistive switching disappears. The sample shows a linear I-V behavior [Figure 3.13 (c)]. As we have described before, the fatigued sample can be refreshed by a voltage sweep without current compliance. Figure 3.13 (d) shows that the resistance increased abruptly at ~2.4V and afterwards the junction exhibits hysteretic I-V curves again. Figure 3.13 (e) shows that we can switch the HRS to LRS by a negative bias, and it makes clear that the fatigued junction was fully recovered. Due to the large spread of resistance in HRS and LRS, we found no junction size dependence in measured devices. The complete switching curve in Figure 3.13 (f) is typical for W/BST/SRO/STO pad structures and it indicates the materials system has potential to be applied in cross-point structure for integration.

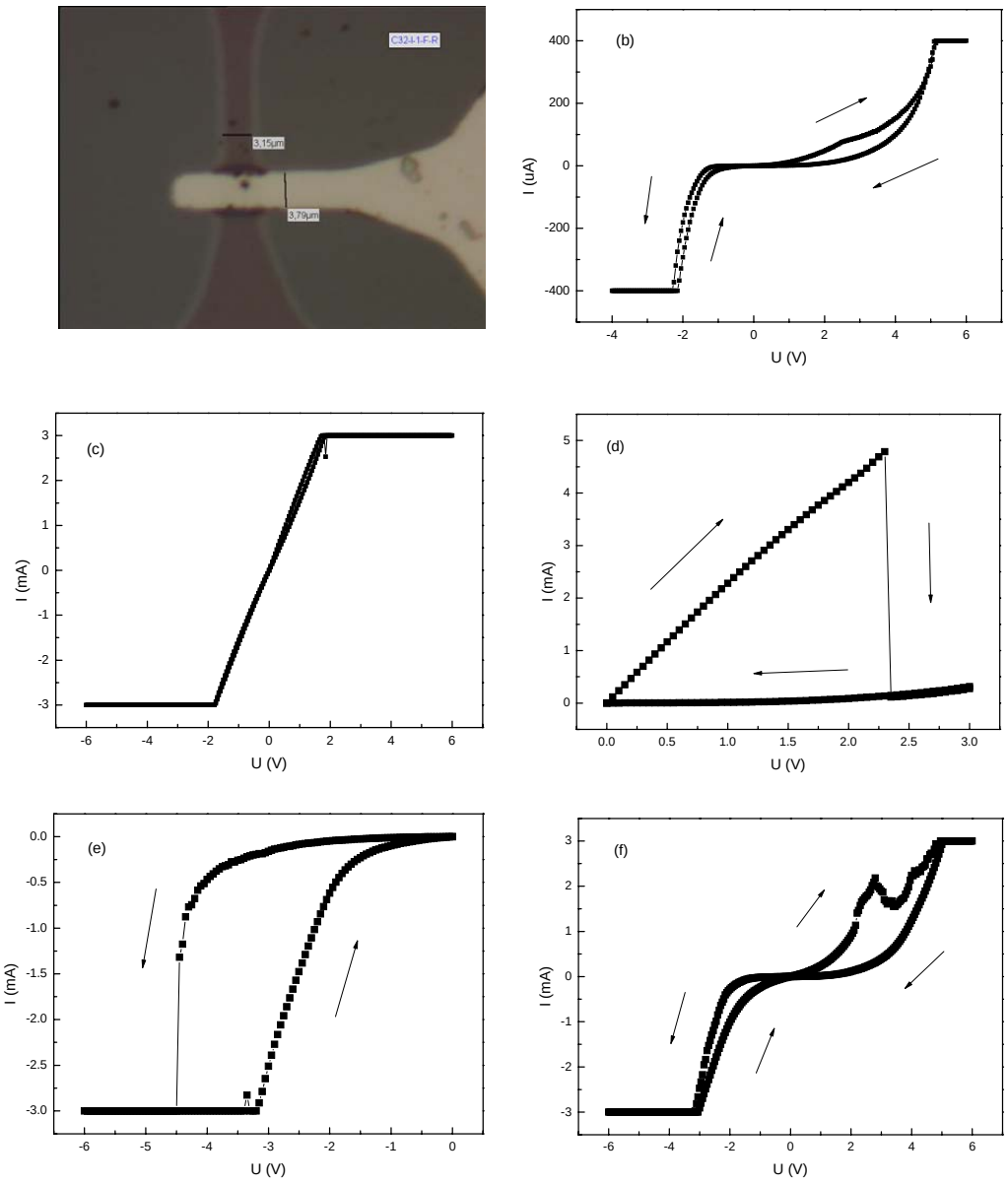


FIG. 3.13. (a) The cross-point junction in microscopy. (b) device switched at μA range. (c) When increase current compliance to 3mA the resistance of the junction degraded and shows a linear I-V behavior. (d) the resistance increased abruptly at ~2.4V and afterwards the junction exhibits HRS again. (e) switch the HRS to LRS by a negative bias and the fatigued junction was fully recovered. (f) The complete switching curve and it indicates the materials system has potential to be applied in cross-point structure for integration.

Chapter 4

Bipolar resistive switching with W and Pt top electrode

It is of considerable importance for potential RRAM application to succeed in finding methods to improve the yield, stability and reliability of the resistive switching devices, besides a further elucidation of the switching mechanism. Successful switching of up to 10^6 cycles has been reported [72] while most others display fast degradation in hundreds of cycles. In this chapter, we compare the resistive switching performance of barium strontium titanate (BST) thin films with platinum (Pt) and tungsten (W) top electrodes which enables us to draw conclusions to fatigue mechanisms present in resistive switching oxide thin films.

4.1 Device fabrication

80nm SRO bottom electrode and 45nm BST working layer were deposited *in-situ* by pulsed laser deposition (PLD). The deposition condition was given in Chapter 2. The (*00l*) oriented epitaxial growth of the bi-layers is confirmed by X-ray diffraction measurements.

The device structures were illustrated in Figure 4.1. The 100nm-thick Pt film which was utilized as top electrodes of the metal-insulator-metal (MIM) structure was deposited on top of the SRO/BST hetero-structures by magnetron sputtering. The W film was deposited by e-beam evaporation and covered by a 100 nm-thick sputtered Pt protection layer in order to avoid the oxidation of W under ambient conditions. The metal films were patterned by lithography and dry etching to areas of $0.04mm^2$ down to $2500\mu m^2$ to form the top electrodes. The bottom electrode was contacted by silver paste through scratches placed in the BST films.

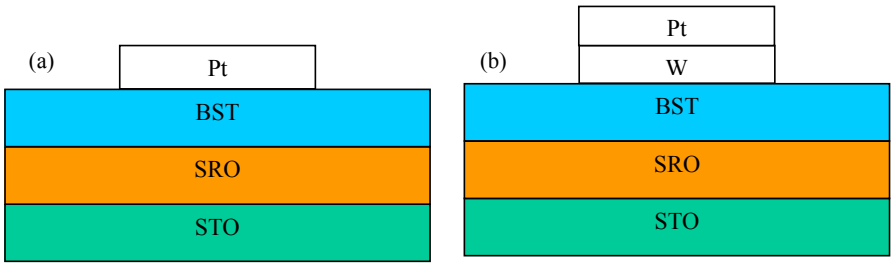


FIG. 4.1 The device structures for Pt/BST/SRO/STO and Pt/W/BST/SRO/STO.

4.2 Characteristics of bipolar resistive switching phenomenon

To evaluate the RRAM property, the current-voltage (I-V) characteristics were measured using Agilent semiconductor analyzer B1500A. The voltage or current was increased by step wise with delay times in the range from milliseconds to seconds. During the I-V measurements the Set voltage, Reset voltage, Set current, Reset current was artificially controlled. The endurance, retention behavior were also measured to test the device stability to work as non-volatile memory.

4.2.1 Current-voltage (I-V) characteristics.

All samples reveal low initial resistances thus no "forming" procedure like thermal or high voltage treatments, which are prerequisite for the observation of resistive switching in STO single crystals, [52] have to be performed. Figure 4.2 (a) shows typical examples of I-V characteristics of Pt/BST/SRO and W/BST/SRO devices, respectively. The voltage was applied on the top electrode and the SRO bottom electrode was grounded. The voltage was swept as follows: $0 \rightarrow V_{max} \rightarrow 0 \rightarrow V_{min} \rightarrow 0$, as indicated by arrows in I-V characteristics and the current compliance was set to protect samples from permanent breakdown. The I-V characteristic of the Pt/BST/SRO sample depicted in Figure 4.2 (a) shows that the initial state of the sample is the low resistance state (LRS) which exhibits linear I-V dependence, suggesting a metallic charge carrier transport. The temperature

dependence of the LRS shown in Figure 4.2 (c) proved this assumption. The I-V branch of the high resistance state (HRS) is strongly non-linear suggesting a semiconducting, thermally activated charge carrier transport, which was proved by the temperature dependence of the resistance depicted in the inset of Figure 4.2 (a). After a certain amount of cycles, the I-V curve of the Pt/BST/SRO sample (the 100th cycle depicted in Figure 4.2 (a)) changes its shape and both the LRS and the HRS are semiconducting.

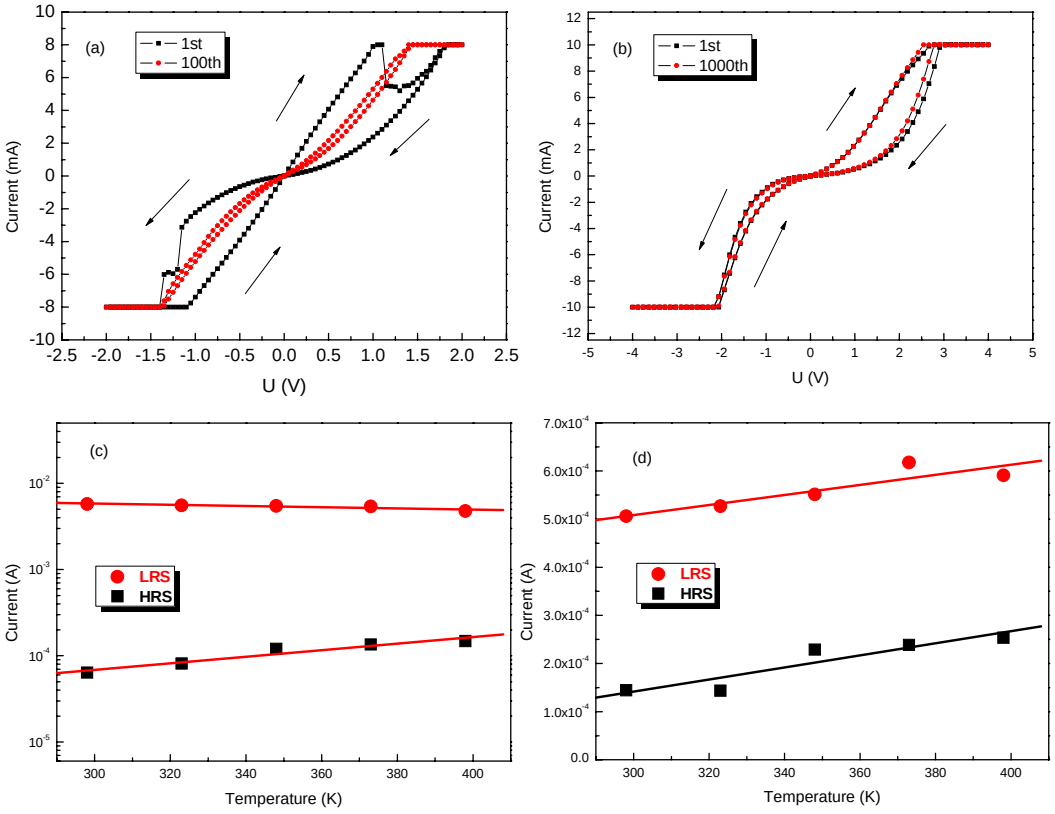


FIG. 4.2 I-V characteristics of Pt/BST/SRO (a) and W/BST/SRO (b) devices. (c) and (d) are corresponding temperature dependence measurements.

In contrast to this, the hysteresis curves of W/BST/SRO devices immediately exhibit a transition between two semiconducting states, as depicted in Figure 4.2 (b). Figure 4.2 (d) shows that both the HRS and LRS are thermally activated. The R_{off}/R_{on} ratio of the metallic to semi-conducting transition can reach more than $2x10^3$ in some Pt/BST/SRO devices but less than 20 for the W/BST/SRO devices. However, the W/BST/SRO device uniformity is greatly improved and all 40 measured pads show stable resistive switching, which is much higher than the devices with Pt top electrodes about 58%, and 40% reported previously. [39] The R_{off}/R_{on} of the W/BST/SRO device, read out at 0.5V, remains about 6 for 1000 cycles, while the R_{off}/R_{on} of the Pt/BST/SRO device already decreases from about 6 to 1.3 after 100 cycles.

4.3 Reliability and switching characteristics of bipolar resistive switching behavior

For memory applications the RRAM devices are preferred to be of high reliability, superior to present memory technology. The Pulse measurements, Retention, R_{off}/R_{on} dependence, multi-level data storage potentials and other issues to prolong the device life time were investigated.

4.3.1 Pulse measurements

Figure 4.3 displays the pulse measurement of Pt/BST/SRO and W/BST/SRO devices which were set/read/reset/read for 10^4 times. The set and reset voltage is ±4.5V and the resistance states are read out at 0.5V. The pulse width is 0.1 second and the pulse height is controlled by the current compliance. The progressive increase of R_{on} and decrease of R_{off} of the Pt/BST/SRO samples depicted in Figure 4.2 (a) can be identified with the first hundreds of cycles in Figure 4.3 (a). With further increased number of cycles, the Pt/BST/SRO devices show fast resistance decay in both HRS and LRS and the memory window is closed after 2000 cycles (Figure 4.3 (a)). In contrast to this, the reliability of W/BST/SRO device is extraordinarily enhanced and the memory window is well kept after switching for 10^4 times (Figure 4.3 (b)).

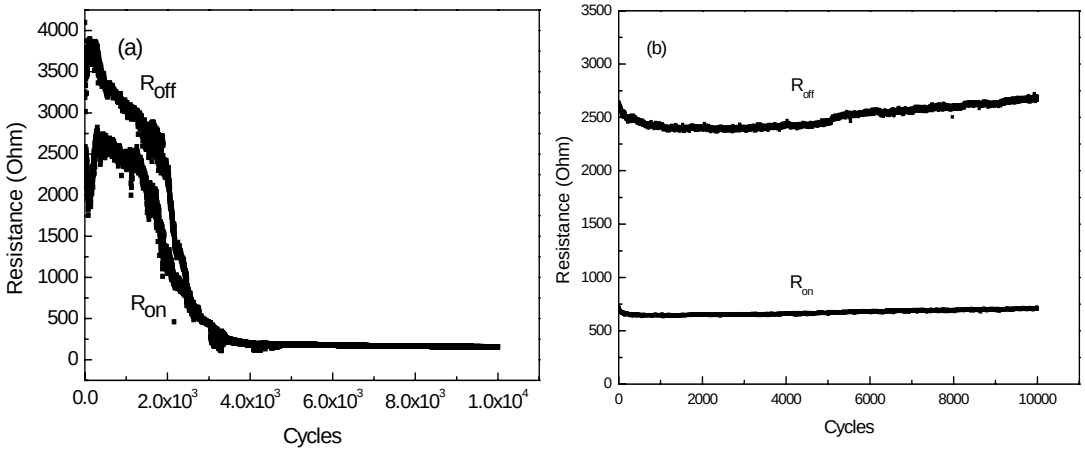


FIG. 4.3 Pulse measurements of Pt/BST/SRO and W/BST/SRO devices which were set/read/reset/read for 10^4 times. (a) Pt/BST/SRO and (b) W/BST/SRO devices.

4.3.2 Retention

The retention is very important for device reliability. The stored data is expected to be kept for 10 years. In our measurements, the resistance switched between HRS and LRS was measured at 0.5V for 10^4 seconds. Figure 4.4 (a) and (b) present the retention behavior for bipolar switching in Pt/BST/SRO and W/BST/SRO devices. The results show that all resistance states in Pt/BST/SRO and W/BST/SRO devices are well stored for 10^4 seconds and exhibit non-volatile behavior. Meanwhile, the low read voltage has no influence on the device resistance.

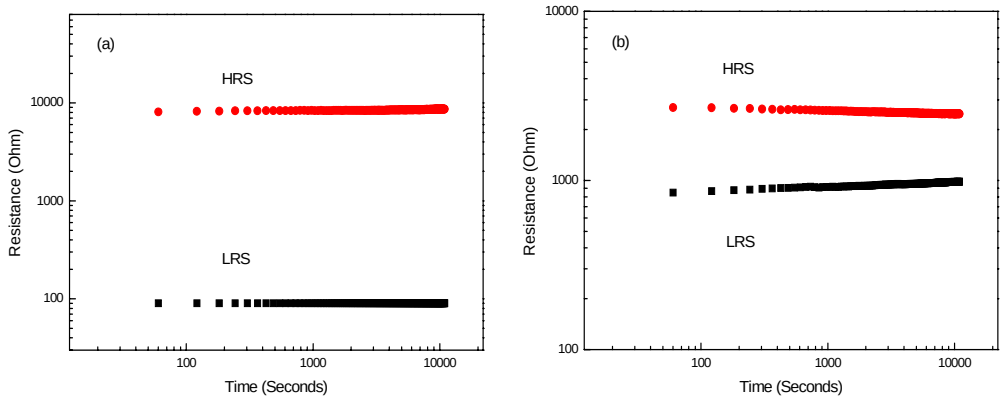


FIG. 4.4 Retention behavior of (a) Pt/BST/SRO and (b) W/BST/SRO structures.

For long term measurements, we choose two pads and set them into HRS and LRS separately. Then the stored resistance states were read out every month at 0.1 V since Jan. 2008 for 15 months. Figure 4.5 shows that during the past 1year the device resistance varied only a little, probably comes from the different contact resistance due to the set up condition measured every time, and the non-volatile property was confirmed.

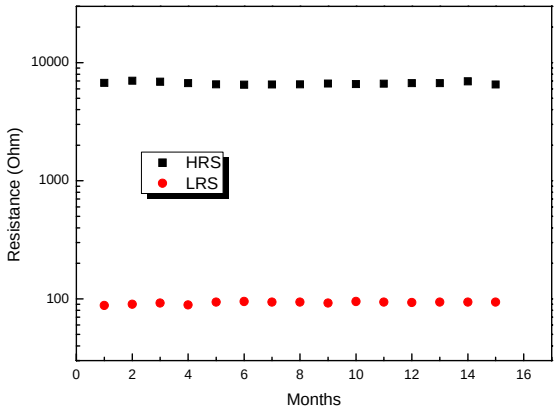


FIG. 4.5 Long term retention measurement since January 2008 up to March 2009. The HRS and LRS were well stored for 15 months and the non-volatile property was confirmed.

4.3.3 Readout disturbance

The RRAM should be non-volatile, and that means the stored data should not be lost or damaged when laid aside for long time or during long term readout process. We checked the readout disturbance of the prepared RRAM devices and results proved that the memory is non-volatile. The reading process at small read voltage has no influence on the stored data and the read-out is a non-destructive process.

The BST based RRAM is firstly set to LRS or Ron by a negative pulse of +6V for 1s. Then the read process was carried out by a 1V 1s pulse for 50 times. Next, a positive pulse of -6V for 1s resets the device resistance to HRS or R_{off}, followed by another 1V pulse last 1s for 50 times. The result was shown in Figure 4.6 (a). It is clear that the resistance of HRS and LRS has almost no change during the continuous readout thus the non-volatile character was confirmed.

Figure 4.6 (b) displays a similar readout result at the same RRAM cell but with different read voltage of 0.5V. All other parameters are the same as mentioned in Figure 4.6 (a). The resistance of HRS and LRS did not change during 50 read processes and it also

exhibits the non-volatile character. The only notable difference compared to Figure 4.6 (a) is the resistance ratio(R_{off}/R_{on}). The R_{off}/R_{on} of read at 1V is 1.5, whereas when read at 0.5V the R_{off}/R_{on} increased to 4.7. The lower read voltage also can reduce the power consumption and meantime obtain higher resistance ratio.

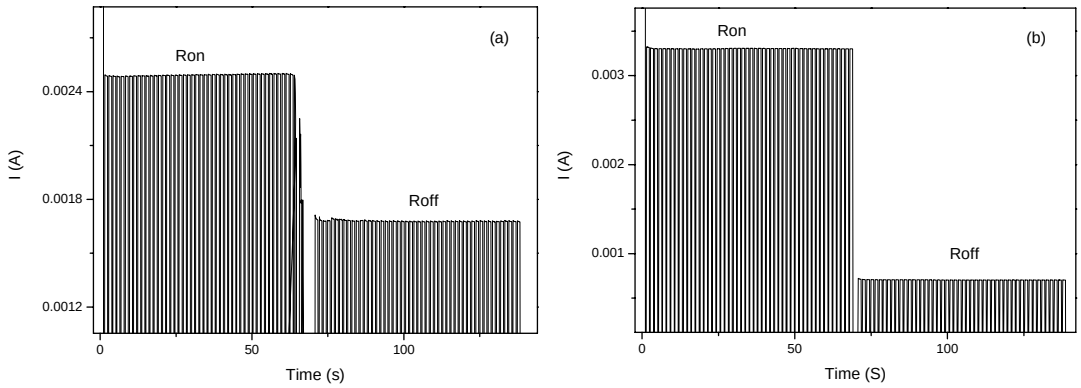


FIG. 4.6 Continues readout for 50 times with (a) R_{off}/R_{on} of 1.5 when read at 1V and (b) R_{off}/R_{on} of 4.7 when read at 0.5V.

4.4 Mechanism of bipolar resistive switching and proposed model

As the work function of Pt (5.65eV) [73] and W (4.55eV) [74] are higher than the electron affinity of BST films (4.1eV) [75], potential barriers could be formed at both interfaces. As a result of the higher work function, a significant Schottky-barrier is expected in the case of the Pt/BST interface whereas for the W/BST this effect should be less pronounced. This is in contradiction to the experimental observation that the initial ON-state of the Pt/BST/SRO devices is metallic. The absence of a Schottky-barrier at the BST-Pt interface may be attributed to the modification of the interface during sputtering of the Pt top electrode. It was reported that accelerated sputtering gas atoms strike the surface of the BST films during the top electrode deposition and cause the formation of oxygen vacancies at the BST-Pt interface, which may suppress the intrinsic Schottky-barrier and result in a low initial resistance of the Pt/BST interface. [76] Furthermore, the observed initial metallic state shows that the as-deposited BST films are oxygen deficient and the BST-SRO interface provides an ohmic contact. After a few cycles when the oxygen vacancies in the film are redistributed, the Schottky barrier at the Pt-BST interface is recovered and the metallic branch of the I-V curve vanishes as depicted in Fig. 4.2 (a).

For W/BST/SRO devices, no initial metallic branch is observed. This may be attributed either to fact that the e-beam evaporation of the W top electrode preserves the oxygen stoichiometry at the interface or to the formation of an insulating WO_x interface layer at the BST-W interface.

In order to elucidate the interface scenario, we performed ToF-SIMS measurements and analyzed the depth profiles of O_2, Ti and W shown in Fig. 4.7 (a). The curves are normalized to the same level in the BST bulk regime in order to visualize the sequence of the different atoms in the W-BST interface region. The most obvious feature in the interface region is the peak in the W signal which has to be attributed to a change of the W sputtering yield in the surface region. Furthermore, it can be clearly seen that the O_2 signal starts to increase simultaneously with the W signal but the rise of Ti signal from the BST layer is delayed for about 6s. This is a clear hint on the existence of a WO_x layer

at the interface, because for an abrupt interface between W and BST, the O_2 signal should rise simultaneously with the Ti signal. By assuming that the WO_x layer has the same etching rate as the W metal, one can estimate the WO_x to be in the order of 1nm.

To eliminate the possibility that a WO_x layer, which may already be formed during the deposition of the W top electrode, dominates the resistive switching and can exist independent of the BST film, a Pt/W/SRO device was prepared in the same condition as mentioned above. No hysteric I-V curve is observed and the device shows ohmic contact at the interface. It indicates that the interplay between BST and WO_x is responsible for the observed switching phenomena.

The WO_x interface layer may strongly affect the movement of oxygen at the interface, the injection into the top electrode and finally the exchange of oxygen with the atmosphere. The improved endurance of our samples with W top electrodes is similar to the phenomenon observed in ZrO_2 films with Ti top electrode [77] and $La_{0.7}Ca_{0.3}MnO_3$ films with samarium (Sm) top electrode, [78] which were also attributed to the existence of a metal oxide layer formed at the interface acting as source and sink for oxygen vacancies.

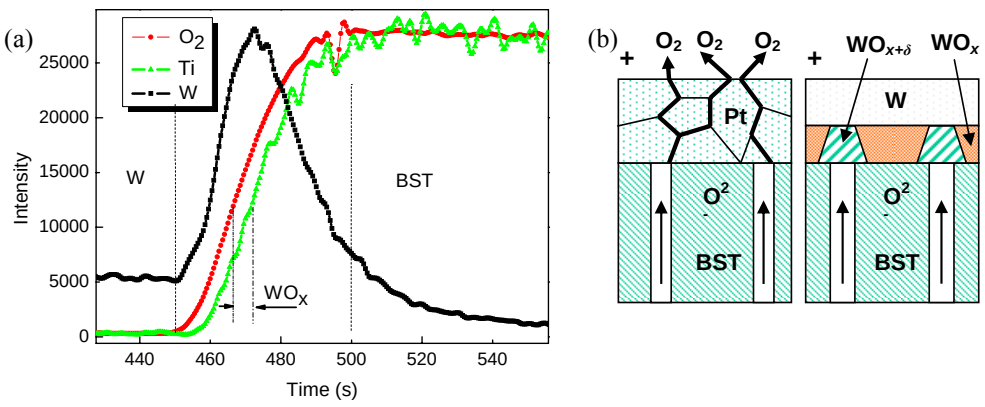
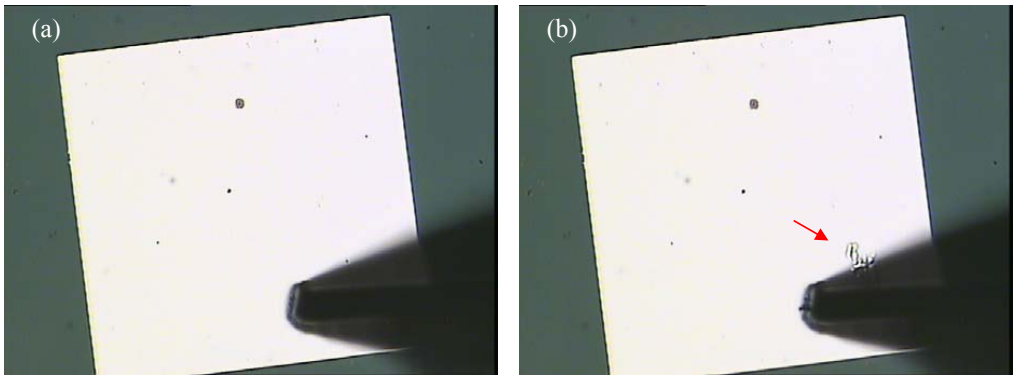


FIG. 4.7 (a) ToF-SIMS of W/BST interface. The W signal is normalized from 1045 and Ti from 240 to the level of the BST bulk regime (O_2 signal). (b) Illustration of switching mechanism when positive bias is applied on the top electrode for Pt/ BST/SRO structure and W/BST/SRO structure.

In order to understand the fatigue behavior of samples with Pt top electrode, shown in figure 4.2(a), one should regard the movement of oxygen vacancies under an applied electric field. When a positive bias is applied on the Pt top electrode, the oxygen vacancies are repelled from the interface. As a result, the Schottky-barrier height increases and the device is switched to the HRS. When a negative bias is applied to the top electrode, the oxygen vacancies are pushed back to the interface, reducing the Schottky-barrier height and resulting in the LRS. According to the diffusion of oxygen along the Pt grain boundaries [79] additional oxygen vacancies could be injected from the anode into the BST film during cycling [80] as sketched in Fig. 4.7 (b) and may cause the experimentally observed reduction of both R_{on} and R_{off} during cycling depicted in Fig. 4.2(a).

Figure 4.8 (a)-(e) show the surface of Pt top electrode before and after switching. The original Pt electrode surface before switching is fairly smooth expect some residual photo resist and dusts as shown in Figure 4.8 (a). However, after switched for a certain cycles, there are some bulges or bubbles observed close to the contact needle [Figure 4.8 (b)-(c)]. The SEM image of the bubbled area clearly show that parts of the Pt electrode surface after switching are changed [Figure 4.8 (d)] and also some cracks observed as shown in Figure 4.8 (e). The bubbles and cracks may come from the oxygen evolution in a very short time and if the Pt top electrode can not export them in time, the Pt surface will transform and oxygen may assemble just beneath the top electrode.

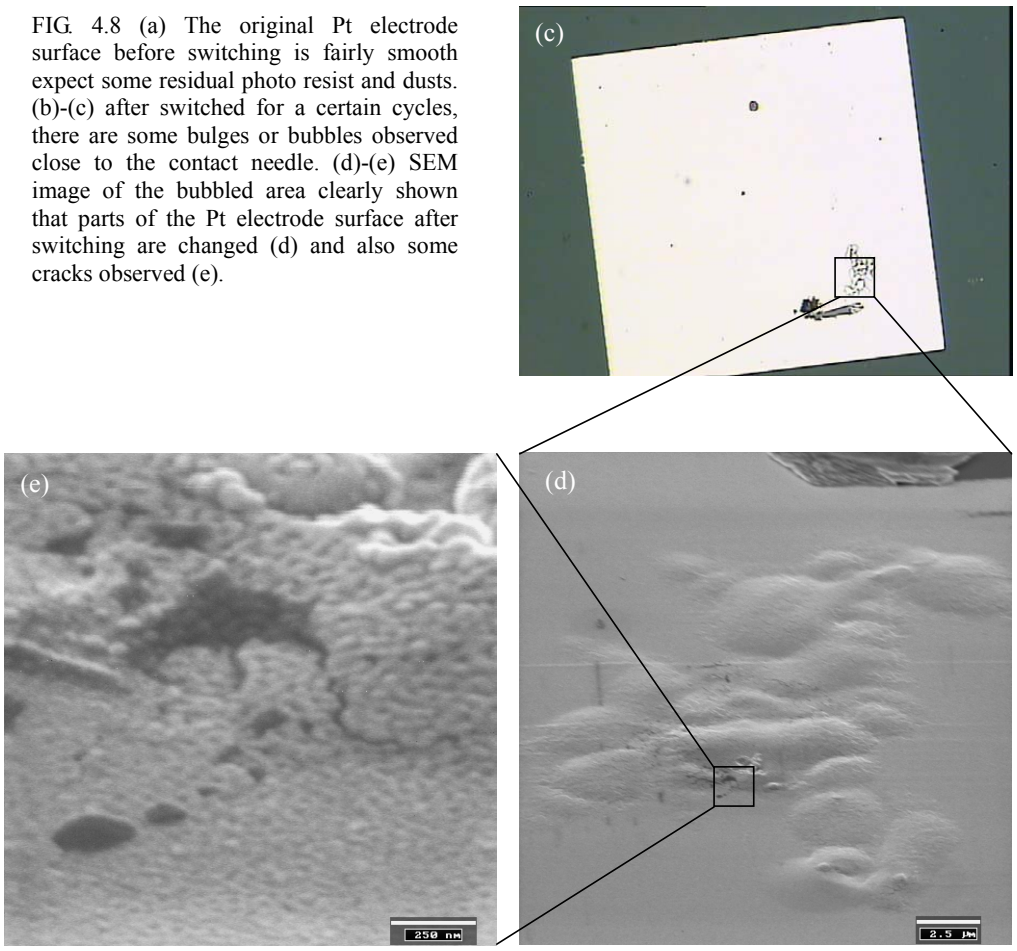
This model is also consistent with the fatigue observed in $La_{0.7}Ca_{0.3}MnO_3$ films which is attributed to the progressive oxygenation of the p-type thin films via the Pt top electrode under ambient conditions. [81] The endurance of the LCMO films was significantly improved under vacuum conditions. In analogy to these results on p-type LCMO, it is reasonable to deduce for the Mn doped BST films used in this paper, that the endurance should be improved in a highly oxygenating environment or when a diffusion barrier, [82] like TaSiN used in DRAM, is introduced in order to block the oxygen infusion to the atmosphere. Moreover, Fig. 4.9 shows that the fatigued Pt/BST/SRO device can be



Original surface

After switching

FIG. 4.8 (a) The original Pt electrode surface before switching is fairly smooth expect some residual photo resist and dusts. (b)-(c) after switched for a certain cycles, there are some bulges or bubbles observed close to the contact needle. (d)-(e) SEM image of the bubbled area clearly shown that parts of the Pt electrode surface after switching are changed (d) and also some cracks observed (e).



refreshed to switch back to the HRS again by applying a positive bias. This indicates that the oxygen is supplied from the sample interior, most likely from the SRO bottom electrode, and thereby the Schottky-barrier is recovered.

In case of W/BST/SRO devices, the resistance of the interface WO_x layer can be increased by reducing the number of oxygen vacancies. [83] When a positive bias is applied on the W top electrode, the positively charged oxygen vacancies are repelled, the number of oxygen vacancies at the W/BST interface is reduced, the WO_x layer is further oxidized to $WO_{x+\delta}$ and the resistance increases. In reversed condition, the oxygen can be released from the WO_x layer in negative electric field, the resistance of the $WO_{x+\delta}$ layer decreases, and the oxidation state of the $WO_{x+\delta}$ is reduced. Thus the WO_x interface layer works like an oxygen sink, stores and releases the oxygen during switching. Also we did not observe any bubbles on W top electrodes which is consistent to above argument.

Even though the resistive switching in our samples is strongly dominated by the interface, we did not find any pad size dependence in the area range we measured. Therefore, we conclude that in case of our switching samples has a filamentary character. The conductive filaments may be connected and disconnected at the interface through the reduction and oxidation of the WO_x layer, respectively, at the end of the filaments as sketched in figure 4.7 (b).

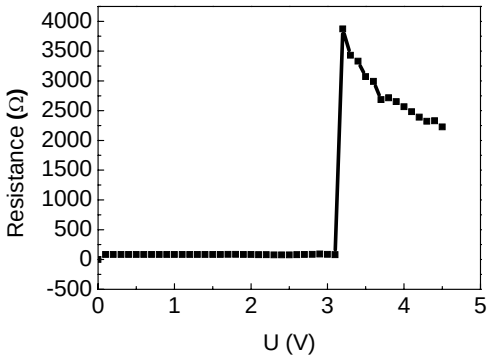


FIG. 4.9 the fatigued Pt/BST/SRO device can be refreshed to switch back to the HRS again by applying a positive bias.

4.5 Switching with asymmetric current compliance

The notable behavior of the I-V curves is the asymmetry in current or voltage. The asymmetric I-V curve may result from the asymmetry of the device structure, different top and bottom electrode. By controlling the system asymmetry, we may improve the device reliability and stability.

I-V measurements

In § 4.2.1 we have shown that the endurance of Pt/BST/SRO devices in symmetric voltage or current is not sufficient to be used as real RRAM. As shown in Figure 4.2 (a) R_{off}/R_{on} decreased from about 6 to 1.3 after 100 cycles and this strong fatigue behavior is not acceptable for application. But by understanding the asymmetric nature of the RRAM devices, we could improve the endurance by apply asymmetric current compliance or switching voltage to keep the R_{off}/R_{on} at an accredited level.

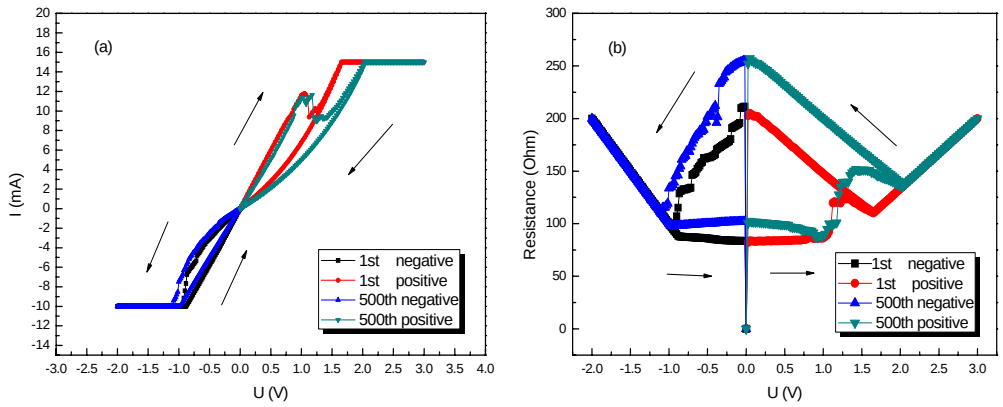


FIG. 4.10 (a) Endurance for a Pt/BST/SRO device switched for 500 cycles with asymmetric current compliance. (b) the resistance Vs. applied voltage shows that resistance of both HRS and LRS are increased, probably due to the higher current applied in positive branch.

Figure 4.10 (a) shows the endurance for a Pt/BST/SRO device switched for 500 cycles with asymmetric current compliance. The positive current compliance is 15mA and for negative branch 10mA was used. Compared to the former case of Pt/BST/SRO device, the I-V curve did not shrink in the negative branch. Surprisingly, in positive branch the opening became even larger. The voltage dependence on device resistance in Figure 4.10 (b) clearly shows that the resistance of both HRS and LRS are increased. Thus the endurance was greatly improved for 500 cycles by asymmetric current compliance.

Pulse measurements

Figure 4.11 (a) shows the pulse measurement with symmetric pulses (±6V, pulse height ±8mA). The resistance was read at +0.5V. The R_{off}/R_{on} remains around 2 for 1000 set/read/reset/read cycles. However, the switching window narrows to ~1.3 and if continues pulses applied, the memory window will be closed eventually. The degradation of both HRS and LRS during cycling is the key factor that influences the endurance.

Contrarily, when asymmetric pulses (±6V, pulse height -8mA, +10mA) were applied, the switching behavior is totally different. As seen in Figure 4.11 (b), the R_{off}/R_{on} slightly decreases from 2.5 to 1.9 for 1000 cycles and the switching window narrows to ~1.6. The most remarkably difference is that both HRS and LRS are increased. The developing trend of HRS and LRS is ascending; while in asymmetric current compliance is descending. This conversed resistance developing can be simply explained by oxygen vacancy movement induced device conductance change. As positive pulse height is higher than negative pulse height, thus more oxygen vacancies were pushed away from top interface to the BST thin film. This will lead the device resistance increase as explained in § 4.4. As the negative current is always not changed thus the device did not switch back to the same LRS, and the LRS is slightly increased together with the HRS. For long term measurement resistance of both HRS and LRS are increased and we obtain the ascending memory window.

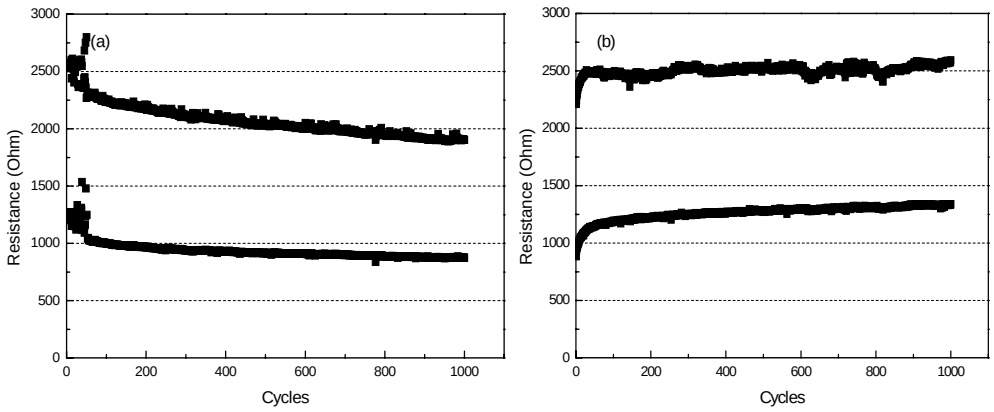


FIG. 4.11 Pulse measurement with symmetric write/erase pulses (±6V, pulse height ±8mA) (a), and (b) asymmetric write/erase pulses (±6V, pulse height -8mA, +10mA). The resistance was readout at 0.5V.

Optimization of memory window with asymmetric pulse

Based on the discussions above, we have the opportunity to artificially control the development of memory window, by using asymmetric pulses. Figure 4.11 (a) and Figure 4.11 (b) represent two extreme situations with descending and ascending memory window. It is natural to think if we could find the intermediate state that the memory will be optimized to be horizontal thus the RRAM device will posses the longest life time.

Figure 4.12 shows the result of optimization of memory window with asymmetric pulses. The pulse height was controlled by limiting the current compliance. Figure 4.12 (a) is the traditional symmetric pulse measurement with current compliance of 10mA for both Set and Reset pulses. The development of memory window is descending, the same as we discussed before, mainly due to the degradation of HRS and LRS. Figure 4.12 (c) presents another situation that with asymmetric current compliance, 20mA for Reset and 10mA for Set, the developing trend was totally changed to be ascending and both HRS and LRS are increased during cycling.

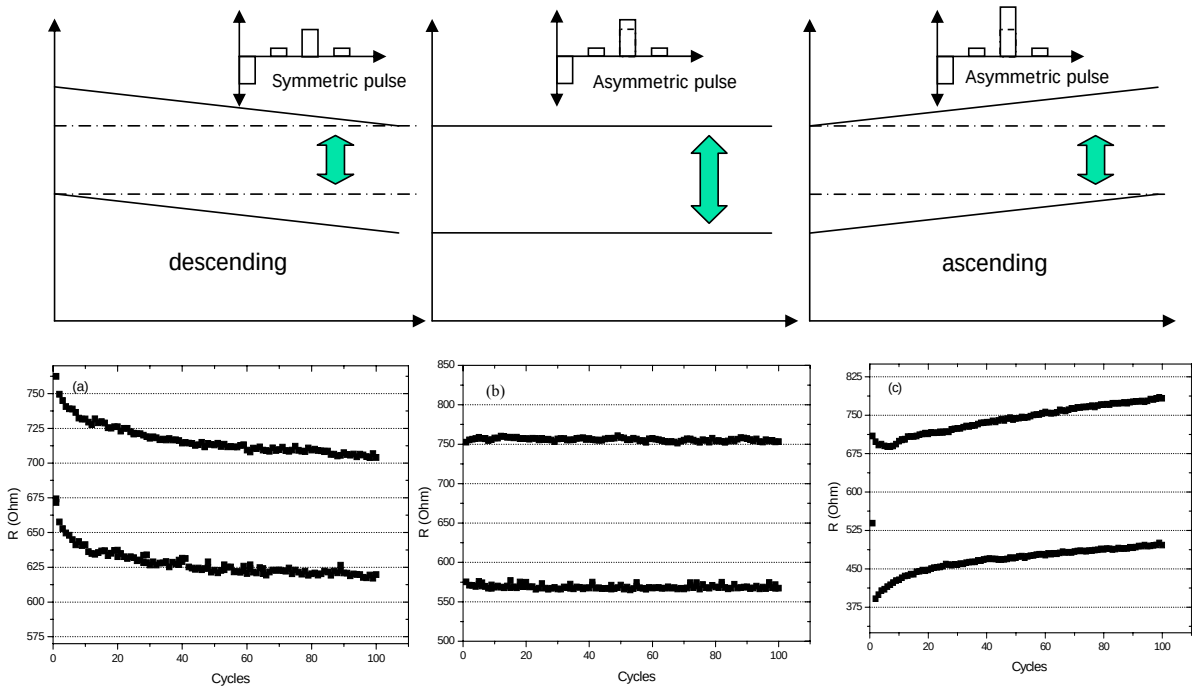


FIG. 4.12 Optimization of memory window with asymmetric pulse. (a) Traditional symmetric pulse measurement with current compliance of 10mA for both Set and Reset pulses. (c) with asymmetric current compliance, 20mA for Reset and 10mA for Set. (b) with intermediate pulse height, 15mA for Reset and 10mA for Set, the memory window is optimized to be horizontal, and HRS and LRS maintains unchanged.

However, if we choose an intermediate pulse height, here 15mA for Reset and 10mA for Set, the memory window is optimized to be horizontal, and HRS and LRS maintains unchanged as sketched in Figure 4.12 (b). It is clear that the detectable memory window in Figure 4.12 (a) shrink to 675Ohm-700Ohm, 525Ohm-675Ohm in Figure 4.12 (c), but in Figure 4.12 (b) is still 575Ohm-750Ohm. The results shown is only for 100 cycles, and for longer measurements the memory window of devices with not horizontal HRS / LRS development curves will ultimately closed and sensors will not be able to distinguish HRS and LRS, and RRAM devices will be regarded to be failure.

The asymmetric pulse is essential for long term pulse measurement because pushing O_2

to the interface needs more power assumption than extracting it from the interface. The long term pulse measurement with symmetric pulse height (± 10mA) shows decreased resistance of LRS and HRS, because of the oxygen loss inducing conductance increase as explained in § 4.4. In addition, asymmetric pulse height (+20mA, -10mA) will push too much oxygen vacancies from interface to the bulk and eventually the resistance of both LRS and HRS increase. However, the finely chosen positive pulse height (15mA) and negative pulse height (10mA) will compensate the oxygen loss and make the number of oxygen vacancy at interface being in equilibrium. It guarantees the unchanged LRS and HRS during cycling, and consequently gives birth to the optimized horizontal memory window.

The optimized horizontal memory window provides an opportunity to extend the device life time. It is rather simple to use asymmetric pulses than to optimize the device fabrication process or materials system. Although consider the circuit design to generate asymmetric pulses, it is still much easier and cheaper compared to other methods.

4.6 Refreshment of RRAM devices

The most common failure observed for RRAM devices is the degradation. Once the device degrades, the memory looks like “short” and there is no resistance difference anymore in normal applied switching voltage. The failed device can not be used as memory and have to be located and shielded thus additional circuits’ costs are unavoidable. Here we find the possibility to refresh the RRAM device by applying a voltage without the current compliance. Once experienced the refresh process, the memory can be used again. This simple process can be preceded like the “format” generally used in computer’s hard disk, and after a long time usage if any abnormal behavior or the volume decrease observed, just simply refresh the RRAM and it will work as new as just been bought. The physical origin of the refreshment may come from the oxygen being supplied from the SRO bottom electrode, and thereby the device resistance was recovered to show switching behavior.

The typical failed or fatigued RRAM device has a linear I-V hysteresis loop as shown in Figure 4.13 (a). The resistance of the failed device is very small and generally lower than hundreds of Ohms. In this case the circuits will only find the device as ON, and it not be switch-able any more. In § 4.5 we have well known that a higher voltage or current compliance will increase the resistance of HRS. Here a similar process is undertaken by applying a positive voltage of 4.5V without current compliance. In Figure 4.13 (b) the current increased with the voltage before 3V, and at about 3.2V the current dropped sharply which means the resistance was covered back. The refreshed device can be switched between HRS and LRS again, as shown in Figure 4.13 (c). The first I-V curve after refresh is not stable and the opening shrinks from the second voltage sweeping. Although the hysteresis loop becomes weak, the endurance is very promising and the shape of I-V curves almost did not change in 100 cycles.

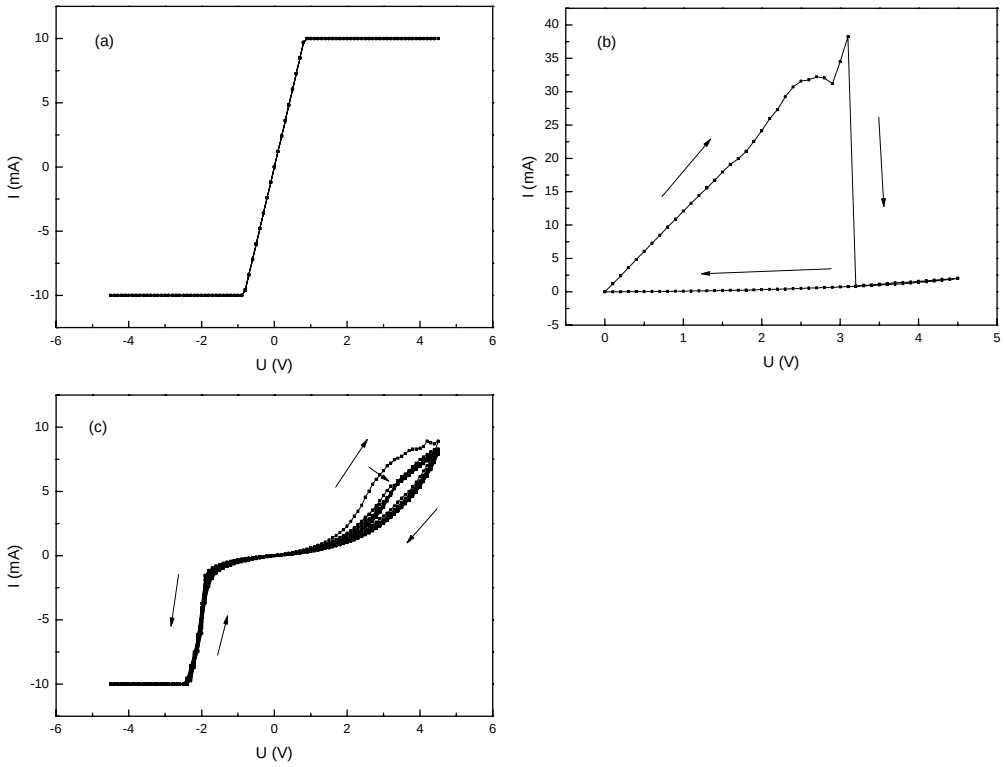


FIG. 4.13 (a) A typical failed or fatigued RRAM device which exihibits a linear I-V hysteresis. (b) the resistance was recovered at about 3.2V (c) refreshed device can be switched between HRS and LRS again.

4.7 Pseudo Unipolar switching

In the next chapter we will show that the unipolar switching occurs in polycrystalline BST films whereas in epitaxial films only bipolar resistive switching was observed. Here we provide more details of the switching mode and the reason why we could not obtain unipolar switching in epitaxial BST films.

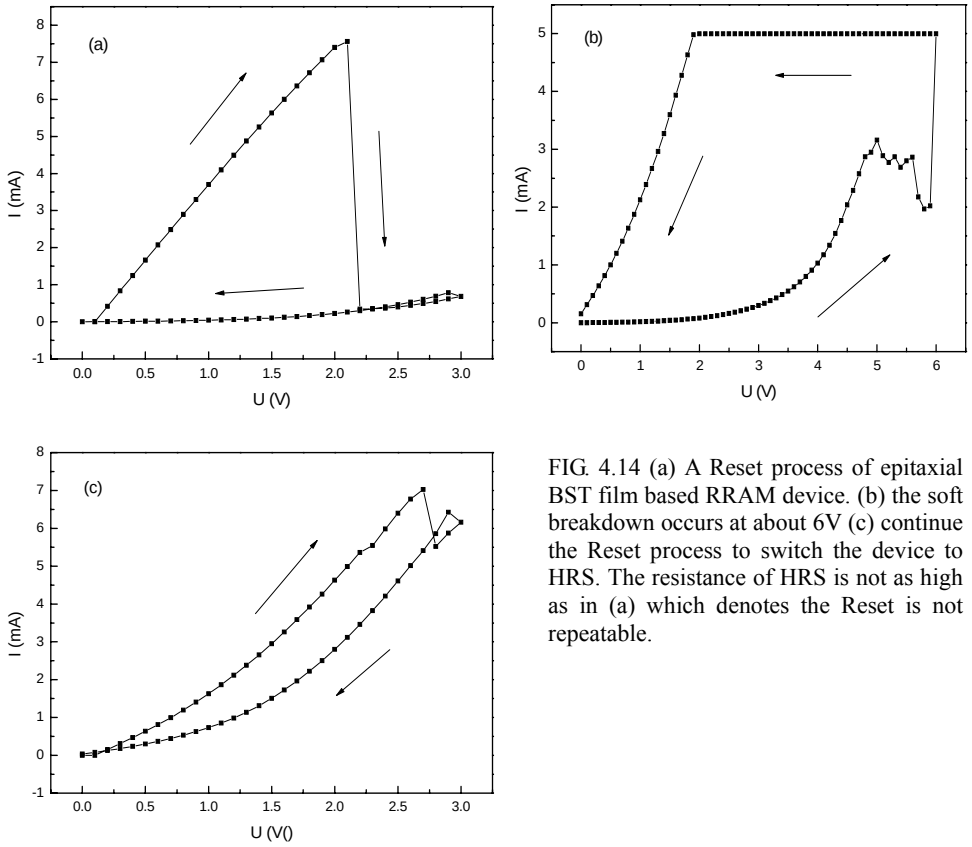


FIG. 4.14 (a) A Reset process of epitaxial BST film based RRAM device. (b) the soft breakdown occurs at about 6V (c) continue the Reset process to switch the device to HRS. The resistance of HRS is not as high as in (a) which denotes the Reset is not repeatable.

Figure 4.14 (a) shows a Reset process of epitaxial BST film based RRAM device. The device was initially switched to metallic conduction behavior (LRS) which exhibits linear I-V curves. Under a positive bias of 3V the device was switched into HRS, and this Reset process is quite normal in Unipolar switching. For Unipolar switching, the Reset current

is always higher than in set process. In the followed Set process, another positive voltage of 6V with current compliance of 5mA was applied. The device resistance was gradually degraded before 6V and finally at about 6V the soft breakdown occurs [Figure 4.14 (b)]and the device was set to LRS again. Up to now the Reset and Set seemingly show unipolar switching behavior, but if we continue the Reset process to switch the device to HRS, as shown in Figure 4.14 (c), the resistance of HRS is not as high as in Figure 4.14 (a), which denotes the Reset is not repeatable. If we continue Set process again, the I-V curve will follow the backward curve of Figure 4.14 (c) and it is obvious that the Set current will be higher than in Reset and we cannot obtain the previous LRS, thus the unipolar switching disappeared.

4.8 Annealed Vs. as-prepared Pt/BST/SRO

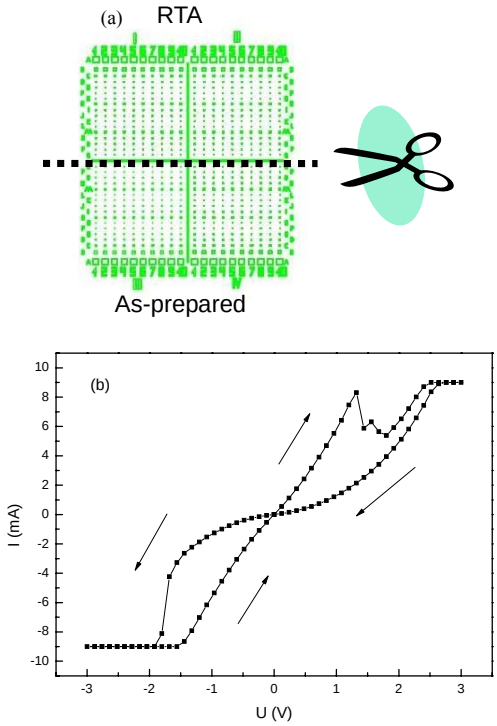


FIG 4.15 (a) Illustration for experiments and (b) a typical I-V curve of measured pad.

TABLE 4.1 Statistics of annealed and as-prepared Pt/BST/SRO structure.

Sample structure	Pt/BST/SRO	Pt/BST/SRO
TEL	Pt	Pt
Optic filter	No	No
BST deposition time (Min)	2	2
RTA	700°C 5min, O_2 200sccm	-
Measured pads	40	40
Switched pads:	~85%	~95%
R_{off}/R_{on} @ -0.5V	2~18	2~21
Initial resistance (Ohm)	1K~10K	200~1K

Rapid thermal annealing (RTA) has replaced the tube furnace in many applications to perform high–temperature (>700°C) processing steps for defect annealing, dopant activation and/or diffusion.[84] Because there is wide spread of HRS and LRS in different pads, we tried the RTA process to improve the uniformity and the yield. The sample with Pt/BST/SRO structure was prepared on a 10mm×10mm STO single crystal substrate by lithography and RIBE. More details of the device fabrication are introduced before. After the preparation of the top electrodes, the sample was cut into 2 parts by wire cutting [Figure 4.15 (a)]. Then one part was sent to RTA at 700°C for 5min with O_2 flow of 200sccm. After the RTA process, the sample was measured together with the as-prepared one. This procedure ensures the same condition of the samples with and without RTA treatment, and makes results more reliable. The type of I-V curves of both as-prepared and RTA sample are similar as shown in Figure 4.15 (b).

The only significant difference is the initial resistance. The sample experienced RTA process has an initial resistance from 1K Ohm to 10K Ohm, while the as-prepared is only 200-1K Ohm (Table 4.1). The increased initial resistance may come from the reduced number of oxygen vacancies [85] thus Schottky barrier height was enhanced at the top Pt/BST interface [86]. The R_{off}/R_{on} of the RTA treated sample is 2-18, almost the same compared to 2-21 of the as-prepared one. The yield of RTA treated sample is 85%, smaller than the as-prepared sample of 95%. Because point defects such as vacancies may responsible for resistive switching as reported before in single crystal STO and epitaxial films[52], the number of defects in RTA treated sample is reduced during annealing thus the yield became smaller than the as-prepared one. The measured R_{off}/R_{on} and yields reveals that the RTA process is not necessary and the as-prepared sample is superior as RRAM.

4.9 Polarity change

In our former reported results the I-V curves we measured are all in mA range. The switching direction in positive voltage branch is clockwise and counter-clockwise in negative branch. That means that the device resistance increased with positive voltage load and decreased when negative voltage was applied.

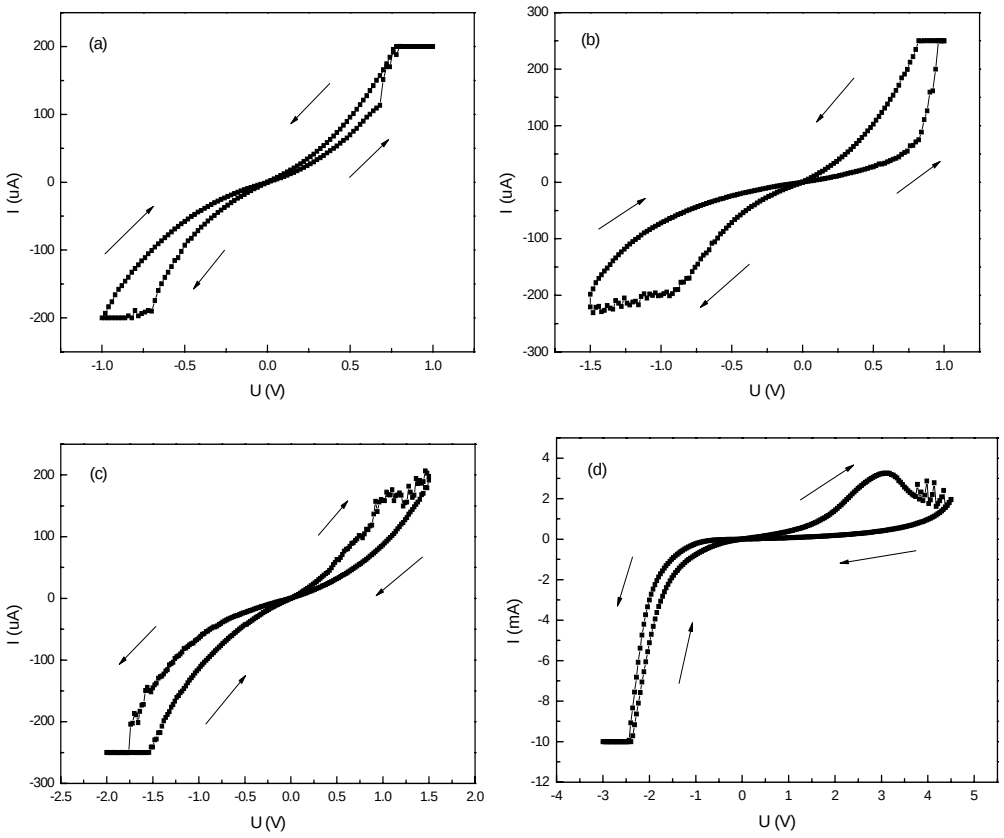


FIG. 4.16 Reversed switching polarity obtained by precisely controlled current compliance. (a) A W/BST/SRO device shows reversed switching polarity with current compliance of 200μA. (b) increase voltage amplitude to -1.5V with current compliance to 250μA the switching direction retained (c) increase voltage to +1.5V/-2V, the switching polarity was changed and (d) increase switching voltage to ±3V and 10mA current compliance the hysteretic developed further and eventually behaves the same as previous measurements.

However, we could obtain reversed switching polarity by precisely controlled current compliance in some devices measured. In Figure 4.16 (a) a W/BST/SRO device was switched between ±1V and the current compliance is limited to 200μA, which is much smaller than we used in previous study. It is interesting to note that the switching direction is opposite. In positive voltage branch the resistance decreased with the increased voltage, and in negative branch the resistance was recovered. Continuously increase voltage amplitude to -1.5V with current compliance to 250μA, the switching direction retained and only the hysteretic became more pronounced [Figure 4. 16 (b)]. When we increase the voltage to +1.5V/-2V, the switching polarity was changed as shown in Figure 4. 16 (c). The observed switching direction became the same as former measured but at lower current. If we gradually increase switching voltage to ±3V and 10mA current compliance as shown in Figure 4. 16 (d), the switching polarity did not change anymore. The hysteresis developed further and eventually behaves the same as in previous measurements.

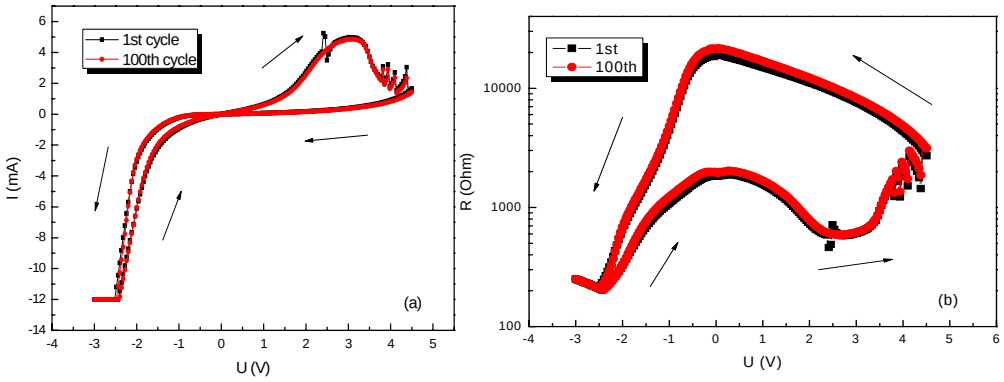


FIG. 4.17 (a) the endurance measurement of the finally observed I-V curves. (b) the resistance change Vs. applied voltage.

Figure 4.17 (a) displays the endurance measurement of the finally observed I-V curves. The resistance change is illustrated in Figure 4.17 (b). The shape of the switching curve has almost no change for 100 cycles and stands for excellent stability. Furthermore, the reversed switching in Figure 4.16 (a) is not as stable as switching in mA range, and the

shape of switching curves changed in every cycle and shrunk to weak loops if swept for long time. It should be noted that once the device was switched in mA range with normal switching direction, we can not convert it back to μA switching with the reversed switching direction. It may relate to the current paths permanently changed when devices switched from μA to mA, thus the resistance cannot return to its initial state.

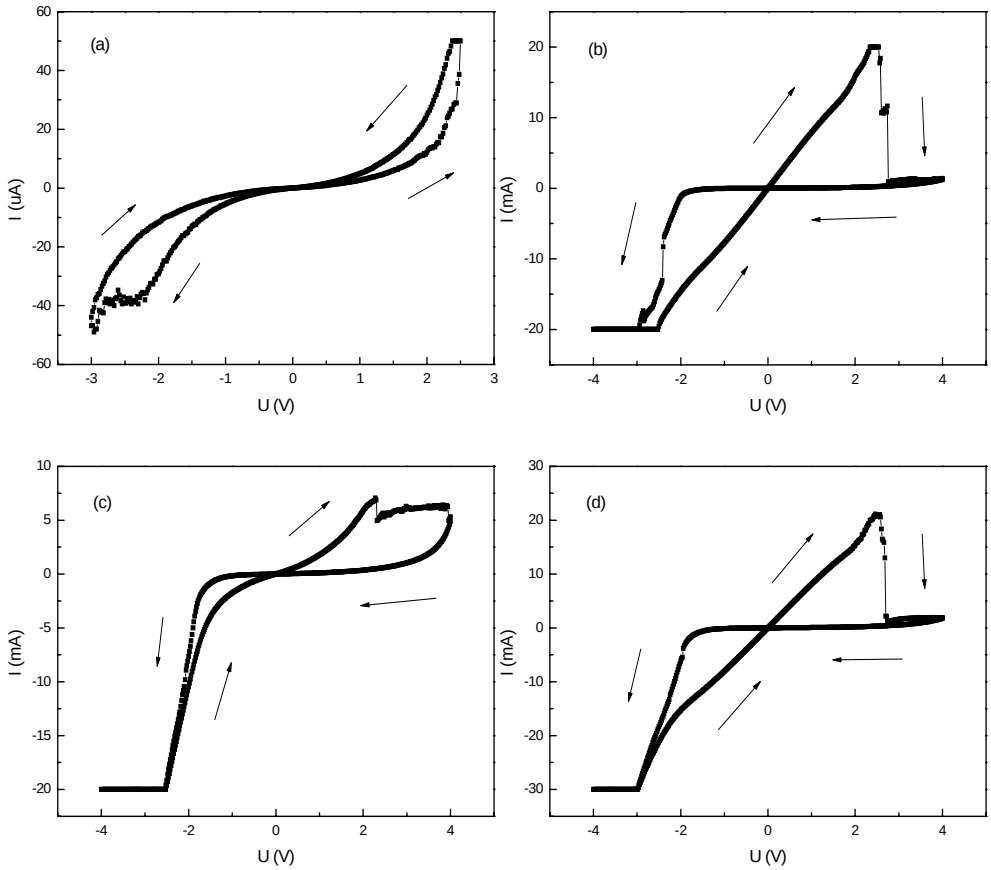


FIG. 4.18 Polarity change when current compliance was increased. (a)-(b) polarity changed with increased current compliance. (c) fatigued device with low R_{off}/R_{on} and (d) resfreshed device with high R_{off}/R_{on}.

Figure 4.18 shows the same result for polarity change when current compliance was increased. The switching direction was reversed from Figure 4.18 (a) to Figure 4.18 (b).

The LRS in Figure 4.18 (b) is more linear than in Figure 4.17 (a) and the resistance is smaller. When this device was switched for 20 cycles, the shape of I-V curve changed and the linear LRS degenerates to a non-linear one [Figure 4.18 (c)], which is similar to the I-V curve in Figure 4.17 (a). The R_{off}/R_{on} in this case was reduced from 334 to 17.

If compare the resistance of HRS and LRS in Figure 4.18 (b) and Figure 4.18 (c), we could find out the LRS increased 560% from 125Ohm to 704Ohm, meantime HRS decreased only 28% from 4.2KOhm to 1.2KOhm. This reveals that increased resistance of LRS maybe more responsible to the reduced R_{off}/R_{on}. The increased resistance of LRS is from the insufficient Set process. Thus we increased the negative current compliance to 30mA and the corresponding switching curve is shown in Figure 4.18 (d). It clearly indicates that the degenerated LRS was recovered and the R_{off}/R_{on} increased to 219.

For voltage-controlled bipolar switching, the voltage sweep range or current compliance should be properly controlled and the oxygen vacancies related electrochemical reaction occurs at only one interface. [53] However, as both interfaces may take part in the reaction by introducing a large amount of oxygen vacancies, the formation and the annihilation of oxygen can take place at both interfaces. If the reaction occurred at both interfaces that means one reaction takes place at one interface and the reverse reaction simultaneously takes place at the other interface. Thus both interfaces may contribute to the change of the total device resistance, but there should be one dominant interface. As the different voltage/current compliance used the reactions at both interfaces may be different. The low and high current compliance may distinguish the dominant switching interface in this case, and result in the switching polarity change.

4.10 Size dependence

For mechanism consideration, it is important to know where the device resistance change happened. The present popular explanations are the interface effect and filamentary conductance induced resistance change. To verify this assumption, the size dependence measurements were carried out to elucidate the origin of the resistance switching phenomena.

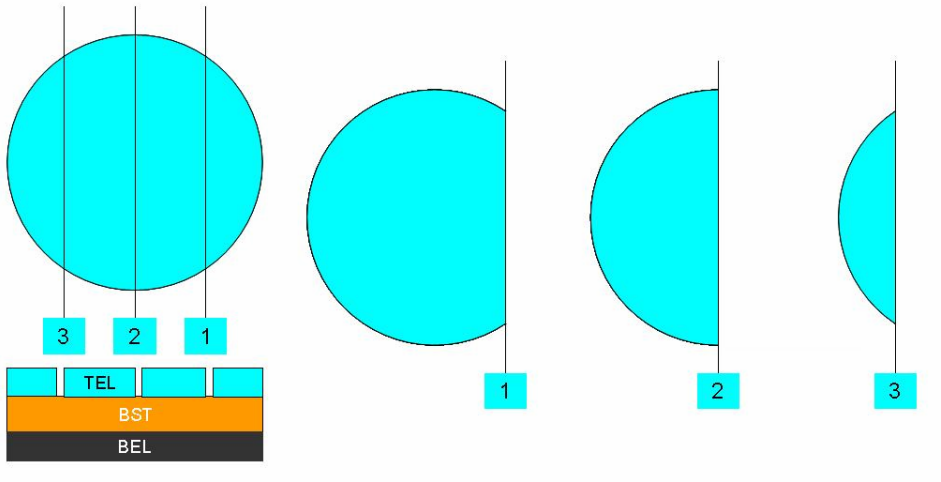


FIG. 4.19 Illustration of the pad size cutting procedure. The pads with size of around 1.0×10^6 um^2 were cut for 3 times by lithography and RIBE to reduce the pad size step by step.

Figure 4.19 shows the procedure how the pad size was reduced. Two pads with size of around 1.0×10^6 um^2 were chosen. One pad was set to HRS and anther one was set to LRS. The device resistance was measured at 0.1V. Then the pads were cut for 3 times by lithography and RIBE to reduce the pad size step by step. After each cut, the device resistance was measured and compared with the original resistance.

Figure 4.20 displays the result of the device resistance after three cuttings. The device resistance of HRS increased with reduced pad size and especially after the third cutting, the device resistance increased sharply. For device of LRS after first cutting the resistance increased but after second cutting, it decreased almost back to the original resistance. Cut for the third time, the device resistance increased again.

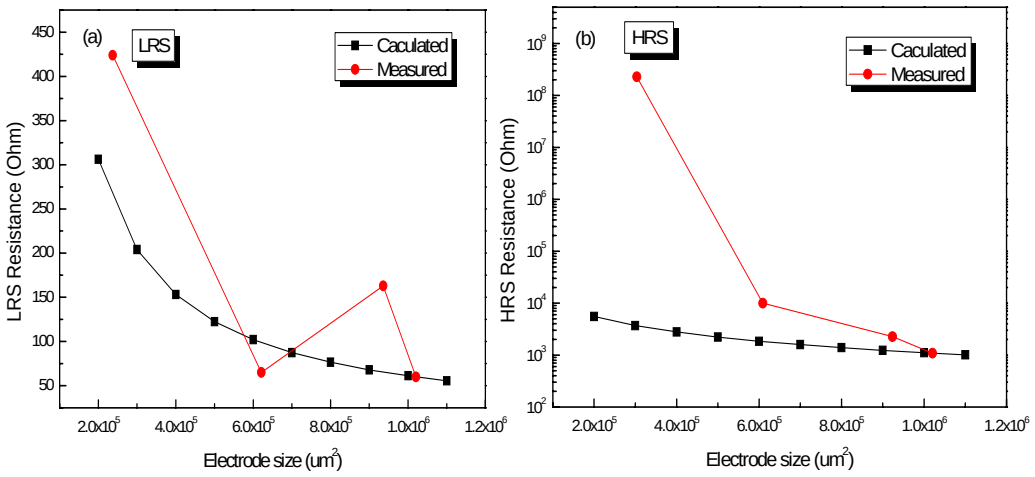


FIG. 4.20 Device resistances after three cuttings. (a) the device set to LRS and (b) the device set to HRS.

If the device resistance change is fully defined by the interface, the resistance should follow

$$R = \rho l/A \tag{4.1}$$

where R is the electrical resistance, ρ is the static resistivity, l is the thickness of the dielectric film (BST) and A is the pad size. The calculated resistances were also shown in Figure 4.20. However, both the resistances of measured HRS and LRS after pad cutting are higher than the calculated data only expect the second cutting of LRS. This means that the mechanism of resistive switching is not simply a pure interface effect, but a more complicated one. The results also clearly show that there are more than one filament existed responsible for the device resistance change. Because if there is only one filament, the device resistance should only change once the filament was cut away and for other cuttings the resistance will not be influenced.

4.11 R_{off}/R_{on} adjustment

For application as RRAM, the resistance change of devices is preferred to be larger in order to be easily detected by sensor circuits. Although an R_{off}/R_{on} ratio of only 1.2 to 1.3 can be utilized by dedicated circuit design as shown in MRAM, R_{off}/R_{on} ratios > 10 are required to allow for small and highly efficient sense amplifiers [28] and, hence, RRAM devices which are cost competitive with Flash.

Figure 4.21 (a) shows the W/BST/SRO device swept with different current compliance ranging from 5mA to 15mA. It is notable that the hysteresis is more pronounced when the device was measured with higher current compliance. The I-V curves are in the same switching directions, clockwise in positive voltage branch and counter-clockwise in negative branch, independent of the different current compliance applied.

The current compliance dependence on R_{off}/R_{on} was shown in Figure 4.21 (b). The HRS and LRS was read at +0.5V. Although there is small variations, the trend is rather clear that the R_{off}/R_{on} increased steadily by increasing current compliance. At current compliance of 15mA, the R_{off}/R_{on} reaches about 7, more than 3 times larger than the R_{off}/R_{on} at current compliance of 5mA. The physical origin of the increased R_{off}/R_{on} may comes from more oxygen vacancies involving in switching process due to higher

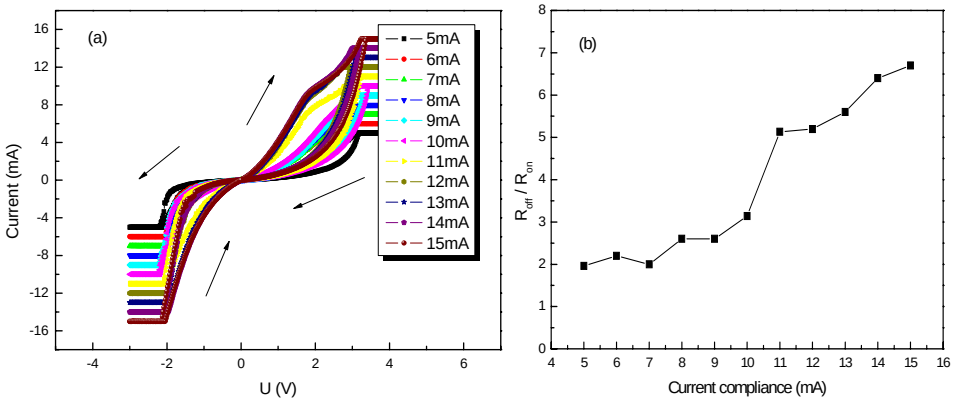


FIG. 4.21 W/BST/SRO device swept with different current compliance ranging from 5mA to 15mA (a) and current compliance dependence on R_{off}/R_{on}. (b) current compliance dependence on R_{off}/R_{on}.

actual electrical field was applied with higher current compliance, and the device resistance were tuned by different numbers of concentration or distribution of oxygen vacancies at W/BST interface.

However, from the power consumption point of view, higher current may lead to more electricity cost. Figure 4.22 (a) shows a typical I-V hysteresis of W/BST/SRO device which has a non-linear transition between HRS and LRS. The corresponding Resistance Vs. applied voltage is shown in Figure 4.22 (b), and it is obvious that the resistance

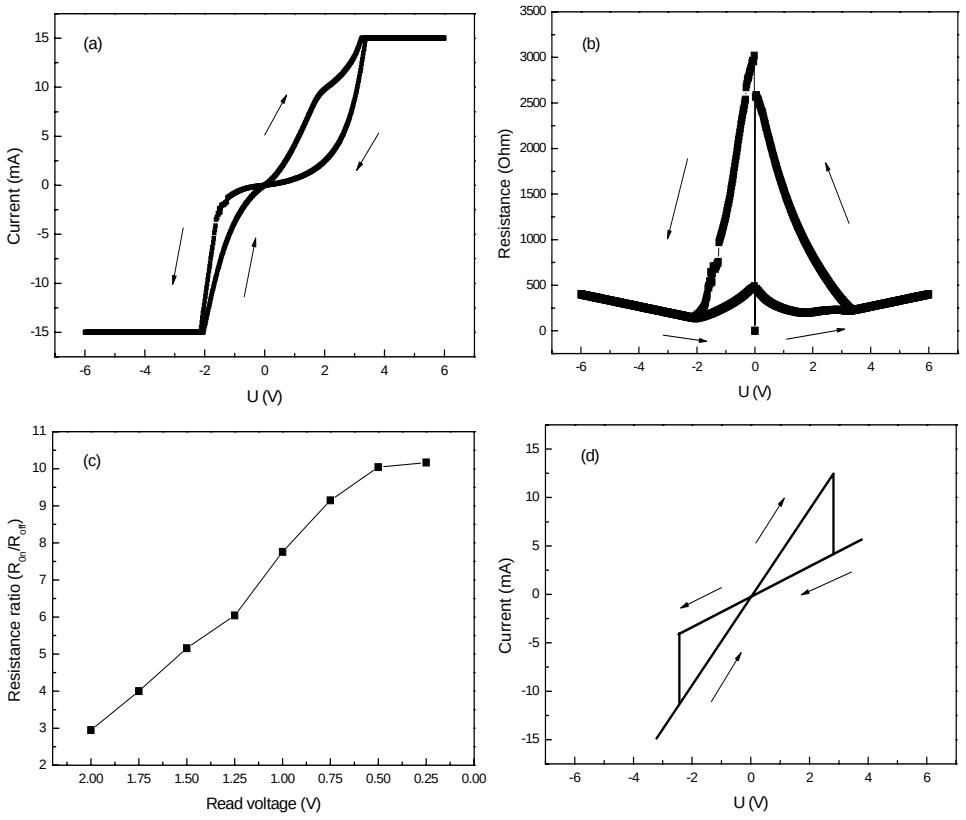


FIG. 4.22 (a) A typical I-V hysteretic of W/BST/SRO device which has a non-linear transition between HRS and LRS. (b) corresponding Resistance Vs. applied voltage and the resistance window (R_{off}/R_{on}) changed at different voltages. (c) read voltage dependence on R_{off}/R_{on}. (d) devices exhibits linear I-V the R_{off}/R_{on} will not be changed by changing the read voltage.

window (R_{off}/R_{on}) changed at different voltages. Here in order to obtain higher resistance ratio, we investigated the readout voltage dependence on the R_{off}/R_{on}. Because the positive resistance window is larger than in negative branch as seen in Figure 4.22 (b), here we choose +0.25V, +0.5V, +0.75V, +1V, +1.25V, +1.5V, +1.75V and +2V as the read voltage. It should be noted that basic principal to read the resistance is not to influence or change the device resistance during read process. The highest readout voltage we chosen is +2V, which is lower than the transition voltage about +3V [Figure 4.22 (b)], thus the read process is safe for evaluation of the resistance ratio. The result is shown in Figure 4.22 (c) and the R_{off}/R_{on} decreased when increasing the read voltage. The highest R_{off}/R_{on} is ~10 at 0.25V.

Furthermore, as there are different types of switching curves, if devices exhibit linear I-V as shown in Figure 4.22 (d), the R_{off}/R_{on} will not be changed by changing the read voltage. Thus the read voltage dependence is only valid for non-linear I-V curves.

4.12 Multilevel switching potential

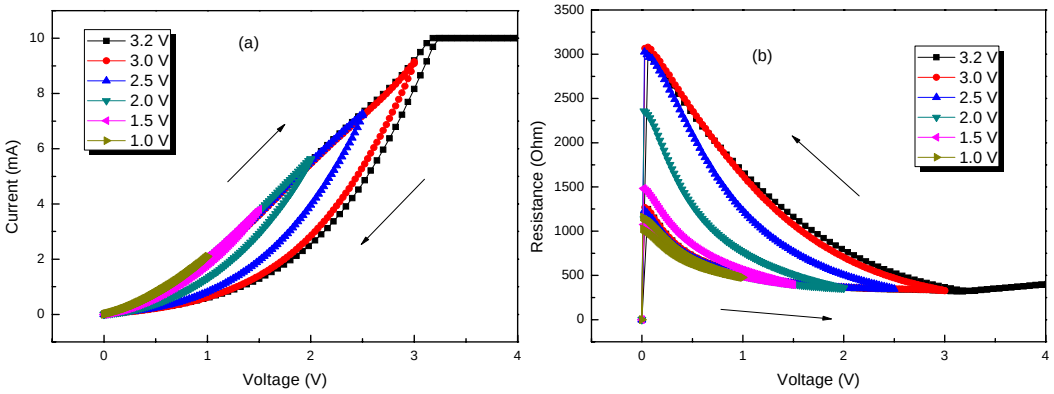


FIG. 4.23 (a)The I-V curve of different applied voltages from 1.0V to 3.2V and (b) different applied voltage leads to different resistance, which ensures the multi bit storage.

In electronics, a multi-level device is a memory element capable of storing more than a single bit of information, generally two or more bits are stored in one memory cell. The multi-bit techniques appear to be able to double or quadruple the density even at existing linewidths. The present NAND Flash memory in the market uses 2bit/cell thus RRAM have to show more bit storage capability in order to beat NAND technology.

Figure 4.23 (a) shows the I-V curves at different applied voltages from 1.0V to 3.2V. The initial resistance state is LRS and after sweeping to a given bias, the device was switched to HRS. Different applied voltage leads to different resistance which can be observed in Figure 4.23 (b). Although all curves starts at the same resistance, the finally reached resistance is different. All the finally reached resistance states are non-volatile thus if we define them to multi-bit, the device could store more data in one cell than the traditional memory.

We could obtain multi-level switching by either controlled voltage or current compliance, which were shown in Figure 4.24 (a) and (b). By sweeping the switching voltage from +1.0V to +4.7V, the device reached different HRS, while at the negative voltage branch the voltage is kept the same. In Figure 4.24 (b) when current compliance ranging from

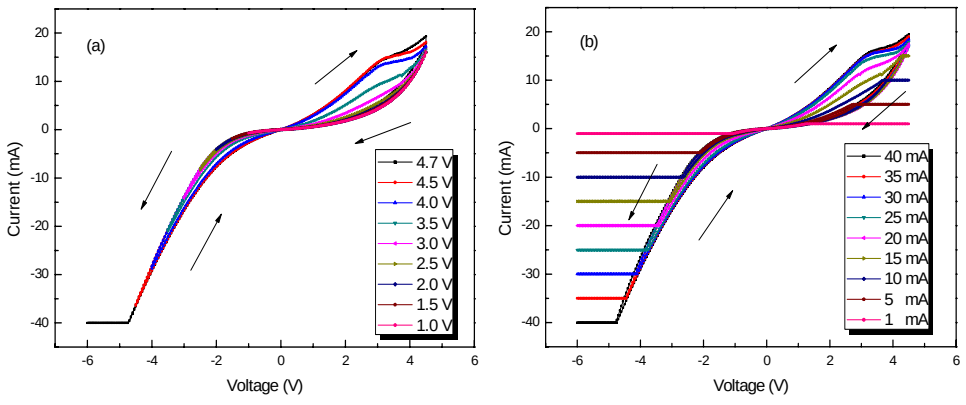


FIG. 4.24 Obtain multi-level switching by either controlled voltage (a) or current compliance (b).

1mA to 40mA was used, we could obtain the same result as shown in Figure 4.24 (a). Thus the controlled voltage works the same as using current compliance, both are applicable to switch devices to multi resistance states.

The controlled voltage or current compliance discussed above are all in voltage driven mode, which means the multi level switching was observed by sweeping voltage. Similar to this, we can also obtain the different resistance states in current driven mode. Figure 4.25 shows the I-V curves of different current amplitude from 5mA to 15mA. The increased current leads to a more pronounced I-V curve and thus the finally observed HRS is increased.

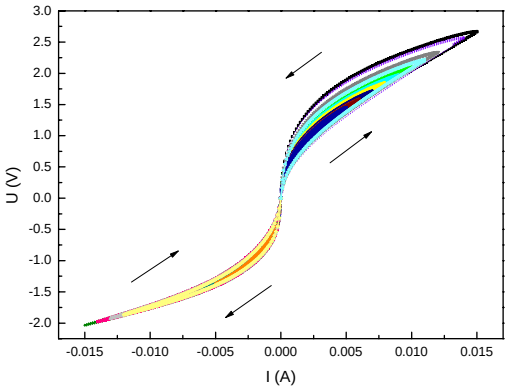


FIG. 4.25 Multi-level switching in current driven mode.

Chapter 5

Bipolar and Unipolar resistive switching transition

The unipolar switching and bipolar switching have been widely observed and researched in simple binary metal oxide such as NiO, [12] ZrO_2, [13] TiO_2, [14] while expect for the report by Choi *et al.*, [15] generally only the bipolar switching is observed for complex perovskite type oxide (ABO_3) films, such as PCMO, [16] Cr-doped $SrZrO_3$, [17] and ($Ba_{0.7}Sr_{0.3}$) TiO_3. [18, 19] Because we could switch device resistance with the same or reversed voltage polarity in unipolar resistive switching, therefore the unipolar switching is also called nonpolar resistive switching. Furthermore, there is only bipolar-unipolar transition observed in binary metal oxide TiO_2. [20]

The unipolar switching has much larger resistance change than the bipolar switching, and this makes it much easier to read the memory state. [21] In addition, devices using unipolar switching can be potentially integrated in higher density. [22] Thus the realization of unipolar switching in perovskite films is of common interest for the potential application of these materials as well as for the elucidation of the microscopic mechanisms.

The unipolar resistive switching is thought to be the fuse/antifuse of conduction paths or filaments and the mechanism of bipolar resistive switching is considered to be the migration of anions. For polycrystalline BST thin films, forming is necessary to transit thin film from highly insulating to a more conductive state to realize the bipolar or unipolar resistive switching. During the electroforming process the device consumes large amount of electric power and the power dissipation in the cell is estimated to be high enough to change the local microstructure or morphology of the RRAM device [53] and to form the conduction paths between top and bottom electrode.

5.1 Device fabrication

The 200 nm-thick BST thin film was deposited on a Pt/Ti/SiO_2/Si substrate. The deposition condition is the same as the epitaxial BST thin films. The BST film is grown polycrystalline which was confirmed by X-ray diffraction measurements [Fig. 5.1 (a)]. The AFM of the topography of the as deposited polycrystalline BST film with RMS=4.25nm is shown in Fig. 5.1 (b). 100 nm-thick Pt thin film was sputtered and then patterned to areas of 0.04mm^2 to form Pt top electrodes and hence sandwich-like Pt/BST/Pt structures.

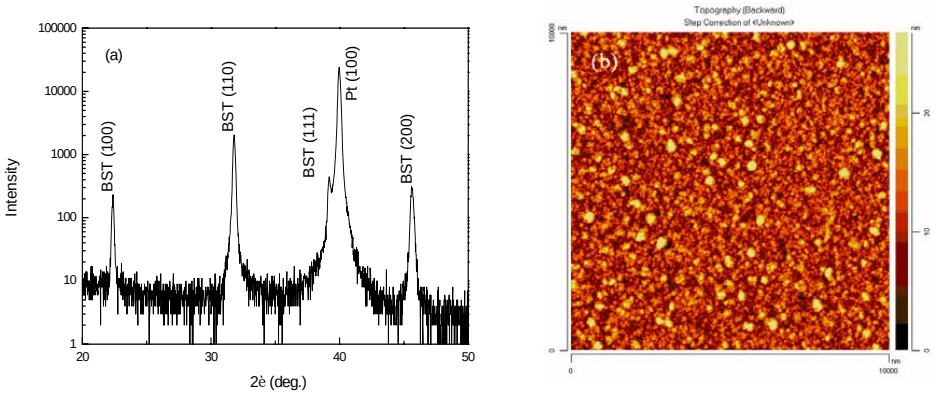


FIG.. 5.1 (a) X-ray diffraction measurement of grown BST film and (b) AFM of the topography of the as deposited polycrystalline BST film with RMS=4.25nm.

5.2 Characteristics of resistive switching phenomenon

5.2.1 Bipolar resistive switching behavior

The as-prepared Pt/BST/Pt devices with polycrystalline BST thin films were highly insulating and no resistive switching characteristic was observed. The initial soft breakdown which was known as the forming process was carried out by applying a positive or negative voltage of 10V with a current compliance of 1mA to trigger the device from the initial highly insulating state to a more conductive state.

After the first forming process, the device became more conducting and the resistance was reduced. In this case, the Pt/BST/Pt device shows bipolar switching behavior which is illustrated in Fig. 5.2 (a). The switching polarity of the I-V curve is similar to the former reported epitaxial BST films, that is the clockwise in positive voltage branch and counter-clockwise in negative voltage branch.[40] However, the R_{off}/R_{on} is smaller than the epitaxial BST films, in which forming is not required as the epitaxial BST films are more conductive, which we have shown in Chapter 4. When the current compliance was continuously increased to 5mA, the second forming occurs at the negative branch and the device became more conducting. Fig. 5.2 (b) shows the bipolar switching behavior of the Pt/BST/Pt device after the second forming and the R_{off}/R_{on} is increased than in Fig. 5.2 (a). In all switched pads (26 switched pads out of 40 measured pads) we could observe the initial bipolar switching at small current compliance after forming and the R_{off}/R_{on} was increased when further formed with higher current compliance.

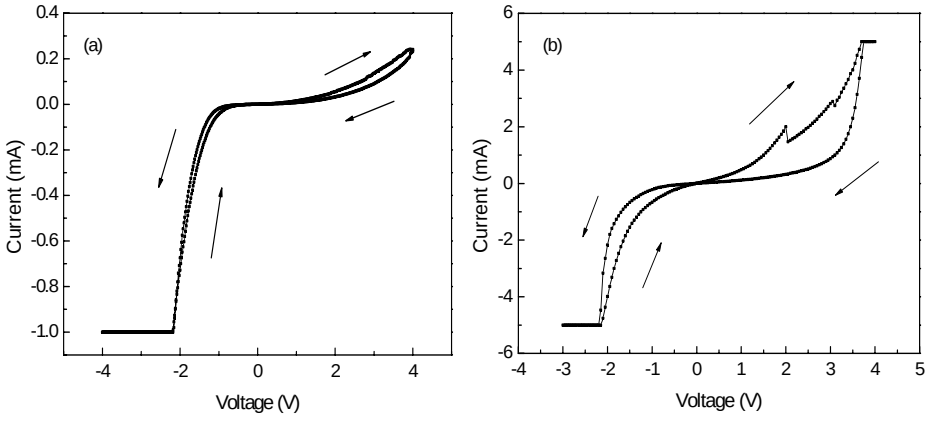


FIG. 5.2 (a) Bipolar resistive switching of Pt/BST/Pt devices after the first forming and (b) after the second forming process.

5.2.2 Unipolar resistive switching behavior

The switching curves in Fig. 5.2 (a) and Fig. 5.2 (b) are all transitions from non-linear HRS to non-linear LRS. However, after the third forming process applied with a higher current compliance of 15mA, the device was transformed to a linear I-V behavior, corresponding to the LRS of the unipolar switching.

Fig. 5.3 (a) shows the I-V characteristics of unipolar switching observed after the third forming process with current compliance of 15 mA. The device shows linear LRS after the third forming at 15 mA, which can not be observed at smaller forming current. When the voltage was swept to 1V, a sudden drop of current is observed and the switching from LRS to HRS occurs (Reset process). While sweeping the voltage again to 4V with a current compliance of 15mA, the current jumped abruptly at about 3 V and the device was switched to LRS again (Set process). The Set and Reset process can also occur with negative voltage. For statistics, all measured pads show bipolar switching can be transited into unipolar switching, although the exact forming current to reach the linear LRS varied from pads to pads.

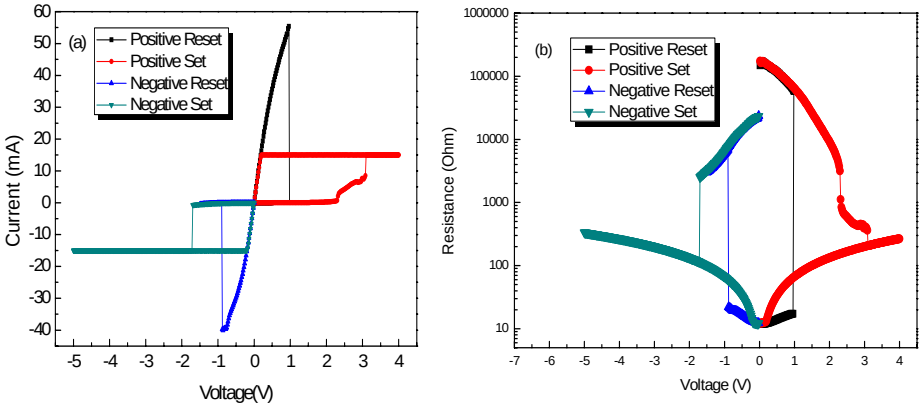


FIG. 5.3. (a) Unipolar switching after the third forming and (b) resistance change vs. applied voltage of Pt/BST/Pt devices.

The measured Pt/BST/Pt devices exhibit bi-stable resistance state and the resistance ratio of high and low resistance (R_{off}/R_{on}) in unipolar switching is more than 1000, which is much larger than the R_{off}/R_{on} in bipolar switching as shown in Figure 5.2. The resistance development with switching voltage was shown in Figure 5.3 (b) and it is easy to read the resistance difference at low voltage regime.

Above mentioned measurements and characteristics are all based on Pt top electrodes. In order to clarify that the bipolar to unipolar switching transition is only related to the BST film, bottom electrode and the substrates, devices with W top electrode were also prepared in the same condition and parameters as used before.

The devices with W top electrode are also of highly insulating state and no resistive switching characteristic can be observed. The initial forming process was necessary to trigger the device from the initial highly insulating state to a more conductive state by applying a positive or negative voltage of 10V with a current compliance of 1mA. After the first forming process, the device shows bipolar switching behavior which is illustrated in Fig. 5.4 (a). The bipolar switching behavior is very stable and in endurance measurement the device can be switched for 300 cycles, and no obvious fatigue was observed. This is consistent with the endurance measurement of epitaxial BST film with W top electrode as discussed in Chapter 4.

When the W/BST/Pt device was further formed with higher current compliance, the device conductance was increased and finally the metallic LRS was reached. Afterwards we could obtain typical unipolar switching behavior as shown in Fig. 5.4 (b). The I-V curve is similar to the Pt/BST/Pt devices, but the difference between Set current and Reset current is smaller than observed in Pt/BST/Pt devices.

Although the W/BST/Pt devices show bipolar-unipolar transition, the same as we have

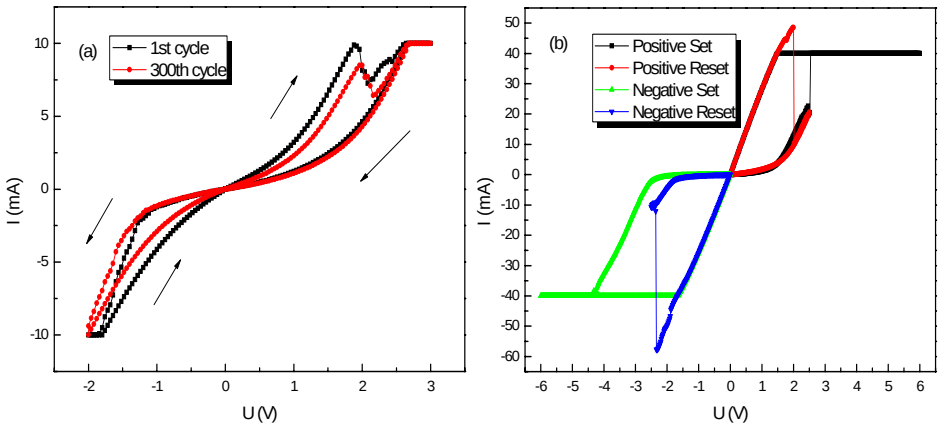


FIG. 5.4 W/BST/Pt device (a) Bipoalr switching after first forming. (b) Unipolar switching observed when devices were further formed. The switching polarity is the same to using Pt top electrodes. Difference between Set current and Reset current in unipolar switching is smaller than observed in Pt/BST/Pt devices

observed in Pt/BST/Pt devices, the performance of bipolar switching and unipolar switching is strongly influenced by the top electrode, i.e. the improved endurance behavior with W top electrodes.

5.2.3 Retention

To ensure the non-volatile property, the resistance switched between HRS and LRS by applied voltage was measured at 0.5V for 10^4 seconds. Figure 5.5 (a)-(c) present the retention behavior for bipolar switching in Figure 5.2(a), Figure 5.2(b) and unipolar switching in Figure 5.3(a). The results show that all resistance states in bipolar and unipolar switching are well stored and also the low read voltage has no influence on the device resistance.

Figure 5.6 displays the resistance evolution after three forming steps. In LRS as shown in Figure 5.6 (a), the resistance is reduced by forming and the resistance is degraded from

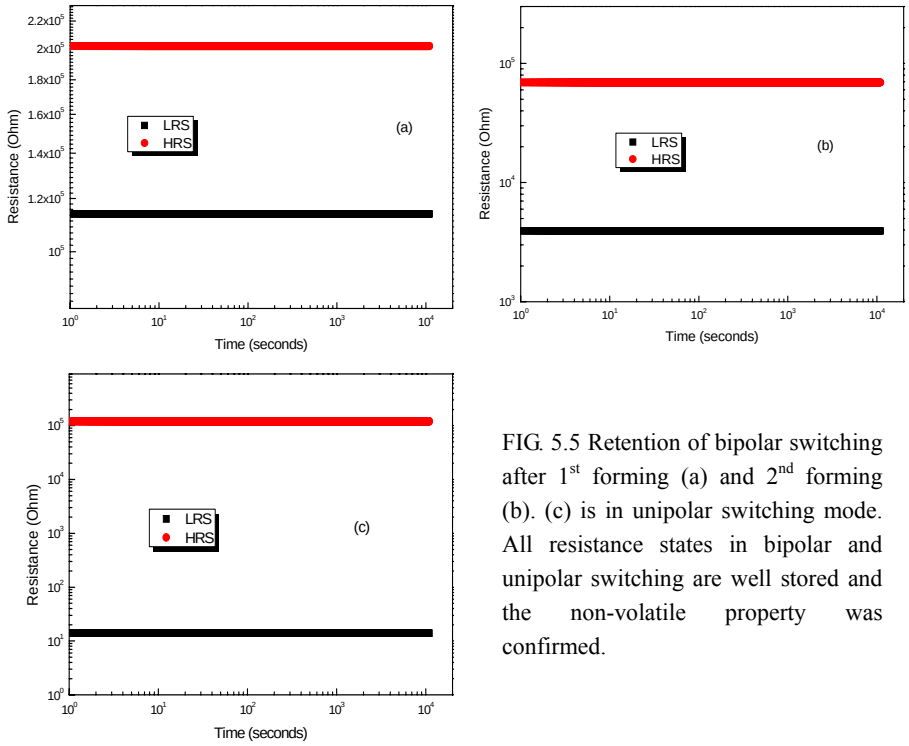


FIG. 5.5 Retention of bipolar switching after 1st forming (a) and 2nd forming (b). (c) is in unipolar switching mode. All resistance states in bipolar and unipolar switching are well stored and the non-volatile property was confirmed.

highly insulating state about 202KΩ to metallic state of 14Ω. The resistance degradation in LRS may relate to filaments growth and metallic phase formed during forming process. The resistance of HRS [Figure 5.6 (b)] in bipolar switching is decreased with the forming steps, however, when device was transformed to unipolar switching mode after third forming, resistance of HRS increased again. In bipolar switching the oxygen movement along filaments may induce the device conductance variation, but in unipolar switching the fuse/anti-fuse filament is regarded to be responsible to distinguish LRS and HRS. Thus in bipolar switching mode the filaments developed with forming and HRS also decreased, whereas when transited to unipolar switching the filament(s) was (were) ruptured and resistance of HRS increased again.

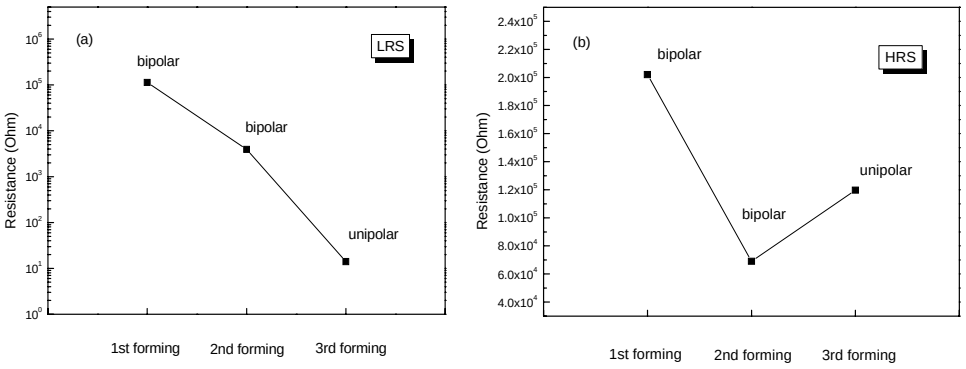


FIG. 5.6 Resistance evolutions after three forming steps. (a) resistance of LRS and (b) resistance of HRS.

5.2.4 Endurance

The endurance of unipolar resistive switching is generally not as good as in bipolar switching. This may result from the high power involved in Set and Reset process. The high power consumption increased the instability of the material system thus RRAM devices used in unipolar switching mode is easier to fatigue.

Fig. 5.7 (a) displays a Pt/BST/Pt device switched for 20 cycles with current compliance of 7mA. The Set process was preceded with same current compliance but resulted in different LRS which can be seen from the different slope of the Reset curve. The Reset process needed higher current to switch the device from LRS to HRS when the LRS became lower and left a slightly varied Reset voltage window like observed in binary oxide. [87-89] The Set voltages also showed a wide distribution. After the 20^{th} cycle, the device can not be switched due to fatigue. However, the W/BST/Pt devices can not switch as well as Pt/BST/Pt device and are easier to fatigue.

During the Set process, the obtained metallic LRS means the metallic conductive channel was formed between top and bottom electrode. The Set process is thought to be

accompanied with a release of huge amount of oxygen. The film maybe permanently changed when oxygen was ejected to the air through top electrodes and the local resistance degradation induced by Joule heating effect. The newly formed conduction paths decreased the resistance of the device and more current was needed to rupture the additional conduction paths. [53]

However, when the current compliance is increased to 8mA, the device was switch-able again for another 78 cycles, as illustrated in Fig. 5.7 (b). Fig. 5.8 (a) shows a complete loop of Reset/Set process with a high Set current compliance. The Reset first happened at about 0.7V and when the voltage is further swept to about 1.6V, the Set process occurred. Because the current compliance was set to 100mA, much larger than the normal Set current compliance which is generally lower than the Reset current, the resistance of LRS was further reduced. This indicates beyond the randomly scaling of the resistance of LRS during unipolar switching, we could control the LRS and realize multilevel switching potential by defining the Set current compliance. This was confirmed by the Set current dependence as shown in Figure 5.8 (b).

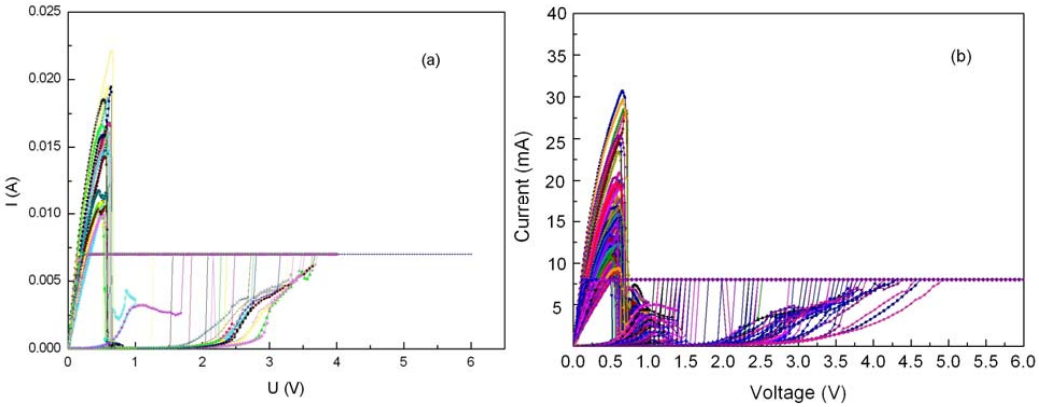


FIG. 5.7 Unipolar switching with Set current compliance of (a) 7mA and (b) 8mA. The same device can be switched for 20 cycles with 7mA Set current compliance, and 78 cycles with 8mA Set current compliance. The Set process was preceded with the same current compliance but resulted in different LRS, and the followed Reset process needed higher current to switch the device back to HRS.

Our endurance measurements are all measured in voltage-driven mode. The Set process in voltage-driven mode will be out of control once the current reached the compliance and we do not know the exact voltage applied on the devices. Therefore, the recovery of the ruptured conduction paths or filaments is believed to occur randomly. Once the filament(s) was(were) recovered, we obtain the LRS of the RRAM device. The fluctuation of the LRS resistance after the voltage-driven Set switching is speculated to be attributed to the filaments random recovery. [53]

During long time switching process the set and reset voltages, the reset current, and the resistances in the HRS and the LRS show quite large fluctuation with respect to the switching cycle numbers. The large fluctuation can cause to misread the resistance state of memory cells or directly lead to device failure, limits the application of unipolar switching devices to be used as RRAM. There are some reports shows that the stability of unipolar switching devices can be improved by modifying the switching devices structures or optimizing the deposition parameters of the switching films. [90, 91] On the

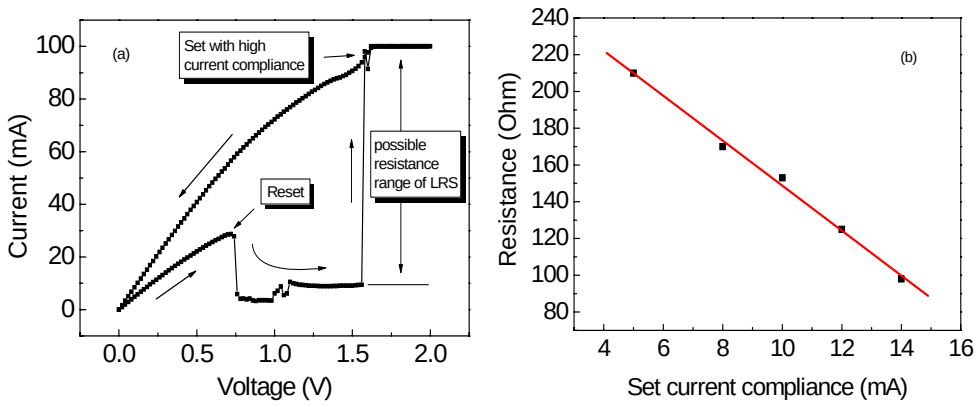


FIG. 5.8 (a) A complete loop of Reset/Set process with a high Set current compliance. The Reset first happened at about 0.7V and when further sweep the voltage to about 1.6V, the Set occurred. Because the current compliance was set to 100mA, much larger than the normal Set current compliance which is generally lower than the Reset current, the resistance of LRS was further reduced. (b) Set current dependence and multilevel switching potential.

other hand, the enhancement of the switching voltage stability in TiO_2 was observed by current-controlled set switching instead of voltage-controlled.[53]

5.2.5 Temperature dependence

The bipolar switching is thought to be due to the oxygen vacancy migration through the filaments at the interface, [49] and for unipolar switching the formation or rupture the metallic filaments with the contribution of Joule heating is suggested as the mechanism [32, 50]. The local temperature of the filaments can reach as high as 700–800 K by the localized Joule heating effect. [92] Chae *et al.* observed the filaments in unipolar switching in TiO_2 thin films by conductive AFM and the resistance of LRS and HRS is distinct after switching.[42]

Fig. 5.9 shows the temperature dependence of both LRS and HRS in bipolar and unipolar switching. The transition from bipolar switching to unipolar switching induced by the third forming is accompanied by a change of the conduction behavior in LRS, from the thermally activated charge carrier transport to the metallic conduction, while in HRS both the bipolar and unipolar switching are thermally activated charge carrier transport, the same as reported elsewhere. [41]

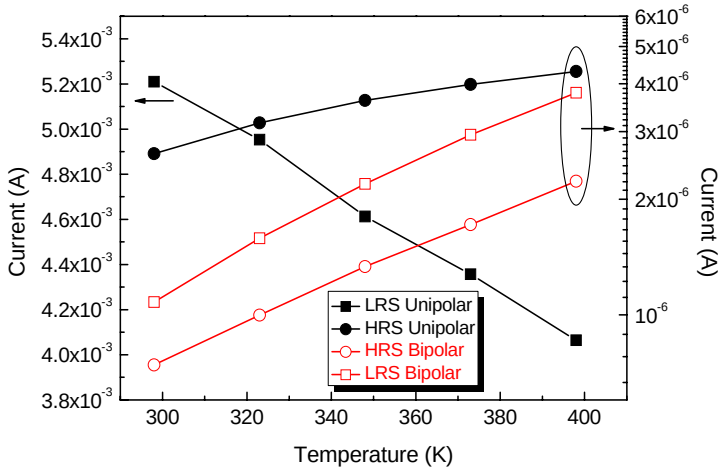


FIG. 5.9. The temperature dependence of both Bipolar and Unipolar switching.

As we attribute both unipolar and bipolar switching to filaments effect, the conduction behavior changed in LRS may comes from the change of filaments property. After the first and second forming [Fig. 5.2 (a) & (b)], the semiconducting filaments may form due to soft breakdown. When a positive bias is applied on the Pt top electrode, the oxygen vacancies can migrate from the interface to the bulk through the filaments and the device is switched to HRS. When a negative bias is applied, the oxygen vacancies are pulled back to the interface and the LRS is obtained. Moreover, once the device was transformed into a linear I-V behavior after the third forming [Fig. 5.3 (a)], the filaments property changed to metallic conduction behavior. When we get the metallic conduction behavior, which is LRS of unipolar switching mode, the device was transformed from bipolar switching to unipolar switching mode.

5.3 Proposed mechanism for bipolar to unipolar resistive switching transition

In general, bipolar switching in perovskite insulators is attributed to a voltage-driven oxygen vacancy migration [49] within extended defects and the resulting redox-process related metal-to-insulator transition. While thermal effects generally are considered to play a minor role for bipolar switching, Joule heating plays a key role for the formation and rupture of metallic filaments in the unipolar switching mode.[32] The conduction paths or so called filaments are considered to be composed of oxygen-deficient phases with a higher conductivity due to self-doping than the stoichiometric phase, which was mainly formed during forming process.[53] In case of unipolar switching, the local metal-to-insulator transition is driven by the energetically favored low valence state in the high-temperature region rather than by a voltage-induced accumulation of oxygen vacancies.[28]

As the bipolar and unipolar resistive switching are all induced by forming process (soft breakdown), it is of great importance to know in details about what happened during

forming process. In ceramics with mixed ionic/electronic grains, grain boundaries often act as barriers for the cross-transport of charges. Due to the segregation of charged cations in the grain boundaries, the resulting space charge depletion regions result in a strong reduction of the leakage currents across the boundaries.[93, 94] Therefore, the resistivity of our virgin polycrystalline BST thin films exceeds the resistivity of the epitaxial thin films several orders of magnitude.

To reduce the device resistance and get resistive switching behavior, a high voltage with controlled current compliance is necessary to be applied to the RRAM devices based on polycrystalline BST films thus forming is the initial process for resistive switching measurements. During forming process the resistance of initially highly insulating polycrystalline BST films degraded under the applied voltage/current. Forming process can be judged as an electrolytic reaction which forms oxygen gas[95] and meanwhile induce oxygen vacancies in BST film. For example, the forming in TiO_2 can be regarded as an electrolytic reaction resulting in the formation of oxygen gas and leaving oxygen vacancies in TiO_2 matrix. The oxygen ions could accumulate at the anode and form oxygen gas by donating two electrons per each oxygen ion to the conduction band. This self-doping process can lead to the formation of conductive paths and reduction of device resistance. [96] The reaction of oxygen gas formation can be expressed in the Kröger-Vink defect notation as

$$O_O^{\times} \rightarrow V_O^{\cdot\cdot} + 2e^{-} + 1/2O_2 \qquad (5.1)$$

Moreover, forming induces not only the resistance degradation of polycrystalline BST film, but also the morphology or local composition change of switching devices. It is known that the power dissipation is inversely proportional to the resistance, thus during forming process when the high voltage was applied to the device, once the resistance decreases abruptly, the power dissipation consumed in the material system is strongly increased. The power dissipation gives rise to Joule heating increasing the lattice

temperature [53] and induces the resistance decrease by a local thermally-induced redox-process. Under such high Joule heating the temperature at the local filament may reach thousands of Kelvin. Obviously the material in the switching device at such a high temperature will have phase transitions. Therefore, the resistance degradation of polycrystalline BST film is expected to be accompanied with changes in the morphology or local composition of the switching devices.

One example of morphology changes induced by forming is the dielectric breakdown induced epitaxy (DBIE) for dielectrics. [97] The epitaxial growth of Si on Si substrate could be induced by DBIE in a metal-oxide-semiconductor capacitor and the Joule heating effect may probably be responsible for this morphology change.

The NiO thin film based RRAM has been intensively investigated and it also shows both bipolar and unipolar switching, thus we choose NiO thin film based RRAM as a model system. Local composition change induced by forming process can be seen in polycrystalline NiO films.[98] After SET process the polycrystalline NiO film reveals a change in the grain shapes and NiO_x grains are microscopically deformed near the Pt TE interface. The local change of the fine NiO_x structure after the set and reset processes seems to be closely associated with the local deoxidization and anodization phenomena of the filaments that occur due to the compliance current stress in the region near the anode and is responsible for the resistance switching. The excess forming voltage makes filamentary conducting paths permanent. Ni-rich atomic arrangements observed at the defective area can be attributed to the high voltage stress of the switching failed state, and this may result in a local density increase of Ni filamentary conducting paths near the grain boundary. The EELS spectrum taken at the NiO_x grain boundary confirms the formation of a Ni filament at the grain boundary.

Because the current compliance of 15mA used in the 3rd forming procedure is higher than

usually used for bipolar switching, a higher electrical power is applied to the sample and the dissipation of heat might become significant within the conducting filament. As a result, additional oxygen might be driven out of the filament due to the tendency of Ti to adopt a lower valence state at higher temperatures. The Reset process occurs, as soon as the threshold voltage for the thermal dissolution of the filaments is exceeded.[99] In Reset process, the sudden resistance increase indicates the rupture of filaments, which probably results from the Joule heating induced by the large external current. [100]

It should be noted that, if the current compliance used in the 1st forming is high enough to completely reach the metallic LRS, the bipolar switching will be skipped and the device will directly show unipolar switching. Accordingly, the forming current is of great importance and the metallic LRS is the prerequisite for observation of unipolar switching behavior in polycrystalline BST thin films.

Since a forming procedure which transforms insulating samples to a metallic LRS is prerequisite for the observation of unipolar switching, we have to regard the forming procedure in our specific case. After the first forming and second forming (Fig. 5.2), semiconducting filaments are formed as proved by the temperature dependence of the LRS shown in Fig. 5.9. We conclude from this observation, that the creation of oxygen vacancies during the first two forming procedures is insufficient for the formation a metallic filament. Once the LRS branch of the I-V curve has changed to a linear shape after the 3rd forming (Fig. 5.3), the filament property changed to metallic conduction behavior and the device exhibits unipolar switching.

Since we observed only bipolar switching in epitaxial BST films as reported before [40] and no unipolar switching in epitaxial perovskite systems have been observed so far, grain boundaries have to play a crucial role for the realization of the unipolar switching mode. A statistics is given in Table 5.1 and it listed that the polycrystalline films are more inclined to show unipolar switching behavior. Consider the existence of boundaries, forming process occurred non-homogeneously in device under external bias. The degradation of the resistance takes place in localized area, and the localized area

contributes to the resistance of the overall resistance. The non-uniform oxygen vacancy distribution gives rise to a non-homogeneous conductivity distribution, implying the formation of local conduction paths, most probably at grain boundaries. The polycrystalline BST film shows higher resistance thus a complete forming process (the 3rd forming) to reach the metallic LRS is required for observation of unipolar switching, while no forming is necessary for more conductive epitaxial BST films. Similarly to our assumption, Lee et al. observed that the epitaxial binary oxide NiO shows bipolar switching while the polycrystalline NiO shows unipolar switching. [101]

TABLE 5.1 A statistics of materials systems showing that the polycrystalline films are more inclined to show unipolar switching behavior.

Dielectric	*Bottom electrode*	*Crystalline*	*Switching style*	*References*
NiO	Pt	Polycrystalline	Unipolar	101
	SRO	Epitaxial	Bipolar	
	Pt	Polycrystalline	Unipolar (stable)	102
	Pt	Epitaxial	Unipolar (instable)	
	Pt	Polycrystalline	Bipolar (CAFM)	103
	Pt	Polycrystalline	Unipolar (CAFM)	104
HfO_2	Pt	Polycrystalline	Bipolar	105
	Pt	Polycrystalline	Unipolar	
ZrO_2	Pt	Polycrystalline	Bipolar	34
	Pt	Polycrystalline	Unipolar	
TiO_2	Pt	Polycrystalline	Bipolar	38
	Pt	Polycrystalline	Unipolar	
SZO: Cr	SRO/Si	Polycrystalline	Bipolar	106

Although epitaxial BST films grown on SRO/STO show bipolar switching and polycrystalline BST films exhibit both bipolar and unipolar switching, the BST film deposited on SRO/SiO_2/Si only shows weak bipolar switching [Figure 5.10 (b)]. The BST film was confirmed to be polycrystalline grown on SRO/Si as shown in Figure 5.10 (a). From the grain boundaries point of view, the lack of transition to unipolar switching in BST/ SRO/SiO_2/Si device may come from the form of grains. In SEM pictures shown in Figure 5.11 the BST grain size of the samples with Pt and SRO bottom electrodes are around 50 nm and 150 nm in diameter, respectively. Although we can not exclude that SRO introduces additional leakage mechanisms, the increased leakage currents for the polycrystalline BST/SRO/SiO_2/Si samples would also be consistent with the increased grain size [Figure 5.11(a) and (b)].

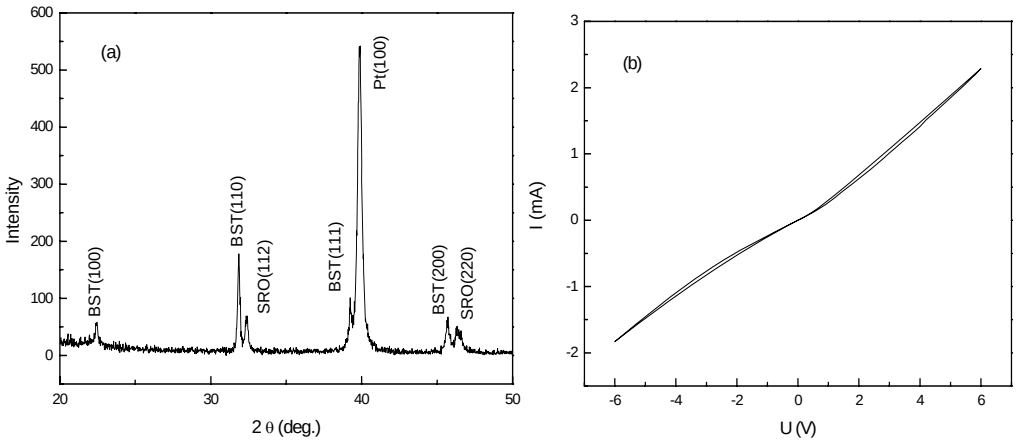


FIG.. 5.10 (a) X-ray diffraction measurement of BST film grown on SRO/Si. (b) The I-V curve of Pt/BST/SRO/Si structure.

In order to investigate the role of grain boundaries in our specific case, we investigated a polycrystalline BST thin film by conductive-AFM. Since the BST films on Pt bottom electrodes are too insulating to be characterized by this method, we investigated a polycrystalline BST thin film on SRO/SiO_2/Si. Figure 5.12 depicts the LC-AFM scan of

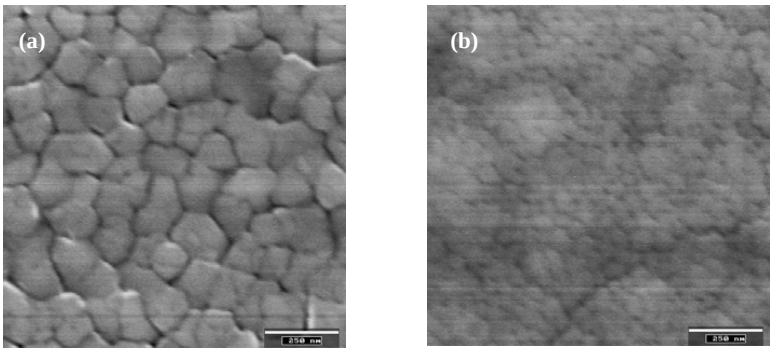


FIG. 5.11 SEM image of (a) Pt/BST/SRO/Si structure and (b) Pt/BST/Pt/Ti/SiO_2/Si structure. The BST film was deposited at 700°C by pulsed laser deposition (PLD), and the oxygen pressure was kept at 0.25 mbar during the deposition.

this sample superimposed to the corresponding topography scan, where the grains are clearly visible. It clearly shows that the grain boundaries are more conductive than the grain interior. This is consistent with the reports about acceptor doped ceramic samples which reveal a n-conduction along grain-boundaries due to an inversion layer in the center of the space charge depletion regions.[107] These conducting grain boundaries in our BST thin film samples may provide percolating current channels during the observed switching processes. The same result was obtained by Son et al. using a Hg drop top electrode to switch a NiO film. [108] After switching into the ON and OFF state, respectively, they removed the Hg drop and investigated the surface by C-AFM. In this experiment obviously the density of the conducting filaments change drastically between the ON and OFF state. It is interesting to note that the filaments in the OFF state (and partially also in the ON state) are mainly located at the grain boundaries of the NiO film.

The crucial role of grain boundaries in terms of unipolar switching was already demonstrated by Park *et al.*[102] They showed that unipolar switching in epitaxial NiO thin films is much less stable than in polycrystalline NiO and attributed it to the reduced

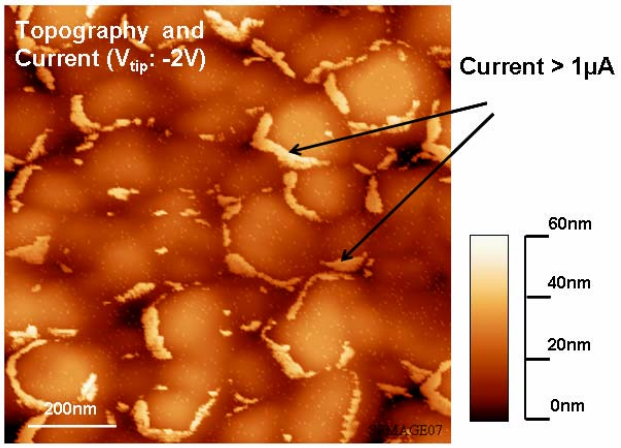


FIG 5.12 The merged topography and current image of polycrystalline BST thin film on SRO/SiO_2/Si measured by conductive-AFM.

oxygen migration energy at the grain boundaries. On the other hand it has been shown that the heat dissipation plays a crucial role in terms of the stability of unipolar switching. Chang *et al.* [109] have investigated the bottom electrode dependence in terms of the thermal stability of conducting filamentary paths, which are closely related to heat dissipation through the bottom electrode. They found that the unipolar resistive switching phenomena become unstable and turn into threshold switching when bottom electrode makes dissipation of Joule heat less efficient. This result indicates that thermal heat dissipation through the electrodes is crucial for RRAM, the same as for phase change random access memory. [110]

In analogy, the difference in the local heat dissipation in single crystalline samples might also be the reason for the lack of unipolar switching in epitaxial BST thin films. A possible explanation could be that the cross transport of heat might be more pronounced in single crystalline samples than in polycrystalline samples with highly insulating grains. For MgO, it has been clearly shown, that single crystalline samples have a larger thermal

conductivity than polycrystalline samples and that the thermal conductivity increases with the grain size.[111] As a result, the local self-heating might be inhibited for single crystalline samples as well as for the BST/SRO/SiO_2/Si samples with increased grain size and will prevent the thermal formation and dissolution of the Ti^{3+} within the conducting filaments. However, detailed calculations of the heat dissipation in polycrystalline samples and single crystalline samples would be necessary to confirm this assumption.

5.4 Transition between bipolar and unipolar resistive switching

The unipolar and bipolar resistive switching behavior has been observed in simple binary metal oxide and we have also found both switching types in perovskite $(Ba_{0.7}Sr_{0.3})TiO_3$ films. The BST based RRAM devices show conductance evolution from insulating to metallic, up to the compliance current controlled in forming process, and the bipolar/unipolar switching were observed in sequence in one cell. However, the former experience and experimental observation is that once the device switches in unipolar switching mode, it will not show bipolar switching any more. [41] The larger R_{off}/R_{on} of unipolar switching makes it much easier to read the memory state and can be potentially integrated in higher density, while generally the bipolar switching has better endurance. The pros and cons of both switching type gives assumption that if we could alternate the bipolar/unipolar switching freely in one cell and it will definitely provide more possibilities for complex logic circuits and other applications.

As discussed before, the as-prepared Pt/BST/Pt devices were highly insulating and a forming process is necessary to trigger the device from the initial highly insulating state to a more conductive state as sketched in Fig. 5.13 (a). After the first forming, the Pt/BST/Pt device shows bipolar switching behavior as illustrated in Fig. 5.13 (b).

If the current compliance is increased to 20mA, the device will show a more conducting, linear behavior resistance state, together with another forming at positive branch. As a

result, we obtain the LRS in unipolar resistive switching mode [Fig. 5.13 (c)]. Afterwards, we could obtain the unipolar switching and the device resistance can be switched between LRS and HRS by the same positive or negative voltages.

It should be noted that there are two kinds of unipolar switching observed depending on the shape of HRS (Set process). The resistance of HRS in Fig. 5.13 (c) is increased gradually with the increased voltage and ended with a small abrupt "breakdown". However, Fig. 5.13 (d) shows another behavior, in which resistance of HRS maintains unchanged until "breakdown" occurs, and the device was directly switched to LRS.

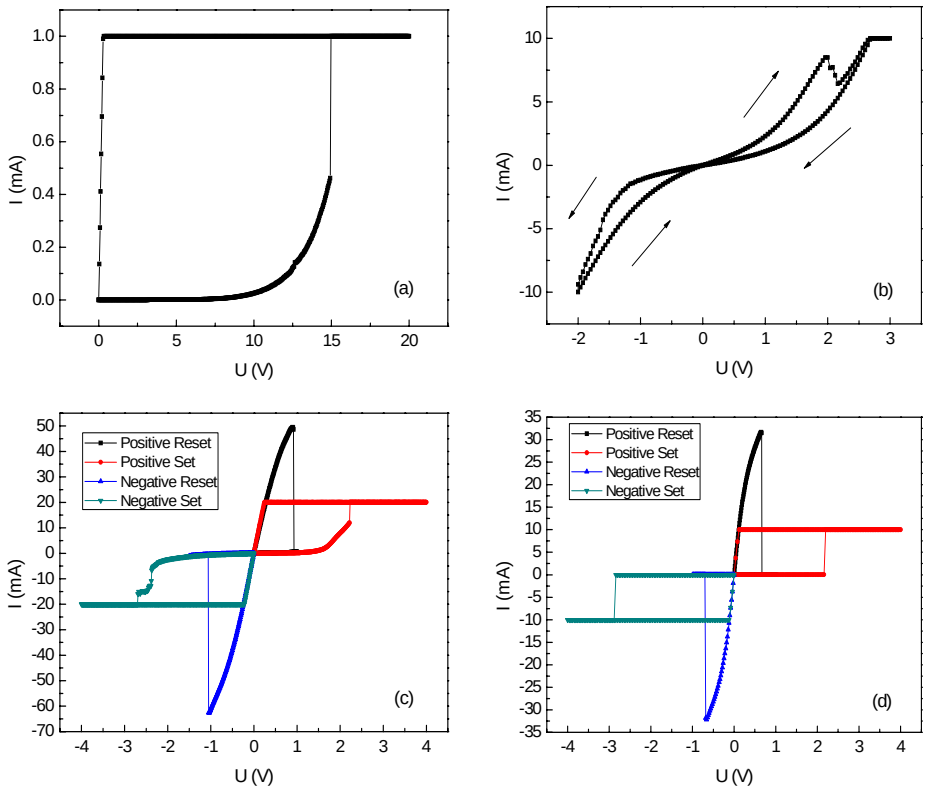


FIG. 5.13 Resistive switching behavior of Pt/BST/Pt devices. (a) Forming process. (b) Bipolar switching behavior. (c) Unipolar switching behavior with an gradually increased HRS and (d) Unipolar switching behavior with an more stable HRS.

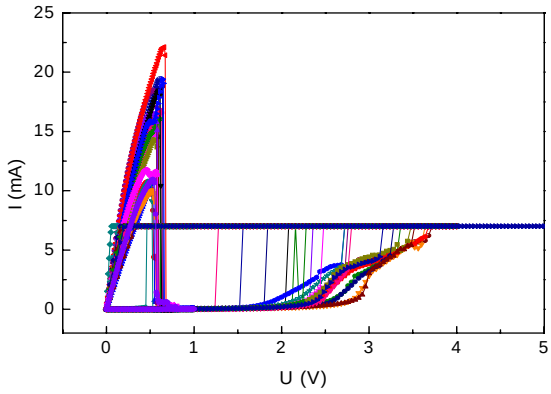


FIG. 5.14 A Pt/BST/Pt device switched for 20 cycles in unipolar switching mode. The different Set processes happened during the endurance measurement. The gradual or abrupt increase of resistance in Set took place randomly, indicates the instability of HRS.

Fig. 5.14 displays a Pt/BST/Pt device switched for 20 cycles in unipolar switching mode. It is clear that the different Set processes happened during the endurance measurement. The gradual or abrupt decrease of resistance in Set took place randomly, indicates the instability of HRS.

The unipolar/bipolar alternation is illustrated in Fig. 5.15 (a)-(d). The resistance of HRS decreased gradually in Fig. 5.15 (a) and finally the device was switched to LRS at about 4V, then the Reset occurs when voltage was swept to 2V without the current compliance, and both processes composed a typical unipolar switching behavior. From Fig. 5.15 (a) we define the ~4V as the threshold voltage, at which the device can be switched from HRS to metallic LRS.

While sweeping the voltage again to 2V, which is smaller than the threshold voltage of ~4V, the device was not switched to a metallic LRS of unipolar switching, but to an even higher HRS, as shown in Fig. 5.15 (b). As a result, the HRS in unipolar switching works as the LRS in bipolar switching mode and the “abrupt current increase” was avoided. At the negative branch, the device was switched from HRS to LRS, and the I-V curve at both

positive and negative branch exhibited a typical bipolar switching behavior. Therefore, we could convert the unipolar switching to bipolar switching by control the voltage, which should be smaller than the threshold voltage to avoid the abrupt current increase.

Moreover, as shown in Fig. 5.15 (c), if we increase the voltage to 6V which is larger than the threshold voltage, the abrupt current increase occurs and the resistance of LRS in bipolar switching was decreased further to leaner metallic LRS, and then the unipolar switching was obtained. Thus the LRS in bipolar switching works as the HRS in unipolar

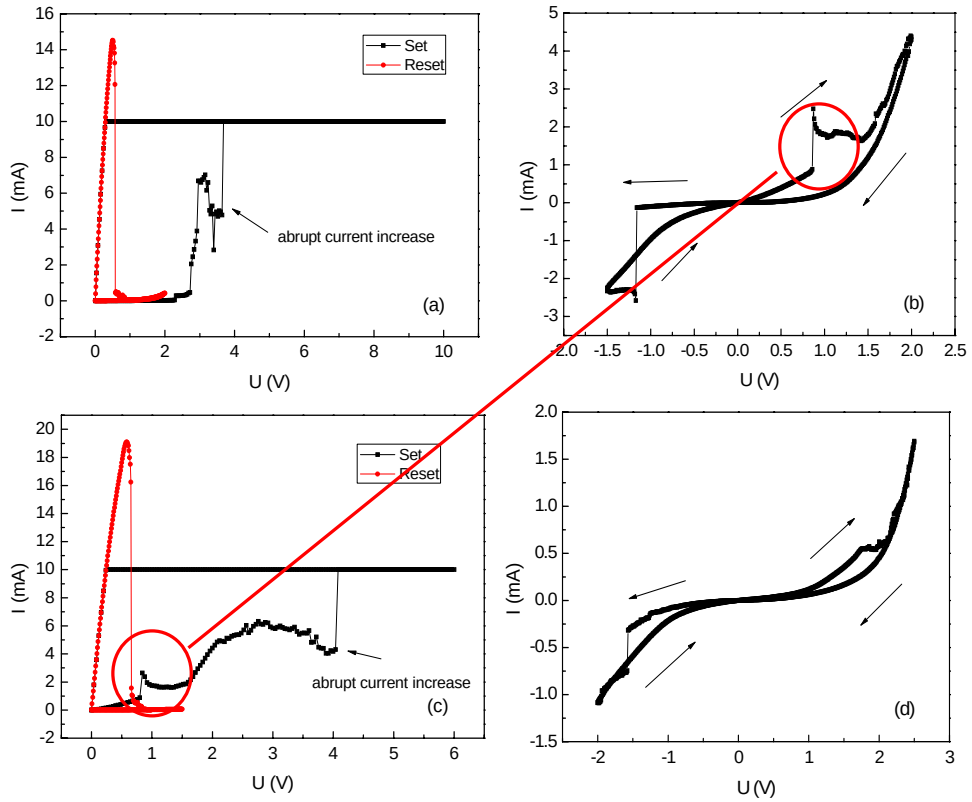


FIG. 5.15 The unipolar/bipolar switching alternation by control of switching voltage. (a) Unipolar switching behavior when switching voltage is higher than threshold voltage ~4V. (b) Bipolar switching behavior when switching voltage is lower than threshold voltage. (c)-(d) Dynamically repeated unipolar/bipolar switching.

switching mode. Moreover, when decrease the voltage lower than threshold voltage, the unipolar switching can be converted to bipolar switching again [Fig. 5.15 (d)]. We have observed the bipolar/unipolar alternation with I-V curves similar to Fig. 5.13 (c) which have gradually increased resistance of HRS, and I-V curves as shown in Fig. 13 (d) in which resistance of HRS maintains unchanged until “abrupt current increase” occurs can not alternate the switching mode.

Consequently, we could obtain either bipolar switching or unipolar switching by controlling the switching voltage. When the applied voltage was higher than the threshold voltage, the soft breakdown occurs and the device exhibit unipolar switching behavior. If the voltage is lower than the threshold voltage, the soft breakdown will be avoided and in this case the device shows bipolar switching mode. The bipolar to unipolar or unipolar to bipolar transition is dynamically repeatable, and it gives engineers more freedom and possibilities to design more complex logic circuits.

The bipolar/unipolar alternation based on a simplified single filament model is illustrated in Fig. 5.16. The mechanism of unipolar switching is related to formation or rupturing the

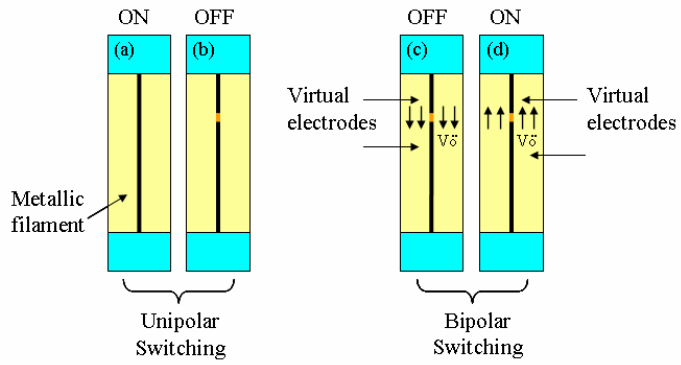


FIG. 5.16 A simplified single filament model for unipolar/bipolar switching alternation. (a) The Pt/BST/Pt device shows unipolar ON when metallic filament is formed and (b) device shows unipolar OFF when metallic filament is broken due to localized Joule heating effect. (c)-(d) The device shows bipolar switching when switching voltage is lower than threshold voltage. Oxygen vacancies could migrate through the trace of broken filament and the conductance of the device was locally modified.

metallic filament with the contribution of Joule heating. [28, 32] In our previous study we have found that the LRS in unipolar switching is metallic conduction, while in HRS the conduction behavior is thermally activated charge carrier transport. During forming process, oxygen deficient regions may form metallic conductive paths in thin film [98, 112] and the device is switched to LRS of unipolar switching mode [Fig. 5.16 (a)]. In Reset process, the sudden resistance increase indicates the rupture of filaments which probably results from the Joule heating effect induced by large external current. [99] The local temperature of the filament can reach 700–800 K by the localized Joule heating effect [92] and the filament may fuse under such high temperature [Fig. 5.16 (b)].

As forming is an irreversible process, the formed device will obtain permanent change in local composition or morphology compared to fresh samples.[98] Thus once the Reset occurs, the trace of the fused or broken filament may still provide fast diffusion channels for oxygen vacancies compared to the highly insulating bulk material, and the oxygen vacancy movement may locally modify the conductance of the fused filament. In such occasion if a positive bias lower than the threshold voltage was applied on the top electrode, the oxygen vacancies could migrate through the fused filament and the device is switched to an even higher HRS [Fig. 5.16 (c)]. When a negative bias is applied, the oxygen vacancies can be pulled back and the LRS is obtained [Fig. 5.16 (d)]. Furthermore, if a positive bias higher than the threshold voltage was applied the devices will show unipolar switching again, probably due to the recover of the broken filament or, new filament was formed from the multi-filament point of view. In addition, there is no absolute HRS or LRS. The HRS or LRS are always defined upon the counter resistance state, and as we have discussed above, the HRS in unipolar switching works as LRS in bipolar switching.

Although we attribute the direct bipolar switching to the redox-reaction at the interface in Chapter 4, the rupture of the filaments in unipolar switching may occur anywhere between top and bottom electrode. Thus the location of the bipolar switching shown in Fig. 5.16(d) depends on the virtual electrodes, not exactly at the interface.

Chapter 6

Conclusions

Summary

The resistive switching behavior of BST thin films with different crystalline properties was investigated within this dissertation. The epitaxial BST thin films were deposited on SRO/STO substrate and polycrystalline BST thin film on Pt/Ti/SiO_2/Si substrate.

The laser fluence dependence was checked intend to optimize the RRAM properties. By introducing the optic filter within the optical path in PLD system the laser energy density was controlled. Although the film epitaxial quality was improved by reducing the laser energy during deposition process, the yields fluctuated and only 3% RRAM devices with highest epitaxial quality of BST film shows resistive switching behavior. It gives a clue that the best thin film quality does not result in the best switching performance, and it is a clear evidence of the importance of the defects to obtain resistive switching phenomena.

The bipolar resistive switching behavior was studied with epitaxial BST thin film on SRO/STO. Compared to Pt top electrode, the yield, endurance and reliability were strongly improved for the samples with W top electrode. Whereas the samples with Pt top electrode show a fast drop of the resistance for both high and low resistance states, the devices with W top electrode can be switched for 10^4 times without any obvious degradation. The resistance degradation for devices with Pt top electrode may come from the diffusion of oxygen along the Pt grain boundaries during cycling whereas for W top electrode the reversible oxidation and reduction of a WO_x layer existed at the interface between W top electrode and BST film attributes to the improved switching property.

By artificially controlled the voltage amplitude and current compliance in current-voltage characteristics and pulse height/width in pulse measurement, we could improve device endurance, optimize the switching memory window and obtain higher R_{off}/R_{on} by simply employing asymmetric voltage/current. The multilevel switching also reveals the potential of RRAM to store more bit in one cell.

The transition from bipolar to unipolar resistive switching in polycrystalline BST thin films was observed. Whereas epitaxially grown BST thin films exhibit solely bipolar switching, polycrystalline samples with Pt bottom electrode can be transformed to unipolar switching mode at high current compliance. A forming process which induces a metallic low resistance state is prerequisite for the observation of unipolar switching behavior. The absence of unipolar switching in single crystalline samples may relate to space charge depletion layers at grain boundaries and their impact on the electronic conduction properties as well as the different local heat transfer in thin films.

By control the switching voltage, the bipolar and unipolar resistive switching can be alternated in polycrystalline BST thin films. When the switching voltage is higher than threshold voltage, the device exhibits unipolar switching while if the switching voltage is lower than threshold voltage, the device shows bipolar switching behavior. The bipolar/unipolar alternation is dynamically repeatable and the alternation may relate to the local modification of broken filaments by breakdown or oxygen vacancy movement.

Outlook

For device applications the RRAM still has a long way to go. The physics behind the switching phenomena needs further investigation to make it clear. As illustrated in this dissertation, the oxygen plays a key role in resistance variation. Thus future works may focus on the role of defects by defects engineering, such as oxygen vacancy distribution in thin films and their movement in electrical field.

Although the endurance has been greatly improved by employing W top electrode, it is still far away for RRAM to challenge the present Flash technology. To understand the role of interface between electrodes and dielectric film, the interface engineering may be introduced. The oxide interface has significant influence on the device reliability. We have shown that the 1nm-thick WO_x layer at the W/BST interface in Chapter 4. However, the oxide layer thickness may strongly relate to the endurance as the oxide layer stores and releases oxygen during switching. This would be a promising aspect for future work in this issue.

The bipolar-unipolar switching transition gives a clue to elucidate the role of filaments. The step-by-step forming process induces the bipolar to unipolar switching transition and obviously the property of filament also evolutes. The Conductive AFM provides a good chance to distinguish the conductive channels under the metal electrode, once we could remove it smoothly. Meanwhile, the bipolar-unipolar switching transition may have more potential applications in device engineering because it provides another choice beyond the solely bipolar or unipolar switching mode.

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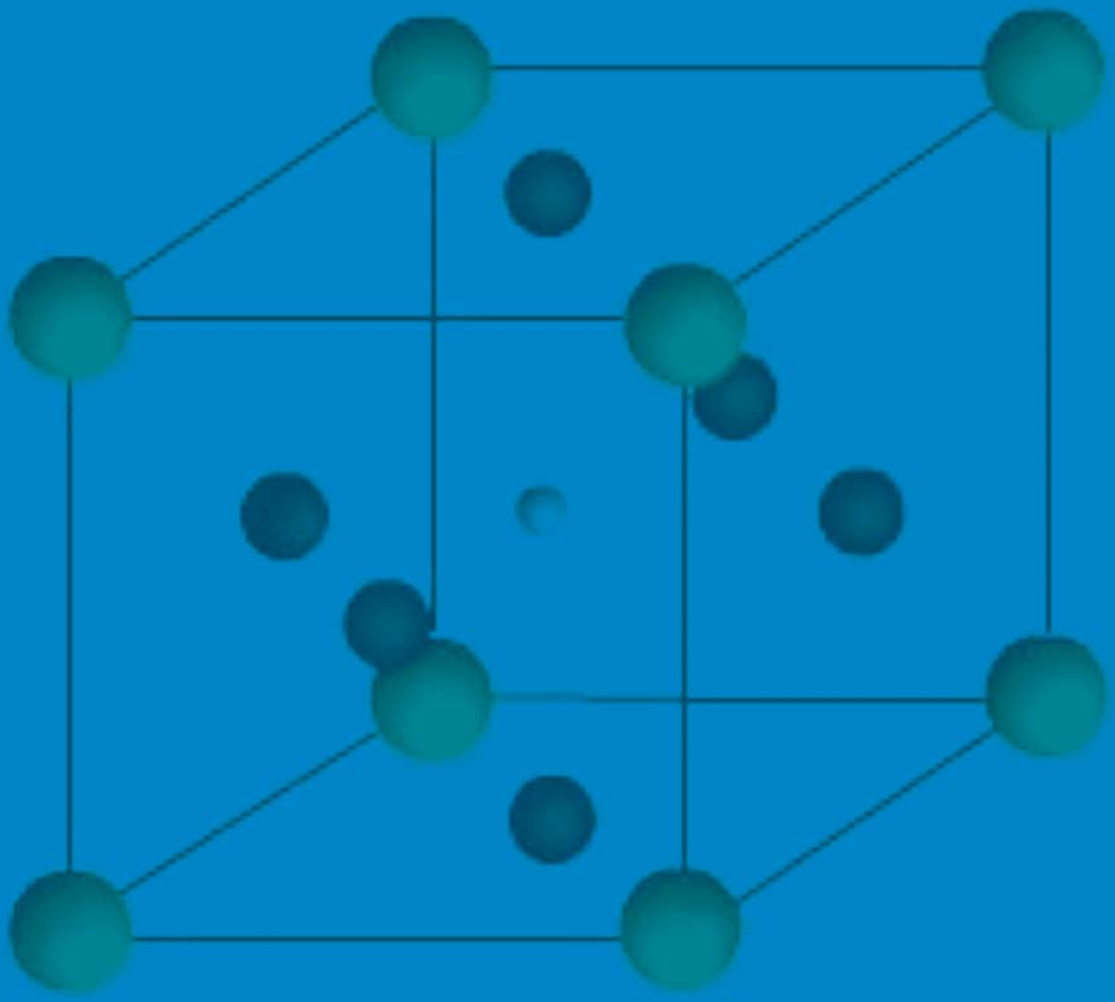

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