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Rate limiting step for the switching kinetics in Cu doped $Ge_{0.3}Se_{0.7}$ based memory devices with symmetrical and asymmetrical electrodes

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We report on the comparison of the resistance switching properties and kinetic behavior of Cu doped $Ge_{0.3}Se_{0.7}$ solid electrolyte based dual layer memory devices integrated with asymmetrical (Pt and Cu) and symmetrical electrodes (only Cu). In spite of the fact that the observed resistance switching properties and its parameters are quite similar for both memory devices, the dependence of the SET-voltage on the voltage sweep rate suggests different microscopic rate limiting factors for the resistance switching behavior. Additionally, in order to alleviate the cross talk problem in passive crossbar arrays, a dual layer oxide stack (TiO_2/Al_2O_3) is integrated with $Ge_{0.3}Se_{0.7}$ based dual layer memory devices to achieve a specific degree of non-linearity in the overall resistance of the low resistance state. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4797488]

I. INTRODUCTION

In the last decade, the resistance switching based memory device concept, commonly known as resistance random access memory (RRAM), has evoked great interest within the scientific community as a potential candidate for non-volatile random access memories, passive crossbar arrays, and neuromorphic computational architectures.[1–9] A lot of promising results have already been reported on single structure resistive switching memory cells integrating a large variety of oxides and solid electrolytes.[10] Some of the most attractive properties of resistance switching memory devices are low power consumption, low threshold voltages, scalability into the nanometer regime, fast write and read access, and low fabrication costs.[10] Thin oxide films such as SiO_2,[11] TiO_2[12] as well as solid electrolyte materials such as Ag and Cu doped amorphous Ge-Se,[13,14] Ge-S,[15] and (Zn, Cd)S[16] are some of the most promising candidates in the race for future RRAM cells. The macroscopic origin of the resistance switching "ON" process in the solid electrolyte material systems, when sandwiched between an electrochemically active metal, such as Ag or Cu, and an electrochemically inert counter electrode, such as Pt or Au, is proposed to be an electrochemical formation of metallic filaments.[10] Under an applied positive bias at the oxidizable electrode (e.g., Cu or Ag), the filament formation process ("SET" process) in the memory cell is supposed to consist of three steps: (1) anodic dissolution of Cu or Ag according to $M \rightarrow M^{z+} + ze^-$, where M^{z+} represents the Cu or Ag metal cations in the thin electrolyte film, (2) drift of the metal cations in the electrolytes under the action of the high electric field, (3) cathodic reaction at the inert electrode, $M^{z+} + ze^- \rightarrow M$, involving the nucleation and growth processes of the metallic filament.[10] Despite recent progress, there remain some open questions and challenges with respect to, for example, the rate limiting step in the resistance switching process, the role of the inert electrodes and existing crosstalk problem in crossbar arrays, which needed to be addressed before the industrial qualification of these devices.

In this article, we report on the resistance switching properties of Cu doped $Ge_{0.3}Se_{0.7}$ solid electrolyte based memory devices integrated with an oxidizable Cu electrode only on the top side (bottom side is an inert Pt electrode) as well as on both sides (top and bottom). Further, the kinetics of the resistance switching process in both types of memory cells are investigated within the framework of the metallic filament growth model. Moreover, we show that by integrating an additional dual layer oxide barrier element with Cu doped $Ge_{0.3}Se_{0.7}$ based memory devices, it is feasible to introduce a specific degree of non-linearity in the low resistance state.

II. EXPERIMENTAL

Single cross-point and planar structures with active areas ranging from 2 μm^2 up to 1600 μm^2 were fabricated using standard photolithography techniques and ion beam etching. The detailed layer sequence of the memory devices as used in this study was the following: Si/SiO_2 substrate/5 nm TiO_2/30 nm Pt or Cu (bottom electrode)/2 nm SiO_x ("with expected pin holes")/$Ge_{0.3}Se_{0.7}$/100 nm Cu (top electrode).

Si (100) wafers with a 400 nm thermal oxide and a 5 nm TiO_2 film as an adhesion layer for the Pt base electrode deposition were used as substrates. A 30 nm thin film of Pt (Cu) was sputtered on top and this bottom Pt (Cu) electrode was patterned by standard optical lithography and by reactive ion beam etching (RIBE). The photo-resist was removed with acetone and a buffer layer of 2 nm SiO_x was deposited by radio frequency (RF) sputtering at a rate of 0.8 nm s^{-1} followed by defining the bottom electrode contact with optical lithography and RIBE. Afterwards, the top structure of the memory cell was defined by a lift-off step. The $Ge_{0.3}Se_{0.7}$ layers were deposited by RF-sputtering followed by the deposition of the 150 nm Cu top electrode. The deposition rates

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for the $Ge_{0.3}Se_{0.7}$ and Cu layers were around 0.2 and 0.5 nm s^{-1}, respectively. Finally, a lift-off in acetone was used to finalize the device structure. All electrical measurements were done using an Agilent B1500 semiconductor parameter analyzer.

The very thin SiO_x buffer layer "with expected pinholes (or weak links)" was introduced between the Cu-Ge-Se layer and the Pt (Cu) bottom electrode to improve the switching characteristics such as endurance and retention. As shown in Ref. 14, introducing a 2 nm SiO_x buffer layer does not affect the switching voltage which indicates the film has pin holes (or weak links). As a test of the robustness of the thin SiO_x layer, we measured the current-voltage characteristics of Pt/SiO_x (2 nm)/Cu cells. The devices were found short which further indicates the thin SiO_x buffer layer having pin holes (or weak links). We believe that a 2 nm SiO_x film "with expected pin holes" basically controls the overgrowth of the filament during repeated switching cycles and, hence, improves the resistive switching characteristics.

III. RESULTS AND DISCUSSION

Figure 1(a) shows the current-voltage (*I-V*) and corresponding resistance-voltage (*R-V*) characteristics of a memory cell, Pt/SiO_x/$Ge_{0.3}Se_{0.7}$/Cu, measured at room temperature. A quasi-static voltage sweep with bias on the top Cu electrode and grounded bottom electrode was applied to the memory cell, starting from 0 V to 0.5 V, then from 0.5 V to −0.2 V and back to 0 V again, at a sweep rate of 0.05 V/s. A current compliance of 100 μA was set during the run to avoid complete breakdown of the memory cell. The typical R_{off}/R_{on} ratio (R_{off} and R_{on} correspond to the resistances of the high and low resistance states, respectively) of these memory cells written with a programming current of 100 μA was found to be in the range of 10^4–10^5. One of the major reliability issues for RRAM and logic devices is data retention which is defined as the ability of a memory cell to retain stored data between the time for writing and subsequent reading of the stored information. The retention behavior of both the high and low resistance states was measured at a temperature of 120 °C with 50 mV of constant applied voltage to the memory cell. As shown in Figure 1(b), there is no degradation of the resistance states up to approximately 10^4 s waiting time. Further details on the memory device properties such as endurance, nanoampere switching, reliability and random telegraph noise, etc., can be found in Refs. 14, 17, and 18.

As shown by Schindler *et al.*,[19] one can get information on the kinetics of the "SET" process by potentio-dynamic *I-V* measurements at different voltage sweep rates. It is proposed that the switching voltage, V_{SET}, depends on the voltage sweep rate ϑ as follows:

$$V_{SET} = \frac{k_B T}{\alpha z e} \ln \vartheta + \frac{kT}{\alpha z e} \ln \frac{Q_{SET} \alpha z e}{i_0 \pi r_f^2 k_B T}, \quad (1)$$

where i_0 is the exchange current density, α is the cathodic charge transfer coefficient, k_B is the Boltzmann constant, e is the elementary charge, and T is the temperature. Q_{SET} is the charge needed for the one-dimensional growth of a Cu filament and πr_f^2 corresponds to the tip area of the growing filament with radius r_f. Therefore, we investigated the V_{SET} dependence on the voltage sweep rate during quasi static *I-V* measurements. Figure 1(c) shows the observed dependence of V_{SET} for medium up to high voltage sweep rates, measured on Pt/SiO_x/$Ge_{0.3}Se_{0.7}$/Cu based memory devices. A clear exponential relationship between the switching voltage and the voltage sweep rate is observed at high sweep rates. There seems to be a threshold voltage for low voltage sweep rates probably originating from a nucleation overpotential. Further, according to Eq. (1), one expects a logarithmic dependence of the switching voltage V_{SET} on the solid electrolyte film thickness.[19] As for thicker films longer filaments

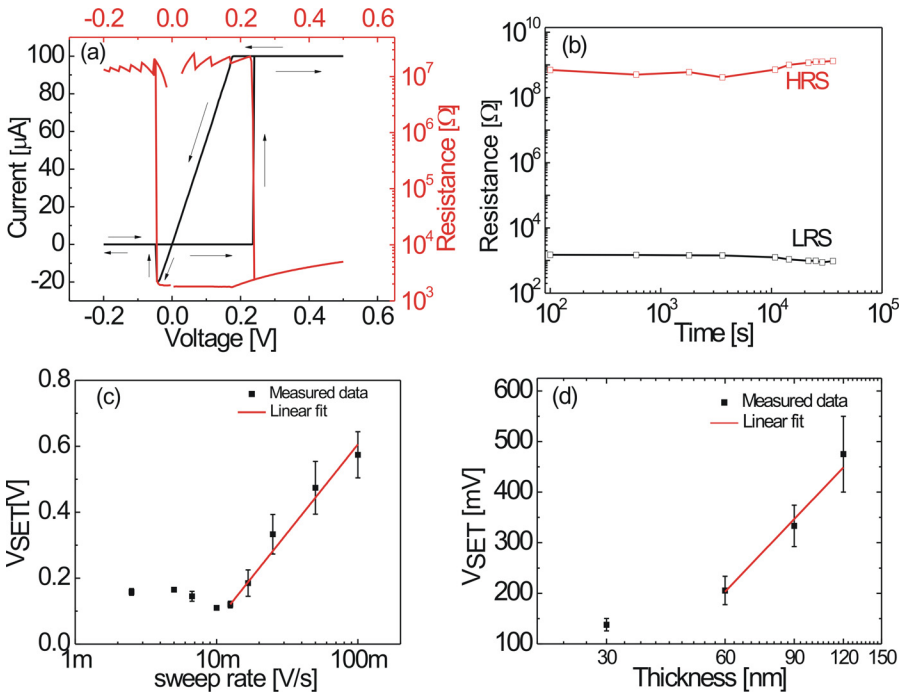

FIG. 1. Pt/SiO_x/$Ge_{0.3}Se_{0.7}$/Cu: (a) Typical *I-V* (*R-V*) characteristics of a memory cell measured at room temperature with a 100 μA compliance current setting. (b) Retention of the resistance states measured at 120 °C. The cell was written with 100 μA programming current and read at 50 mV. (c) Dependence of the SET-voltage V_{SET} on the voltage sweep rate measured at room temperature. (d) Dependence of V_{SET} on the $Ge_{0.3}Se_{0.7}$ film thickness at a sweep rate of 0.05 V/s measured at room temperature.

have to grow, it requires more Cu atoms, and, hence, more charge Q_{SET} has to be supplied. The dependence of the switching voltage V_{SET} on the $Ge_{0.3}Se_{0.7}$ film thickness was investigated quasi-statically with a sweep rate of 0.05 V/s at room temperature. As expected, a logarithmic dependence was observed for $Ge_{0.3}Se_{0.7}$ films with thicknesses ranging from 60 nm to 120 nm (see Fig. 1(d)).

In order to understand the importance of an inert counter electrode in the resistance switching process, we investigated devices with oxidizable Cu as top and bottom electrodes. Before going further, it is important to point out that, even at room temperature, Cu dissolves easily in amorphous germanium chalcogenide films of micrometer thickness.[20] Therefore, it is not possible to realize a pure thin $Ge_{0.3}Se_{0.7}$ film integrated non-volatile memory device with symmetrical active Cu electrodes. However, in case of dual layer memory devices, the SiO_x buffer layer "with expected pin holes" (or weak links) limits the Cu dissolution in amorphous germanium chalcogenide films in abundance and, hence, makes it feasible to use symmetrical active Cu electrodes.[21] Figure 2(a) shows a typical current-voltage and corresponding resistance-voltage characteristics of a dual layer memory device, Cu(bottom electrode)/SiO_x/$Ge_{0.3}Se_{0.7}$/Cu(top electrode), with bias applied on the top Cu electrode and grounded bottom electrode. The typical R_{off}/R_{on} ratios $\sim 10^3$–10^4 of memory devices with symmetrical oxidizable Cu electrodes were found to be comparable with those of devices with asymmetrical electrodes. Essential characterizations for RRAM non-volatile memories such as endurance, retention, and multilevel switching were performed at room temperature on these memory devices. Initial measurements have shown a promising endurance behavior of 500 cycles with a retention of 10^3 – 10^4 s for both resistance states and the possibility of multibit data storage due to dependence of the low resistance state on writing current (see supplementary material S1).[29] The observed similarities in resistance switching characteristics for both types of memory devices imply that it is not essential to have an inert counter electrode in electrochemical metallization cells.

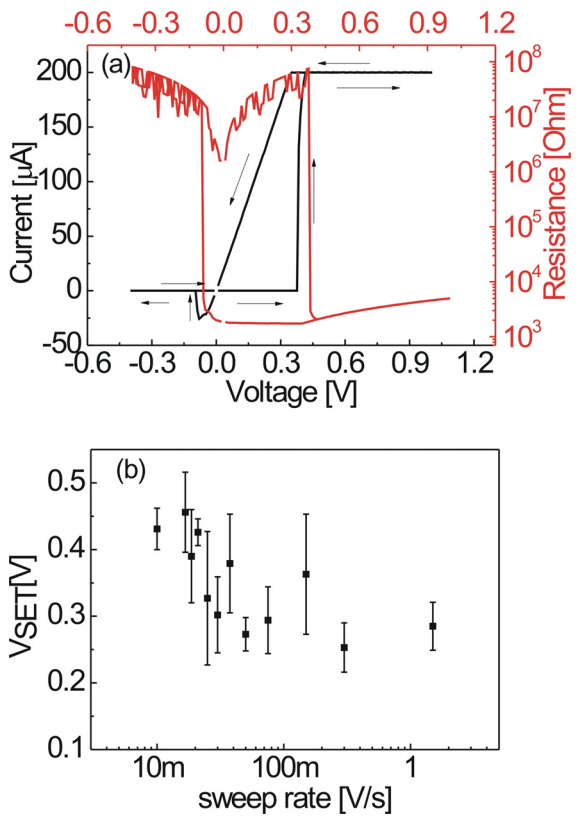

FIG. 2. Cu/SiO_x/$Ge_{0.3}Se_{0.7}$/Cu: (a) Typical *I-V* (*R-V*) characteristics of a memory cell measured at room temperature with a 100 μA compliance current setting. (b) Dependence of the SET-voltage V_{SET} on the voltage sweep rate measured at room temperature.

Further, we investigated the V_{SET} dependence on the voltage sweep rate to understand the rate limiting step in the resistance switching process for memory devices with symmetrical oxidizable Cu electrodes. Figure 2(b) shows the observed results which were obtained at room temperature. The dependence of V_{SET} on the voltage sweep rate is completely different from that found for devices with asymmetrical electrodes. We believe that nucleation as the rate limiting step, not the filament growth, might qualitatively explain the behavior found in these resistance switching devices for the measured voltage sweep range. Further studies on the breakdown behavior of such devices under constant bias for different time ranges could shed more light on the rate limiting step in the switching process of these devices.[21]

One possible application for the above resistance switching devices would be their integration into passive crossbar-array based architectures, which are ideal building blocks for configurable logic circuits.[10] In spite of the simple geometrical structure and ultimate scaling potential, the use of this array based architectures has largely been blocked by the existing crosstalk problem, i.e., misreading a designated cell within a passive crossbar array due to interferences from sneak-path currents through neighbouring cells with low resistance states. As suggested before, the integration of a serial element with a particular non-linearity to each cell would solve the crosstalk problem.[10] For unipolar resistance switching based memory cells, this could be a rectifying diode such as a p-n junction.[22] However, it is not feasible to use a conventional diode for bipolar resistance switching based memory cells because the diode also prevents reverse current into the cell which is important for the bipolar switching process.[23] Hence, in the case of bipolar-type memory cells, more complicated varistor type-elements with specific degrees of non-linearity (high current density and threshold voltage) are required at both polarities.[23] Recently, different concepts such as complementary resistance switches,[24,25] inherent rectifying resistance switching elements,[26] and Schottky interface based selection devices[27] have also been investigated to solve crosstalk problem for bipolar resistance switching based crossbar arrays.

We investigated the feasibility to introduce a specific degree of non-linearity in the resistance of the low resistance state of memory cells via combining an additional dual layer oxide barrier element with Cu doped $Ge_{0.3}Se_{0.7}$ based memory devices. The dual layered oxide barrier Pt (30 nm)/ TiO_2 (5–6 nm) /AlO_2 (2 nm)/Pt (30 nm) was fabricated on a Si/SiO_2 substrate to introduce different non-linearities for

different polarities. At first, a 5–6 nm blanket TiO_2 thin film was deposited on a platinized Si substrate by reactive sputtering using a gas mixture of 77% Ar and 23% O_2. Afterwards, a thin film of ~ 2 nm Al was sputtered on top of the TiO_2 film. The Al film was exposed in situ to an atmosphere of 5 mbar O_2 and UV light at room temperature to prepare a thin Al_2O_3 barrier.[28] Then, a 30 nm blanket Pt electrode was sputtered on top of the Al_2O_3 film. Finally, the $Ge_{0.3}Se_{0.7}$ based memory devices were fabricated on this dual layer oxide barrier stack. Figure 3 shows the resistance switching properties of $Ge_{0.3}Se_{0.7}$ based memory devices integrated with a dual layered oxide barrier. As it can be seen, it was possible to achieve a specific degree of non-linearity for the low resistance state of the combined cell. The observed R_{off}/R_{on} ratio of these devices was found to be around 10 at 500 mV, which is still reasonable to allow for small and highly efficient sense amplifiers.[10] The non-linear current-voltage characteristics of the dual layer oxide stack was measured at room temperature and is presented in the inset of Fig. 3(b). Finally, we performed the sweep endurance test on these cells and the result is shown in Fig. 3(b). The resistive switching behavior was found to be stable and reproducible for the measured 10 sweep cycles. However, in future, a detailed analysis of the transport properties is required to understand the non-linear behaviour of dual layer oxide stacks. At the end, it is important to point out that the non-linearity in the low resistance state can be further enhanced by optimizing the oxide barrier.

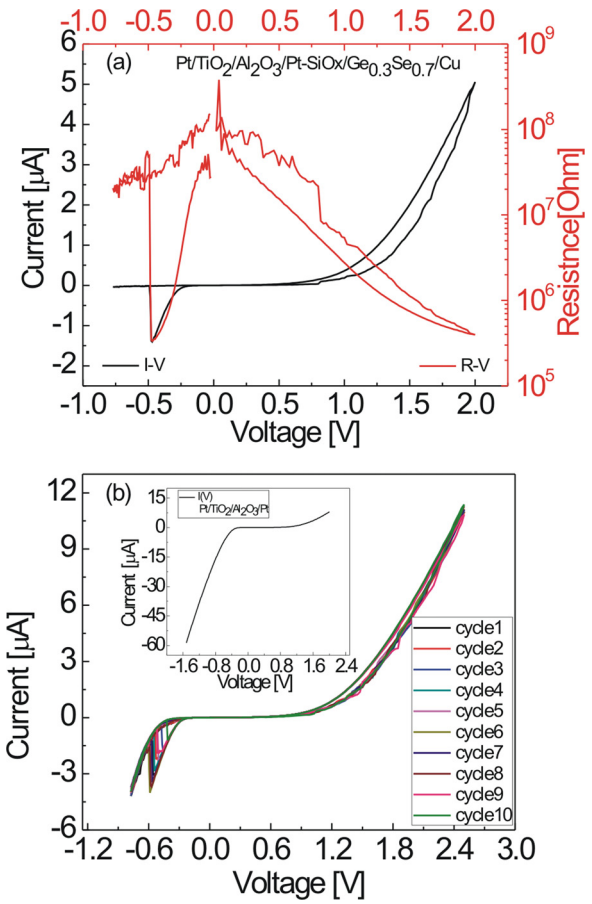

FIG. 3. Pt/TiO_2/Al2O_3/Pt (dual layer oxide stack)—/SiO_x/$Ge_{0.3}Se_{0.7}$/Cu (resistive switching stack): (a) Typical *I-V* (*R-V*) characteristics of $Ge_{0.3}Se_{0.7}$ based memory devices integrated with a dual layered oxide barrier with a non-linear low resistance state characteristic measured at room temperature. (b) Endurance behaviour of the memory device measured at room temperature. The inset shows the typical non-linear *I-V* characteristics of the dual layer oxide stack (Pt/TiO_2/Al_2O_3/Pt) measured at room temperature.

IV. CONCLUSION

In summary, the resistance switching properties and kinetic behavior of Cu doped $Ge_{0.3}Se_{0.7}$ solid electrolyte based memory devices integrated with asymmetrical (Pt and Cu) and symmetrical electrodes (only Cu) were investigated in this study. The observed similarities in resistance switching characteristics and its parameters imply that it is not essential to have inert counter electrodes in electrochemical metallization cells. However, the dependence of the SET-voltage, V_{SET}, on the voltage sweep rate suggests that different rate limiting steps are involved in the resistance switching process for both memory devices. Further, a dual layer oxide stack was used to achieve a specific degree of non-linearity in the overall resistance of the low resistance state of $Ge_{0.3}Se_{0.7}$ based memory devices.

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