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CMOS Technology for SPAD / SiPM

Results from the MiSPiA Project

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JÜLICH
FORSCHUNGSZENTRUM

OUTLINE

- Introduction
- MiSPiA CMOS FrontSPADs
  - Technology Issues
  - Thorough Characterization Results
  - Bench-Marking
- MiSPiA CMOS BackSPADs
- Conclusions

INTRODUCTION

SINGLE-PHOTON DETECTION APPLICATIONS:

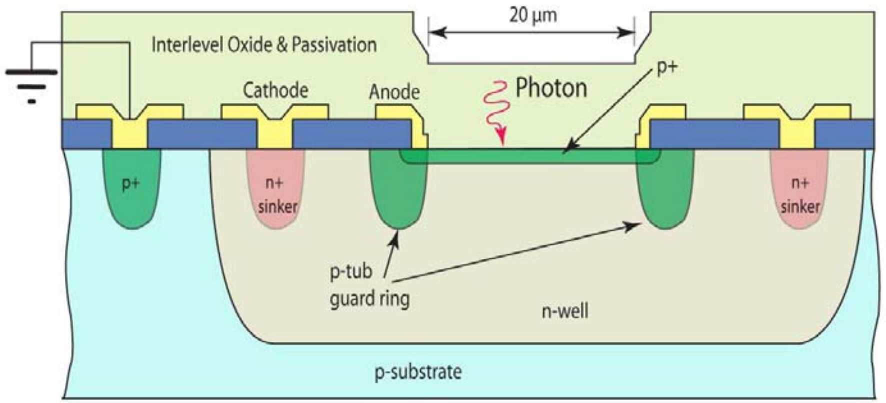
- Time-resolved spectroscopy
- Fluorescence lifetime imaging
- Positron Emission Tomography
- Time-of-Flight ranging and 3D Imaging
- …

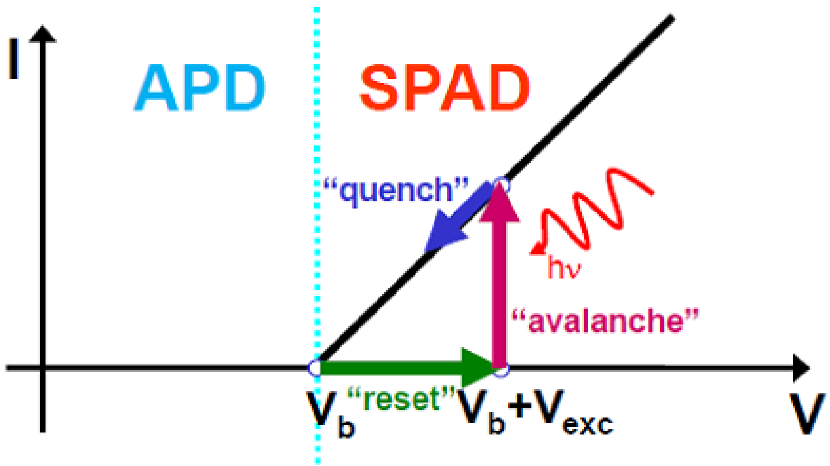
Single photon counting with picosecond time-resolution!

DEMANDING REQUIREMENTS

- High Photon Detection Efficiency
- Low Noise (low DCR, Afterpulsing)
- Picosecond Timing Resolution, low quenching times
- Low Cross-Talk

SINGLE-PHOTON AVALANCHE DIODEs (SPADs)





CMOS SPADs

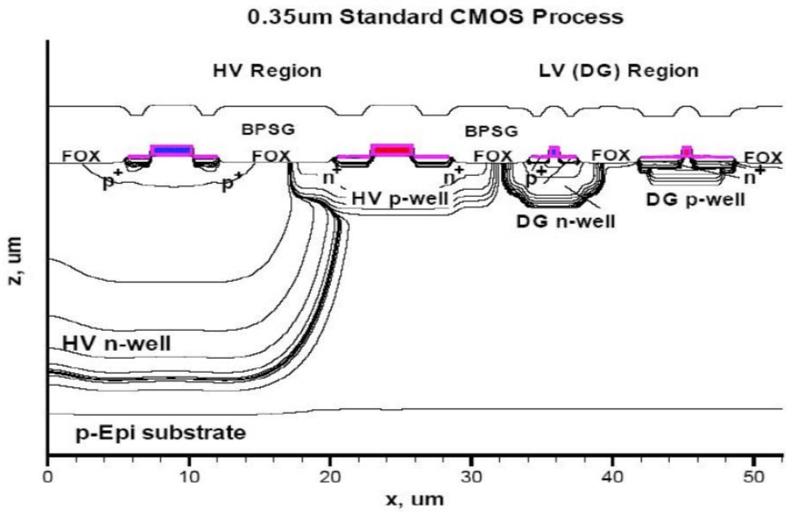
- ✓ Cost-effective
- ✓ Good yield for mass production
- ✓ Suitable for arrays
- ✓ Good spatial resolution
- ✓ Quenching circuit, signal and data processing "on-chip"
- ✓ Good t_{jitter}
- ✓ Compatible with magnetic resonance imaging

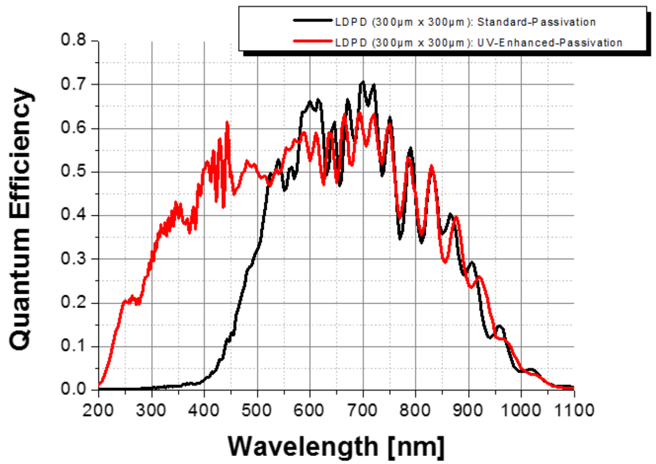
- ✘ Small Fill-Factors for acceptable spatial resolutions
- ✘ High DCR
- ✘ High After-Pulsing

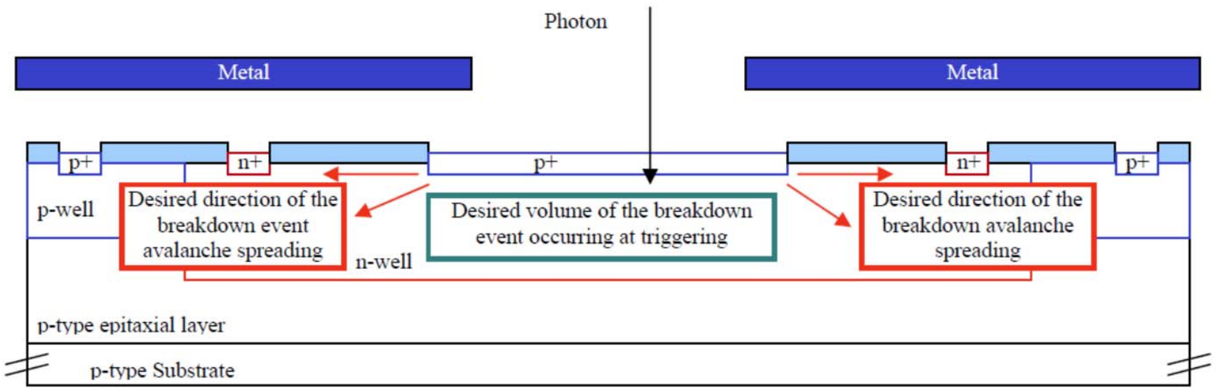
- Bias: **ABOVE** V_{BR} (breakdown voltage)
- Geiger Mode: it's a **TRIGGER** device!
- Opposite to APDs: **GAIN is MEANINGSLESS**!

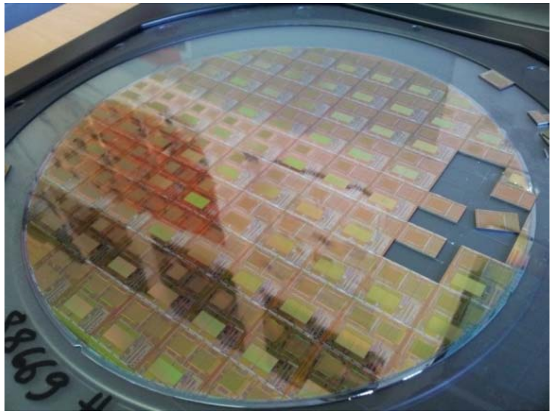
MiSPiA CMOS FrontSPADs

2P4M 0.35µm CMOS Process Line at Fraunhofer IMS





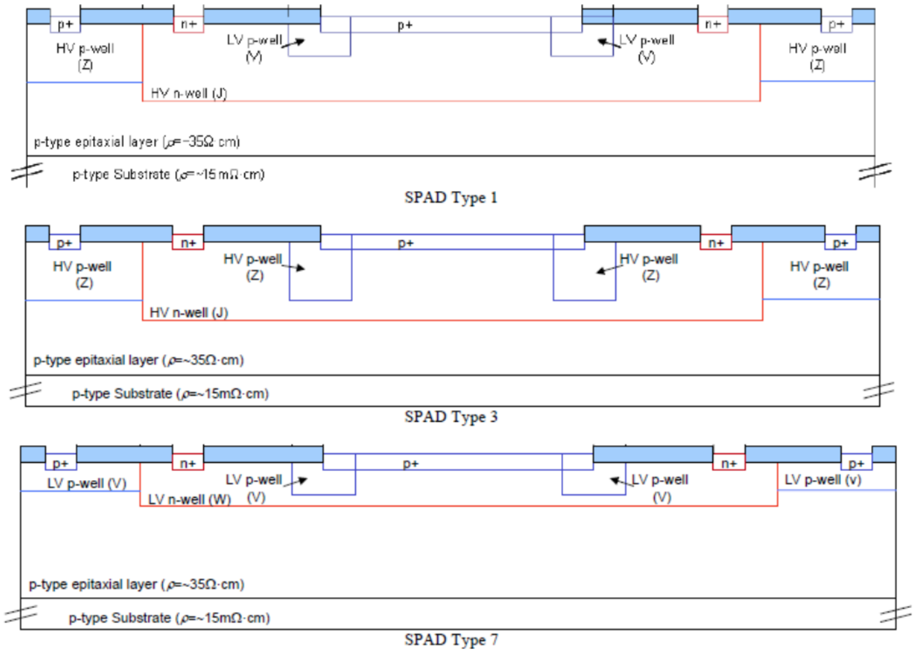


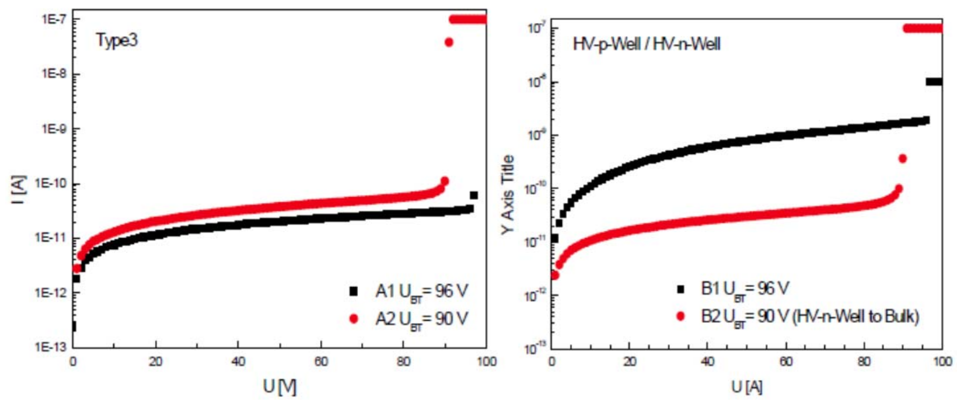


8" Wafers

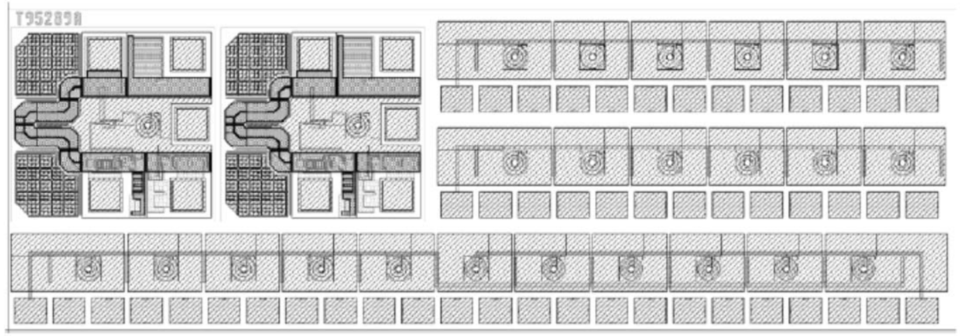
2P4M 0.35µm CMOS Process Line at Fraunhofer IMS

Can we use the standard CMOS process setup?



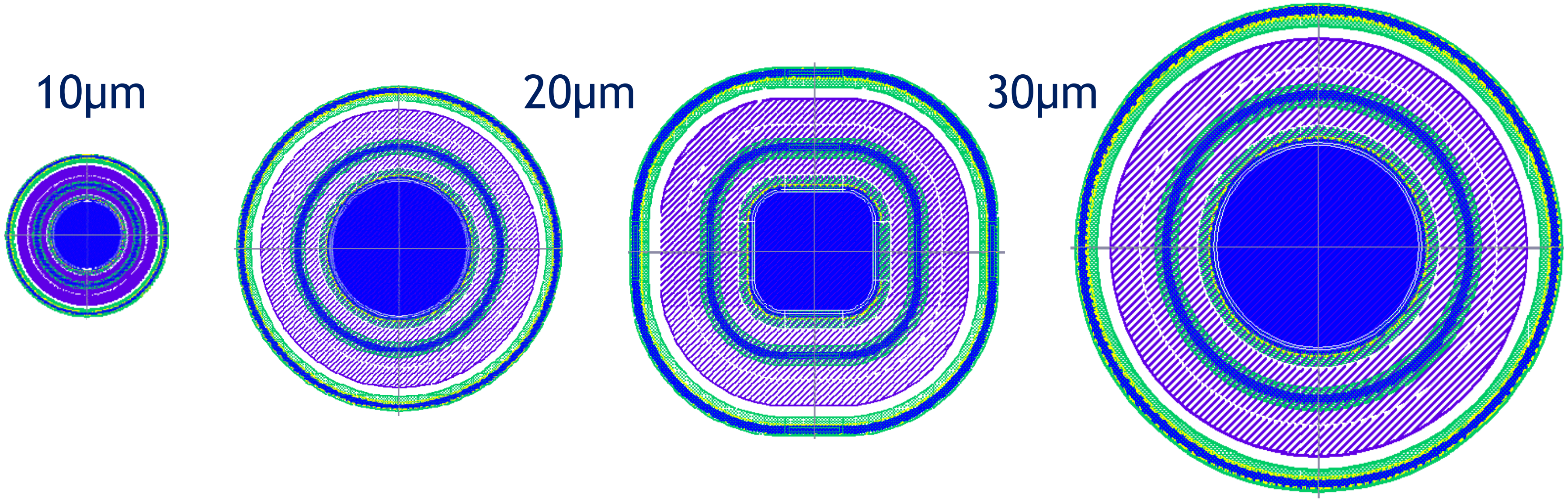


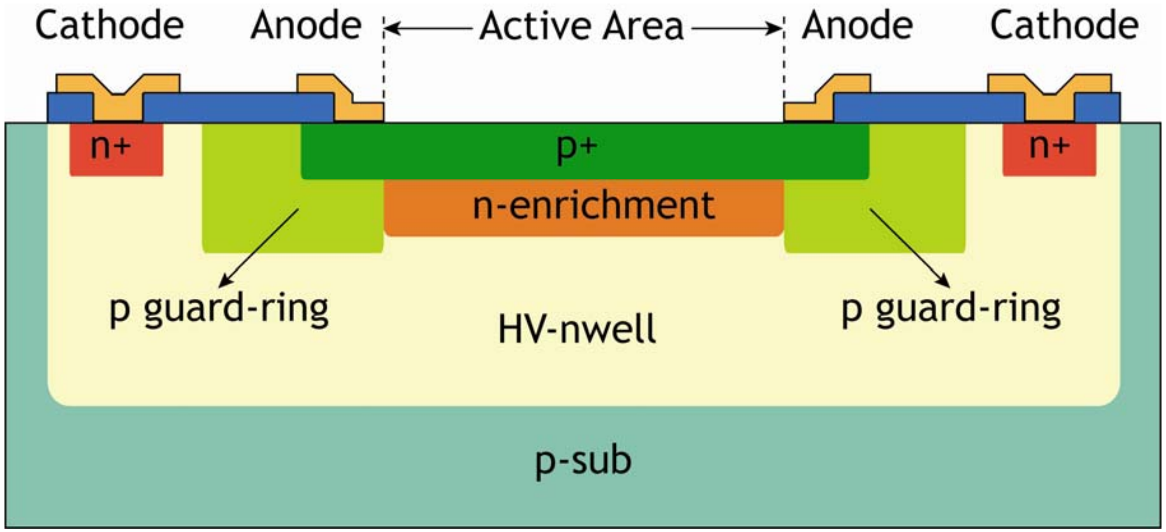
Too high V_{br} → bad time jitters, high dark counts, and no isolation between neighbouring SPADs!



Chip layout for the first MiSPiA batch.

MiSPiA CMOS FrontSPADs

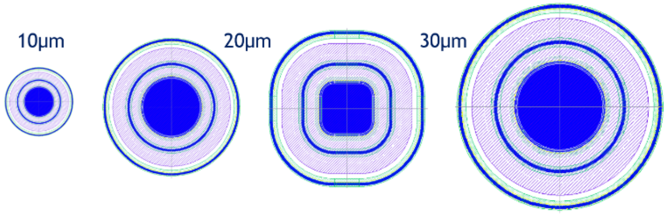




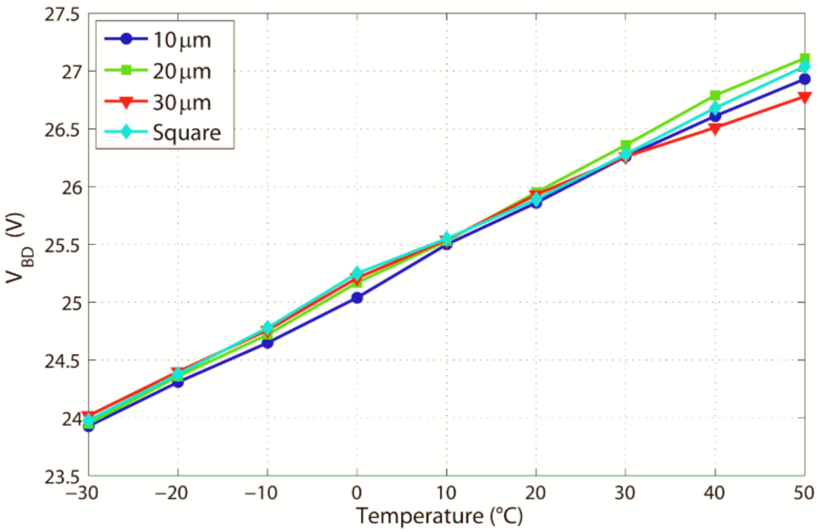
0.35µm HV-CMOS PROCESSING

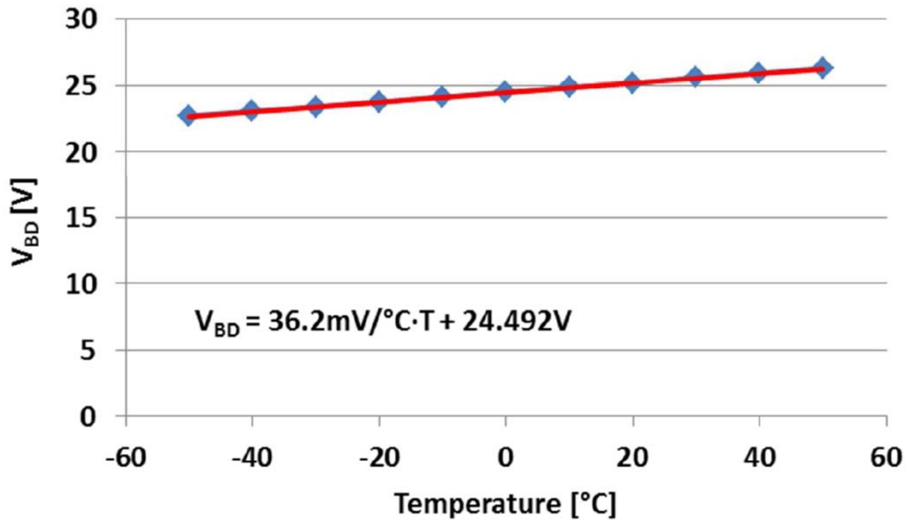
MiSPiA CMOS FrontSPADs

0.35 µm CMOS SPAD Breakdown Voltage



SPAD test structures with diameters: 10 µm, 20 µm, 30 µm, 50 µm, 100 µm, 200 µm, and 500 µm





Temperature drift: 37.8 mV/°C

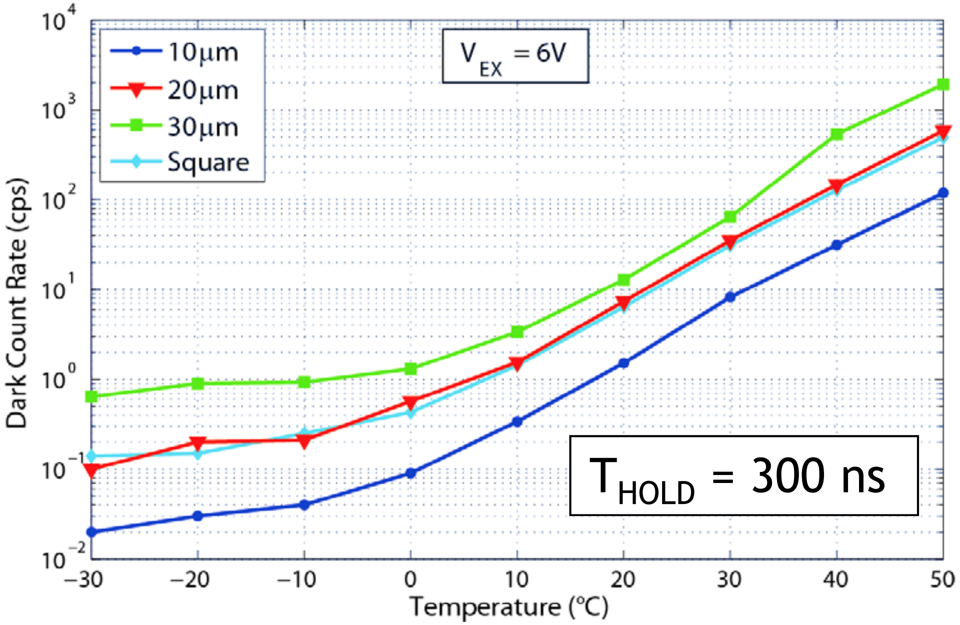
Temperature drift: 36.2 mV/°C

Source: F. Villa et al. "CMOS SPADs with up to 500 µm diameter and 55% detection efficiency at 420 nm", J. Modern Optics, Vol. 61, No. 2, 2014, pp. 102 - 115

Uniformity over different shapes and areas: variation < 6% with respect to room temperature, no peripheral activation.

MiSPiA CMOS FrontSPADs

SPAD Dark Count Rate

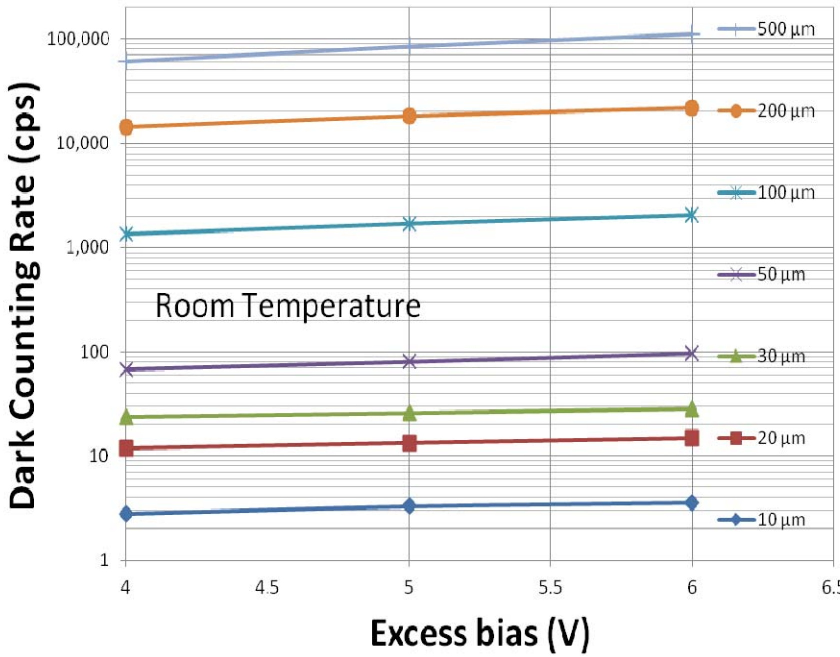


Source: F. Villa et al. "CMOS SPADs with up to 500 μm diameter and 55% detection efficiency at 420 nm", J. Modern Optics, Vol. 61, No. 2, 2014, pp. 102 - 115

STATE-OF-THE-ART DARK COUNT RATE

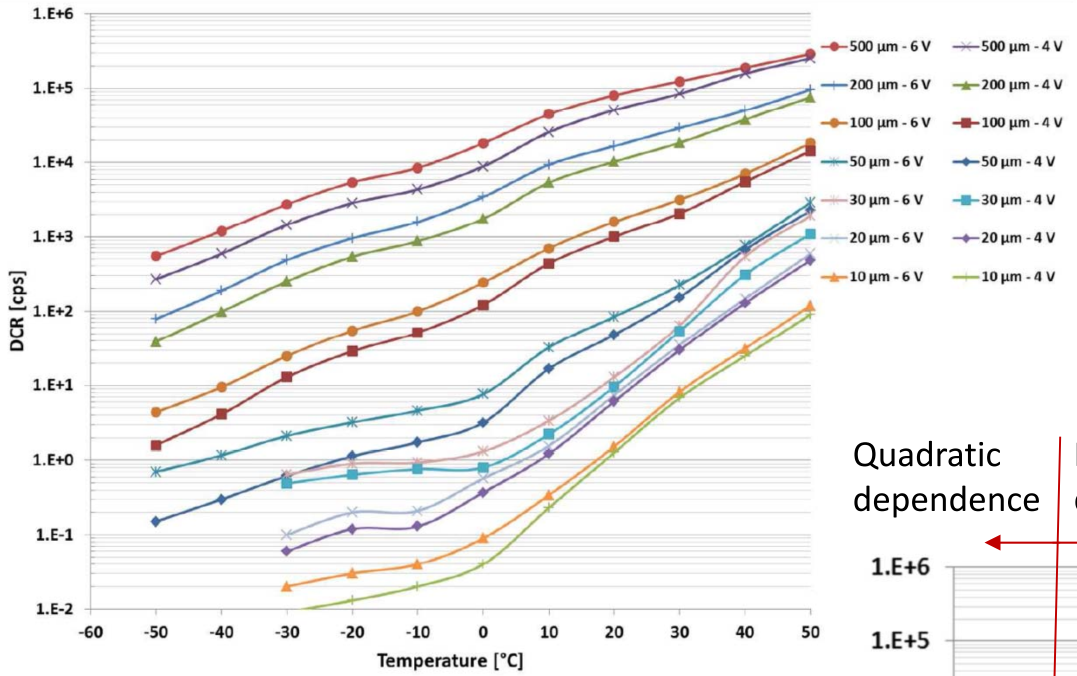
- < 2 kcps @ 50 °C (Ø = 30 μm)
- < 50 cps @ room temp. (Ø = 30 μm)
- Negligible DCR @ low temperature

Acceptable DCR for large SPAD areas



MiSPiA CMOS FrontSPADs

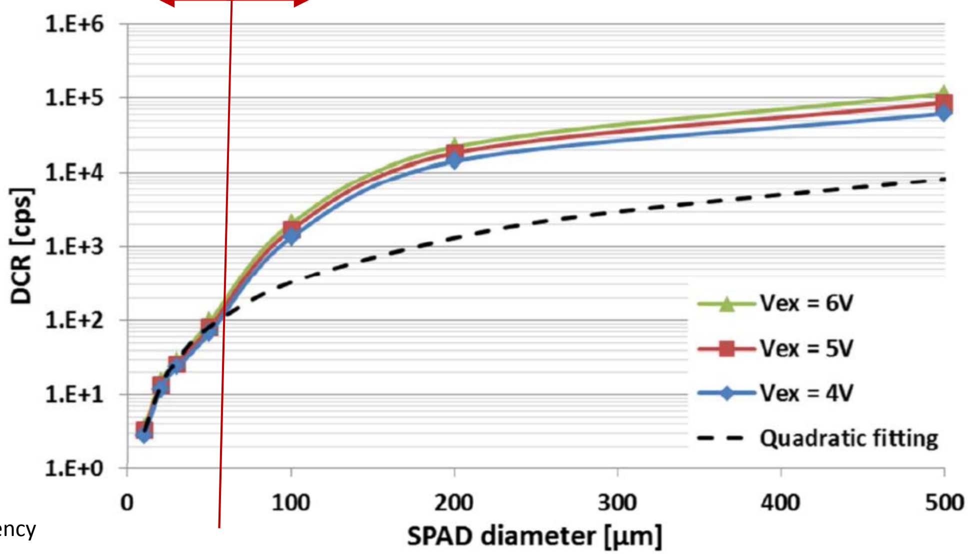
SPAD Dark Count Rate



DCR vs T for SPADs with different diameters and excess biases between 4 V and 6 V.

Quadratic dependence

Higher order dependence

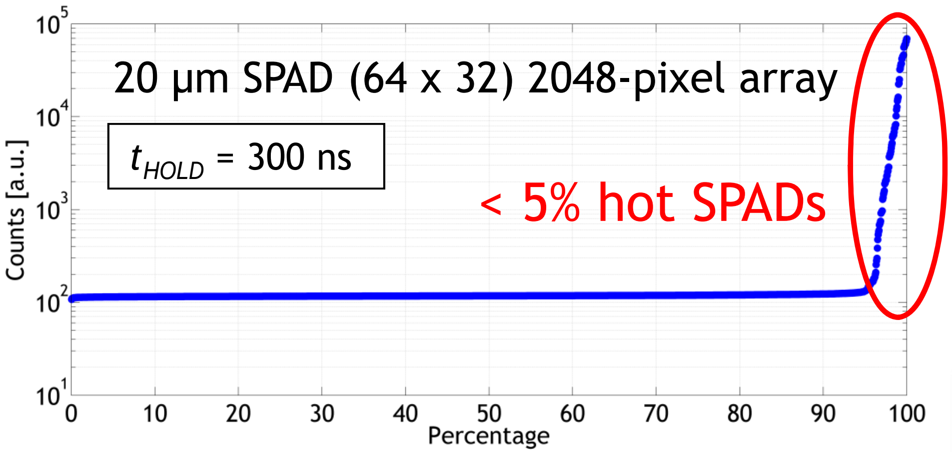


DCR SPAD diameter dependence at room temperature (25°C) for excess biases between 4 V and 6 V.

Source: F. Villa et al. "CMOS SPADs with up to 500 µm diameter and 55% detection efficiency at 420 nm", J. Modern Optics, Vol. 61, No. 2, 2014, pp. 102 - 115

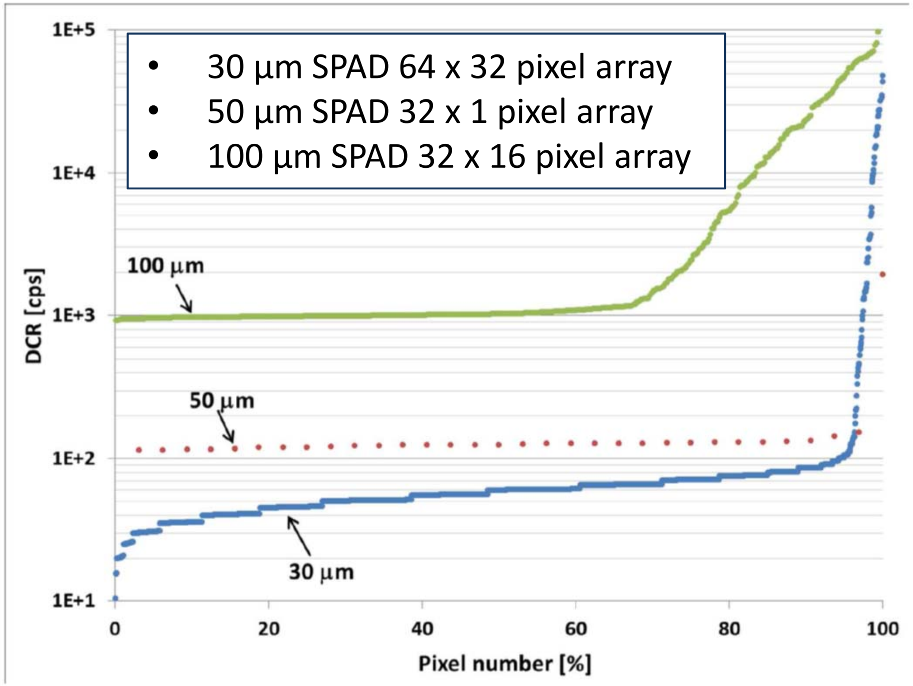
MiSPiA CMOS FrontSPADs

SPAD Dark Count Rate Cumulative Distribution Function



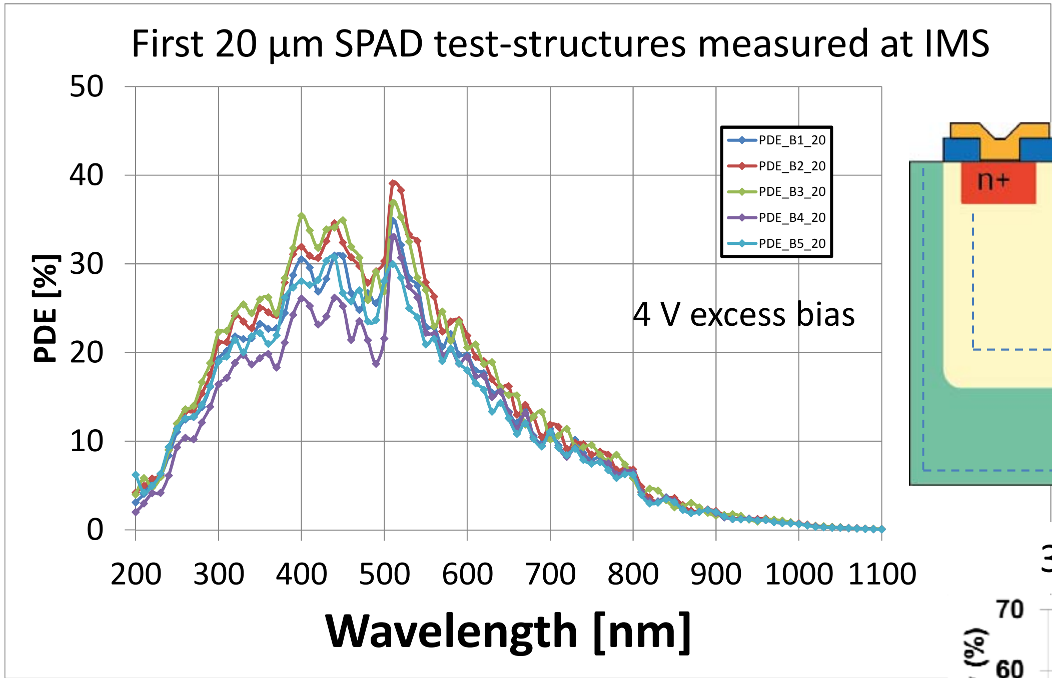
VERY HIGH DCR UNIFORMITY!

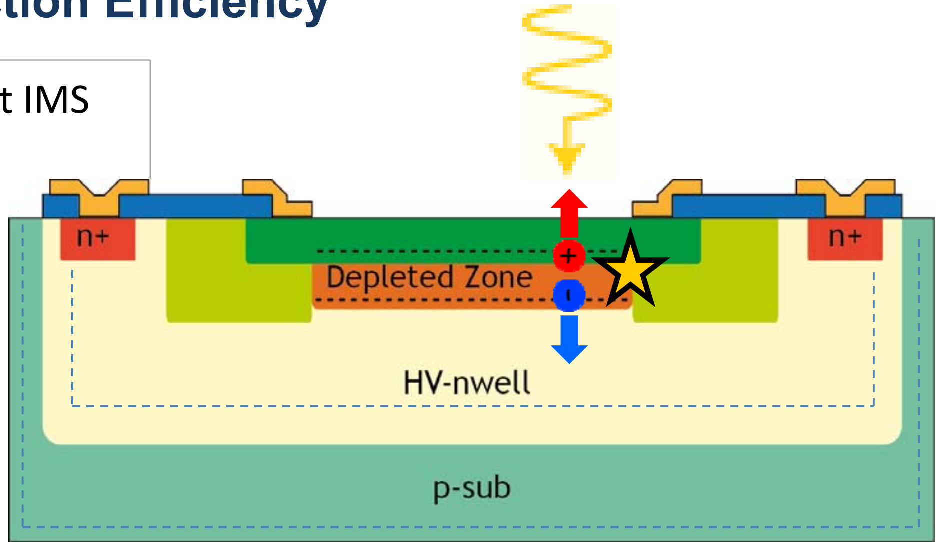
Larger area SPADs show higher DCR and also more „hot“ pixels…



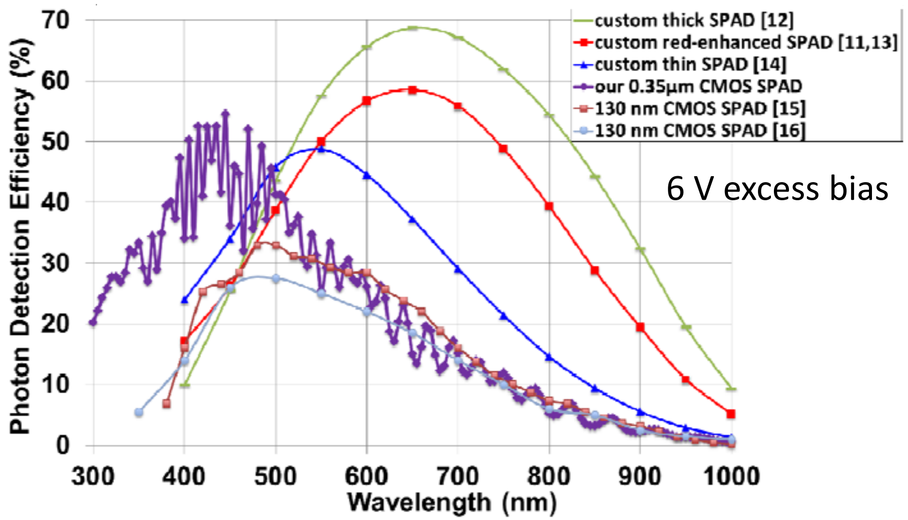
MiSPiA CMOS FrontSPADs

Photon Detection Efficiency





30 µm SPAD pixels measured at POLIMI



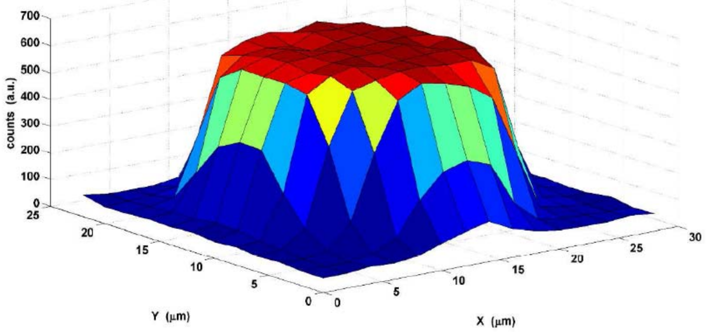
0.35 µm CMOS SPADs compared to:

- the state-of-the-art custom-process reach-through thick SPAD by Excelitas
- red-enhanced SPAD by Polimi and MPD
- planar silicon thin SPAD from MPD, and
- CMOS SPAD in 130 nm technology (MegaFrame Project, 2009)

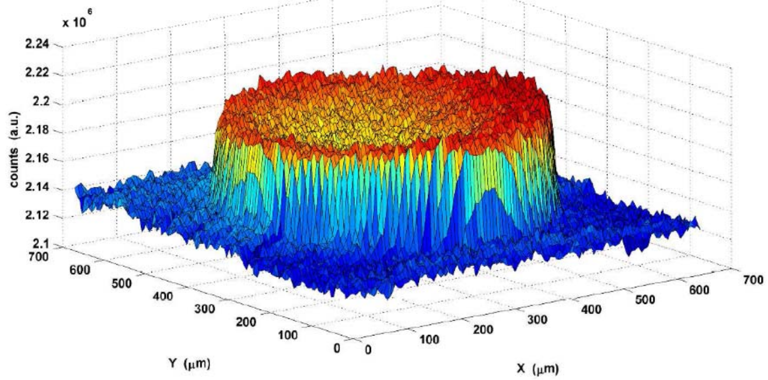
MiSPiA CMOS FrontSPADs

Uniformity of the photoactive area

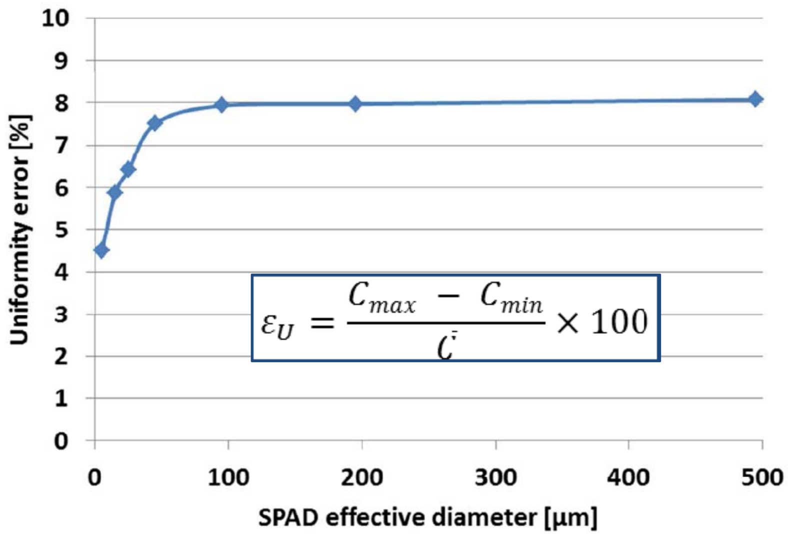
Detection uniformity was measured by scanning the SPAD photoactive area with a laser spot with 2 µm and 6 µm steps



20 µm SPAD
(effective diameter without the guard-ring)



500 µm SPAD
(effective diameter without the guard-ring)

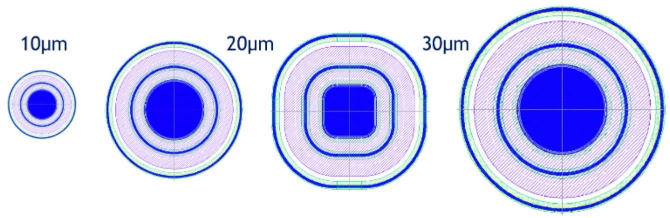


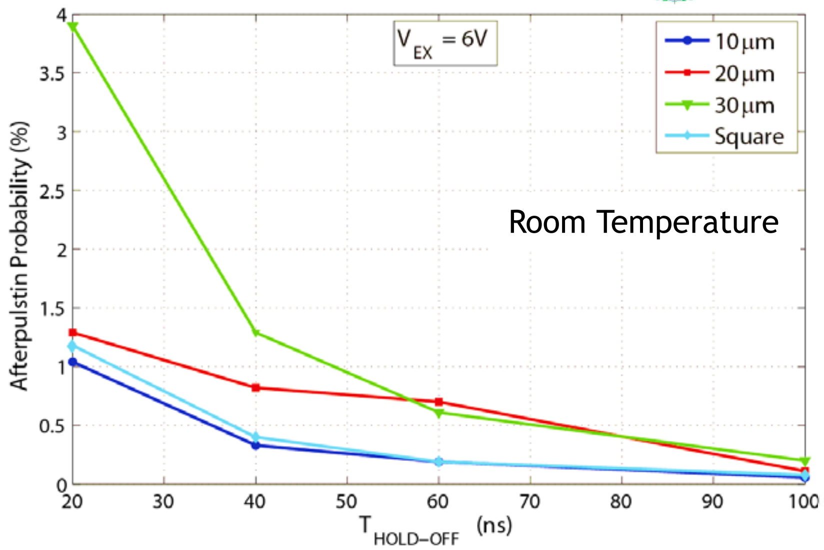
$$\varepsilon_U = \frac{C_{max} - C_{min}}{\bar{C}} \times 100$$

<u>Source</u>: F. Villa et al. "CMOS SPADs with up to 500 µm diameter and 55% detection efficiency at 420 nm", J. Modern Optics, Vol. 61, No. 2, 2014, pp. 102 - 115

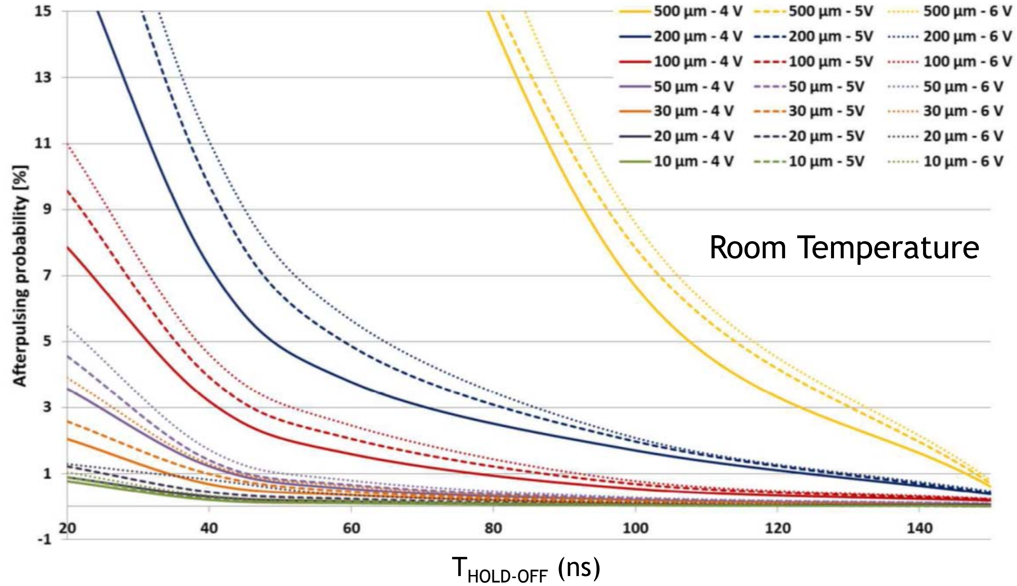
MiSPiA CMOS FrontSPADs

Afterpulsing Probability





SPAD test structures with diameters: 10 μm, 20 μm, 30 μm, 50 μm, 100 μm, 200 μm, and 500 μm



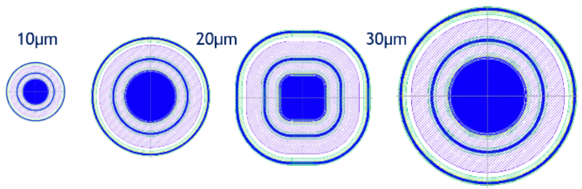
Source: F. Villa et al. "CMOS SPADs with up to 500 μm diameter and 55% detection efficiency at 420 nm", J. Modern Optics, Vol. 61, No. 2, 2014, pp. 102 - 115

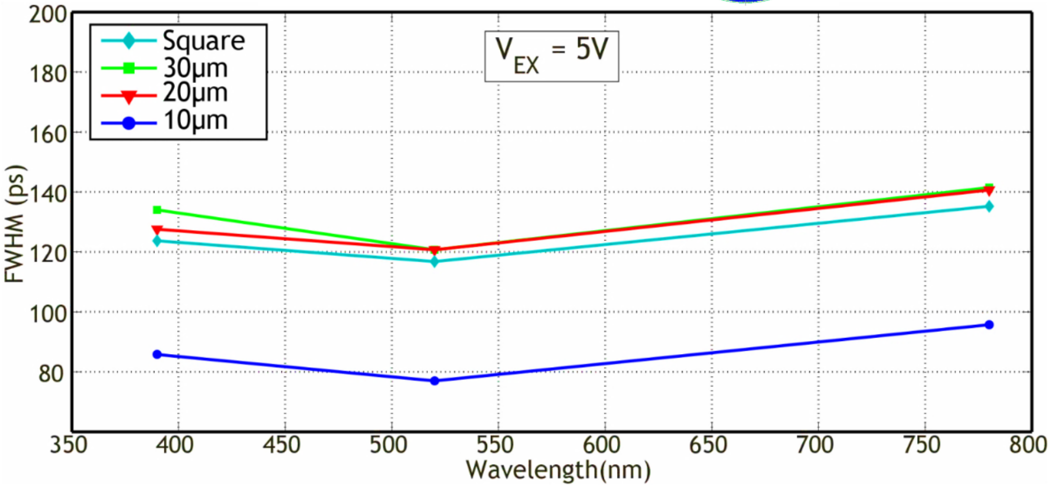
LOW AFTERPULSING PROBABILITY

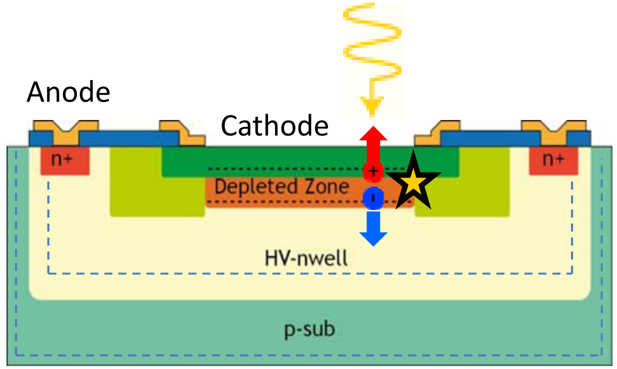
- Negligible AP (< 1%) @ $T_{HOLD-OFF}$ > 50 ns for SPAD areas up to 50 μm diameters
- Negligible AP (< 1%) @ $T_{HOLD-OFF}$ > 90 ns for SPAD areas > 50μm diameters (150ns for 500μm)
- Maximum Count Rate = 50 Mcps

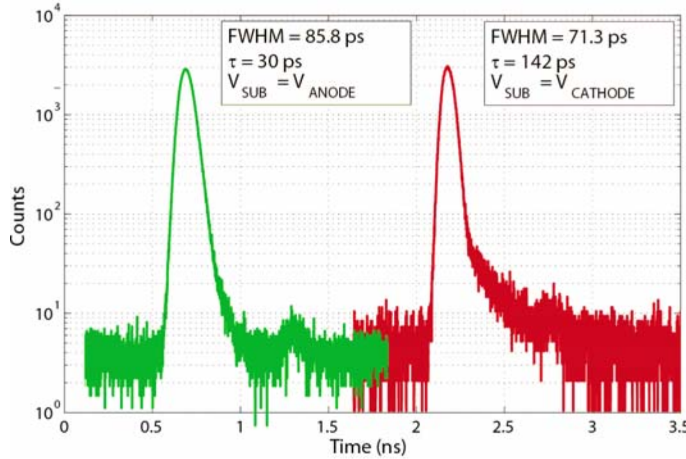
MiSPiA CMOS FrontSPADs

Timing Response







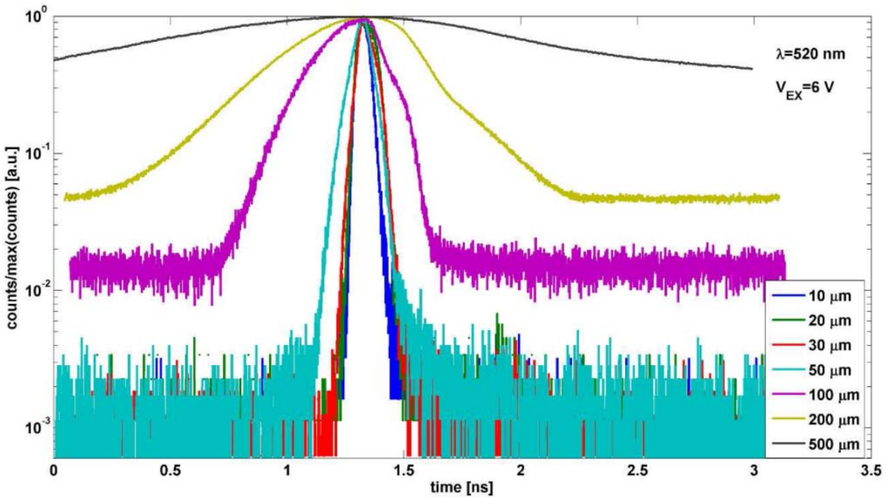


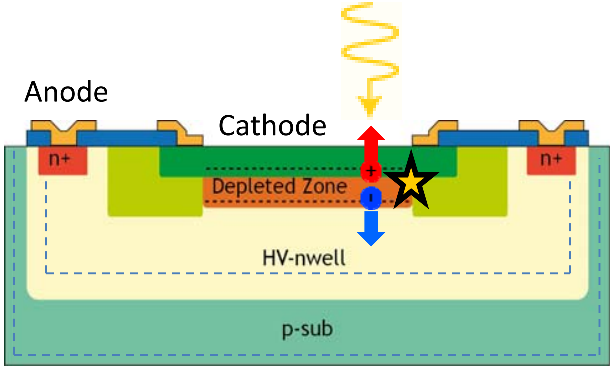
GOOD TIMING RESPONSE

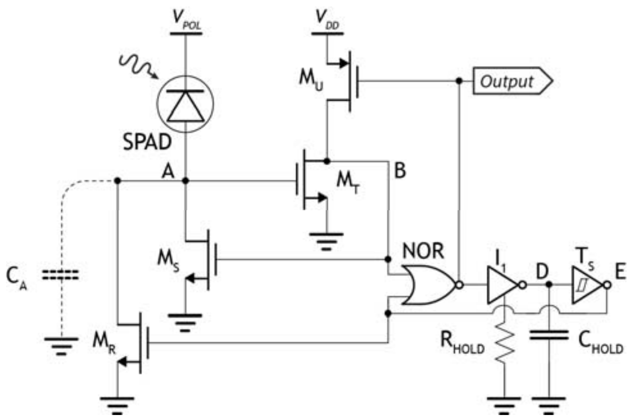
- FWHM < 100 ps (Ø = 10 µm)
- FWHM < 140 ps (Ø = 20 - 30 µm)
- Reduced variations among big devices ($\%\sigma_{FWHM} < 3$)
- Small wavelength influence ($\%\Delta_{FWHM} < 5$)

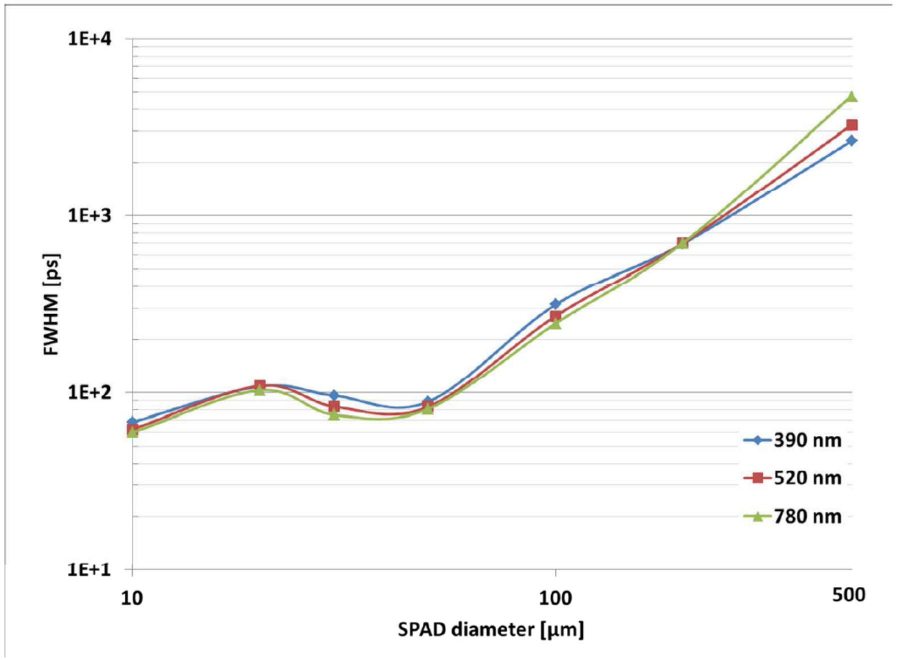
MiSPiA CMOS FrontSPADs

Timing Response



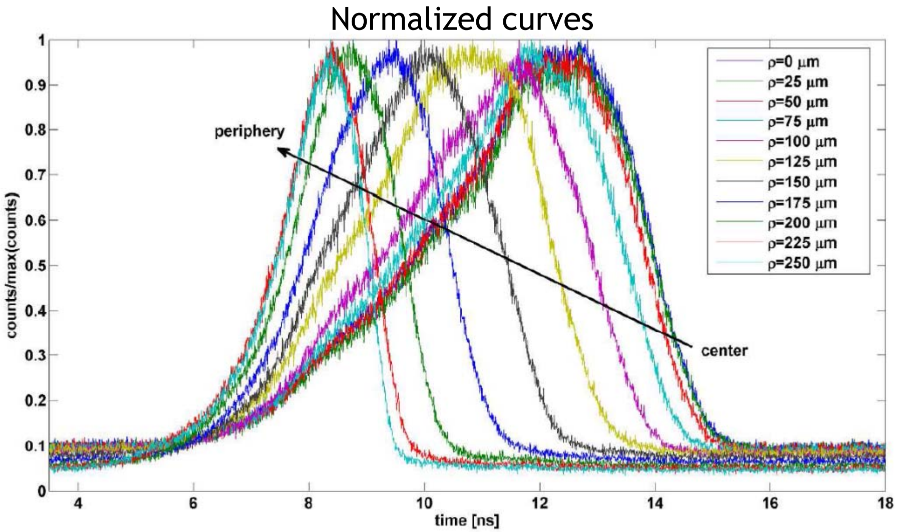


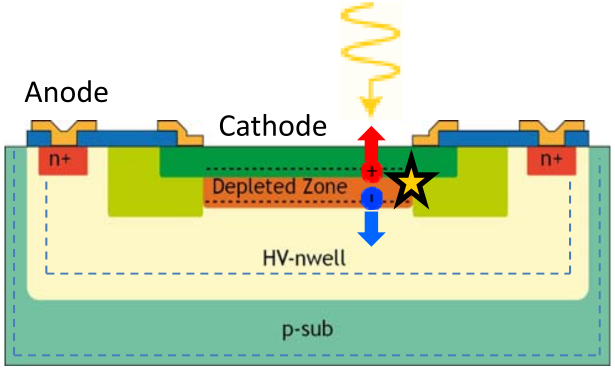




Results obtained using the on-chip integrated quenching circuit with tunable hold-off time and reduced electronics

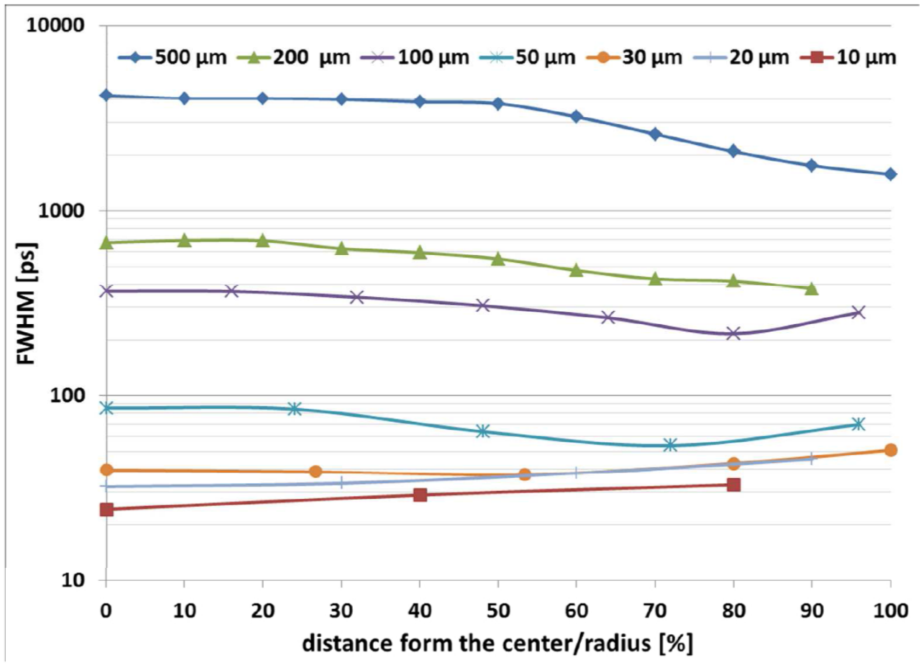
Timing Response





Photon timing response of a 500 µm SPAD at different radial positions of the illumination spot (ρ) from 0 µm (SPAD centre) to 250 µm (periphery of the SPAD photoactive area)

Photon timing response vs. radial position of the illumination spot (expressed in % of the radius length)



MiSPiA CMOS FrontSPADs

A bit of SPAD Bench-Marking, just to see where we are…

SPAD Technology	PDE [%]			DCR/area @ 25°C [cps/µm²]	$T_{HOLD\text{-}OFF}$ [ns]	Time-Jitter, FWHM [ps]	SPAD Photoactive Area Diameter [µm]
	λ = 400nm	Peak	λ = 850nm				
This work [1]	45	53 (470 nm)	4.5	0.055	40 (AP < 1%)	85	10 20 **30** 50 100 200 500
Red-enhanced SPAD by Polimi and MPD [2]	18	60 (650 nm)	29	0.051	n.a.	93	50
0.35 µm CMOS planar silicon thin SPAD (not this technology) from MPD [3]	25	42 (550 nm)	4.5	3.979	600 (AP < 1%)	39	20
CMOS SPAD in 130 nm technology (MegaFrame Project, 2009) [4]	14	28 (500 nm)	6	0.249	100 (AP < 0.02%)	200	8
CMOS SPAD in 90 nm technology (SPADNet Project, 2012) [5]	17	44 (690 nm)	21	3.466	15 (AP < 0.375%)	52	6.4

[1] F. Villa et al., "CMOS SPADs with up to 500 µm diameter and 55% detection efficiency at 420 nm", *Journal of Modern Optics*, Vol. 61, Issue 2, pp. 102-115, 2014

[2] A. Gulinatti et al., "New silicon SPAD technology for enhanced red-sensitivity, high resolution timing and system integration", *Journal of Modern Optics*, 59(17), pp. 1489-1499, 2012

[3] F. Guerrieri et al., "Single-Photon Camera for high-sensitivity high-speed applications", Photonic Journal, IEEE, Vol. 2 (5), 759-774, 2010

[4] J. A. Richardson et al., A low dark counting single photon avalanche diode structure compatible with standard nanometer scale CMOS technology", *IEEE Phot. Techn. Letters*, 21 (14), 120-122, 2009

[5] E. A. G. Webster et al., "A single-photon avalanche diode in 90-nm CMOS imaging technology with 44% photon detection efficiency at 690 nm", IEEE Electron Dev. Letters, 33 (5), 694 - 696, 2012

MiSPiA CMOS FrontSPADs

A hypothetical SiPM Bench-Marking, just to see where we are…

SPAD Technology	PDE [%]			DCR/area @ 25°C [cps/µm²]	$T_{HOLD\text{-}OFF}$ [ns]	Time-Jitter, FWHM [ps]	SPAD Photoactive Area Diameter [µm], cell-size [µm²], and FF [%]
	λ = 400nm	Peak	λ = 850nm				
This work [1]	45	53 (470 nm)	4.5	0.055	40 (AP < 1%)	85	10 20 **30** 50 100 200 500 current SPAD cell pitch: 70 µm, goal cell-pitch: 56 µm, current FF= 18.4 %, goal FF= 28.7 %
Philips Digital Photon-Counting (PDPC) Model DLS-3200-22-44 [2]	37	40 (420 nm)	~7	DCR (95 cells active) = 7MHz, 3200 cells/pixel, cell size: 59.4 µm x 64 µm, FF = 75%: **0.807**	n.a.	44	~30 (cell size: 59.4 µm x 64 µm, FF = 75 %)
HAMAMATSU Multi-Pixel Photon-Counter (MPPC) Series S10985 [3]	40	50 (440 nm)	~7	DCR/channel = 6 MHz, 3600 pixels/channel, pixel size: 50 µm x 50 µm, FF = 61.5%: **1.084**	n.a.	n.a.	~22 (cell size: 50 µm x 50 µm, FF = 61.5 %)

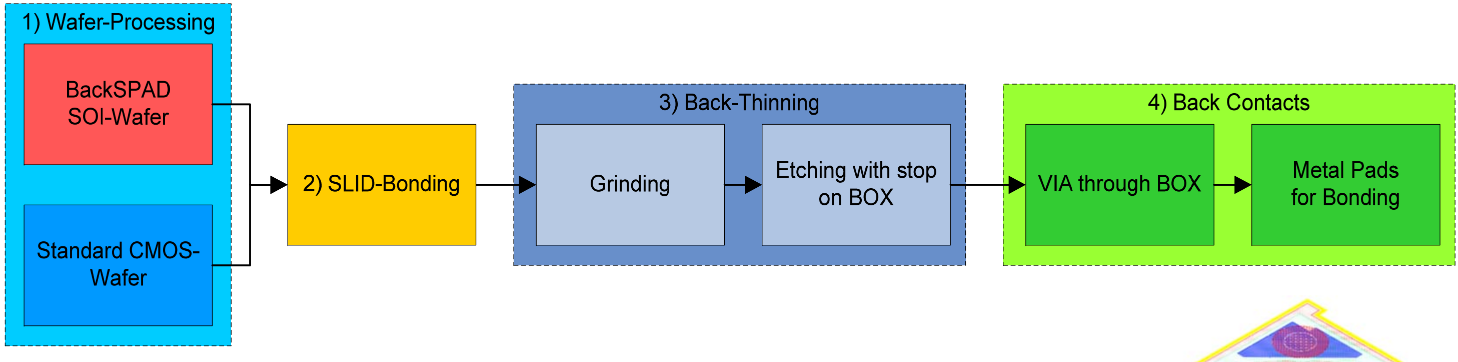
[1] F. Villa et al., "CMOS SPADs with up to 500 µm diameter and 55% detection efficiency at 420 nm", *Journal of Modern Optics*, Vol. 61, Issue 2, pp. 102-115, 2014

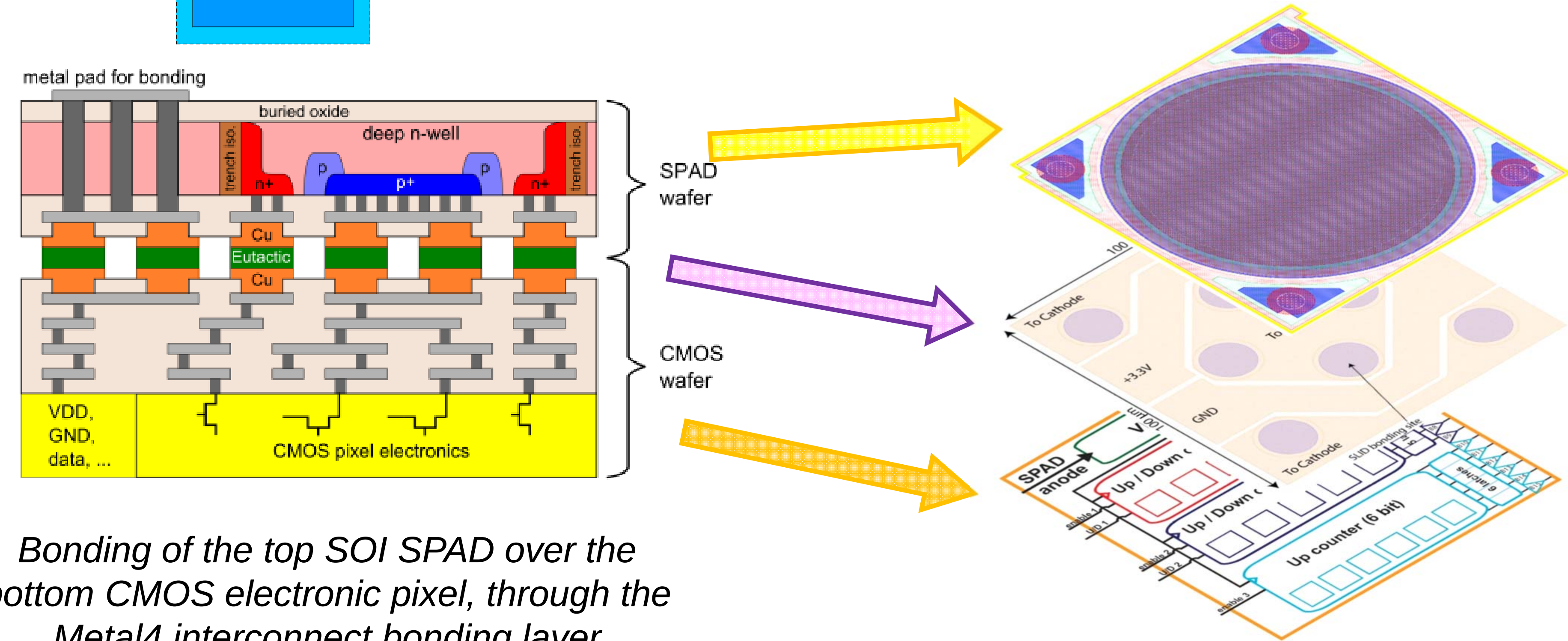
[2] http://www.digitalphotoncounting.com/wp-content/uploads/dSiPM-Leaflet_A4_2013-11_A4.pdf

[3] http://www.hamamatsu.com/resources/pdf/ssd/s10984_series_etc_kapd1024e03.pdf

MiSPiA CMOS BackSPADs

Schematic representation of the BackSPAD process flow and back-side thinning

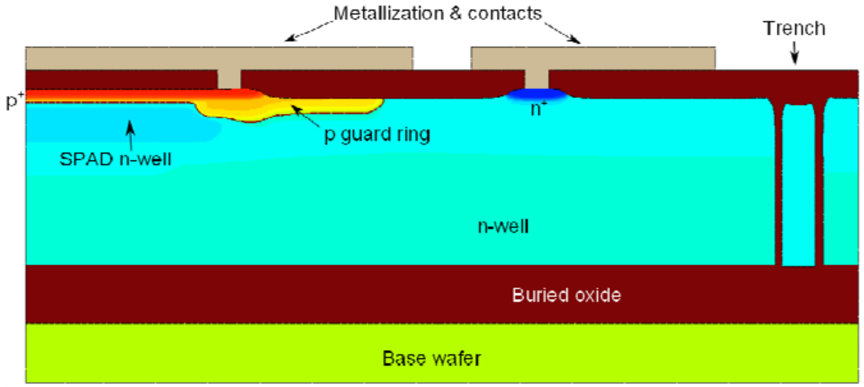




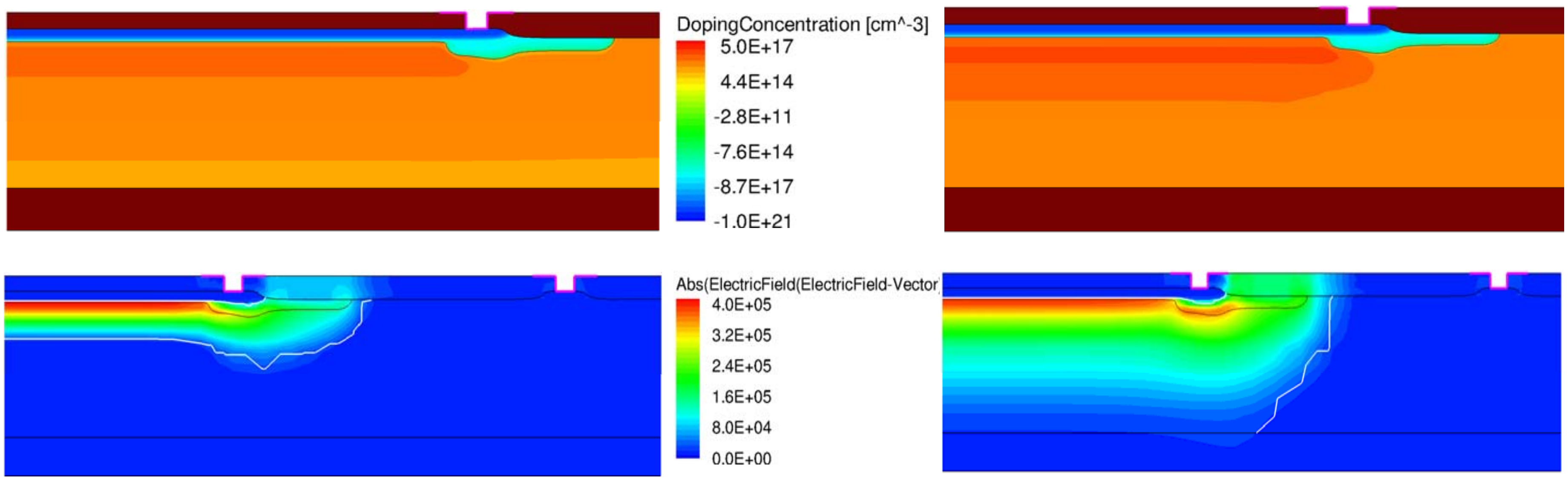
Bonding of the top SOI SPAD over the bottom CMOS electronic pixel, through the Metal4 interconnect bonding layer

MiSPiA CMOS BackSPADs

Process simulation of a cross-section of the SOI BackSPAD wafer

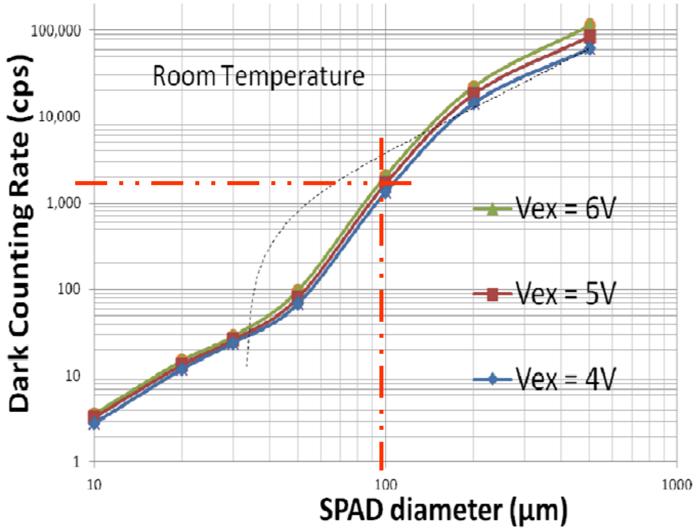


Fully-Depleted (HV) BackSPADs | **Partially-Depleted (LV) BackSPADs**



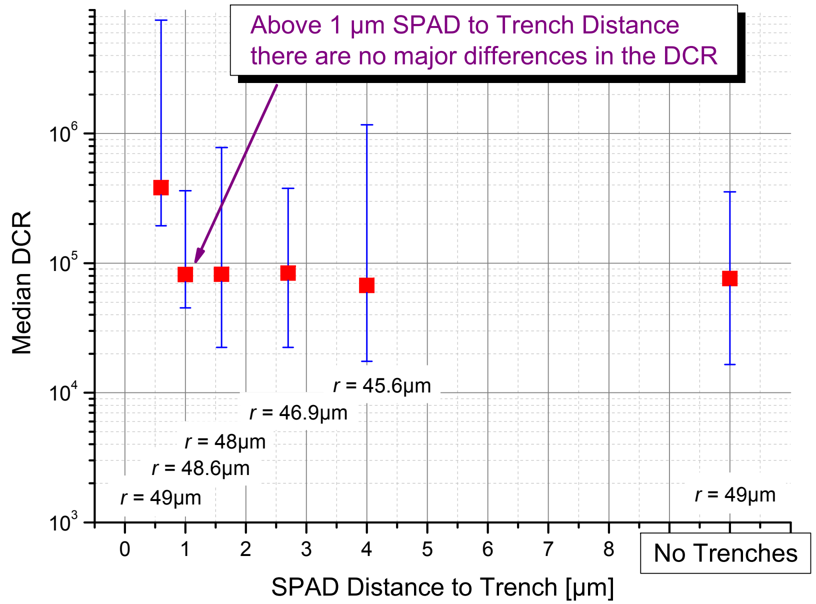
MiSPiA CMOS BackSPADs

State-of-the-Art MiSPiA FrontSPAD DCR:



For approx. 100 µm BackSPAD diameter:

$DCR_{BackSPAD} \approx 40 \times DCR_{FrontSPAD}$



For 150 µm FrontSPAD pixels with 30 µm SPAD diameter

→ $DCR_{FrontSPAD}$ ≈ 100 cps with a Fill-Factor of 3.14%

Equivalent 150 µm BackSPAD pixels with 143 µm SPAD diameter

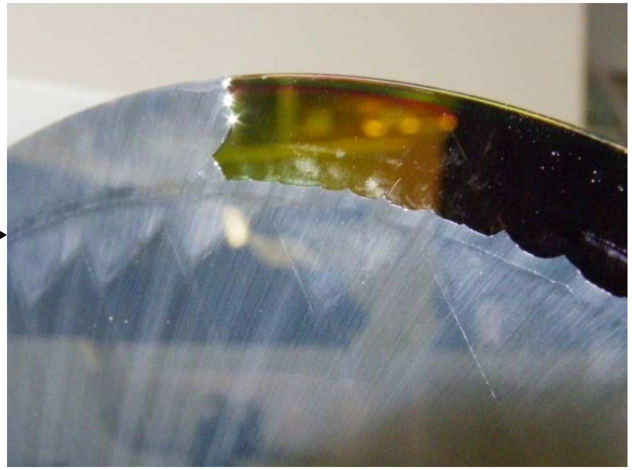
→ $DCR_{BackSPAD}$ ≈ 240 kcps with a Fill-Factor of 71.4%!

A trade-off must be met between the BackSPAD DCR and the photoactive area!

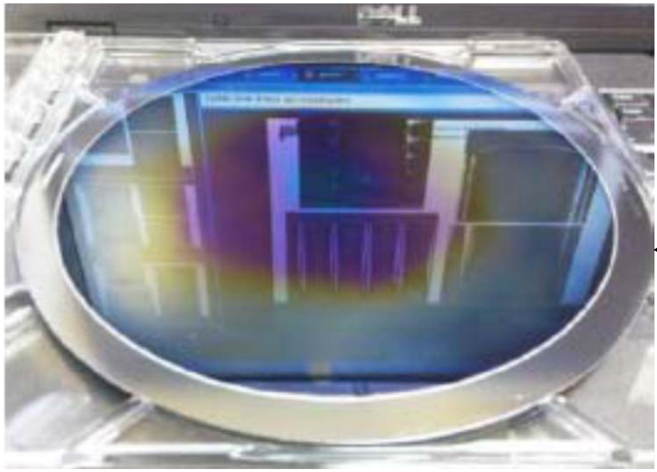
MiSPiA CMOS BackSPADs

Wafer-bonding of the BackSPAD SOI/CMOS array chips

Wafer without seal ring after back grinding



Wafer with seal ring after back grinding

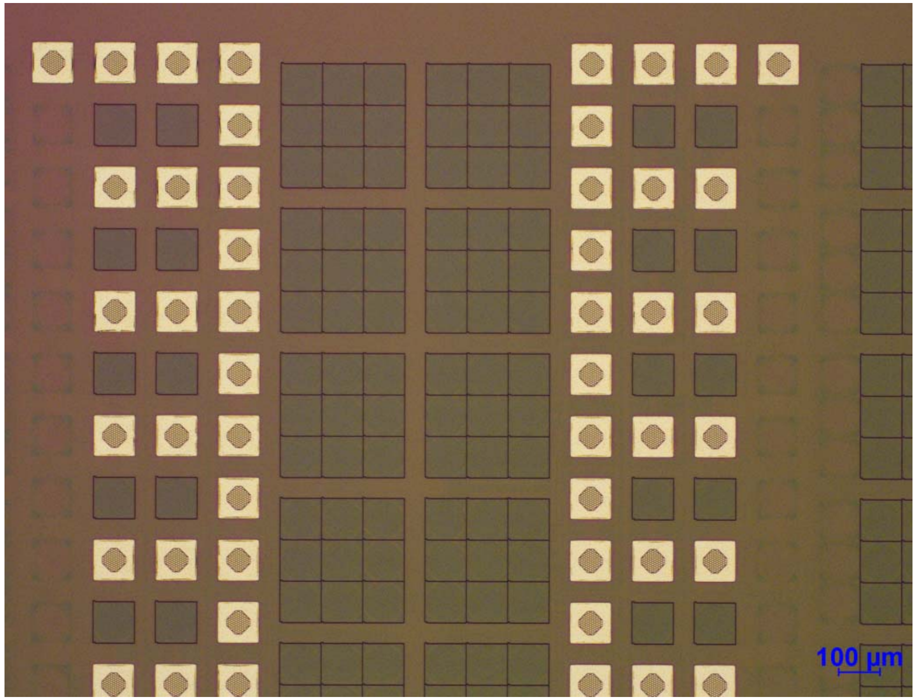


Wafer with seal ring after reduced back grinding and dry etching

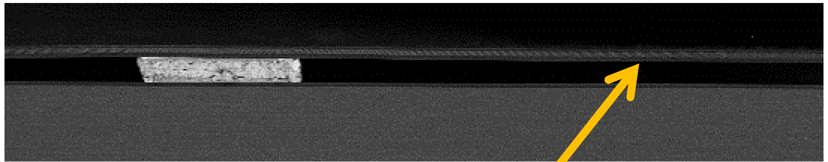
MiSPiA CMOS BackSPADs

Wafer-bonding of the BackSPAD SOI/CMOS array chips

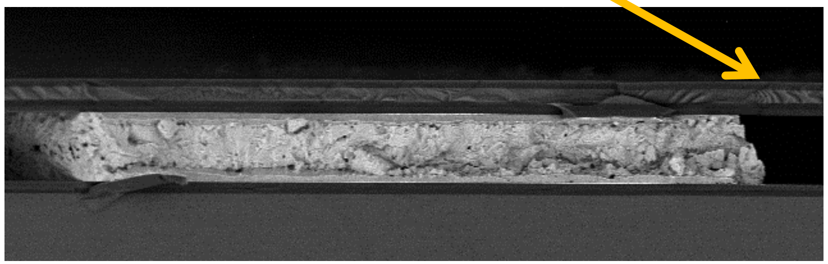
Pads and SPADs on wafer bonded BackSPADs



Cross section of SOI wafer after waferbonding and backthinning



4 µm thick Si/SiO2 film



CONCLUSIONS

- The MiSPiA FrontSPADs deliver:
    - the lowest DCR reached so far in CMOS technologies
    - high UV-PDE due to the special UV-transparent Silicon-Nitride based passivation layer

- BackSPADs are based on a standard SOI-CMOS technology, the ROIC is developed in the standard 0.35 µm CMOS technology

- The measured DCR are higher than those measured in FrontSPADs, but still in the expected range of state-of-the-art CMOS SPADs (kcps)

- The presence of deep trench isolation minimizes cross-talk issues, drastically decreases the minimum distance between adjacent SPAD structures (7µm), and does not increase the DCRs for distances above 1 µm to the BackSPAD device area

- The developed technology is suitable also for SiPM developments, where further optimization of the fill-factors should be addressed

“Microelectronic Single-Photon 3D Imaging Arrays for low-light high-speed Safety and Security Applications”

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