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Single trap dynamics in electrolyte-gated Si-nanowire field effect transistors

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Liquid-gated silicon nanowire (NW) field effect transistors (FETs) are fabricated and their transport and dynamic properties are investigated experimentally and theoretically. Random telegraph signal (RTS) fluctuations were registered in the nanolength channel FETs and used for the experimental and theoretical analysis of transport properties. The drain current and the carrier interaction processes with a single trap are analyzed using a quantum-mechanical evaluation of carrier distribution in the channel and also a classical evaluation. Both approaches are applied to treat the experimental data and to define an appropriate solution for describing the drain current behavior influenced by single trap resulting in RTS fluctuations in the Si NW FETs. It is shown that quantization and tunneling effects explain the behavior of the electron capture time on the single trap. Based on the experimental data, parameters of the single trap were determined. The trap is located at a distance of about 2 nm from the interface Si/SiO_2 and has a repulsive character. The theory of dynamic processes in liquid-gated Si NW FET put forward here is in good agreement with experimental observations of transport in the structures and highlights the importance of quantization in carrier distribution for analyzing dynamic processes in the nanostructures. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4883757]

I. INTRODUCTION

Semiconductor nanowires (NWs) have been the subject of comprehensive research in recent years due to their unique physical properties. NWs are promising candidates for application in a variety of fields, such as engineering, electronics, optoelectronics, biophysics, and biomedicine.[1–6] Over the past few decades, great progress has been made in the fabrication, device physics, modeling, and simulation of the electrical properties of NW field effect transistors (FET).[7–9] Among other electronic devices, silicon NW FETs play a major role in modern electronics due to their compatibility with the CMOS process. The small NW cross-section offers significant gate control over the drain current, therefore NW FETs represent ultimate building blocks for nanoelectronics. However, a comprehensive understanding of the transport mechanisms in FET structures is of crucial importance for the development of ultrasensitive devices. Transport through the nanosize FETs can be conditioned by drift, diffusion, ballistic effects, tunneling, and thermionic emission. Tunneling current is crucial for lateral FETs, while carrier transport in axial FETs can be described within the Schottky emission theory.[10–12] Transport through FETs can also be regarded as ambipolar electrical transport.[13] Currently, the unified charge control model for metal-oxide-semiconductor (MOS) FETs is generally accepted.[14–16] It describes the I-V characteristics of the MOSFET for the entire range of parameters from sub-threshold to above-threshold regimes as well as linear and saturation modes. However, in the case of liquid-gated NW FETs, there are still a number of open questions. For example, two main concepts are being considered at present for optimizing the sensitivity of Si NW sensors: using the sub-threshold mode or above-threshold mode.[17,18]

Another parameter to be considered for sensor development is the transistor noise, because it is always a limiting factor for high-sensitivity applications. Therefore, noise spectroscopy and current fluctuation studies are usually employed in order to investigate the main noise sources as well as the overall noise behavior in different device operating modes. Fluctuation analysis is a powerful approach to study the transport properties of different kinds of devices, including nanoscale liquid-gated structures. The noise properties of MOSFETs have been studied since van der Ziel's work in the 1986.[19] Noise in MOSFETs increases as the devices are scaled down. A decrease in the feature size L leads to an increase in the normalized 1/f noise density proportional to L^{-3}.[20,21] Flicker noise originates from the oxide-trap-induced carrier number fluctuations as well as from the carrier mobility fluctuations.[22] Extensive measurements of low-frequency noise in ion sensitive field effect transistors (ISFETs), introduced by Bergveld[23,24] under various bias conditions corresponding to the gate voltage changing from subthreshold to saturation range were performed.[25] The measured ISFETs exhibit clearly 1/f noise down to 1 Hz and governed by trapping-detrapping processes on the insulator interface. The 1/f noise of Si NW bio-FETs is characterized and compared with various fabrication approaches, specifically, a wet orientation-dependent etch

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versus common plasma-based etching methods. The wet-etched devices are shown to have significantly lower noise and subthreshold swing.[26] It is shown that the particular etch process used will be critical in determining the density of surface states and, ultimately, the noise performance. Investigations of the mechanisms responsible for the low-frequency noise in liquid-gated nanoscale Si NW-FETs show that the charge-noise level is lower than elementary charge. Dielectric polarization noise also seems to be at the origin of the 1/f noise. It is noted that the estimated spectral density of charge-noise gives opportunity for the electrical detection of a small number of molecules.[27] The noise level at the nanoscale generally depends on the traps located in an oxide layer. 1/f noise in Si NW-ISFETs having different wire widths ranging from 100 nm to 1 μm and operated under different gating conditions is analyzed.[28] It is found that the gate-referred voltage noise spectral density S_V is constant over a large range of Si NWs resistances tuned by a DC gate voltage. The measurements of S_V for Si NWs with two different gate-oxide thicknesses, but otherwise similar device parameters, are only compatible with the so-called trap state noise model in which the source of 1/f noise is due to trap states residing in the gate oxide (most likely in the interface between the semiconductor and the oxide).S_V is found to be inversely proportional to the wire width for constant wire length. No influence of the ions in the buffer solution on the noise in BioFET was found.[28] Studies on nanoscale field-effect sensors reveal the crucial importance of the low-frequency noise for determining the ultimate detection limit. Investigations of the 1/f-type noise of Si nanoribbon field-effect sensors show that the signal-to-noise ratio can be increased by almost two orders of magnitude if the nanoribbon is operated in an optimal gate voltage range.[29] An effect of coupling between the liquid and back gate has been revealed in Ref. 30, and utilized to increase the sensitivity of the liquid-gated FET by 50%. Usually, in the case of very small channel cross sections ($\propto 10^{-10} \div 10^{-12}\,\mathrm{cm}^2$), only a single trap may determine the channel current fluctuations. In this situation, the capture and emission of mobile carriers on the trap lead to discrete modulation of the drain current similar to the random telegraph signal (RTS).[31] RTS noise is extremely important in determining the performance and reliability of the nanoscale devices.[27,32,33] Trapping-detrapping processes can also be used for development of different memory cells.[34] RTS amplitude measurements can be used also to extract tiny gate capacitance value.[35] An individual charged trap can significantly change the drain current I_{ds}, thus affecting the performance of the entire circuit.[36] Nevertheless, studies of these single-trap events provide the major advantage of characterizing the device properties and transport mechanisms at the ultimate, "atomistic" level. The interaction of a single trap with the conducting channel is mainly determined by the distribution of the mobile charge carriers in the close vicinity of the gate oxide/silicon interface.

The distribution of the mobile charge carriers and the magnitude of their mobility determine the static and dynamic behavior of the transistor, especially in the case of RTS fluctuations. Indeed, the distribution in the NW FETs channel may differ from its classical counterpart due to quantum confinement in the space charge region of the channel cross-section. This may lead to overestimation of different kinds of FET parameters during fitting. Quantization may result in the shift of the maximum location of the electron density from the front gate interface. This can be considered to be equivalent to increasing the effective tunneling distance to the trap. The impact of the size quantization of charge carrier distribution on the tunnel mechanisms to the single oxide trap of the nano-size channel of liquid-gated FETs has not yet been reported.

In this paper, we report on transport and dynamical properties of liquid-gated Si NW FETs. The influence of the channel quantization on the Si NW FET transport peculiarities, capture and emission processes of the single oxide trap, and random telegraph signal noise behavior is analyzed. We show the importance of considering the size quantization effect in the inversion layer. Our theoretical results and experimental data are in good agreement. The behavior of the ratio between capture and emission time constants was explained on the basis of the quantization effect and tunneling, modeled for liquid-gated Si NW FET devices.

II. EXPERIMENTAL DETAILS

A. Nanowire FETs fabrication

A silicon-on-insulator (SOI) substrate with low boron doping of the active layer ($10^{15}\,\mathrm{cm}^{-3}$) was used to fabricate the Si NW FET devices. The SOI substrate consists of a 70 nm $\langle 100 \rangle$ oriented top active silicon layer, a 145 nm buried oxide (BOX) layer, and a 675 μm substrate. Firstly, a thin layer of 37 nm SiO_2 was formed by dry oxidation. The layer was structured using electron beam lithography (EBL) and then used as a mask to define the silicon NWs structures. The structure in SiO_2 was transferred to the silicon layer by tetramethylammonium hydroxide etching.[26] In order to protect the interface between the NW channel and gate oxide from ion implantation damage, a 5 nm SiO_2 sacrificial oxide layer was grown using thermal oxidation at 1000 °C. Then the areas of the Si NWs were protected from implantation by hydrogen silsesquioxane (HSQ) resist and arsenic ion implantation was performed to fabricate low-resistive source and drain ohmic contacts to the nanowires (beam energy: 20 KeV, dose: $0.5 \times 10^{15}/\mathrm{cm}^2$). Next, the damaged sacrificial oxide and HSQ were removed by immersing the sample into the diluted HF solution. Etching the NW protection layer was followed by formation of a 9 nm thick front oxide (FOX) layer, which was grown in a thermal furnace at 1000 °C. The source/drain contact pads were fabricated by means of conventional lithography, electron-beam metal evaporation (300 nm of Al), and a lift-off process. The Si NW devices were encapsulated to protect the contact pads from the liquid. We used wire bonding on a 20-pin carrier and a small dish made of a glass ring glued on top of the carrier. The volume between the chip and glass ring was filled with polydimethylsiloxane (U300 8OZ, Epo-TEK, USA). SEM (scanning electron microscope) images of the fabricated Si NW FETs are shown in Figure 1.

B. Electrical characterization of Si NW FETs

The electrical properties of liquid-gated nanowire FETs are characterized by measurements of current-voltage

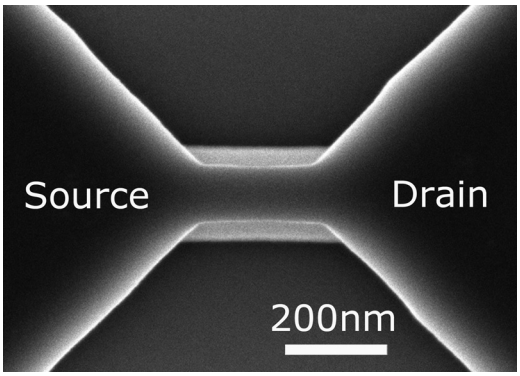

FIG. 1. Scanning electron micrograph of a Si NW FET device. The scale bar is 200 nm.

characteristics and low-frequency noise spectra. The front gate voltage was applied through a Ag/AgCl reference electrode (RE) (Super Dry-Ref (SDR2), WPI, Germany) using a droplet of electrolyte solution in the center of the sensor array. The drain voltage and the front gate voltage were set against the grounded source contact. A dynamic signal analyzer (HP35670A) was used for the low-frequency noise measurements in the frequency range from 1 Hz to 100 kHz.

III. RESULTS AND DISCUSSION

Fabricated NW structures represented inversion n-channel FETs and were characterized using I-V curves and time traces of the drain current to extract information about single-trap dynamics. A scanning electron image of the silicon nanowire FETs studied is shown in Fig. 1. The experimental results obtained are treated theoretically by considering both classical and quantum distribution of the carriers in the channel. In order to model the transport properties of the liquid-gated Si NW FET, we started by describing the potential profiles of the structure.

A. Distribution of the potentials

The main physical processes taking place in the investigated device are sketched in Fig. 2: a schematic representation of the device structure and the distribution of the potentials over the layered structure of the sensor. Here, RE is the reference electrode, V_g is the gate voltage applied, Q_{dl}, Q_{fox}, Q_{box}, Q_{NW}, and Q_{Si} are the charges of the electrolyte double layer, FOX, BOX, NW, and Si substrate, respectively.

The balance equation for the potentials from Fig. 2 can be represented as follows:

$$V_g = \phi_{dl} + \phi_s + \phi_{fox} + \phi_{box} + \phi_d + \phi_{Si}, \tag{1}$$

where ϕ_{dl}, ϕ_{fox}, ϕ_{box}, ϕ_s, ϕ_d, and ϕ_{Si} are potentials of the double layer, FOX, BOX, NW surface, substrate Si depletion layer, and Si substrate, respectively. To estimate these potentials as well as the threshold voltage, V_{th}, and flat-band voltage, V_{FB}, we can use the following relations:[12,37–42]

$$V_{th} = V_{FB} + 2\varphi_F + \phi_d;$$
$$V_{FB} = E_{Ref} - \phi_s + \phi_{dl} - \frac{\Phi_{Si-}\Phi_{ox}}{q} + \frac{Q_{fox}}{C_{fox}} + \frac{Q_{box}}{C_{box}};$$
$$E_{Ref} = \phi_{bulk,sol} \approx 0; \quad \phi_{Si} = \phi_{bulk,Si} \approx 0; \quad \varphi_F = 2\varphi_T \ln\frac{N_A}{n_i};$$
$$\phi_d = \sqrt{\frac{4q\varepsilon_0\varepsilon_{Si}N_A\varphi_T}{C_{box}}}; \quad \varphi_T = \frac{kT}{q};$$
$$\phi_{dl} = 2\varphi_T\left(\frac{\varepsilon_w}{\varepsilon_r}\frac{N_{sol}}{K_{AK}^+ + H_s^+}\right); \quad \phi_{fox} = \frac{qN_{t,fox}}{C_{fox}};$$
$$\phi_{box} = \frac{qN_{t,box}}{C_{box}}; \quad \eta = 1 + \frac{C_d}{C_{fox}} \approx 1 + \sqrt{\frac{q\varepsilon_0\varepsilon_{Si}N_A}{2\varphi_T C_{fox}^2}}. \tag{2}$$

Here, φ_T is the thermal voltage; φ_F is the Fermi potential; $\phi_{bulk,sol}$ and $\phi_{bulk,Si}$ are the electric potentials of the bulk solution and the bulk silicon substrate; C_d, C_{fox}, and C_{box} are the capacitances of the silicon depletion layer, FOX, and BOX layers, respectively; ε_0, ε_{Si}, ε_{ox}, ε_w, and ε_r are the dielectric permittivities of free space, silicon, silicon dioxide, water and electrolyte, respectively; N_A is the doping acceptor concentration in both the Si substrate and Si-NW; n_i is the intrinsic carrier concentration in bulk silicon; K_{AK}^+ is the molar concentration of the cations, H_s^+ is the molar concentration of the hydrogen ions at the oxide surface; N_{sol} is the molar concentration of the solution; N_t is the trap surface concentration per unit area, and η is the factor of the transistor non-ideality.

The main processes take place in the NW channel so that we have to define the surface potential of the NW-FOX interface ϕ_s for the further calculations. It can be calculated using Eqs. (1) and (2) and the density of minority carriers per unit area

$$\phi_s = \varphi_T \ln\left(\frac{\eta C_{fox}\varphi_T N_A}{qtn_i^2}\right) + \varphi_T \ln\left\{\ln\left[1 + \frac{1}{2}exp\left(\frac{V_g - V_{th}}{\eta\varphi_T}\right)\right]\right\}. \tag{3}$$

Now having defined all the potentials in the structure, we consider classical and quantum approaches for calculating the concentration of charge carriers in the channel.

B. Distribution of the mobile charge carriers in the channel

1. General considerations

The statistical and dynamical behavior of the source-drain current is defined by the distribution of the concentration of the mobile charge carrier over the conducting channel. We consider the case of an inversion n-channel liquid-gated FET. The majority of processes in the structure are therefore determined by the electrons. Obviously, the concentration of mobile carriers in the channel depends on both the coordinate x (see Fig. 3) and the applied gate voltage. At the same time, the surface concentration is only dependent

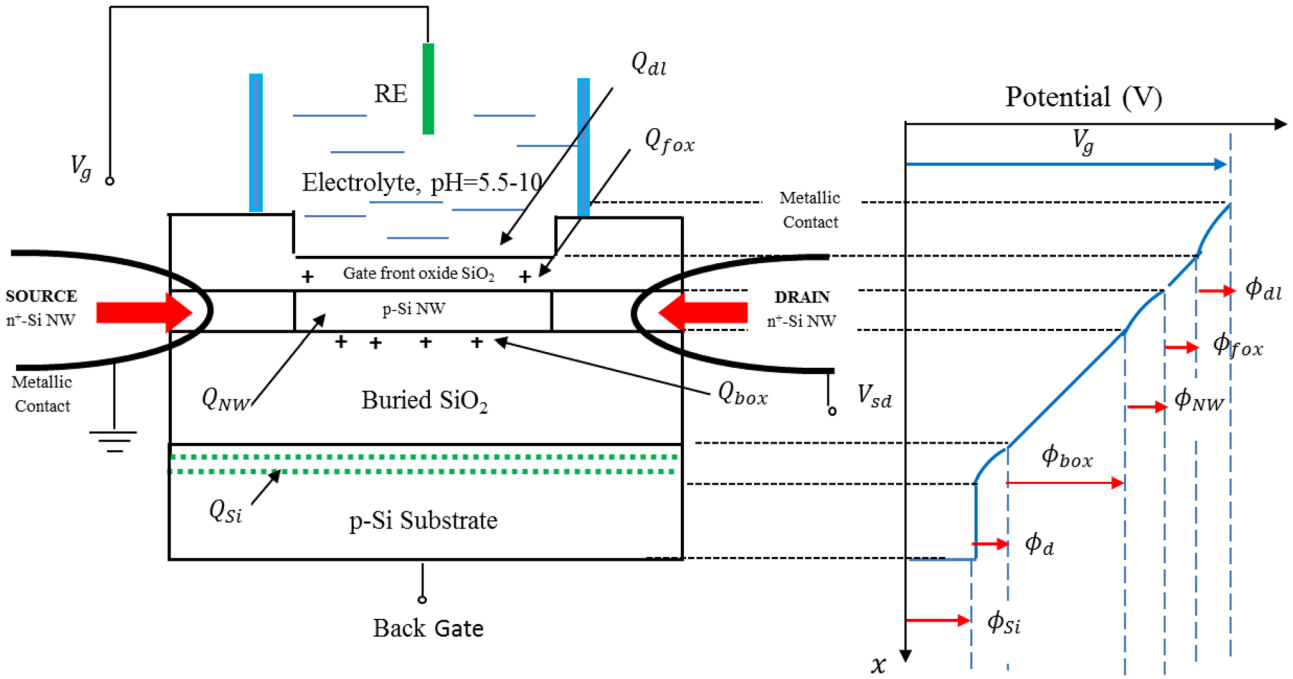

FIG. 2. Schematic of the liquid-gated FET sensor and potential profile. The layered structure consists of electrolyte, FOX, Si NW, BOX, and substrate. RE is the reference electrode, V_g is the gate voltage applied, Q_{dl}, Q_{fox}, Q_{box}, Q_{NW}, Q_{Si} are the charges of the electrolyte double layer, FOX, BOX, NW, and Si substrate, respectively.

on the gate voltage. Hence, the overall concentration can be presented as follows:

$$n(x, V_g) = n_s(V_g) \times f(x, V_g). \tag{4}$$

Here, $n_s(V_g)$ is the electron surface concentration per unit area at the FOX interface and $f(x, V_g)$ in [cm^{-1}] is the function which describes the charge carrier distribution in the $x - z$ plane of the channel (Figure 3).

The surface concentration can be described using the unified charge control model:[18]

$$V_g - V_{th} = \frac{q}{C_{fox}}(n_s - n_{s,t}) + \eta V_{th} \ln\left(\frac{n_s}{n_{s,t}}\right), \tag{5}$$

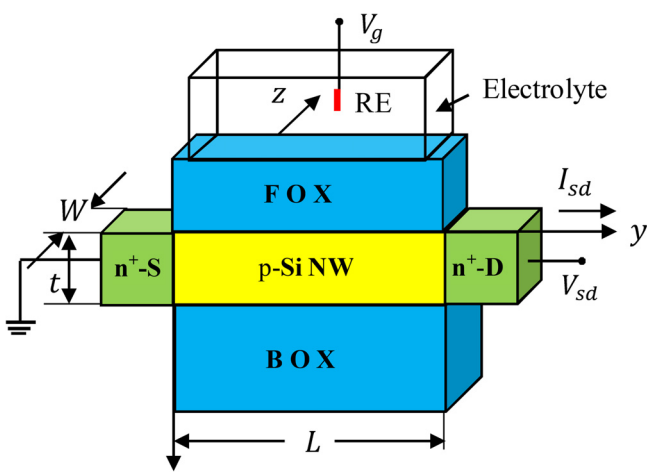

FIG. 3. Schematic of the channel between the FOX and BOX, source (S) and drain (D), t is the thickness of the NW active layer, W is the nanowire width, and RE is the reference electrode.

where $n_{s,t}$ is the surface density of electrons per unit area at the threshold voltage: $n_{s,t} = n_s$ at the $V_g = V_{th}$. It should be noted that the influence of the electrolyte is included in the V_{th} value (see Eq. (2)). The concentration $n_{s,t}$ can be expressed as follows:

$$n_{s,t} = \frac{\eta C_{fox} \varphi_T}{2q}. \tag{6}$$

Equation (5) has no analytical solution for n_s in terms of V_g. The following approximate solution is suitable for strong inversion and sub-threshold regimes:[41]

$$n_s = 2n_{s,t} \ln\left[1 + \frac{1}{2} exp\left(\frac{V_g - V_{th}}{\eta \varphi_T}\right)\right]. \tag{7}$$

After determining $n_s(V_g)$, we calculate the function $f(x, V_g)$ according to classical and quantum-mechanical (QM) approaches in order to evaluate the influence of peculiarities of the carrier distribution for both cases on the physical processes taking place in the channel.

2. Classical approach

In order to find $f(x, V_g)$ for the case of the classical approach, we use the following dependence of $n(x)$:[12]

$$n(x) = N_c exp\left[-\frac{E_c(x) - E_F}{kT}\right] = N_c exp\left[-\frac{(E_c - q\phi(x)) - E_F}{kT}\right] = n_0 exp\left[\frac{\phi(x)}{\varphi_T}\right]. \tag{8}$$

Here, N_c is the density of states in the conduction band of a semiconductor, E_c is the conduction band energy, and $\phi(x)$

is the contact potential at the FOX-NW interface. To determine $\phi(x)$, we have to solve the Poisson equation:

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_0\varepsilon_{Si}}. \quad (9)$$

Here, $\rho(x)$ is the space charge density for the fully ionized acceptor centers (boron in silicon)

$$\rho(x) = -q(N_A^- + n - p) = -qp_0\left[1 - exp\left(-\frac{\phi}{\varphi_T}\right) + \frac{n_0}{p_0}exp\left(\frac{\phi}{\varphi_T}\right)\right]. \quad (10)$$

Here n, p and n_0, p_0 are the concentrations of the carrier's non-equilibrium and equilibrium, respectively. We can use following boundary conditions to solve Eq. (9) (see Fig. 3):

$$x \to \infty => \phi \to 0, \quad x \to 0 => \phi \to \phi_s. \quad (11)$$

Using Eqs. (10) and (11), we obtain the following solution of Eq. (9):

$$\phi(x) = \left\{\phi_s + \frac{qn_0}{\varepsilon_0\varepsilon_{Si}}\left[1 - exp\left(-\frac{x}{l_s}\right)\right]\right\}exp\left(-\frac{x}{l_s}\right), \quad (12)$$

where

$$l_s = \frac{L_D}{1 + n_0/p_0}, \quad L_D = \sqrt{\frac{\varepsilon_0\varepsilon_{Si}\varphi_T}{qp_0}}, \quad (13)$$

L_D is the Debye screening length.

Then using expression for ϕ_s from Eq. (3) finally we have

$$f(x, V_g) = \frac{n_0}{n_s} \times exp\left\{\left[\ln\left(\frac{\eta\varphi_T C_{fox}N_A}{qtn_i^2}\right) + \ln\left[\ln\left(1 + \frac{1}{2}exp\left(\frac{V_g - V_{th}}{\eta\varphi_T}\right)\right)\right] + \frac{qt^2n_i^2}{\varepsilon_0\varepsilon_{Si}\varphi_T N_A}\right] \times exp\left(-\frac{x}{l_s}\right)\right\}, \quad (14)$$

where t is the thickness of the active layer of the SOI wafer for NW fabrication.

Figs. 4(a) and 4(b) show classical dependencies of functions $f(x, V_g)$ and $n(x, V_g)$, calculated using Eq. (14) and the parameters described below. For numerical computation, we use the following values, which correspond to the sample geometry and the parameters of the materials for the investigated structure: $\varphi_T = 0.026$ V, $N_A = 10^{15}$ cm^{-3}, $N_{sol} = 0.015$ mol/l, $K_{AK}^+ = 0.001$ mol/l, $t = 50$ nm, $W = 100$ nm, $L = 200$ nm, $d_{fox} = 9$ nm, $d_{box} = 500$ nm, $\varepsilon_{Si} = 11.6$, $\varepsilon_{ox} = 3.9$, $\varepsilon_w \approx 80$, $\varepsilon_r \approx 78$, $\varepsilon_0 = 8.85 \times 10^{-14}$ F/m, $m^* = 0.26m_0$, and $T = 297$ °C.

Now, we consider peculiarities of carrier distribution in the case of the quantum approach.

3. Quantum approach

The QM distribution of mobile carriers within the inversion layer in the NW FET can be obtained by self-consistently solving Schrödinger's and Poisson's equations.[43,44] The QM calculation gives the following result for the $f(x, V_g)$ function:

$$f(x, V_g) = |C_i|^2 \times \left|Ai\left[\left(x - \frac{E_i}{q\varepsilon}\right)\left(\frac{2m^*q\varepsilon}{\hbar^2}\right)^{\frac{1}{3}}\right]\right|^2, \quad (x \geq 0), \quad (15)$$

where

$$|C_i|^2 = \left[\int_0^\infty \left[Ai\left\{\left(x - \frac{E_i}{q\varepsilon}\right)\left(\frac{2m^*q\varepsilon}{\hbar^2}\right)^{\frac{1}{3}}\right\}\right]^2 dx\right]^{-1} \quad (16)$$

and

$$E_i = -\frac{(q\hbar\varepsilon)^{\frac{2}{3}}}{(2m^*)^{\frac{1}{3}}} \times s_i, \quad (17)$$

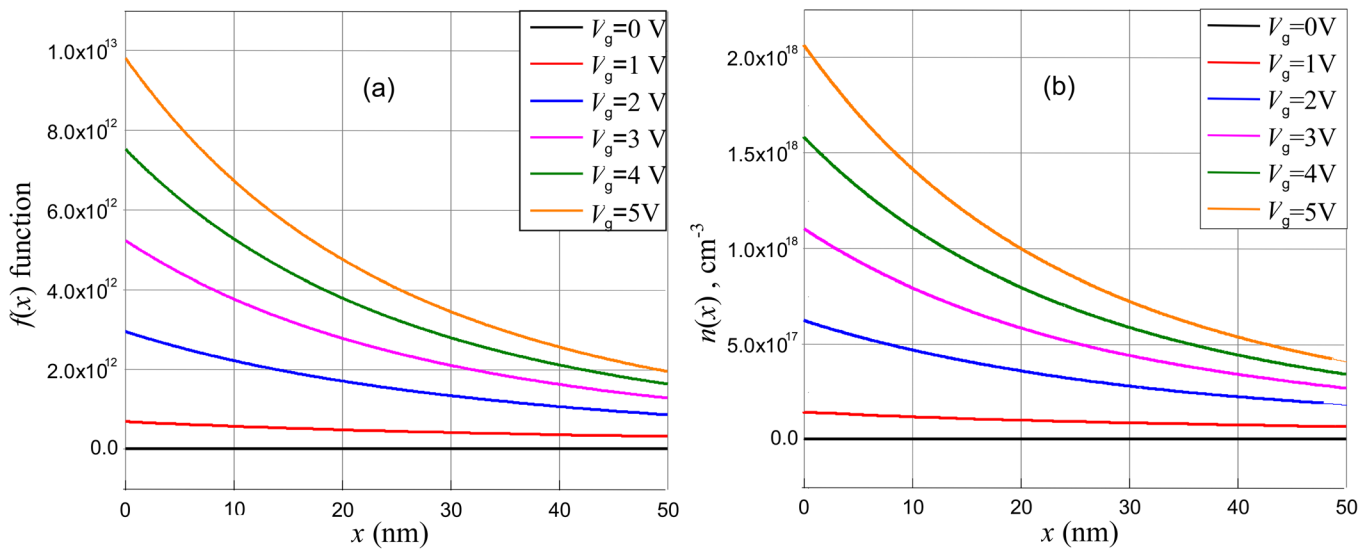

FIG. 4. (a) The function $f(x, V_g)$, which describes the carrier's distribution in the $x - z$ plane of the channel, and (b) the carrier concentration functions $n(x, V_g)$ calculated using Eqs. (14) and (4) for the several values of gate voltages at room temperature.

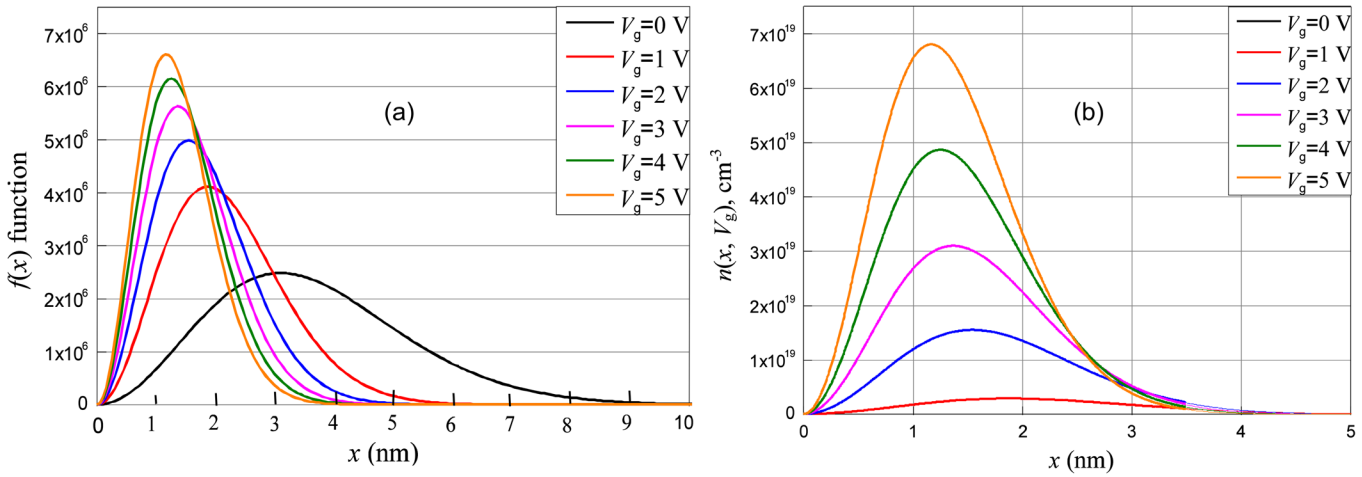

FIG. 5. (a) Calculated dependencies of function $f(x, V_g)$, which describes the carrier distribution in the x – z plane of the channel (Eq. (15)) and (b) carrier concentration $n(x, V_g)$, calculated using Eqs. (4), (7), and (15) for several values of gate voltages at room temperature.

$Ai(x)$ is the Airy function, m^* is the effective electronic mass, ε is the electric field in the NW channel, E_i is the quantized energy levels for electrons of the inversion channel in a triangular potential well,[45] s_i is the i-th solution of equation: $Ai(s) = 0$.

The surface electric fields are typically $\propto (10^4 \div 10^5)$, the energy levels $E_i \approx (0.03 \div 0.06)$ eV, and the typical value of s_i for silicon FETs is 2.338.[44]

Using Eqs. (4), (15), (16) and the parameters listed above for the investigated structure, we computed the dependencies of $f(x, V_g)$ and $n(x, V_g)$ for different gate voltages. Figs. 5(a) and 5(b) show the results obtained. As we can see, the concentration of the mobile charge carriers in the QM approach differs considerably from the classical case (Figure 4). The curves have well-pronounced peaks near the interface.

Such behavior is caused by the energy quantization of the electrons in the triangular potential well near the FOX-NW interface (see Eq. (17)). The growth of the gate voltage results in an increase in the maximal concentration and also in a shift of the maximum towards the FOX-NW interface. The majority of the electrons is located near FOX and occupies the region at a depth of 1–2 nm. More than 90% of the channel thickness does not contribute to the dynamical processes and is in a passive state. In the quantum case, a conception of the uniform inversion layer approximation becomes inappropriate. It should be emphasized that in the QM case, the maximal concentration values are one order of magnitude higher than in the classical distribution case. After defining the charge carrier distribution for classical and quantum cases, we can now evaluate the drain current of the Si NW transistor for both cases. Such theoretically calculated transfer characteristics can be compared with those obtained experimentally.

C. Drain current: QM and classical cases

The channel current consists of drift and diffusion components. The diffusion component is dominant in the sub-threshold mode and the drift component is dominant in the over-threshold region. The channel current can be calculated using the following equation:

$$I_d(y) = \mu_{ef} W \left[Q_{ch} \frac{dV}{dy} + \varphi_T \frac{dQ_{ch}(y)}{dy} \right]. \tag{18}$$

Here, Q_{ch} is the charge of the channel mobile carriers

$$Q_{ch} = \int_0^t \frac{1}{t} q n(x, V_g) dx. \tag{19}$$

The field caused by the applied gate voltage in the inversion layer of liquid-gated FETs changes the transport behavior of the charge carriers and results in more frequent scattering events than in the absence of the gate voltage. The carrier's mobility degrades as the result of scattering processes.[46–48] The mobility dependence on the transversal electric field (y direction) at the applied gate voltage was taken into account using the following empiric equation:[49]

$$(\mu_{ef})_x = \mu_0 - \theta(V_G + V_{th}), \tag{20}$$

where μ_0 is the low-field magnitude of the mobility and θ is the coefficient taken as 28 $cm^2/(V^2\ s)$.[49,50] Since the modeling and the measurements are performed for low drain biases in linear mode, the effect of the electron velocity saturation on the drain current can be neglected.

The influence of the FOX interface on the sub-threshold current of the transistor can be taken into account by introducing the capacity of the FOX interface traps into the quality factor η_1:[12]

$$\eta_1 = 1 + \frac{C_d + C_{D_{it}}}{C_{ox}}, \quad C_{D_{it}} = qD_{it}, \tag{21}$$

where $C_{D_{it}}$ is the capacity determined by the charge of interface states and D_{it} is the density of the interface traps.

The effect of series resistance is also taken into account in our calculation. A part of the drain voltage drops on the series resistance. This results in the lower effective drain bias applied to the channel. Such a consideration explains the sub-linear behavior of the transfer curves (at voltages above 1 V, Fig. 6) in a strong inversion regime. The real values of the current can be extracted using the following equation:

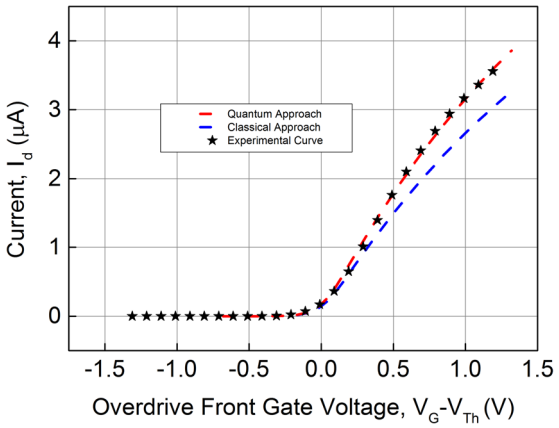

FIG. 6. Comparison of measured and calculated data obtained by classical and quantum approaches for drain current dependence on gate voltage.

$$I_{ds}(R_{ch} + R_c) = V_{ds}, \tag{22}$$

where R_{ch} and R_c are the channel and contact resistances, respectively. On the basis of our measurements of NW FETs with different lengths, we estimated the value for the series resistance to be 3.5 kΩ. Also for a further simulation taking the linear regime into account, the following can be assumed:

$$Q_{ch}(y) = Const, \quad \varepsilon(y) = Const = \frac{dV}{dy} \equiv \frac{V_{sd}}{L}. \tag{23}$$

Finally, the drift component of the drain current using Eq. (18) can be described by following equation:

$$I_{drift}(y) \approx \frac{qWn_sV_{ds}}{L}\left[(\mu_0 - \theta(V_G + V_{th})\right]\int_0^t f(x, V_g)dx, \tag{24}$$

where n_s is determined from Eq. (7).

Figure 6 shows the measured $I_{ds}(V_g)$ dependency for Si NW with a channel length of 200 nm and 100 nm width as well as the dependencies calculated according to Eq. (24) for both the classical and quantum-mechanical approaches using corresponding $f(x, V_g)$ functions.

The shapes of measured and calculated I-V characteristics are in good agreement in both sub-threshold and over-threshold regions due to taking into account effects of contact resistance, mobility degradation, scattering on the surface states. For the case of quantum approach, the value of D_{it}, estimated from fitting the sub-threshold current is 4×10^{12} $cm^{-2}eV^{-1}$ and the value of mobility is $\mu_0 = 250\,cm^2V^{-1}s^{-1}$, respectively. It should be emphasized that value of mobility for the case the classical distribution of mobile carriers would be higher than in the case of quantum-mechanical one, due to difference in overall quantity of carriers in the inversion layer. This result stresses the importance of charge carrier distribution in the NW channel of the FETs. The dynamical behavior of the drain current for classical and quantum approaches will be analyzed below.

D. Random telegraph signal behavior of drain current

Capture and emission processes of the carriers from the channel to the oxide trap (or vice versa) result in discrete modulation of the channel current, demonstrating random telegraph signal fluctuations. RTS is the result of the decomposition of the 1/f spectrum into individual fluctuating components. RTS noise can be a useful tool for the characterization of traps for energy and spatial distribution aspects. Using RTS, we can determine the trap position near the interface. A single RTS can be considered as one of a number of Lorentzian components of the flicker noise and can be related to fluctuations in channel carrier number and mobility.

According to the united flicker noise model, the capture of channel carriers by the oxide traps induces the carrier density fluctuations in the channel (also known as the number fluctuations).[51] On the other hand, mobility fluctuations can be considered to be due to Coulomb scattering of carriers. Both these sources contribute to the drain current noise. It is known that the 1/f low-frequency noise level decreases in smaller channel diameters Si NW FETs.[52] This channel diameter-dependent noise behavior is clarified in terms of the effective oxide trap density and the fraction of electrons near the Si-SiO_2 interface.

It should be noted that randomness in the distribution of traps in the oxide has a significant influence on the capture and emission times of the channel carriers to/on the traps as well as for the further formation of RTS and flicker noise.[53] In small-area devices, a two-level fluctuation of drain current, known as RTS noise, is often registered.[31] When the channel area of NW FETs is smaller than 1 μm^2, only a single trap in the gate may have a high impact on the conductivity of the entire channel. Fig. 7 shows the time dependence of the measured drain current in the form of RTS fluctuations in the liquid-gated FET sample. We show below that peculiarities in the distribution of charge carriers in the channel may result in a difference in capture time values.

As is known, the capture and emission times of electrons on/from the traps in the oxide layer are defined as follows:[31]

$$\tau_c = \frac{1}{\sigma_n \upsilon_{th} n(x, V_g)}, \quad \tau_e = \frac{exp(E_t/kT)}{\sigma_n \upsilon_{th} n_1}, \tag{25}$$

where σ_n is the capture cross-section for electrons, n_s is the surface concentration of the mobile charge carriers on the

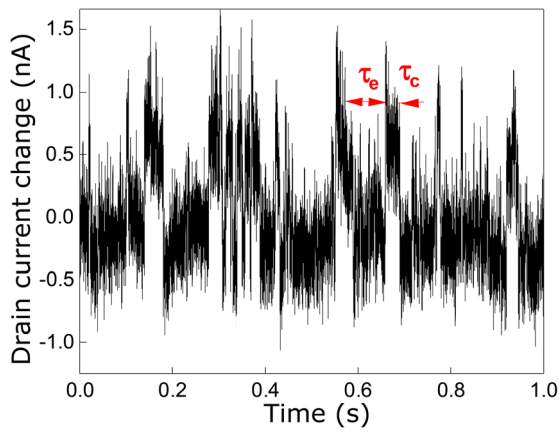

FIG. 7. Drain current demonstrates RTS behavior at gate voltage equal to 1.5 V.

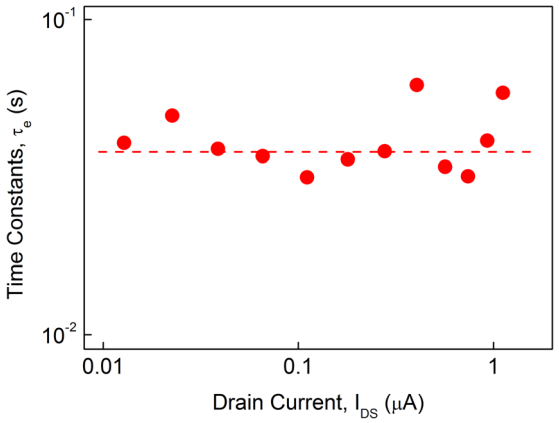

FIG. 8. Measured emission time of the registered RTS plotted versus the drain current. Red line is merely a guide for the eyes.

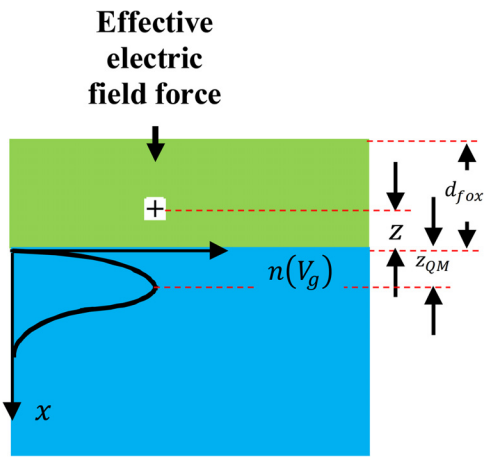

FIG. 9. Schematic of the FOX-NW interface with the single trap, where z stands for distance between trap and FOX/NW interface, z_{QM} stands for distance between maximum concentration in the channel and FOX/NW interface.

interface FOX-NW, E_t is the trap activation energy, n_1 is the Shockley-Read stat-factor (density of electrons in the conduction band when Fermi level coincides with E_t). It should be noted that $\sigma_n = \text{const}$, because according to our measurements, emission time does not depend on drain current (see Fig. 8). As is shown in Ref. 54, a strong (exponential) dependence of the cross-section on the field in the oxide is observed. This can be presented as follows:[54]

$$\sigma_n = \sigma_{n0} exp\left(\frac{V_g - V_{th}}{z\varepsilon_{cr}}\right). \tag{26}$$

Here, σ_{n0} is the low-field magnitude of the cross-section and ε_{cr} is the critical electric field in the oxide layer.

In the case of the quantum approach for calculating the concentration of the charge carrier, the maximum concentration in the inversion layer shifts towards the NW-FOX interface with increasing applied gate voltage (see Fig. 5(b)). Therefore, the trap capture cross-section area increases and consequently increases the probability of capturing the carriers to the oxide trap. In such a case, the capture time decreases. Double and Helmholtz layers were taken into account in the case of the electrolyte gate. Quantization results in the shift of the maximum electron density from the FOX interface (see Fig. 5(b)). This is equivalent to increasing the FOX effective thickness.

We assume that carriers tunnel to the trap from the conducting channel. It is known that in such a case, τ_c increases exponentially with z[55] (see Fig. 9) and τ_c in Eq. (25) will be multiplied by the factor $e^{\gamma z}$, where z is the trap depth, and γ is the attenuation coefficient of the electron wave function in the oxide layer

$$\gamma = \frac{4\pi}{h}\sqrt{2m^*_{ox}\Phi_B}, \tag{27}$$

and for silicon dioxide it equals $10^8\,\text{cm}^{-1}$, Φ_B is the tunneling barrier height for the carriers at the interface, m^*_{ox} is the electron effective mass in the oxide, which should be taken into account as an energy-dependent value:[56]

$$\frac{m^*_{ox}(E_0)}{m^*_{ox}(0)} = 1 + \sum_{i=1}^{3} a_i E_0^i \tag{28}$$

with $a_1 = -0.178\,\text{eV}^{-1}$, $a_2 = 0.025\,\text{eV}^{-1}$, $a_3 = -0.0023\,\text{eV}^{-1}$. E_0 is the energy distance from the bottom of the conduction band to the valence band.

Multiplying τ_c by the $e^{\gamma z}$ term and then using Eqs. (25) and (26) we can find

$$\frac{\tau_c}{\tau_e} = \frac{n_1}{n(x, V_g)} \times exp\left(\gamma z - \frac{V_g - V_{th}}{\varepsilon_{cr} z} - \frac{E_t}{kT}\right). \tag{29}$$

For the case of traps in the gate dielectric (see Fig. 9), we can assume that

$$\varepsilon_{cr}(d_{fox} - z) = V_g - V_{th}, \quad z = d_{fox} - \frac{V_g - V_{th}}{\varepsilon_{cr}}, \quad \frac{z}{d_{fox}} = 1 - \frac{V_g - V_{th}}{d_{fox}\varepsilon_{cr}}. \tag{30}$$

As is shown above, the majority of charge carriers are located at a distance of 1–2 nm from the front oxide interface and therefore, the probability of the electron tunneling to the oxide trap is decreased (Fig. 10). In general, the carrier tunneling rate of the classical case, where carriers tunnel directly from the interface, should be corrected by a

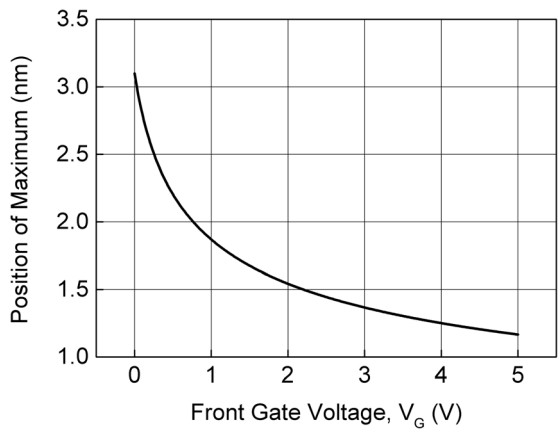

FIG. 10. Position of the maximum electron concentration in the QM approach extracted from Figure 5(b) and plotted as a function of the gate voltage.

tunneling factor from the maximum of concentration to the interface, which can be given by[57,58]

$$T = T_0 e^{-\beta z_{QM}}, \tag{31}$$

where T_0 and β are constants. Assuming that tunneling factor T is equal to 1 at the interface ($z_{QM} = 0$), we obtain $T_0 = 1$.

It should be noted that at the inversion regime the Fermi energy E_F is already quite far from the trap activation energy E_t, therefore small changes of gate voltage cannot significantly change the Shockley-Read stat-factor and consequently the τ_e. On the other hand, the electrons captured in the trap are less likely to jump off and return to the region, which is fully filled by electrons. This also follows from measurement data (see Figure 8). Further analysis of the electron capture time behavior will be performed for the fixed trap assuming that $z = const$ and $E_t \approx const$.

Let us now consider Eq. (25).

For the classical case, $n_s(V_g)$ is the (maximal) surface concentration at the FOX-MW interface and is defined by Eq. (8) with the substitution of $\phi(x)$ to the ϕ_s (see Eq. (3)). In this case, we have

$$\left(\frac{\tau_c}{\tau_e}\right)_{Cl} = \frac{q n_1 t d_{fxo}}{\varepsilon_0 \varepsilon_{ox} \eta \varphi_T} \frac{exp\left(\gamma z - \dfrac{V_g - V_{th}}{\varepsilon_{cr} z} - \dfrac{E_t}{q\varphi_T}\right)}{\ln\left[1 + \dfrac{1}{2} exp\left(\dfrac{V_g - V_{th}}{\eta \varphi_T}\right)\right]}. \tag{32}$$

For the quantum-mechanical case, we take into account both the distribution of the electron concentration in the channel and the tunneling of electrons from the maximum concentration region. The maximum of the distribution is located near the FOX-NW interface at a distance of z_{QM} (Fig. 9), which depends on gate voltage (Fig. 10). It should be noted that shift effect of the charge centroid was considered in Ref. 59. The effect results in change of the equivalent electrical oxide thickness, which determines the direct current in strong inversion for the FET. This was confirmed by simulation results and direct C-V measurements data. We applied similar consideration, therefore instead of n_s, we use $T \times n_s$ and finally obtain

$$\left(\frac{\tau_c}{\tau_e}\right)_{QM} = \left(\frac{\tau_c}{\tau_e}\right)_{Cl} \times \frac{1}{T_0} exp(\beta z_{QM}). \tag{33}$$

Note that the graphical approximation of the curve in Figure 10 is as follows:

$$z_{QM} \approx 1.21 + 1.64 \times exp(-0.88 V_g)\,\text{nm}. \tag{34}$$

Fig. 11 shows the ratio of capture and emission times obtained experimentally and compared with the calculated curves, using the classical and the QM approaches. Note that in order to plot the theoretical curves, we use $\varepsilon_{cr} \approx 4.5 \times 10^6 \text{V/cm}$ and $\beta \approx 0.1\gamma$ cm (see below).

The relation between depths of trap occurrence in the QM approach (z_{trap}^{QM}) and classical approach (z_{trap}^{Cl}) is as follows:

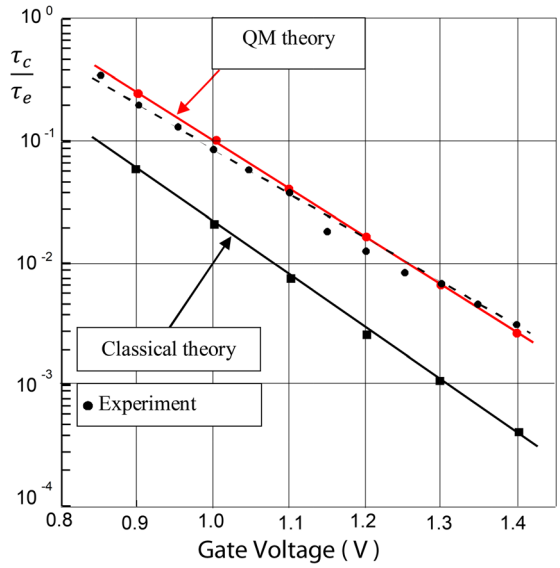

FIG. 11. Measured data obtained from the time dependence of drain current change and calculated dependencies of τ_c/τ_e on the gate voltage.

$$z_{trap}^{Cl} - z_{trap}^{QM} = \beta t_{ox} \frac{kT}{q} \frac{dz_{QM}}{dV_G}, \tag{35}$$

where

$$z_{trap}^{Cl} = -t_{ox} \frac{kT}{q} \frac{dln\left(\dfrac{\tau_c}{\tau_e}\right)_{Cl}}{dV_G}, \quad z_{trap}^{QM} = -t_{ox} \frac{kT}{q} \frac{dln\left(\dfrac{\tau_c}{\tau_e}\right)_{QM}}{dV_G}. \tag{36}$$

Calculated values of the depths of trap based on Eq. (36) and Fig. 10 are as follows:

$$z_{trap}^{Cl} = 2.3\,\text{nm}, \quad z_{trap}^{QM} = 2.0\,\text{nm}. \tag{37}$$

The difference (quantum correction) between QM and classical approaches is equal to

$$\beta t_{ox} \frac{kT}{q} \frac{dz_{QM}}{dV_G} = 0.3\,\text{nm}. \tag{38}$$

It is defined by the parameter β, connected with the effects of quantization and different transport distances for the carriers from the maximum of carrier distribution in the inversion layer to the trap and the Si/SiO_2 interface. The maximum moves away from the interface into the depths of the silicon nanowire. This significantly weakens the tunneling effect by a factor of approximately 10 times according to our fitting.

We fitted the QM curve to the experimental data and this enabled us to estimate that the trap is located near the FOX/NW interface at the distance $z \approx 2$ nm. An analysis of the measured data using the method described in Refs. 51, 60–62 shows that trap has a repulsive character due to the very small capture cross-section of $10^{-20}\,\text{cm}^2$, and that its activation energy is equal to 0.47 eV. It should be noted that the capture cross-section in the case of the dielectric is typically several orders of magnitude smaller than for the bulk Si

material trapping. This can be explained by the difference in the distance to be covered by the electron to become captured on the trap in the dielectric or in the Si material. In order to plot the theoretical curves in Fig. 11, we used $T_0 = 1$ and assumed that the Shockley-Read stat-factor is determined by the boron acceptor's atoms in p-Si NW with a Coulomb blockade energy of 0.045 eV. At the same time, the effects of ions or pH should be also taken into account in the result. Impact of the ionic solution strength on the noise in the NW channel has been investigated in Ref. 17. The RTS time constants change with variation of the pH value in a liquid-gated transistor because capture and emission times are functions of the carrier concentration as well as the drain current.[63]

It should be emphasized that the classical solution (32) gives a different ratio from that obtained in the QM approach. Such behavior can be explained by the fact that in the QM case electrons should also reach the interface before being captured in the trap. Therefore using the QM treatment will always give lower values (15%) for the trap depth than the classical approach. This result proves the importance of considering the quantization in the channel of liquid-gated NW FETs in order to determine the correct positions of the traps in the dielectric layer.

IV. CONCLUSION

The RTS was registered and used to analyze transport behavior within the framework of QM and classical models. In order to explain the capture time dynamics, we consider tunneling of the mobile carriers from the channel to the oxide single trap. Classical and QM models of electron charge distribution were applied to find an appropriate description of the physical phenomena in the electrolyte-gated Si NW FETs. The classical calculation approach gives a charge carrier distribution with a maximum at the FOX/NW interface, whereas in the QM approach the maximum concentration is displaced away from the interface. The value of the electron concentration increases with increasing gate voltage and its maximum relocates closer to the FOX/NW interface. The majority of the electrons concentrate near the FOX surface and occupy the region of 1–2 nm. The fact should be taken into account in the design of submicron devices.

It is shown that the difference between change carrier distributions in the classical and QM cases determines FET behavior.

The behavior of the ratio of the capture time to emission time dependence on gate voltage obtained theoretically using the quantization and tunneling effects is in good agreement with the measured data. Using capture and emission times measured from $I_{sd}(t)$ dependencies, we identified the position of the oxide trap. Analysis shows that the single trap has a repulsive character, located near the oxide surface at a distance $\approx$2 nm. Its activation energy is equal to $\approx$0.47 eV and the cross-section area of the trap is close to 10^{-20}cm^2.

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