Dynamical Exascale Entry Platform: the DEEP Project

DEEP is one of the three Exascale projects funded in 2011 by the EU 7th framework program. The DEEP project will last three years starting in October 2011 and is developed in a collaboration constituted by 16 partners from 8 different countries, coordinated by the Research Centre Jülich. DEEP aims at developing a prototype Exascale-enabling supercomputing platform consisting of two parts: a Cluster part based on multi-core-chips with InfiniBand interconnect, and a Booster part based on Intel many-core MIC processors connected through a Terabit EXTOLL network. This Cluster-Booster Architecture (Fig. 1) will serve as proof-of-concept for a next-generation 100 PFlop/s PRACE production system. Furthermore, the innovative hot water cooling concept of DEEP has the potential to improve the power efficiency of HPC systems. A novel open source system software stack (Fig. 2) will be developed for cluster management and resource allocation, based on the ParaStation cluster management software from ParTec. ParaStationMPI will be extended with communication functions to connect the Cluster and Booster via InfiniBand and the interconnection architecture EXTOLL, developed by the University of Heidelberg.

Figure 1: Sketch of the DEEP Architecture (CN=Cluster Node, BN=Booster Node, BI=Booster Interface)

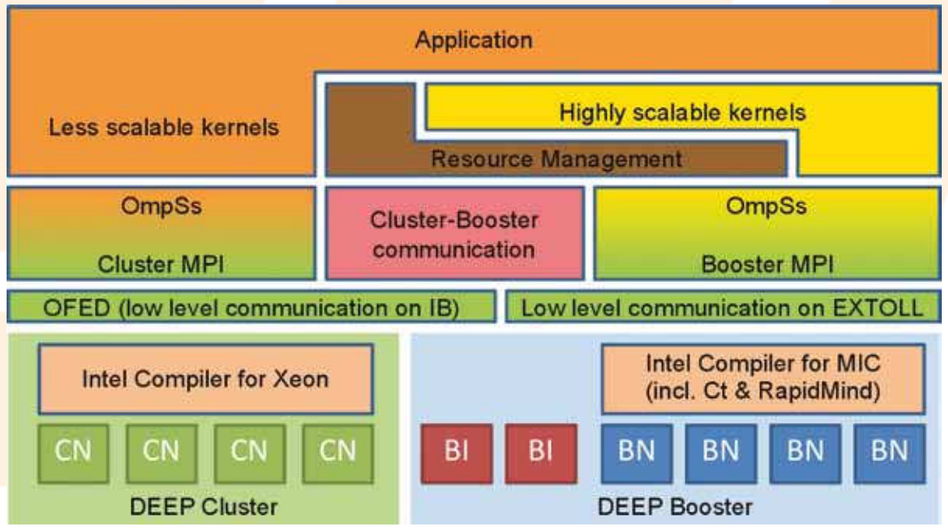

Figure 2: Software layer for programming environment

In addition, the programming environment OmpSs (OpenMP Superscalar) of the StarSs family from Barcelona Supercomputing Centre will be ported to the DEEP System. Adapting mathematical libraries and performance analysis tools such as Scalasca, provided by the Jülich Supercomputing Centre, will complete the platform to program applications, enabling unprecedented scalability on millions of cores. Representative HPC application codes from Health and Biology, Climatology, Seismic Imaging, Industrial Design, Space Weather, and Superconductivity will be optimized on DEEP. The scalability of the DEEP hardware-software concept shall be demonstrated with respect to the generic multi-scale, adaptive grid, and long-range force parallelization models underlying the application codes. Altogether, the DEEP concept allows an extrapolation to millions of cores for future systems, with the potential to achieve Exascale between 2018 and 2020.

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