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Read-Out Electronics for Digital Silicon Photomultiplier Modules

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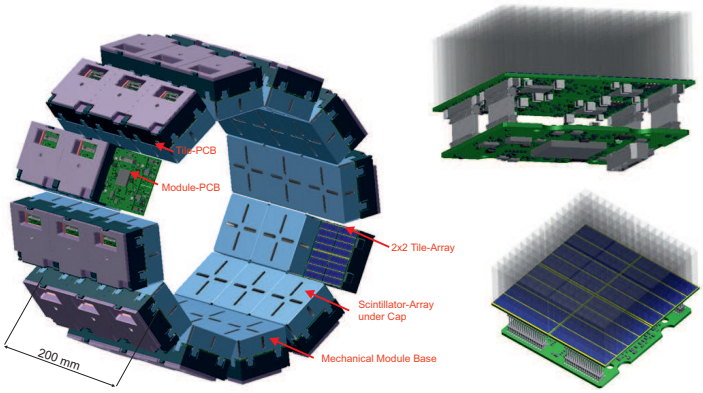
Introduction

A new kind of a PET-Scanner (PET = positron emission tomography) for phenotyping in plant research is developed as a joint project of the Forschungszentrum Jülich and Philips Digital Photon Counting (PDPC). This scanner will utilize digital silicon photomultipliers (dSiPM- called Digital Photon Counter (DPC) by Philips) for the very first time in order to improve on spatial resolution, sensitivity and count rate behavior of such a PET system. To acquire a detailed knowledge of the operation of the DPC, a test-facility for these new photo detectors has been installed at the central institute of engineering, electronics and analytics (ZEA-2 electronic systems) in order to determine the different usage modes of these sensors with regard to their future use as scintillation detectors in a PET-Scanner. The work described here has its focus on the development of a fast read-out electronics for the used photo sensors type DPC3200-22-44. In order to accomplish the high data rates in PET, a fast USB 3.0 interface has been used. All the necessary processing and data handling has been implemented on a state of the art FPGA.

phenoPET Concept

The PET under development will be based on DPC-Modules by Philips, with each module consisting of a 2x2 TILE array of DPC3200-22-44 dSiPMs. The DPC3200-22-44 dSiPM itself is a array of 64 pixel fully digital silicon photomultipliers, each containing 3200 Geiger-Mode APDs (GAPDs). As the PET will have an optical FOV of 18cm X 18cm, the scanner will be build as a stack-up of three rings with 12 modules each.



This picture shows the complete PET-Scanner on the left and four DPC3200 arrays attached to the module board and coupled to crystal arrays on the right

Photon Counting Pixel

In order to determine the maximum data rates it is necessary to calculate the number of pixels in this scanner. The following table shows the amount of used SiPM channels. The usage of fully digital photon counters (DPC) is one of the great benefits in this scanner.

Tile				64 pixel
Module			4 tiles	256 pixel
Ring		12 modules	48 tiles	3072 pixel
Scanner	3 rings	36 modules	144 tiles	9216 pixel

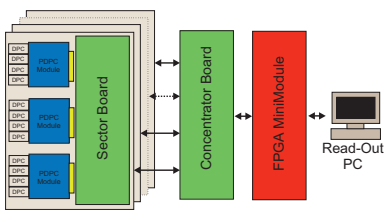
Each TILE is capable of achieving a maximum event rate of 672 events in a 327 µs frame. However the events are read out by the connected electronics every 327 µs and consist of 11 Bytes containing pixel and timestamp information. Based on this information one can calculate the maximum data rate for each TILE:

$$data\ rate = \frac{672\ events}{327\mu s} \cdot 11\ Byte \sim \frac{2 \cdot 10^6\ events}{s} \cdot 11\ Byte \sim \mathbf{22\ MByte/s}$$

To handle the high amount of data, a preprocessing of the incoming event data is already performed inside the PDPC module FPGA.

Architecture of Read-Out-Electronics

The data acquisition is subdivided into several devices. The acquisition of the incoming photon counts is already happening inside the PDPC module FPGA, while the data sorting and processing will be performed inside a central concentrator board FPGA. The generated sensor data will be routed to a sector board after it is processed by the PDPC module FPGA. This module interconnects to the concentrator board which is gathering all signals of the 36 modules and interfaces it to a FPGA. The FPGA firmware handles the event sorting as well as the image preprocessing, furthermore it provides interconnections to the read-out-PC.



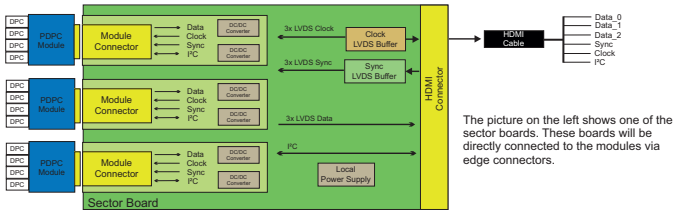
The hardware is divided into the following blocks:

- **PDPC Module:** Developed by PDPC, Read-Out of TILE-Data, preprocessing and setup of sensor device, Power Supply for TILEs
- **Sector Board:** Physical connection of 3 PDPC Modules, Clock- and Sync-Buffering, PowerSupply for PDPC Modules, merge into HDMI
- **Concentrator Board:** Physical connection of 12 sector boards (36 PDPC modules), Clock- and Sync-Buffering, FPGA interconnect

DAQ Hardware-Blocks

Sector Board:

Three PDPC modules are connected to a so called sector board. This board holds DC/DC converters in order to provide the proper voltages for the digital logic and for the GAPDs. The signals of three modules are clustered to a HDMI 1.4a cable, providing 5 differential pairs and I²C on one cable. High precision LVDS Buffers are used to distribute clock- and synchronization-signals. The scanner will utilize 12 sector boards in total .

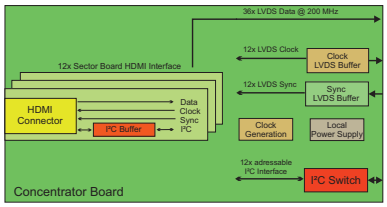


The picture on the left shows one of the sector boards. These boards will be directly connected to the modules via edge connectors.

Concentrator Board:

The system will hold one so called concentrator board. This board bundles the data-lines of the 12 incoming HDMI cables towards the FPGA Mini module. Moreover, here also the global clock is generated and distributed to both the MiniModule and the PDPC modules. Furthermore the incoming Sync signal is buffered and spread out to the the 12 sector boards.

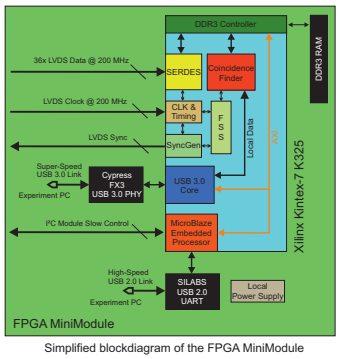
The slow-control commands to all the modules are transfered in the I²C standard from the FPGA MiniModule to the PDPC modules. To extend the adress area of the PDPC modules and to prevent the bus from reflections an active I²C switch as well as I²C buffers are implemented.



The picture on the left shows one of the concentrator boards. This board is directly connected to the MiniModule FPGA and provides physical interconnection to the HDMI cables.

FPGA MiniModule:

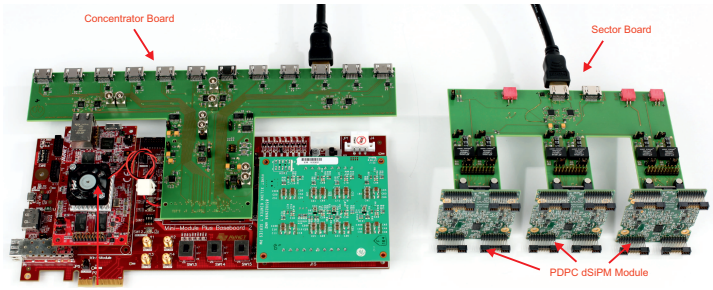
The main data processing is performed inside a XILINX KINTEX-7 FPGA. We use a so called MiniModule from AVNET as a development system. In the later hardware setup this module will be directly placed onto the concentrator board. Right now the MiniModule is connected to the concentrator board via a FMC connector. The FPGA does all the necessery timing corrections to the LVDS signals and provides proper synchronization signals to the modules so that highly accurate time stamps can be generated. An image preprocessing algorithm using timing and energy information is currently under development and will be implemented inside the FPGA. A high-speed USB 3.0 serial link providing a high bandwidth is used as a fast digital link to the read-out-PC. Commands from the read-out-PC are transferred over a USB to UART link directly into an implemented MicroBlaze embedded processor. The MicroBlaze contains routines to initiate transfers and to handle the slow control, therefore the embedded core is connected via an AXI-Interface to the logic.



Simplified blockdiagram of the FPGA MiniModule

Status of Development

The first PCB's are assembled and the firmware development of the KINTEX-7 FPGA on the MiniModule is ongoing. It has already been shown, that the data transfer from the module FPGA towards the concentrator FPGA is working at rates of up to 600 MHz. The MicroBlaze embedded processor design has been implemented and is beeing tested. The USB data transfer is working under Windows as well as under Linux. Future work will concentrate on the parametrization of the sensor device with the here presented hardware, as well as developments on the coincidence algorithm.



Development status of the read-out-hardware in Jülich