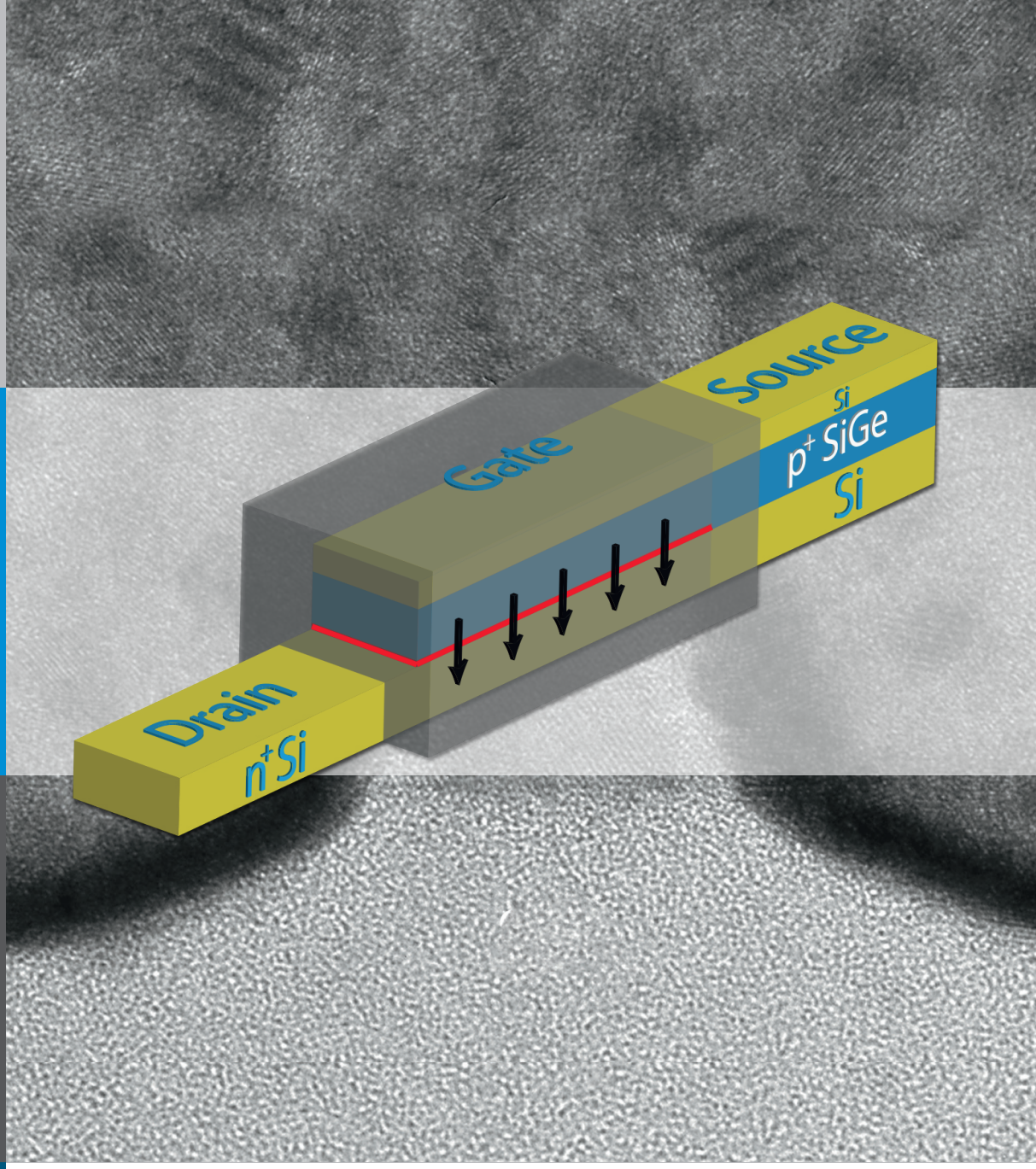

Strained Silicon and Silicon-Germanium Nanowire Tunnel FETs and Inverters

Simon Richter

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Abstract

Reducing power consumption is an important issue for integrated circuits in portable devices relying on batteries and systems without external power supply. Scaling of the supply voltage V_{DD} in integrated circuits is a powerful tool for reducing the power consumption, due to the quadratic dependence on V_{DD}. MOSFETs, however, exhibit a fundamental limitation for the drain current increase per applied gate voltage difference. The tunnel field-effect transistor (TFET) provides the ability for beating this limitation, thus offering a performance advantage over MOSFETs for ultra-low V_{DD}.

In this work, TFETs are fabricated with respect to design rules deduced from basic physical relations for the tunneling probability. The aim is to increase the tunneling probability in order to obtain higher drive currents in the devices. A tri-gated nanowire design in combination with a high-κ/metal gate stacks is employed in order to increase the electrostatic gate control. Devices are fabricated on tensile-strained Si on insulator (SSOI) as well as compressively strained SiGe on SOI substrates. Fabricated devices reveal enhanced current for smaller band gap and effective carrier mass in those materials. In order to further increase I_{ON} and prevent I_{OFF} degradation occurring in small band gap TFET homostructures, a NW based heterostructure design with enlarged tunnel junction area is conceived and fabricated. Device characterization of this structure reveals superior performance and large I_{ON}/I_{OFF} ratio. TCAD simulations demonstrate how the structure could be adapted to utilize line tunneling in an inverted source region for further current improvement.

SSOI NW TFET characteristics are investigated and compared to MOSFETs fabricated with analog processing. Temperature dependence of TFET characteristics is analyzed and hot carrier effects in the tunnel junction are revealed by charge pumping measurements. Furthermore, the feasibility of TFETs for logic application is studied by fabrication of inverter structures. A comparison of TFET and MOSFET inverters reveals degradation of the voltage transfer characteristics caused by the ambipolarity of TFETs. An emulated TFET structure based on the fabricated SiGe/Si heterostructure with reduced ambipolarity proves to prevent output degradation of the TFET inverter and demonstrates sufficiently high noise margins down to ultra-low supply voltages.

Low frequency noise measurements are performed on SSOI NW TFETs and MOSFETs revealing a dominant noise contribution by the tunnel junction in TFETs. The confined tunnel junction area provides a higher probability for RTS noise generation.

Kurzfassung

Die Reduzierung des Energieverbrauchs ist ein wichtiges Thema für integrierte Schaltungen in mobilen Geräten und Systemen ohne externe Stromversorgung. Durch die quadratische Abhängigkeit der Leistungsaufnahme von V_{DD}, bietet die Skalierung der Versorgungsspannung eine effektive Möglichkeit zur Reduzierung des Energieverbrauchs. MOSFETs besitzen eine physikalische Begrenzung für die mögliche Erhöhung des Drainstroms bezogen auf eine angelegt Gatespannungsdifferenz, die wiederum ein Skalierung von V_{DD} begrenzt. Der Tunnel-Feldeffekttransistor (TFET) besitzt diese Begrenzung nicht und bietet daher Vorteile gegenüber dem MOSFET bei sehr kleinen Versorgungsspannungen.
In dieser Arbeit werden TFETs hergestellt und optimiert nach Designkonzepten basierend auf physikalischen Modellen für das Band-zu-Band-Tunneln. Ziel ist es, die Tunnelwahrscheinlichkeit zu erhöhen, um höhere Ströme in den Bauelementen zu ermöglichen. Die TFETs basieren auf Nanodrähten, die an drei Seiten von einem High-κ/Metall-Gate umgeben sind. Diese Struktur erhöht die elektrostatische Gatekontrolle. Die Bauelemente werden auf verspanntem Silizium auf Isolator (SSOI) und Silizium-Germanium auf SOI Substraten prozessiert. Die Bauelemente zeigen eine Zunahme des Tunnelstroms mit abnehmender Bandlücke und effektiver Masse der Ladungsträger. Um den An-Strom weiter zu erhöhen und eine Vergrößerung des Aus-Stromes, wie sie bei Homostruktur TFETs mit kleiner Bandlücke auftritt, zu verhindern, wird ein Heterostruktur TFET basierend auf dem Nanodrahtdesign entwickelt und hergestellt. Dieser Heterostruktur TFET zeigt weiter verbesserte An-Ströme bei reduzierten Strömen im Aus-Zustand.
Die Eigenschaften der SSOI Nanodraht TFETs werden mit äquivalent prozessierten MOSFETs verglichen. Die Temperaturabhängigkeit der TFETs wird charakterisiert und eine Verschlechterung des Gatedielektrikums durch hochenergetische Ladungsträger im Tunnelkontakt wird mittels der "Charge Pumping"-Methode nachgewiesen. Des Weiteren werden die Eigenschaften von TFETs in Bezug auf Logikschaltungen anhand von Invertern analysiert. Der Vergleich von TFET und MOSFET Invertern zeigt, dass sich die ambipolaren Eigenschaften der TFETs negativ auf die Spannungstransfercharakteristik des Inverters auswirken. Ein emulierter TFET Inverter basierend auf der hergestellten SiGe/Si Heterostruktur mit reduzierter Ambipolarität verhindert dies und zeigt gutes Schaltverhalten bei sehr kleinen Spannungen.

Die Charakterisierung des Niederfrequenzrauschens in TFET und MOSFET zeigt, dass der Tunnelkontakt im TFET das Rauschen dominiert. Der örtlich eingeschränkte Tunnelkontakt trägt zu einer höheren Wahrscheinlichkeit für das Auftreten von RTS-Rauschen bei.

Contents

1 Introduction

In 2013, 4. 5 billion people worldwide are in possession of a mobile subscription, which means that 63% of the world population uses mobile communication [110]. In the most recent quarter, the number of subscriptions increased by over 100 million. Nowadays, more than half of the sold mobile phones are smartphones, that have caused the mobile data traffic to increase by about 80% in the past year. Current predictions assume an increase of mobile data traffic by a factor of 10 until 2019. The evolution of smartphones and the need for increasing computational speed in the palm of our hand, however, causes a trade-off with battery life time, which is down to one or two days for a current smartphone under typical usage. Thus, power consumption of mobile devices becomes a growing issue.

Power consumption is also an issue for new electronic systems, such as sensors with application in industry, medicine and every day products, running without external power supply. For those devices, that rely for example on photo voltaic, thermoelectric generators or external radio frequencies (RFID) as power supply, low power consumption of the integrated circuits is essential.

Today, semiconductor based processors are utilized in almost every portable electronic device. These processors rely on metal-oxide-semiconductor field-effect transistors (MOSFETs) as switches for performing logic operations. MOSFETs allow for switching current by applying a voltage to a control gate. In contrast to an ideal switch, which should have zero current in the off-state and switch to the on-state instantaneously, a finite current flows in the off-state of a MOSFET and a certain voltage difference, the supply voltage V_{DD}, has to be applied to the gate to switch the device from the off- to the on-state. The gate voltage difference to increase the current in a transistor is described by the parameter S. The broadening of the Fermi distribution function sets a physical lower limit for S in a MOSFET. Thus, scaling V_{DD} is limited under consideration of sufficient current difference between on-state and off-state.

The current flowing through a transistor dissipates energy by heating the device. Even though the current and thus the dissipated heat in a single transistor are small, the dense packing of billions of transistors in modern CPUs causes a considerable energy dissipation, which discharges the battery in mobile devices. The power consumed in integrated circuits for switching transistors scales quadratic with the power supply ($P \sim V_{DD}^2$), which makes scaling of V_{DD} a powerful tool for reducing power consumption.

In order to switch a transistors with smaller V_{DD} novel concepts relying on different charge transport mechanisms, that allow for values of S beating the MOSFET limitation, are needed. One example of such a new concept is the impact ionization transistor, which enables very steep values of S [31]. It has been shown though that this concept has essential drawbacks concerning switching speed since the finite time for the carrier multiplication process limits the minimum switching time of the device [93]. Another concept that was proposed as a steep switching device relies on a superlattice heterostructure to filter the Fermi distribution function and thus enables small values of S, which was proposed and investigated by simulations in [29]. However, device fabrication and integration of this structure proves to be rather challenging due to high requirements in terms of process variation.
One of the most promising concepts for a steep switching device is the tunnel field-effect transistor (TFET), that relies on quantum mechanical band-to-band tunneling (BTBT) as transport mechanism. The phenomenon of BTBT was already observed and described by Esaki in 1958 in narrow germanium p-n diodes [21] while the concept of a BTBT transistor device was first proposed an experimentally demonstrated in the late 1980s [5][99]. Since that time various TFET designs have been proposed and fabricated [91][41]. However, a BTBT transistor experimentally demonstrating subthreshold swings S smaller than the 60 mV/dec limitation of MOSFETs was realized first in 2004 [3]. Even though subthreshold swings below 60 mV/dec have been demonstrated up to now in TFETs with various concepts and materials, the average switching slopes are still well above 60 mV/dec and drive currents are typically below the limits of the international technology roadmap for semiconductors (ITRS), setting the aims for developments in future CMOS technology. Theoretical predictions, however, show that TFETs offer superior performance and consume less power at V_{DD} below 0.3 V, compared to MOSFETs [4].
Furthermore, the TFET concept offers the advantage of easy integration in current CMOS technology, since basically TFETs can be fabricated with a MOSFET process just by using opposite doping species in source and drain, in contrast to doping source and drain with the same doping type like in a MOSFET. However, the optimization of TFET structures follows different rules due to the deviating physical transport mechanism in the devices. Increasing the on-current in a TFET is especially important since the on-current defines the switching speed of the transistor. Due to the BTB tunneling probability, that is always smaller than one, on-current in a TFET is smaller compared to a MOSFET, where the probability of transmitting carriers from the source to the drain is equal to one in the on-state.

Within the framework of this thesis, different TFET structures based on silicon and silicon-germanium nanowire structures are realized experimentally. The focus of the TFET device design is to increase the tunneling probability. Different fabricated TFET structures are analyzed in detail and concepts for optimization are deduced from measurement results as well as TCAD simulations.

The content of this thesis is subdivided in eight chapters. Subsequent to this introductory chapter, chapter 2 presents the theoretical background and the underlying physical relations, which are used to develop the design and process for the TFETs and to interpret the measurement results. Chapter 3 exhibits experimental results on nanowire TFET and MOSFET structures fabricated on strained silicon on insulator substrates. The current-voltage characteristics of MOSFETs and TFETs are compared and various peculiarities of the TFET are explained. Chapter 4 presents results on nanowire TFETs fabricated on silicon-germanium substrates. The process implications of this material system are studied and performance improvement by different germanium concentrations is investigated. Chapter 5 introduces a heterostructure based TFET concept, that enhances BTBT by an enlarged tunnel junction area and in situ doping of the source. TCAD simulations are performed to further study the device characteristics and differences of the homo- and heterostructure TFET concept. Chapter 6 exhibits experimental results on inverters as simple logic elements build from TFETs presented in chapter 3. Furthermore, the implications of TFET device improvement on the inverter performance are demonstrated based on the heterostructure TFETs from chapter 6. Chapter 7 presents a comparative analysis of low frequency noise in MOSFETs and TFETs fabricated within the framework of this thesis. Chapter 8 concludes the findings and gives an outlook on possibilities for continuing the research on TFETs based on this work.

2 Theoretical Background

In this chapter the theoretical background and basic physical relations correlated with the later on presented experimental work are established. The metal-oxide-semiconductor field-effect transistor (MOSFET) and tunnel field-effect transistor (TFET) are introduced and their subthreshold characteristics are derived. Since this work focuses on TFETs, several additional effects influencing the TFET device performance are explained. The possibilities to increase the TFET performance by various design aspects are discussed subsequently. Finally a measurement technique for gate interface characterization is introduced, that is used to analyze the fabricated TFETs.

2.1 Power Consumption in Integrated Circuits

The power which is dissipated by integrated circuits can be divided into two contributions. The first is the dynamic power consumption $P_{dynamic}$, which is correlated with the charging and discharging of load capacitances C_{load} when the transistors switch their state:

$$P_{dynamic} = C_{load} \cdot V_{DD}^2 \cdot f \,, \tag{2.1}$$

where f is the switching frequency. $P_{dynamic}$ has a quadratic dependence on the supply voltage V_{DD} of the integrated circuit. The second contribution is the static power consumption of the transistors in the off-state:

$$P_{static} = I_{OFF} \cdot V_{DD} \,, \tag{2.2}$$

depending on V_{DD} and the leakage current of the transistor in the off-state I_{OFF}.
An important figure of merit is the inverse subthreshold swing or subthreshold slope S that relates I_{OFF} to V_{DD} [41]:

$$I_{OFF} \approx I_{ON} \cdot 10^{-\frac{V_{DD}}{S}} \,. \tag{2.3}$$

This equation shows that a decrease of V_{DD} at constant I_{ON} and S results in a rapid increase of I_{OFF}. This relation is illustrated in the schematic I_D-V_G characteristics in Fig.2.1 . Switching devices with a steeper average subthreshold swing are needed in order to maintain low off-state leakage for scaled down V_{DD} and thus reduced power consumption.

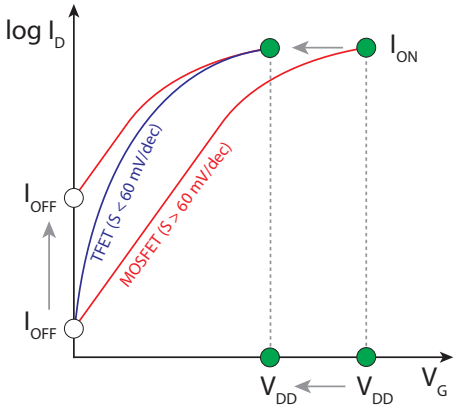

Figure 2.1: Schematic I_D-V_G characteristics of a MOSFET limited to $S > 60\,\mathrm{mV/dec}$ and a TFET with $S < 60\,\mathrm{mV/dec}$. Smaller average S is needed for supply voltage V_{DD} scaling without increasing I_{OFF}.

2.2 MOSFET

A metal-oxide-semiconductor field-effect transistor (MOSFET) is a three terminal device based on a MOS capacitor. A schematic illustration of a n-channel MOSFET structure is shown in Fig.2.2. The gate electrode is electrically isolated from the semiconductor channel by a gate dielectric. In case of the n-channel MOSFET, the source and drain regions are n^+-doped. Fig.2.2 also shows the conduction and valence band edge energies in the semiconductor channel from source to drain. The principle of current switching in a MOSFET is the injection of carriers from a thermally broadened Fermi distribution function in the source over the potential barrier of the conduction band in the channel region. By applying a positive gate voltage V_G the bands in the channel region move down and electrons transport from source to drain is enabled. The increase of drain current I_D with applied V_G depends on the broadening of the Fermi distribution function.

2.2.1 Subthreshold Characteristics

The Landauer formalism can be used as a simple 1D model to calculate the current flow in a MOSFET [15]:

$$I_D = \frac{2e}{h} \int_{-\infty}^{\infty} dE\, T(E)\, (f_s(E) - f_d(E)) = \frac{2e}{h} \int_{\Phi_f^0}^{\infty} dE\, (f_s(E) - f_d(E)) \;, \tag{2.4}$$

where e, h, f_s and f_d are, respectively the elementary charge, the Planck constant and the Fermi distribution functions in the source and drain. Φ_f^0 is the potential barrier height for

the electrons, which is given by the conduction band edge energy in the channel. $T(E)$ denotes the transmission probability, which is $T(E) = 1$ for $E > \Phi_f^0$ and $T(E) = 0$ else. In the subthreshold regime f_s and f_d can be approximated by the Boltzmann distribution, since Φ_f^0 is much larger than the chemical potentials μ_s and μ_d in source and drain, respectively. Since $\mu_s > \mu_d$, due to the applied V_{DS}, $f_d \ll f_s$ in this regime and f_d can be neglected. Based on these assumptions (2.4) becomes:

$$I_D = \frac{2e}{h} \int_{\Phi_f^0}^{\infty} dE \exp\left(-\frac{E-\mu_s}{k_B T}\right) = \frac{2e}{h} k_B T \exp\left(-\frac{\Phi_f^0 - \mu_s}{k_B T}\right). \tag{2.5}$$

Φ_f^0 is a function of the gate voltage V_G [49]:

$$\partial \Phi_f^0 = e \left(\frac{C_{ox}}{C_{ox} + C_{depl} + C_{it}}\right) \partial V_G \tag{2.6}$$

where C_{depl}, C_{it} and C_{ox} are the depletion, interface and gate oxide capacitance, respectively. The inverse subthreshold slope S can be calculated from the I_D-V_G characteristics using (2.5) and (2.6):

$$S = \left[\frac{\partial \log I_D}{\partial V_G}\right]^{-1} = \ln(10) \left[\frac{\partial I_D}{\partial \Phi_f^0} \frac{\partial \Phi_f^0}{\partial V_G} \frac{1}{I_D}\right]^{-1} = \ln(10) \frac{k_B T}{e} \left(1 + \frac{C_{depl} + C_{it}}{C_{ox}}\right). \tag{2.7}$$

Hence S in a MOSFET has a lower limit depending on the broadening of the Fermi distribution function with temperature. At 300 K and in the case of $C_{ox} \gg C_{depl} + C_{it}$ this lower limit is

$$S = \ln(10) \frac{k_B T}{e} \approx 60\,\mathrm{mV/dec}\,. \tag{2.8}$$

2.3 Tunnel Field-Effect Transistor

A tunnel-FET (TFET) is a gated p-i-n structure, which is operated in reverse bias. This means in contrast to the MOSFET source and drain are doped with opposite dopant species. A schematic of a TFET structure is shown in Fig.2.3. The transport mechanism in a TFET relies on band-to-band tunneling (BTBT) instead of thermal emission over a potential barrier as in a MOSFET. The band edge energies of valence and conduction band in a p-channel TFET structure are shown schematically in Fig.2.3. In p-channel configuration the source is n^+-doped and a negative voltage V_{DS} is applied to the p-doped drain. By applying a negative voltage to the gate the bands in the channel region are moved up and an energy overlap $\Delta\Phi$ of source conduction and channel valence band edge is created. The energy interval $\Delta\Phi$ allows for BTBT from the source into the channel. Here the confined tunneling window acts like a band-pass filter for electrons from the source cutting off the high and

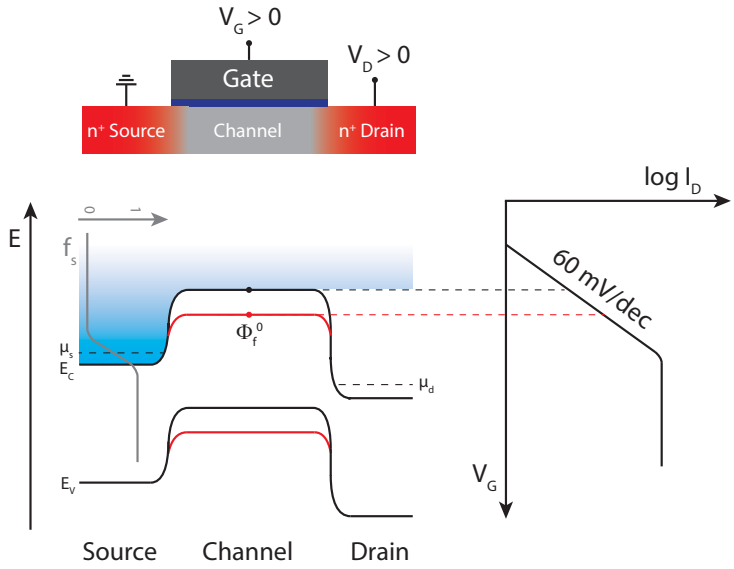

Figure 2.2: Schematic illustration of a n-channel MOSFET structure, the valence and conduction band edge energies along transport direction for two different gate voltages and the corresponding I_D-V_G characteristics.

low energy tail of the Fermi distribution function. Thus, the carrier transport in the TFET becomes independent from the broadening of the Fermi function.

2.3.1 Band-to-Band Tunneling

In quantum mechanics particles, such as electrons, can be represented by wave functions. In contrast to the classical picture these wave functions do not terminate on a finite potential barrier, but penetrate into it. Thus, there is a certain probability that an electron can tunnel through a potential barrier of finite width. In the Wentzel-Kramers-Brillouin (WKB) approximation a potential $U(x)$, that does not change rapidly with x, is approximated with infinitesimal wide rectangular potentials. The WKB tunneling probability T_{WKB} is given by [98]

$$T_{WKB} = \exp\left(-2\int_{x_1}^{x_2} |k(x)|dx\right) , \tag{2.9}$$

where $k(x)$ is the wave vector of the carrier and $x_{1,2}$ the starting and end point of the tunneling path, respectively. The tunneling barrier for a BTBT process can be approximated as a triangular barrier, which is illustrated in Fig.2.4. The wave vector for an electron with

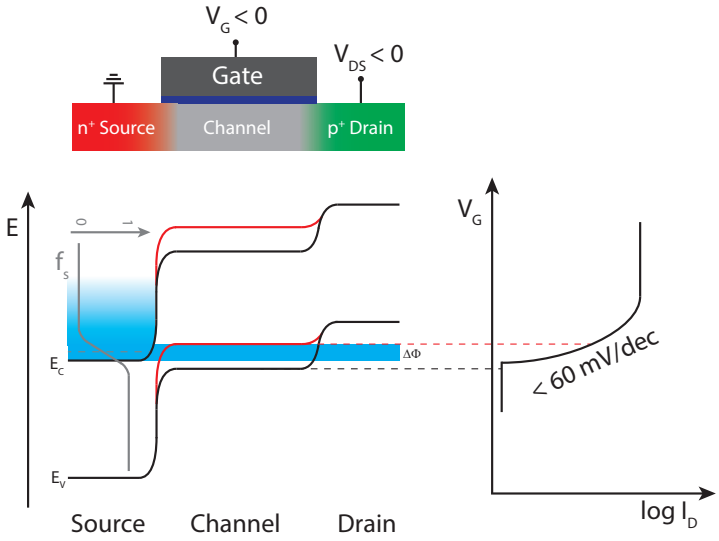

Figure 2.3: Schematic illustration of a p-channel TFET structure, the valence and conduction band edge energies along transport direction for two different gate voltages and the corresponding I_D-V_G characteristics.

the energy E in the conduction band can be written as:

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}(E - E_C)} = \sqrt{\frac{2m^*}{\hbar^2}(-e\mathcal{E}x)}\,, \tag{2.10}$$

where the energy difference of the electron to the conduction band $(E - E_C)$ was substituted in the second step by the corresponding electric field $\mathcal{E}$ in the junction. Plugging (2.10) into (2.9) and using $x_1 = 0$ and $x_2 = E_g/e\mathcal{E}$ yields:

$$T_{WKB} = \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3\hbar\, e\mathcal{E}}\right). \tag{2.11}$$

The spatial width of the tunnel junction is determined by the sum of the screening length in the source λ_{dop} and the channel λ_{ch} [46][88]. λ_{dop} is small for a steep doping profile in the source, whereas λ_{ch} decreases for high electrostatic channel control by the gate. The electric field in the junction can hence be expressed as $e\mathcal{E} \approx (E_g + \Delta\Phi)/(\lambda_{dop} + \lambda_{ch})$ and (2.11) becomes:

$$T_{WKB} = \exp\left(-\frac{4(\lambda_{dop} + \lambda_{ch})\sqrt{2m^*}E_g^{3/2}}{3\hbar\,(\Delta\Phi + E_g)}\right). \tag{2.12}$$

This result shows that a large tunneling probability is observed for a small effective mass, small E_g, a steep source doping profile and a good electrostatic channel control.

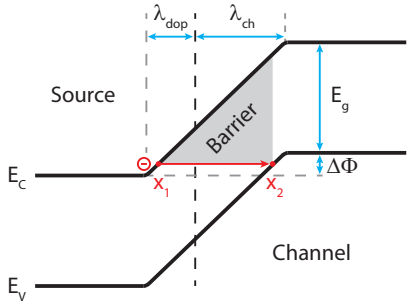

Figure 2.4: Approximation of the BTBT barrier as a triangular potential.

2.3.2 Subthreshold Characteristics

In order to calculate the subthreshold characteristics of a TFET the Landauer formalism from equation (2.4) can be used with $T(E)$ given by T_{WKB} from equation (2.12). Carrier injection from the drain side can be neglected ($f_d = 0$) and the energy interval where tunneling occurs is given by the energy overlap $\Delta\Phi = E_{CV} - E_{SC}$ of channel valence and source conduction band for the p-channel TFET. Assuming the band edge energies can be approximated as shown in Fig.2.4, T_{WKB} is independent of E for the energy interval $\Delta\Phi$. Hence, I_D can be expressed as:

$$I_D = T_{WKB} \cdot \frac{2e}{h} \int_0^{\Delta\Phi} dE\; f_s(E) = T_{WKB} \frac{2e}{h} F(\Delta\Phi)\,, \tag{2.13}$$

where $F(\Delta\Phi)$ is the integral over the Fermi function. Assuming that the channel potential varies one to one with the applied gate potential $\partial V_G / \partial\Delta\Phi = 1/e$, the derivative of I_D becomes:

$$\frac{\partial I_D}{\partial V_G} = e\frac{\partial I_D}{\partial \Delta\Phi} = \frac{2e^2}{h}\left[\frac{\partial T_{WKB}}{\partial \Delta\Phi} F(\Delta\Phi) + T_{WKB}\frac{\partial F(\Delta\Phi)}{\partial \Delta\Phi}\right]. \tag{2.14}$$

A high tunneling probability is necessary to achieve reasonable on-current and performance in a TFET. If a tunneling probability close to unity is achieved, T_{WKB} varies only slightly with $\Delta\Phi$ and the first term in equation (2.14) can be neglected. Combining (2.13) and (2.14) S can be calculated by:

$$\begin{aligned} S &= \left[\frac{\partial \log I_D}{\partial V_G}\right]^{-1} = \ln(10)\left[\frac{\partial I_D}{\partial V_G}\frac{1}{I_D}\right]^{-1} = \ln(10)\left[e\frac{\partial I_D}{\partial \Delta\Phi}\frac{1}{I_D}\right]^{-1} \\ &= \ln(10)\left[\frac{2e^2}{h} T_{WKB}\frac{\partial F(\Delta\Phi)}{\partial \Delta\Phi}\frac{1}{T_{WKB}\frac{2e}{h}F(\Delta\Phi)}\right]^{-1} \\ &= \frac{\ln(10)}{e}\frac{F(\Delta\Phi)}{\frac{\partial F(\Delta\Phi)}{\partial \Delta\Phi}}\,. \end{aligned} \tag{2.15}$$

For small $\Delta\Phi$ a Taylor expansion of the integral function $F(\Delta\Phi)$ to the first order yields:

$$S = \frac{ln(10)}{e}\Delta\Phi\,. \tag{2.16}$$

This relation reveals that S for a TFET has no first order temperature dependence, in contrast to the MOSFET. However, S in a TFET depends linearly on $\Delta\Phi$ and thus S increases for increasing V_G, whereas S in a MOSFET is independent of V_G.

2.3.3 Ambipolarity

Due to the symmetric p-i-n structure of a TFET, BTBT can occur at the n-i as well as at the p-i junction when the bands in the channel region are shifted up and down, respectively. The applied gate voltage V_G causes a shift in the channel band energy edges by Φ_C. Fig.2.5 shows an illustration of the valence and conduction band edges in a TFET. The drain voltage V_{DS} is applied to the n-doped region, which corresponds to a n-channel TFET configuration. In TFET operation the p-i-n diode is reverse biased and hence V_{DS} is positive in the n-channel configuration, shifting down the drain bands by the energy Φ_D.

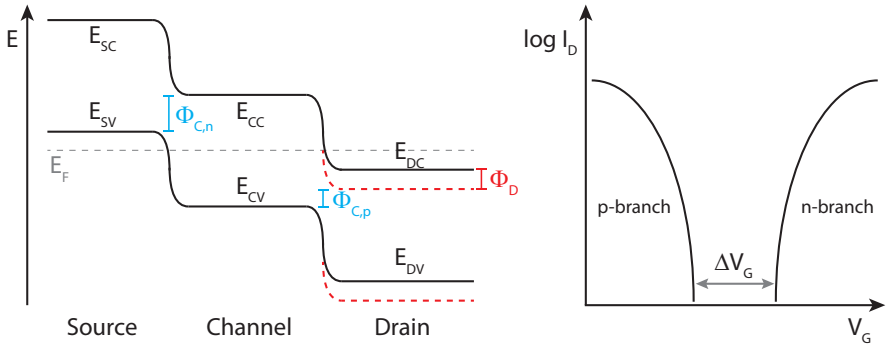

Figure 2.5: Illustration of the valence and conduction band edge energies in a p-i-n TFET structure (left) and the corresponding I_D-V_G characteristics with symmetric p- and n-branch (right).

Fig.2.5 shows a schematic I_D-V_G characteristics of a TFET. The on-set of the p- and n-branch are separated by a gate voltage diffenrence ΔV_G, that corresponds to a shift of the channel bands by $\Phi_{C,n} + \Phi_{C,p}$:

$$\begin{aligned} e\Delta V_G = \Phi_{C,n} + \Phi_{C,p} &= E_{CC} - E_{SV} + E_{DC} - \Phi_D - E_{CV} \\ &= E_g - \Phi_D - (E_{SV} - E_{DC})\,. \end{aligned} \tag{2.17}$$

E_{CC}, E_{CV}, E_{SV} and E_{DC} are the band edge energies as given in Fig.2.5 and $E_{CC} - E_{CV}$ can also be expressed as the band gap E_g. $E_{SV} - E_{DC}$ is positive in case of degenerately

doped source and drain regions, when the Fermi energy E_F lies within the band. This demonstrates that the separation of p- and n-branch in the I_D-V_G characteristics depends on E_g and decreases with applied V_{DS} and high source and drain doping level. Hence, for too small E_g or too high V_{DS} p- and n-branch can intersect and degrade the off-state.
The separation of p- and n-branch given by equation (2.17), however, is the ideal case when BTBT is the only transport mechanism occurring in the TFET. The following sections introduce additional effects causing a further closing of the gap between p- and n-branch.

2.3.4 Trap Assisted Tunneling

In addition to the BTBT process that sets in when the applied V_G is large enough to create an energy overlap of source and channel bands trap assisted tunneling (TAT) processes have to be taken into account in experimental TFET structures. TAT describes the process when carriers from the source tunnel into trap states within the channel band gap and reach the channel bands by thermal excitation from the trap states [73]. Trap states in the tunnel junction are introduced by oxide interface traps, defects due to ion implanted junctions or simply by the presence of dopant atoms. TAT sets in at smaller values of V_G, before an energy window for BTBT from source to channel band edges is opened. Hence the separation of p- and n-branch, which was calculated before, is reduced.
Since the transfer of the carriers from the trap states into the channel relies on thermal excitation it depends on the broadening of the Fermi distribution function. Thus, current generated by TAT has the same limitation of S to 60 mV/dec as a MOSFET. Due to the temperature dependence the thermal excitation and thus TAT can be suppressed at low temperatures.

2.3.5 Phonon-Absorption Assisted Tunneling

The scattering of electrons with phonons influences TFET performance. For BTBT in indirect semiconductors, such as silicon with a Γ-Δ band gap, phonon interaction with tunneling charge carriers is needed for momentum conservation. Due to electron-phonon scattering the energy of electrons in the source can be increased above the valence band edge as shown schematically in Fig.2.6. If the electron energy exceeds the conduction band energy in the channel BTBT is enabled, even though there is no energy overlap of source valence and channel conduction band. The maximum energy an electron can gain in Si is given by the transversal-optical phonon with 63 meV at corresponding wave vector [7]. Also transversal-acoustic phonons with 18. 6 meV contribute to the phonon-absorption assisted tunneling [90].
Due to the onset of BTBT at smaller V_G, caused by electron-phonon scattering, S of the TFET is degraded and the n- and p-branch in the I_D-V_G characteristics move closer together [55][53][63]. The phonon assisted tunneling also introduces a temperature dependence of S for small V_G since the phonon occupation is larger at higher T.

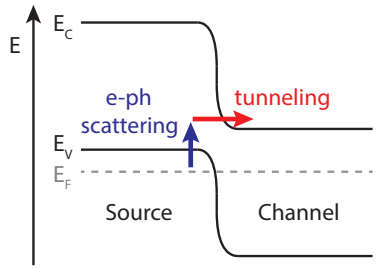

Figure 2.6: Illustration phonon assisted BTBT in a n-channel TFET.

2.3.6 Shockley-Read-Hall Recombination

The Shockley-Read-Hall (SRH) recombination mechanism describes the recombination of conduction band electrons and valence band holes with the assistance of trap states within the band gap [87]. These trap states are for example introduced by dopant atoms. The recombination process is non-radiative and the electron energy is transfered to lattice vibrations. The SRH recombination is much more likely compared to direct recombination due to the smaller energy difference. The recombination rate R_{SRH} for a single-level trap is given by [20]:

$$R_{SRH} = \frac{np - n_i^2}{\tau_p \cdot (n + n_1) + \tau_n \cdot (p + p_1)}, \tag{2.18}$$

with

$$n_1 = n_i \exp\left(\frac{E_T - E_F}{k_B T}\right), \; p_1 = n_i \exp\left(\frac{E_F - E_T}{k_B T}\right), \tag{2.19}$$

where τ_n and τ_p are the carrier lifetimes of electrons and holes, respectively. E_T is the energy level of the trap state and E_F is the Fermi energy. The number of intrinsic carriers in a semiconductor is given by:

$$n_i = \sqrt{N_C N_V} \exp\left(-\frac{E_g}{2k_B T}\right) = A T^{\frac{3}{2}} \exp\left(-\frac{E_g}{2k_B T}\right), \tag{2.20}$$

where N_C and N_V are the densities of states in conduction and valence band, respectively. A is a constant depending on the density of states, effective masses of electrons and holes and the number of equivalent conduction bands [98]. Equation (2.20) shows that the intrinsic carrier concentration increases with decreasing band gap E_g [34].

Although the channel region of a TFET is called intrinsic, the substrates used to fabricate the devices have a slight background dopant concentration in the order of $10^{16}\,\mathrm{cm}^{-3}$ allowing for SRH generation-recombination in the channel region. This process is illustrated in Fig.2.7. The p-i-n diode in a TFET is reversed biased in standard operation, and electrons and holes flow from the channel region to the n-doped and p-doped region, respectively. n

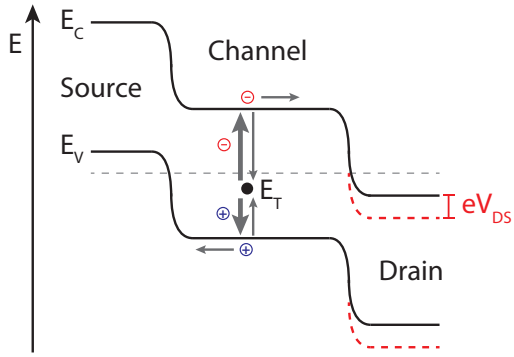

Figure 2.7: Illustration of the SRH generation-recombination process at trap states within the band gap. Under reverse bias conditions holes flow to the p-doped source and electrons to the n-doped drain.

and p decrease in the channel region below the intrinsic carrier number n_i and R_{SRH} in equation (2.20) becomes negative. This means the SRH generation exceeds the recombination. The SRH generation contributes to the off-state current in a TFET and is largest under flat band voltage conditions. An accumulation of either electrons or holes in the channel by applied V_G above or below V_{FB} decreases the generation current.

2.3.7 Drain Induced Barrier Thinning

In contrast to the MOSFET that shows a linear onset in I_D-V_{DS} characteristics, most experimental demonstrated TFETs exhibit a superlinear onset [88][83]. This characteristic is undesired since the current saturation is degraded. The reason for the superlinear behavior can be explained by Fig.2.8. When a gate voltage V_G large enough to enable BTBT is applied under zero V_{DS} electrons can tunnel into the channel and form an inversion charge Q_{inv} that screens the gate potential. Due to the screening of the gate potential the bands in the channel region can not be shifted further by larger applied V_G. By applying a positive V_{DS} the inversion charge and hence the screening of V_G in the channel is reduced. Thus, the bands in the channel move down and the tunnel distance at the source-channel junction decreases with increasing V_{DS}. This effect is called drain induced barrier thinning (DIBT). The DIBT can be avoided by going to the quantum capacitance limit, where the oxide capacitance C_{ox} is large compared to the quantum capacitance C_q [47]. In this case the channel potential changes one-to-one with the applied V_G. However, since C_q is proportional to the density of states (DOS) this limit can only be effectively reached in one-dimensional structures. For Si devices this limit is only reached for nanowire devices with diameters below 5 nm.

Also the source doping concentration influences the DIBT. A degenerately doped source provides a small λ_{dop}, reducing the tunneling distance and increasing the tunneling proba-

bility. Under these conditions the tunneling distance varies only slightly with a change of the channel band position and thus also DIBT is reduced [68][30]. However, there is a trade-off since for a highly degenerated source the Fermi function lies well within the band and the energetic window allowing for tunneling cuts out the Boltzmann part of the distribution function [49]. This limits S to 60 mV/dec as in the case of a MOSFET.

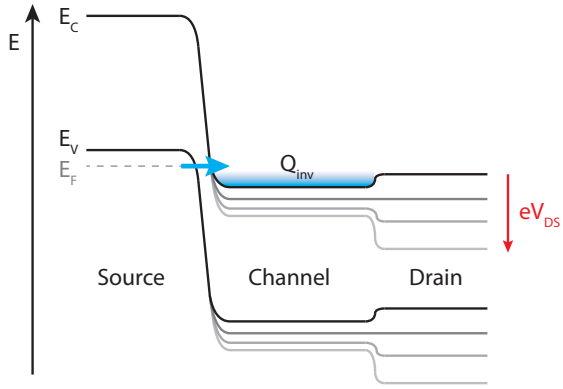

Figure 2.8: Schematic illustration of the drain induced barrier thinning (DIBT) at constant V_G and increaing V_{DS}.

2.4 TFET Design Considerations

Based on the theoretical considerations about the working principle of TFETs presented in the previous sections, design concepts and rules for the fabrication of such devices can be deduced. The design concepts, which are utilized in the devices presented in this work are described in the following sections.

2.4.1 Multi-Gate Structures

As previously discussed a good electrostatic gate control, which is represented by a small screening length λ_{ch}, is crucial in TFETs in order to achieve a high tunneling probability and thus high on-current. λ_{ch} can be calculated for a fully depleted SOI MOSFET with a single planar gate from Poisson's equation [13]:

$$\lambda_{ch} = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{si} t_{ox}}\,, \tag{2.21}$$

where ε_{si}, ε_{ox}, t_{si} and t_{ox} are, respectively, the dielectric constants and layer thicknesses of the silicon and gate oxide layer. λ_{ch} can further be reduced by going from a planar device concept to multi-gate configurations [22]. Different types of multi-gate structures with double-, tri-, Ω-, Π- and gate-all-around (GAA) - configuration are depicted in Fig.2.9.

Analytical calculations [13] and numerical simulations [59] reveal that λ_{ch} in double-, tri- and GAA-configuration for a square channel cross-section is given by (2.21) multiplied by a factor $\sqrt{1/2}$, $\sqrt{1/3}$ and $\sqrt{1/4}$, respectively.
Fig.2.10 exhibits calculated values of λ_{ch} for different gate configurations as a function of the Si thickness for a square cross-section and a gate dielectric of 3 nm HfO_2. The GAA structure provides the best possible gate control. However, the processing complexity for these type of gates is much larger compared to a tri-gated structure, due the need for freestanding nanowires. In this work tri- and Ω-gated nanowires are utilized for TFET application, since they provide a good compromise between process complexity and improved gate control. Fig.2.10 reveals that the improvement of λ_{ch} for a tri-gate compared to a planar single gate is quite large, while the additional improvement due to a GAA structure is rather small.

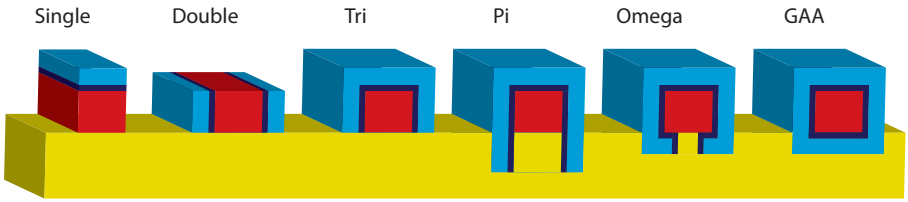

Figure 2.9: Schematic of various gate configuration types.

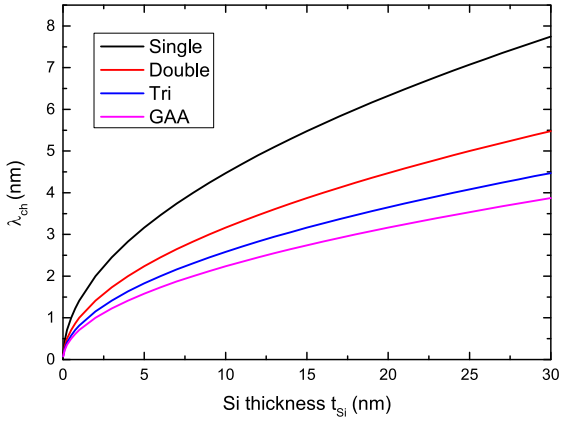

Figure 2.10: Calculated values of λ_{ch} for different gate configurations as a function of the Si thickness t_{Si}.

2.4.2 High-κ Gate Dielectrics

A large oxide capacitance C_{ox} is crucial in field-effect controlled devices to gain a good electrostatic control of the channel potential by the applied gate voltage, as shown in equation (2.6). Larger C_{ox} can be realized by decreasing the gate oxide thickness t_{ox} according to:

$$C_{ox} = \varepsilon_0 \varepsilon_{ox} \frac{A}{t_{ox}}, \tag{2.22}$$

where A is the area of the capacitor, ε_0 and ε_{ox} are the vacuum permittivity and the relative permittivity of the oxide, respectively. However, if t_{ox} is in the range of 1 nm the leakage current from the channel to the gate through the gate dielectric becomes too large to achieve acceptable device performance.
Originally, SiO_2 was used as a gate dielectric, since it has a large band gap, large band offsets to Si and can be fabricated simply by thermal oxidation of Si structures. One way of increasing C_{ox} further is utilizing dielectric materials that offer higher values of ε_{ox}, that is also sometimes denoted with κ in this context. These so called high-κ dielectrics offer ε_{ox} values that can be many times higher than $\varepsilon_{ox} = 3.9$ for SiO_2. Hence, t_{ox} can be increased for high-κ materials compared to SiO_2 and the leakage currents decrease. Especially rare earth based oxides like HfO_2 exhibit sufficiently high ε_{ox} and are well suited for CMOS integration [109][33]. HfO_2 was introduced in the 45 nm node in 2007 [70].
In this work Al_2O_3 with $\varepsilon_{ox} \approx 9$ and HfO_2 with $\varepsilon_{ox} \approx 18$, both grown by atomic layer deposition (ALD), are employed in order to increase C_{ox} and decrease λ_{ch} (see eq.(2.21)) in TFETs.

2.4.3 Density of Interface and Oxide States

Charged interface states between semiconductor channel and gate dielectric can screen the gate electrical potential and deteriorate the control of the channel potential by the applied gate voltage. Charged interface trap states are for example introduced by surface contamination prior to the gate stack deposition or unsaturated chemical bonds of the semiconductor or high-κ dielectric, which are always present in fabricated devices. Thus, characterization and improvement of the density of interface states D_{it} is important in the TFET optimization process.
One possibility to investigate D_{it} is measuring the charge-pumping (CP) current I_{cp} [32]. CP measurements can be performed on bulk MOSFETs where source and drain are shortcut and I_{cp} is measured between source/drain and the bulk substrate. However, the CP technique can also be applied to gated p-i-n structures [19] which makes it applicable for TFETs.
The CP measurement setup for a TFET on SOI device is shown in Fig.2.11. The signal from a pulse generator is applied to the gate, while a small reverse bias is applied to the drain contact and the source is at ground potential. The charge pumping current I_{cp} is measured at the drain contact.

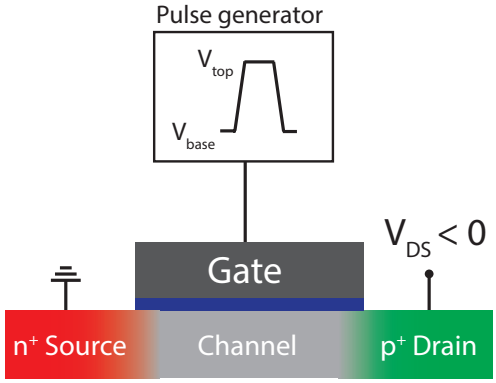

Figure 2.11: Schematic of the setup for charge pumping measurements on a TFET.

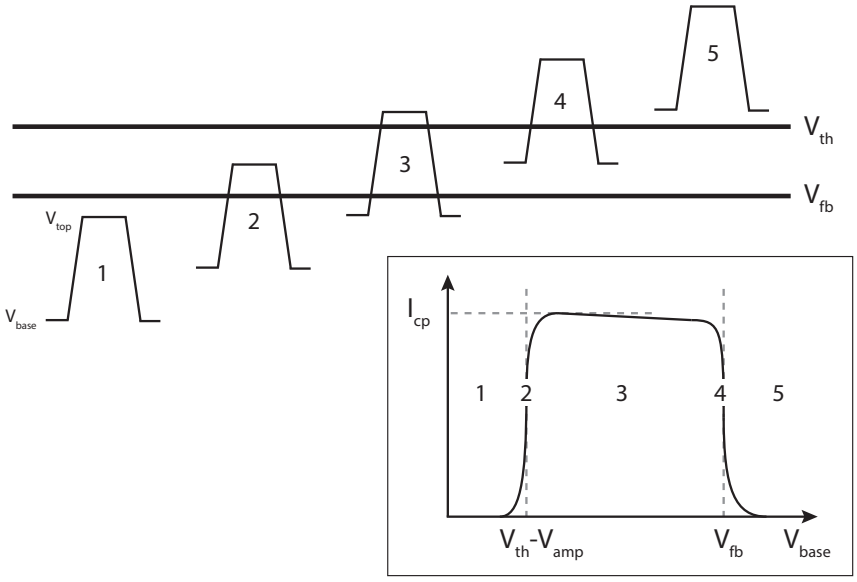

Figure 2.12: Schematic of the base-level charge pumping technique and the corresponding CP-current I_{cp} as a function of the base voltage V_{base}.

The working principle of the CP measurement is illustrated in Fig.2.12. Voltage pulses with constant amplitude V_{amp} and frequency f are applied to the gate contact. I_{cp} is measured at the drain while the base voltage V_{base} of the pulses is swept from $V_{base} < V_{fb} - V_{amp}$ to $V_{base} > V_{th}$. The maximum I_{cp} is generated when for the applied voltage pulse V_{base} is below V_{fb} and V_{top} above V_{th}. In this case the channel is pumped from accumulation to inversion and the traps in the interface and oxide are filled in inversion with electrons. When the channel is pumped back into accumulation, within a time that is small compared to the trap lifetime, holes that are injected as majority carriers from the drain, recombine with the trapped electrons, thus causing a recombination current.
For very thin oxide layers a gate leakage current can add to I_{cp} and also a band-to-band tunnel current can occur due to the highly doped source and drain in a TFET. These current contributions can be determined by measuring I_{cp} at low frequency ($f \approx 1\,\mathrm{kHz}$), since they are not frequency dependent compared to the CP recombination current.
The measured I_{cp} is given by

$$I_{cp} = N_t A f e\,, \tag{2.23}$$

where A is the gate area and N_t the number of interface and oxide traps per area. In high-κ gate stacks both, interface and oxide traps, contribute to I_{cp} [100]. The density of interface and oxide states D_t follows from normalizing N_t to the energy interval. A profile of the traps as a function of the distance from the interface can be measured by changing the discharge time, due to the spatial life time dependence of the traps.

3 Strained SOI Nanowire TFET

This chapter presents results on nanowire (NW) tunneling field effect transistors (TFETs) with high-κ/metal gate fabricated on strained silicon on insulator (SSOI) substrate. As discussed in the theory section 2.3.1 the on-current in a TFET benefits especially from a small band gap E_g and a small screening length of the electrical potential λ. The design of the NW TFET presented here was conceived in order to improve exactly these two important device parameters. The biaxially tensile SSOI substrate offers reduced E_g, while the HfO_2/TiN gate stack in combination with the NW array design guarantees good electrostatic gate control, and hence small λ. In the first part of this chapter the fabrication of NW array TFETs on SSOI is described. In the second part the resulting strain in the processed NWs is discussed. Part three compares the current-voltage (I-V) characteristics of the NW TFETs to reference NW MOSFETs highlighting fundamental differences between both device types. Part four analyzes the influence of the nanowire cross-section on the device performance. Part five presents a temperature dependent I-V analysis of the devices including comparisons to analytical models and device simulation.

3.1 Device Fabrication

SSOI Substrate

Strained silicon (sSi) on insulator substrates with a sSi thickness of 15 nm were used to fabricate the NW array TFETs. The biaxial tensile strain in the sSi layer is $\epsilon = 0.8\,\%$ which correspondes to a stress of $\sigma = 1.3\,\mathrm{GPa}$ [27]. To fabricate the sSOI wafers a silicon layer is grown pseudomorphically on relaxed $Si_{1-x}Ge_x$ with a Ge content of $x = 20\,\%$ [36][37]. Subsequently the sSi layer is transferred by wafer bonding technique onto a wafer with 145 nm thick SiO_2 on Si [9][27]. The sSi layer of the resulting SSOI wafer has a (001) surface and a background p-doping level of $1 \times 10^{15}\,\mathrm{cm}^{-3}$.

Process Steps

Fig.3.1 shows schematic images of the sample at important process steps during the fabrication. The process was carried out on $19.5 \times 19.5\,\mathrm{mm}^2$ pieces cut from a 300 mm wafer. Because of the nanowire array design very high resolution and alignment accuracy for the lithographic steps during the process are needed. Patterning of the NWs as well as the alignment of the gate and implantation windows require electron-beam lithography. In the

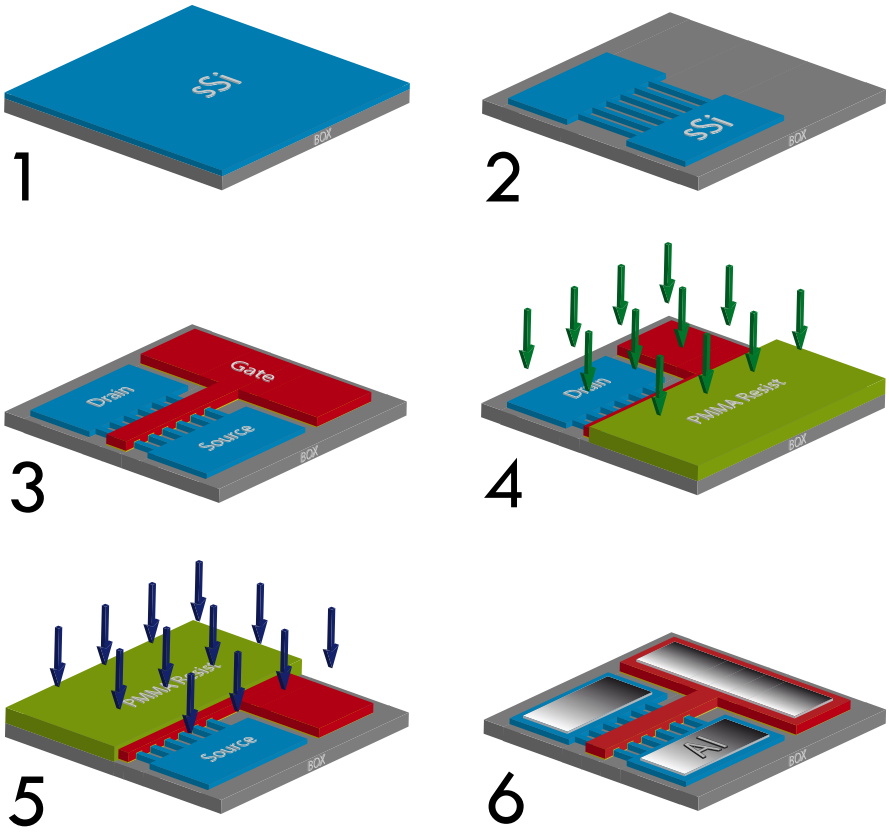

Figure 3.1: Schematic illustration of a TFET device at differnt steps during the processing.

following the process for the SSOI NW array p-TFET fabrication will be described in step by step:

1. A **precleaning** of the sample pieces was performed to remove the resist protecting the samples during sawing of the wafer into pieces. To remove the resist acetone and propanol were used in combination with an ultrasonic bath. Subsequently the samples were cleaned in Piranha etch with $H_2SO_4 : H_2O_2$ $(4:1)$.

2. Optical lithography using UV6.06 resist was used to transfer the **electron-beam marker** pattern with $15 \times 15\,\mu m^2$ squares on the sample. Subsequently the markers were etched by reactive ion etching (RIE) in a three step process etching the top sSi layer with SF_6/O_2, the buried oxide with CHF_3 and the Si substrate with SF_6/Ar plasma. The UV6.06 resist mask was removed using acetone and propanol. The resulting marker depth is about 700 nm.

3. The sample was coated with electron-beam sensitive PMMA resist 949.04/200K and the pattern for the **nanowire array and mesa structure** was written by electron-beam lithography. After development of the resist the pattern was transferred into the strained Si layer by RIE using a SF_6/O_2 plasma at low temperature. The remaining PMMA resist was removed in an O_2 plasma process. The resulting NW array connecting two larger areas of sSi was shown schematically in Fig.3.1(2).

4. Subsequent to a standard RCA cleaning the **gate stack** was deposited. The high-κ dielectric HfO_2 is deposited by atomic layer deposition (ALD) and the gate metal TiN by atomic vapor deposition (AVD).

5. The sample was coated with negative electron-beam resist hydrogen silsesquioxane (HSQ XR-1541) and the **gate pattern** and gate pads were written by e-beam lithography. After development of the HSQ resist the TiN layer was patterned by RIE using SF_6/Ar plasma. The HfO_2 was structured by wet chemical etching with HF acid. The resulting NW array with patterned gate stack was shown in Fig.3.1(3).

6. Two e-beam lithographies were needed as masks for the ion implantations. In both cases a 650 nm thick layer of PMMA 669.07/600K was used as **ion implantation** mask. First the source side of the TFET was covered and the implantation of $BF_2{}^+$ ions into the drain was performed. Only half of the gate was covered with resist in order to allow for a self aligned implantation process. In the second step the drain side of the TFET was covered and As^+ ions were implanted into the source region. This process is illustrated in Fig.3.1(4) and (5). Activation of the dopants was carried out by a rapid thermal spike annealing at 1000 °C in nitrogen atmosphere.

7. The sample was coated with negative tone photoresist nLOF2020 and contact windows at source, drain and gate were opened using optical lithography. After HF dipping to remove the native oxide, 150 nm Al was deposited for **contact metalization** by electron-beam evaporation. The redundant Al was removed by a lift-off process in acetone.

8. A **forming gas annealing** at 400 °C in 90% N_2 and 10% H_2 for 10 minutes was performed in order to improve the high-κ interface quality as well as contact quality of the Al pads on the doped Si layer.

The processed p-TFETs can also be measured as n-TFET just by redefining source and drain contacts. Ion implantation energy and dose have been chosen carefully according to TRIM simulations, based on the amorphization limit in Si at a vacancy concentration of $8.95 \times 10^{21}\,\mathrm{cm}^{-3}$ [69]. The implantation peak of the ion distribution was chosen to be close to the top of the sSi layer in order keep a thick enough crystalline seed layer to allow for solid phase epitaxial regrowth (SPER) during rapid thermal annealing (RTA) as shown in

[10]. Both dopant types were implanted to a fluence of $1.5 \times 10^{15}\mathrm{cm}^{-2}$.
The NW array of each device consists of 1000 NWs in parallel with a pitch of 200 nm. Four different lengths of NWs with 500, 800, 1200 and 2400 nm and corresponding gate lengths of 100, 400, 800 and 2000 nm have been fabricated. Two batches of these TFETs with NW cross-sections of $10 \times 50\,\mathrm{nm}^2$ and $10 \times 10\,\mathrm{nm}^2$ have been processed, respectively. Fig.3.2 (a) shows a scanning electron microscope (SEM) image of a NW array with 10 nm wide and $2.5\,\mu$m long NWs. A section of a NW array with 500 nm long wires and a 100 nm gate length TiN gate is shown in Fig.3.2 (b). Fig.3.3 (a) and (b) exhibit cross sectional transmission electron microscope (TEM) images of single NWs with 50 nm and 10 nm width, respectively, underneath the HfO_2/TiN gate.
In the batch with the 10 nm wide NWs, MOSFETs have been processed on the same chip together with the TFETs. For processing additional MOSFETs only the implantation mask in step 6 of the process description was changed. In case of the BF_2 implantation the whole n-MOSFET was covered by resist while boron was implanted in source and drain of the p-MOSFET and vice versa in case of the As implantation.

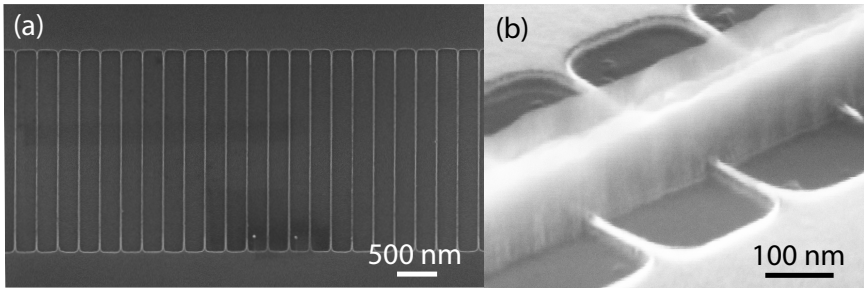

Figure 3.2: (a) Scanning electron microscope (SEM) image of a nanowire array with $2.4\,\mu$m long and 10 nm wide NWs; (b) SEM image of 500 nm long NWs with a 100 nm long TiN gate.

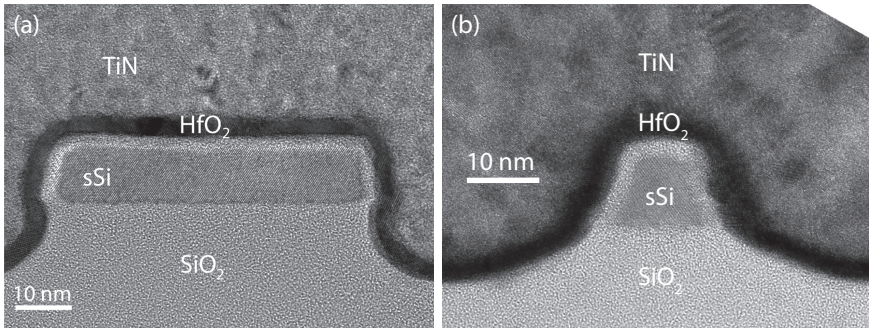

Figure 3.3: Cross-sectional transmission electron microscope (TEM) images of single NWs with (a) $10 \times 50\,\mathrm{nm}^2$ and (b) $10 \times 10\,\mathrm{nm}^2$ in a SSOI NW array TFET with high-κ/metal gate.

3.2 Uniaxial NW Strain

The 15 nm thick sSi layer of the (001) SSOI substrate has a biaxial tensile strain of $\varepsilon = 0.8\,\%$. The channel of the fabricated NWs is oriented in [110] direction. Several publications show that due to the patterning of nanowires on biaxially tensile strained silicon the strain accross the NW relaxes while the strain along the NW is maintained. This effect is demonstrated theoretically by 2D finite element simulations in [23] and experimentally by X-ray diffraction in [6]. Raman measurements performed on nanowires, fabricated by a process similar to the one used in this work, confirm that uniaxial strain along ion implanted nanowires recovers after spike annealing of the partially amorphized sSi layer [69].

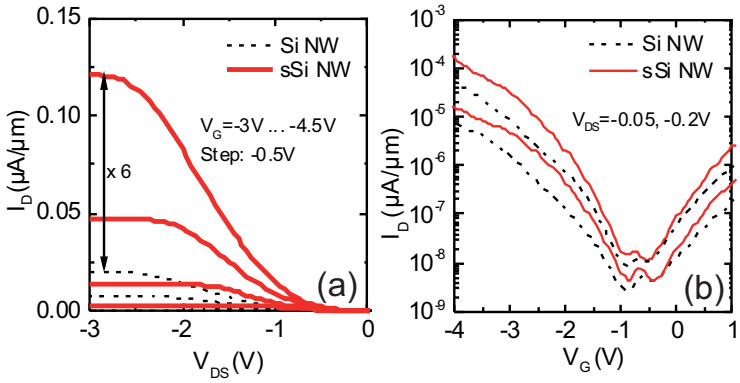

Figure 3.4: (a) Output and (b) transfer characteristics of strained Si NWs with HfO_2/poly-Si gate stack fabricated by Sandow [83].

Nanowire array TFETs using SiO_2 as a gate dielectric and poly-Si as gate are demonstrated in [89]. Fig.3.4 exhibits output and transfer characteristics of these devices. The comparison of TFETs fabricated on SOI and sSOI substrate reveals an increase in on-current by a factor of six for the strained Si. The transfer characteristics in Fig.3.4 also show a slight increase in the off-current (I_{OFF}) of the TFET with sSi NWs. From this change in I_{OFF} the actual reduction of E_g for strained Si NWs compared to unstrained NWs was estimated. I_{OFF} in a TFET is dominated by a Shockley-Read-Hall (SRH) generation-recombination current in the reverse-biased p-i-n diode causing the small hump in between the two branches of the transfer characteristics. The SRH current is proportional to the intrinsic carrier concentration $n_i = \exp(-E_g/2k_BT)$, where k_B is the Boltzmann constant and T the temperature. The band gap difference ΔE_g between Si and sSi can be extracted from the I_{OFF} values of both devices by:

$$\frac{I_{OFF(sSi)}}{I_{OFF(Si)}} = \exp\left(\frac{\Delta E_g}{2k_BT}\right). \tag{3.1}$$

With I_{OFF} values shown in Fig.3.4 at $V_{DS} = -0.05\,\mathrm{V}$ the strain induced decrease of E_g was calculated to approximately $\Delta E_g = 30\,\mathrm{meV}$.

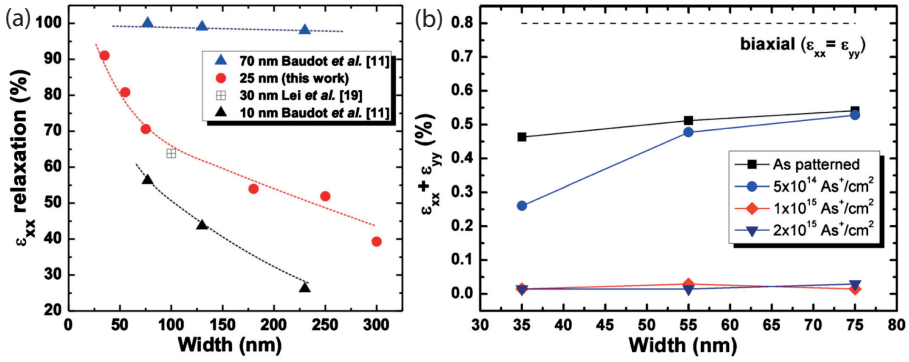

Figure 3.5: (a) Relaxation of strain across sSi Nanowires patterned from biaxial tensile strained Si layers as a function of NW width. (b) Strain in patterned NWs after implantation with different As fluence and spike annealing as a function of NW width measured by Raman spectroscopy. [69]

Deformation potential theory calculations in [62] provide values for the reduction of band gap energy in Si for strain ε of $\Delta E_g = -17.01\,\text{eV}\times\varepsilon$ for biaxial and $\Delta E_g = -6.19\,\text{eV}\times\varepsilon$ for uniaxial [110] tensile strain, respectively. In [69] NWs of different widths are patterned on SSOI substrate with a sSi thickness of 25 nm. Fig.3.5(a) shows the strain relaxation across a sSi NW in dependence of the NW width for different layer thicknesses. Fig.3.5(b) exhibits the sum of the lateral strain components measured by Raman spectroscopy for as-patterned NWs and NWs with different As^+ implantation fluence after spike annealing. According to these results one can assume that the strain across the sSi NWs with a cross-section of $20\times20\,\text{nm}^2$ in [89] is almost completely relaxed. This implies that the remaining strain in the NW is uniaxial in the [110] direction and ε can be estimated from Fig.3.5(b) to approximately $0.5\,\%$. Based on these results the band gap reduction due to the uniaxial strain in the NW of [89] becomes $\Delta E_g = -17.01\times0.5\,\% = -31\,\text{meV}$. This value is in good agreement with ΔE_g deduced from measured I_{OFF} values in Fig.3.4 (b). In order to increase the performance of SSOI NW TFETs further in this work a high-κ/metal gate stack is introduced in the fabrication process, enhancing electrostatic gate control.

3.3 Current-Voltage Characteristics of NW TFET and MOSFET

TFETs are a promising candidate for replacing MOSFETs especially in low power application. However, the possibility for steep switching slopes and small off-currents are only some of the points where TFETs differ from MOSFETs. Also other differences in the current-voltage (I-V) characteristics of TFETs and MOSFETs can have crucial implications on the behavior of integrated circuits for digital logic or analog applications. Thus, the I-V characteristics of a TFET need to be studied in depth to enable suitable circuit design. Deviations

in the *I-V* characteristics from a MOSFET may result in challenges but also in opportunities for new applications. In this section *I-V* characteristics of NW array TFETs and MOSFETs are presented and compared. The MOSFET and TFET devices are fabricated with the same process described in section 3.1 on the same chip. The only difference of MOSFET and TFET is the doping of source and drain regions. Whereas source and drain of the TFET are doped with the opposite doping type, in the MOSFET, both are doped with either As or B to form a n-MOSFET and p-MOSFET, respectively.
The *I-V* characteristics of the SSOI NW TFETs and MOSFETs were measured using a *Keithley SCS4200* semiconductor analyzer. Due to the symmetric design of the devices the TFET can be operated in n-channel as well as in p-channel mode. In the p-channel configuration the n-doped region acts as the source, whereas in the n-channel TFET the p-doped region becomes the source. The p-i-n junction in the TFET is reverse biased. For this reason the applied drain voltage V_{DS} is negative in case of the p-channel device and positive in case of the n-channel device. The source is in both cases put to ground potential. The applied gate voltage V_G, which opens the energy window for BTBT at the source-channel junction is negative in case of the p-channel and positive in case of the n-channel TFET. V_G is measured with respect to the grounded source contact. For the MOSFET applied V_{DS} and V_G are positive for the n-channel and negative for the p-channel device.

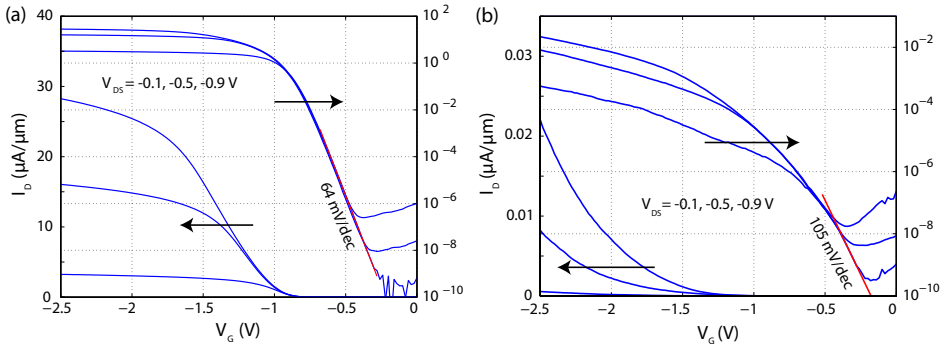

Figure 3.6: I_D-V_G characteristics of SSOI NW array (a) MOSFET and (b) TFET with $10 \times 10\,\mathrm{nm}^2$ NW cross-section and 400 nm gate length in linear and logarithmic scale of the I_D.

In the following, *I-V* characteristics of NW array MOSFETs and TFETs with $10 \times 10\,\mathrm{nm}^2$ NW cross-section and 400 nm gate length are compared. The drain current I_D is normalized to the circumference of the NW which is covered by the gate. The comparison is limited to p-channel TFET and MOSFET devices, since the performance of p-channel Si TFETs exceeds that of n-channel devices due to better tunnel junction quality at the As doped junction, which will be further discussed in section 3.4.2. The drain current I_D is measured for both devices in dependence of V_G at various fixed values for V_{DS} and in dependence of

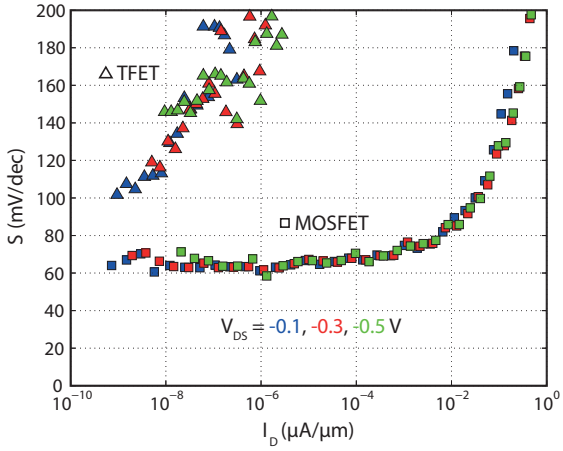

Figure 3.7: Inverse subthreshold slope S in dependence of I_D for SSOI NW array MOSFET and TFET with 400 nm gate length.

V_{DS} at different values for V_G. The former is also referred to as transfer characteristics while the latter is called output characteristics.

Fig.3.6 exhibits a comparison of transfer characteristics of p-MOSFET and p-TFET, both shown in logarithmic and linear y-axis scale. The characteristics of MOSFET and TFET reveal fundamental differences. The NW p-MOSFET switches over more than seven orders of magnitude of I_D with almost constant slope. This is shown more clearly in the graph of the inverse subthreshold slope S in dependence of I_D in Fig.3.7. S is close to the ideal 60 mV/dec with an average of 64 mV/dec between $I_D = 10^{-9}\,\mu$A/μm and $I_D = 10^{-5}\,\mu$A/μm. The shift of the transfer curves with increasing V_{DS} is very small proving a negligible drain induced barrier lowering (DIBL) effect. The close to ideal S and small DIBL indicates excellent gate control. The logarithmic TFET transfer characteristics in Fig.3.6 (b) exhibits a rather round shape compared to the MOSFET characteristics. S increases with I_D as shown in Fig.3.7 in contrast to the MOSFET, where S is constant over several orders of magnitude. The minimum slope in the TFET is 105 mV/dec. This behavior of transfer characteristics is conform with the theoretical expectation. The inverse subthreshold slope of a MOSFET is given by [49] (p.347):

$$S = \left(\frac{\partial \log(I_D)}{\partial V_G}\right)^{-1} = \frac{k_B T}{q} \ln 10 \left(1 + \frac{C_d + C_{it}}{C_{ox}}\right), \tag{3.2}$$

where C_{ox} is the oxide capacitance, C_d the depletion capacitance and C_{it} the interface capacitance. Hence, S is independent of V_G and constant in the subthreshold region. The ideal value for $S = (k_B T/q) \ln 10 \approx 60$ mV/dec at 300 K can only be reached, if C_{ox} is much larger than $C_d + C_{it}$. Small C_d requires a low channel doping and C_{it} depends on the interface

state density between channel and gate dielectric. The observed close to ideal value for S proves that this condition for the capacitances is fulfilled.
For a TFET the subthreshold slope is calculated as [48]:

$$S \approx \frac{\ln(10)}{e}\Delta\Phi\,, \tag{3.3}$$

if the tunneling probability T_{WKB} is close to unity, which means that the change of T_{WKB} with V_G is small. The dependence on the energetic overlap of source conduction and channel valence band $\Delta\Phi$, causes S to increase with the applied V_G, since the overlap $\Delta\Phi$ increases with rising gate potential. This dependence of S on V_G has crucial implications on TFET performance, since the average subthreshold slope over the whole current range from I_{OFF} to I_{ON} needs to be below 60 mV/dec to actually reduce the supply voltage compared to the MOSFET.
The off-currents (I_{OFF}) in MOSFET and TFET both are below $10^{-9}\,\mu$A/μm at $V_{DS} = -0.1\,$V. I_{OFF} increases in both devices with increasing V_{DS}. This effect is known as gate induced drain leakage (GIDL) in a MOSFET and is caused by BTBT at the channel drain junction due to the strong band bending at large gate-to-drain voltage difference. It is pronounced for devices with high-κ gate dielectrics and good electrostatic channel control due to the large potential variation of the channel bands with respect to the bands in the drain. The strong band bending decreases the BTBT distance at the channel-drain junction. In a TFET the increase of I_{OFF} with increasing V_{DS} is also caused by BTBT at the channel drain junction. The n-channel TFET is switched on due to the symmetric TFET design. The ambipolar behavior of a TFET degrades I_{OFF} and is especially problematic in digital logic circuits, since the OFF-state of the device is not well defined (see chapter 6).
Fig.3.8 shows the transconductance g_m of the NW MOSFET and TFET derived from the transfer characteristics. Also g_m exhibits a distinct difference for both devices. Whereas g_m of the MOSFET has a peak at V_G between $-1\,$V and $-1.5\,$V depending on V_{DS}, g_m of the TFET increases over the whole range of V_G.

Fig.3.6 and Fig.3.8 reveal that I_{ON} and g_m of the p-MOSFET are about three orders of magnitude higher compared to the p-TFET at the same bias conditions. This means that the resistance of the TFET is also three orders of magnitude higher. Since the NW p-TFET and p-MOSFET are fabricated with the same process on one chip, only with opposite doping types for the source, the channel resistance R_{ch} is comparable for both devices. From n- and p-MOSFETs with four different gate length the source-drain resistance $R_{S/D}$ was extracted. $R_{S/D}$ is 820 Ω and 1049 Ω for n- and p-MOSFETs, respectively [84]. Due to the n-doped source and p-doped drain of the p-TFET, $R_{S/D}$ of this device should be in between these values. Since R_{ch} and $R_{S/D}$ are in the same range for MOSFET and TFET the additional large series resistance of the TFET can be attributed to the resistance of the tunneling barrier R_{TB}. Channel resistance in a MOSFET is caused by the limited carrier mobility. Due to the much smaller current in the TFET channel mobility does not influence the

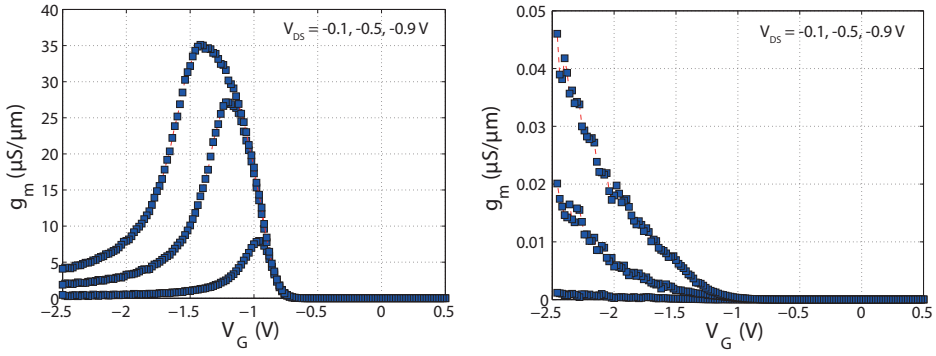

Figure 3.8: Transconductance g_m of the SSOI NW array MOSFET and TFET with 400 nm gate length.

TFET performance for the measured devices. However, one should note that R_{TB} depends on T_{WKB} with exponential dependence on the tunnel junction parameter E_g, m^* and λ. In the case of improved tunnel junction parameter, when T_{WKB} in eq. (2.12) becomes close to unity, the tunneling resistance can become comparable to R_{ch} and $R_{S/D}$. At this point the TFET current can be limited by channel mobility as in a MOSFET.

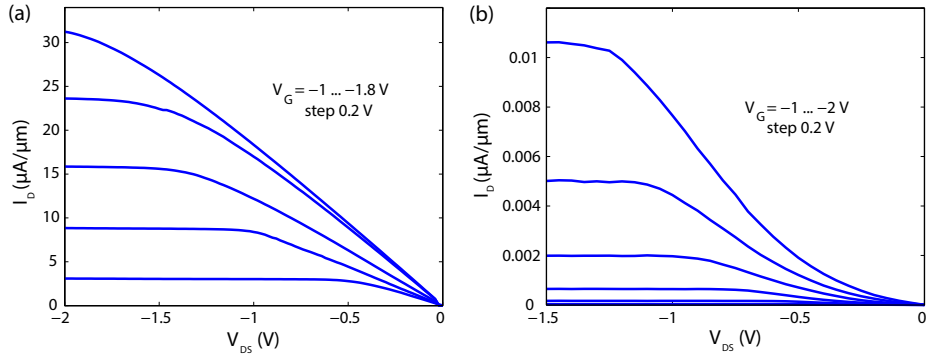

Figure 3.9: I_D-V_{DS} characteristics of SSOI NW array (a) MOSFET and (b) TFET with $10 \times 10\,\mathrm{nm}^2$ NW cross-section and 400 nm gate length.

Output characteristics of p-MOSFET and p-TFET are shown in Fig.3.9. Besides the difference in I_{ON}, also the shapes of the output curves differ. The onset of the MOSFET is linear and I_D saturates for increasing V_{DS}. The good current saturation of the devices once more proves small DIBL. The output characteristics of the TFET reveal a distinct S-shape, which is caused by drain induced barrier thinning (DIBT) [49]. The super-linear on-set, although it is often observed in TFET output characteristics, it is not an intrinsic TFET feature. Linear output characteristic of TFETs can be restored by adjusting the

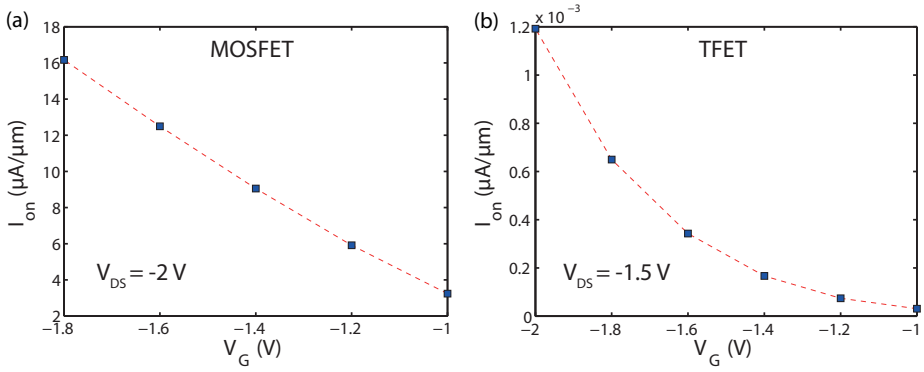

Figure 3.10: Gate voltage dependence of the on-current I_{ON} showing a linear dependence for the MOSFET (a) and en exponential dependence for the TFET (b).

Fermi distribution function in source and drain by a proper choice of doping levels [68][30]. Linear output characteristics are important in terms of digital logic application, since S-shaped I_D-V_{DS} characteristics would deteriorate the device performance. An additional striking difference of MOSFET and TFET output characteristics is the V_G dependence of I_{ON} shown in Fig.3.10 at $V_{DS} = -2\,\mathrm{V}$ and $-1.5\,\mathrm{V}$ for MOSFET and TFET, respectively. Values are extracted from the output characteristics in Fig.3.9. In case of the MOSFET I_{ON} increases linearly with V_G, indicating current limitation by velocity saturation due to large source-drain electric field [98]. For a MOSFET with lower source-drain electric field current is limited by the mobility. In the case of a constant mobility I_{ON} then increases with V_G^2. Thus, the V_G dependence of I_{ON} is always expected between these two extreme cases of constant mobility and velocity saturation. I_{ON} in the TFET, in comparison, exhibits an exponential dependence of V_G. This is in agreement with the theoretical expectation, since current in the TFET is limited by BTBT probability. I_{ON} is proportional to T_{WKB}, which depends exponentially on V_G.

3.4 TFET Performance

The performance of TFET devices is influenced by several different factors. From eq.(2.12) it is known that the material parameters E_g and m^* and the parameter λ, which is defined by the device structure and junction quality, are the most important ones. In the following the influences of device dimensions and junction quality on these parameters will be discussed and an additional effect caused by high electric fields in the junction is described.

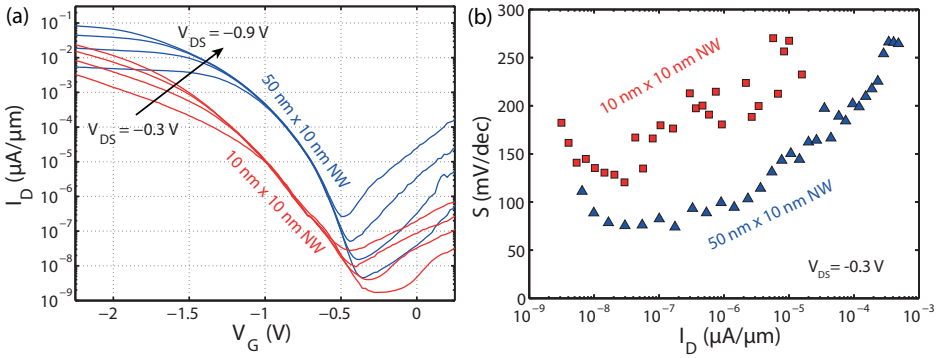

Figure 3.11: (a) Transfer characteristics of SSOI TFETs with 100 nm gate length and NW cross-sections of $50 \times 10\,\mathrm{nm}^2$ and $10 \times 10\,\mathrm{nm}^2$, respectively. (b) Inverse subthreshold slope S in dependence of I_D.

3.4.1 NW Cross-section and Gate Length

NW TFETs on SSOI have been fabricated with different NW cross-sections and gate lengths as described in section 3.1. A decrease in NW width results in an enhanced electrostatic gate control and thus a decreased λ_{ch} parameter in equation (2.12), which increases I_{ON} of the TFET. However there are additional effects that need to be taken into account, which will be discussed in this section.

Fig.3.11 (a) shows the comparison of transfer characteristics of SSOI NW TFETs with 100 nm gate length and NWs with 10 nm and 50 nm width, respectively. The transfer characteristics reveal higher on-current as well as steeper S for NWs with $50 \times 10\,\mathrm{nm}^2$ cross-section compared to $10 \times 10\,\mathrm{nm}^2$ NWs. Fig.3.11 (b) shows a comparison of S in dependence of I_D for these two devices. The minimum slope of the TFET with 50 nm NW width is 76 mV/dec and 120 mV/dec for the 10 nm NWs. S degrades more rapid with increasing I_D for the thinner NWs than for the wider NWs. This result is unexpected since a better electrostatic gate control and hence higher performance are expected for a TFET with narrower NWs at constant gate dielectric thickness. However, this result can be explained by the two contributions to the screening length λ, which is given by $\lambda = \lambda_{ch} + \lambda_{dop}$. λ_{ch} is influenced by the electrostatic channel control, whereas λ_{dop} depends on the steepness of the source doping profile.

In case of the narrower NWs on the one hand λ_{ch} is decreased, but on the other hand λ_{dop} increases. The tunnel junction formation by ion implantation and spike annealing for activation is affected by the width of the NW. Dopant diffusion in Si NWs can be much higher compared to bulk Si [52]. The diffusion coefficient D of boron in vapor liquid solid (VLS) grown Si NWs for example was reported to be as high as $D = 4.22 \times 10^{-16}\,\mathrm{cm}^2/\mathrm{s}$ [11] compared to a bulk diffusivity of $\approx 10^{-18}\,\mathrm{cm}^2/\mathrm{s}$ at 500 °C [67]. The increased diffusivity is presumably caused by a larger dopant diffusion along the NW surface, due to impurities at

the interface to the gate dielectric [52]. The smaller NW has a larger surface to volume ratio, which could further enhance dopant diffusion compared to the wider NW. Increased dopant diffusion causes a broadening of the doping profiles in the junctions leading to degradation of λ_{dop} and thus smaller I_{ON} and larger S. I_{OFF} in the 10 nm NW TFET benefits from the increased boron diffusion at the drain junction. BTBT at the channel-drain junction is suppressed leading to reduced ambipolarity and smaller I_{OFF} compared to the 50 nm NW. Another aspect why the TFET with wider NWs outperforms the one with thinner NWs could be the reduction of E_g by the tensile strained substrate. As shown in section 3.2 the strain across a patterned NW relaxes and uniaxial strained NWs are obtained. The degree of relaxation, however, depends also on the NW cross-section. According to Fig.3.5 the strain across thin but wide NWs does not fully relax. Hence, a larger remaining strain component across the 50 nm NW would result in a smaller band gap compared to the 10 nm NW. Also a smaller crystalline seed layer in the narrower NWs after ion implantation may prevent SPER during dopant activation and result in higher trap density in the tunnel junction.

Fig.3.12 shows the dependence of I_{ON} on the gate length l_g of a TFET with 50 nm NW width for different V_{DS}. In comparison to a MOSFET, where I_{ON} increases with decreasing gate length, I_{ON} in the TFET is constant for gate length between 100 nm and 2 μm. As discussed above I_{ON} in a MOSFET is determined by the channel resistance, which decreases for shorter channel length l_{ch}. As long as the source-drain resistance is small compared to R_{ch} I_{ON} is proportional to $1/l_{ch}$. In the TFET, however, the dominant resistance is given by the tunnel junction. BTBT is confined to a small region of only a few nanometer around the source-channel tunnel junction at the edge of the gate. Hence the current in the TFET is independent of the gate length.The assumption of a dominant tunnel junction resistance is valid for the measured devices as shown in the comparison of MOSFET and TFET in section 3.3. However, for further improved tunnel junctions with lower resistance channel length and mobility could influence I_{ON} in a TFET and introduce a gate length dependence to I_{ON}.

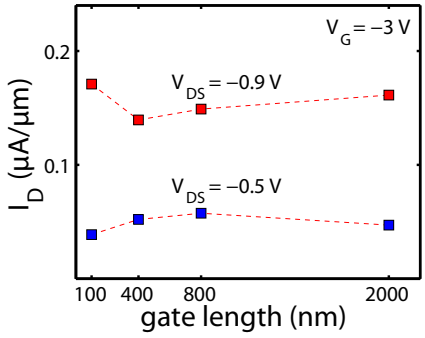

Figure 3.12: Drain current I_D of SSOI NW array TFET with 50 nm NW width in dependence of the gate length.

3.4.2 Doping Profiles

As discussed in the previous section λ_{dop} has an important influence on the TFET performance. This can also be seen when p- and n-channel characteristics of the TFETs are compared. The transfer characteristics of a p- and n-channel NW array TFET with 100 nm gate length and a NW cross section of $50 \times 10\,\mathrm{nm}^2$ are shown in Fig.3.13 for various V_{DS}. A minimum S of the p-channel device with 76 mV/dec and an average slope of 97 mV/dec over four orders of magnitude of I_D at $V_{DS} = -0.3\,\mathrm{V}$ were achieved. The I_{ON}/I_{OFF} ratio reaches 10^6 at these bias conditions. The n-channel TFET in comparison reveals a minimum S of 240 mV/dec. Also I_{ON} is about one order of magnitude smaller for the n-TFET compared for $\Delta V_G = 1.5\,\mathrm{V}$ from the minimum of the I-V curve. The inferior n-channel performance can be attributed to a broader doping profile in the corresponding tunnel junction. The dopant diffusivity D in dependence of the temperature T is calculated by $D = D_0 \cdot \exp(-E_A/k_B T)$ with the activation energy E_A. At 1000 °C the diffusivity of As and B in bulk Si is $1.46 \times 10^{-15}\mathrm{cm}^2/\mathrm{s}$ and $1.39 \times 10^{-14}\mathrm{cm}^2/\mathrm{s}$, respectively [92]. Due to the one order of magnitude smaller diffusivity of As compared to B, the n^+-channel junction, which acts as the tunnel junction in a p-TFET, has a steeper doping profile compared to the p^+-channel junction in a n-TFET. The thermal treatment for dopant activation is crucial with regard to the dopant profile in the junction. The 1000 °C spike annealing, which was chosen for activation, is supposed to result in a high dopant activation and limit dopant diffusion by short process time. However, the time to ramp up to the 1000 °C and down again in the rapid thermal processing (RTP) system leads to a broadening of the dopant distribution at the junction. This effect is pronounced in NWs due to even larger diffusion coefficients compared to bulk Si as discussed in the previous section.

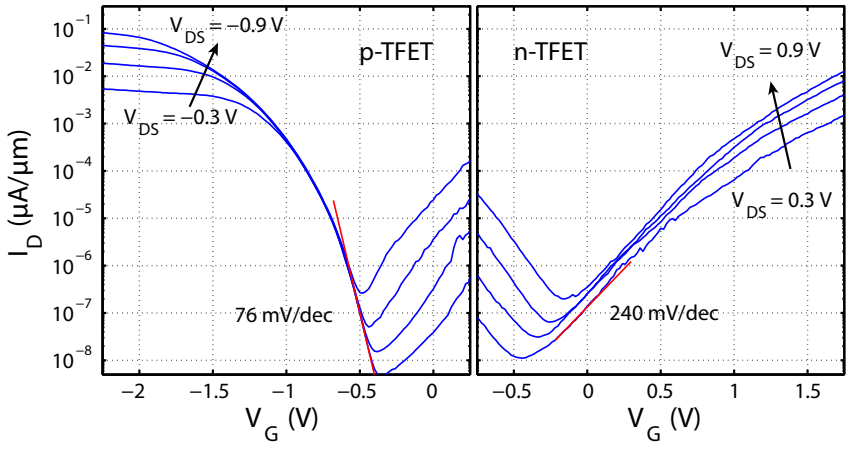

Figure 3.13: Transfer characteristics of p-channel (left) and n-channel (right) SSOI NW array TFET with 100 nm gate length.

Dopant activation by flash lamp annealing (FLA) and excimer laser annealing (ELA) are possible ways of decreasing dopant diffusion. ELA in combination with a low temperature regrowth anneal at 650 °C in a RTP-system in [95] increased I_{ON} by one order of magnitude and lowered S compared to reference devices activated by spike annealing.
The GIDL like increase of I_{OFF} in the transfer characteristics of the TFET is caused by BTBT tunneling at the channel-drain junction. This effect is demonstrated in Fig.3.14. I_D is measured as a function of V_{DS} at $V_G = 0\,\mathrm{V}$ for p- and n-channel configuration. An energy overlap of drain valence and channel conduction band in the p-TFET and drain conduction and channel valence band in the n-TFET occurs at sufficient high voltage difference between drain and channel. This condition is illustrated in the band structure plot in the insets of Fig.3.14. Under these conditions the ambipolar nature of the TFET becomes visible since electrons tunnel into the conduction band of the p-TFET whereas holes tunnel into the valence band of the n-TFET. I_D in the n-TFET configuration is about one order of magnitude higher than I_D in the p-TFET configuration. This again demonstrates the higher junction quality of the As doped n^+-junction compared to the B doped p^+-junction.

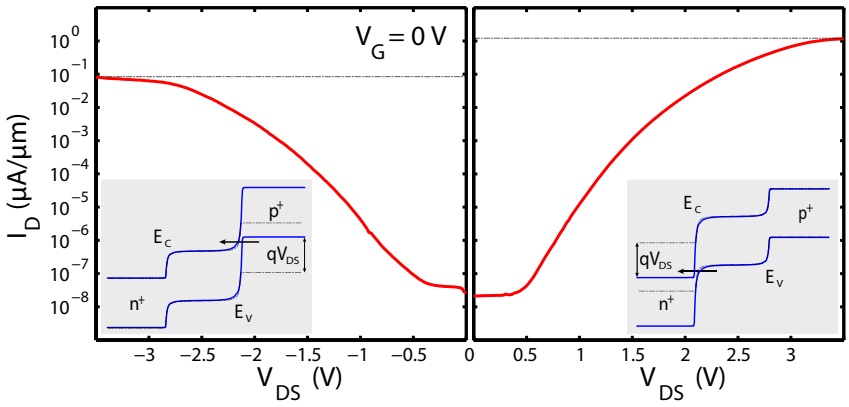

Figure 3.14: Measured drain current I_D as a function of applied drain voltage V_{DS} for $V_G = 0\,\mathrm{V}$ in p-channel (left) and n-channel (right) configuration.

A comparison of the p-channel TFET presented here to SSOI NW TFETs with similar processing but SiO_2 dielectric and poly-Si gate in [89] reveals an increase in I_{ON} of two orders of magnitude for the same bias conditions. For $V_{DS} = -0.5\,\mathrm{V}$ and $\Delta V_G = -1.5\,\mathrm{V}$ from the minimum of the transfer curve the p-TFET with high-κ dielectric and metal gate reaches $I_D = 0.02\,\mu\mathrm{A}/\mu\mathrm{m}$. The increased gate control by the high-κ dielectric also improves the I_{ON}/I_{OFF} ratio by the steeper S and smaller I_{OFF}. The performance of the p-channel TFET is similar to that of in-situ doped Si NW TFETs reported in [75].

3.4.3 Hot Carrier Effects in Tunnel Junctions

High-κ gate dielectrics enable good electrostatic gate control and enhance TFET performance as shown in the previous section. However, the increased electric fields in the devices can also cause additional effects deteriorating performance and reliability. Fig.3.15 (a) shows the output characteristics of a p-channel SSOI NW TFET with 100 nm gate length. I_{ON} reaches $2.3\,\mu\text{A}/\mu\text{m}$ at $V_{DS} = -2.4\,\text{V}$ and $V_G = -4.5\,\text{V}$. The output characteristics exhibit a negative differential conductance (NDC) for $\mid V_G \mid \geq 3.5\,\text{V}$. The origin of this NDC can be explained by a hot carrier effect. In a MOSFET hot carriers are created at the channel-drain junction due to the large electric field [14], whereas in a TFET hot carriers are created at the source-channel junction [72]. The inset in Fig.3.15 (a) demonstrates how the I_D-V_{DS} curve is degraded when measured consecutively at $V_G = -4.5\,\text{V}$.
Simulations of the valence and conduction band energies in a TFET biased at $V_G = -3.5\,\text{V}$ and $V_{DS} = -2\,\text{V}$ are shown in Fig.3.15 (b). The gate dielectric used in the simulation constists of 2 nm SiO_2 and 3 nm HfO_2 as in the measured TFET device. The tunnel junction between the n^+-source and the intrinsic channel is strongly reverse biased causing a large electric field at this junction. Fig.3.15 (c) exhibits the simulated electric field E as a function of the distance from source-channel interface in the devices with a 2 nm SiO_2/3 nm HfO_2 dielectric layer as well as with a 5 nm SiO_2 gate dielectric at $V_{DS} = -2\,\text{V}$ and $V_G = -3.5\,\text{V}$ and $-4.5\,\text{V}$, respectively. E in a device with the high-κ HfO_2 exceeds the electric field in a device with SiO_2 even for 1 V less gate voltage.
The large electric field in the tunnel junction creates hot carriers which are capable of entering the oxide and introducing traps. These oxide traps screen the gate electric field, lowering $\Delta\Phi$ from equation 2.12 in the channel region. The reduction of gate control hence leads to a decrease in tunneling probability and decreased I_D.

In order to prove the trap generation at the oxide interface, charge pumping measurements (as explained in 2.4.3) have been performed at the TFETs before and after I-V characterization of the devices. Fig.3.16 shows the charge pumping current I_{cp} measured in dependence of the base voltage V_{base} of the applied gate voltage pulses. I_{cp} is measured before and after measuring the I_D-V_{DS} characteristics. The number of oxide interface traps N_{it} per area can be calculated from I_{cp} by

$$N_{it} = \frac{I_{cp}}{A \cdot f \cdot q} \tag{3.4}$$

where A is the area of the gate channel interface, f the frequency of the voltage pulses and q the elementary charge. The gate-channel interface area for the tri-gated NW with a cross-section of $50 \times 10\,\text{nm}^2$ and 100 nm gate length is $7 \times 10^{-8}\,\text{cm}^2$. I_{cp} was measured with $f = 1\,\text{MHz}$. N_{it} extracted from the measurement in Fig.3.16 is $8.7 \times 10^{11}\,\text{cm}^{-2}$ before and $3.14 \times 10^{12}\,\text{cm}^{-2}$ after measuring I_D-V_{DS} characteristics up to $V_G = -4.5\,\text{V}$. This confirms interface trap generation at the gate oxide leading to the NDC in the output characteristics.

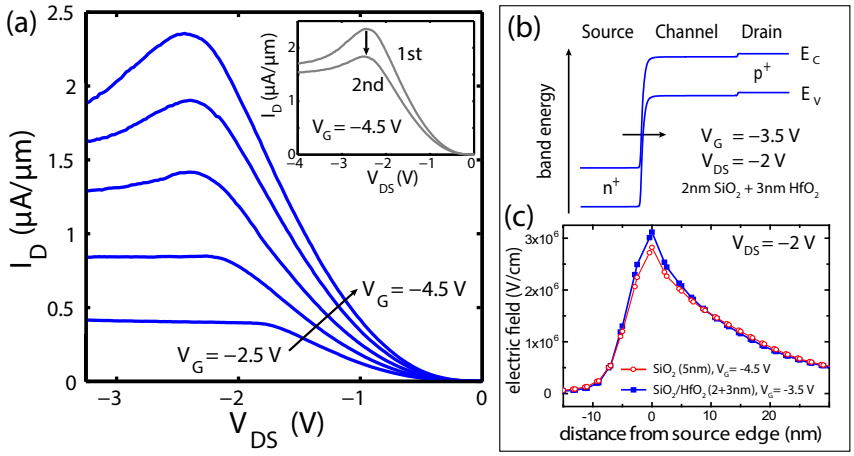

Figure 3.15: (a) Output characteristics of p-channel NW TFET with 100 nm gate length and 50 nm NW width. Negative differential conductance occurs for $\mid V_G \mid \geq 3.5\,\mathrm{V}$. Inset shows the deterioration of repeatedly measured I_D-V_{DS} curves; (b) Simulated band energies of valence and conduction band under bias condition $V_G = -3.5\,\mathrm{V}$ and $V_{DS} = -2\,\mathrm{V}$; (c) Electric field as a function of the distance from the source-channel junction.

One should note that the applied voltages for V_G and V_{DS} in this case are too high for actual TFET application, since TFETs are supposed to work as energy efficient switches at low voltages. However, for decreased equivalent oxide thickness (EOT) and smaller NW cross section this effect could become significant also at smaller bias voltage. Moreover hot electrons in the tunnel junction could lead to heating effects in the devices influencing device performance.

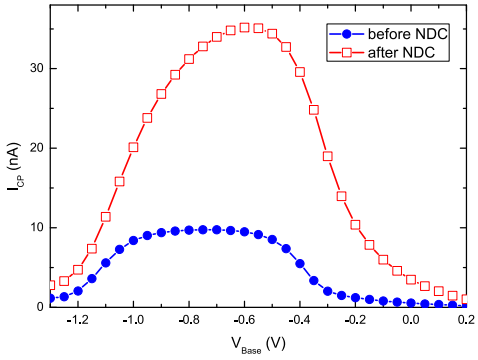

Figure 3.16: Charge pumping current I_{cp} measured as a function of V_{base} before and after I-V characteristics of the TFET device were measured up to $V_G = -4.5\,\mathrm{V}$.

3.5 Low Temperature I-V Characteristics

Temperature dependent measurements of the fabricated devices allow for a more detailed analysis of the transport mechanism in TFETs. Therefore the I-V characteristics of the SSOI NW TFET were measured temperature dependent at a probe station cooled with liquid nitrogen. Fig.3.17 (a) shows transfer characteristics of a p-TFET with 100 nm gate length and 50 nm NW width measured at $V_{DS} = -0.3\,\mathrm{V}$ in a temperature range from 100 K to 350 K. I_D decreases with decreasing temperature. At $V_G = -1\,\mathrm{V}$ I_D decreases by only a factor of 4, while I_D reduction at $V_G = -0.4\,\mathrm{V}$ is about three orders of magnitude. The flattening of transfer characteristics in the off-region at lower temperature is caused by the limitation of the measurement setup. Hence, I_{OFF} can only be reliably measured for the two highest temperatures. In Fig.3.17 (b) the minimum S of the transfer curves in Fig.3.17 (a) is extracted. As a comparison the theoretical expected dependence of S on T for a MOSFET with the same initial S at 350 K is shown. As already seen in equation (3.2) S of the MOSFET has a first order linear dependence on T. Even if the electrostatic gate control is not ideal and hence the condition $C_{ox} \gg C_d + C_{it}$ is not valid, S goes to zero for 0 K. At 0 K the Fermi distribution function becomes step function and thermal emission over the potential channel barrier starts instantaneously when a certain V_G is reached.

For a TFET no first order temperature dependence for S is expected as shown in equation (3.3). In the BTBT transport process the high- and low-energy tail of the Fermi-Dirac distribution are cut off, which makes the BTBT independent of the broadening of the distribution. The thickness of the tunneling barrier depends on the shift of the bands in the channel region and hence on the applied V_G but not on T. The dependence of S on T for the TFET in Fig.3.17 (b) exhibits a much smaller temperature dependence compared to the MOSFET, however, it is not constant. Temperature dependence in the TFET arises for example due to the change of band gap energy E_g with T. I_D depends exponentially on E_g as shown in equation (2.12). Furthermore BTBT is a phonon assisted process in indirect semiconductors such as Si. Temperature dependence of phonons could also influence the transfer characteristics. An important aspect for the temperature dependence is given by trap assisted tunneling (TAT) processes, which freeze out at low temperatures. TAT can add a large contribution to I_D and degrade S especially at low V_G, when the energetic overlap of source conduction and channel valence band is not sufficient to allow for direct BTBT. The freeze out of TAT can explain the large T dependence of I_D at small V_G.

Fig.3.18 exhibits the drain current I_D as a function of T for $V_G = -1\,\mathrm{V}$. At sufficiently high V_G BTBT dominates I_D and TAT can be neglected. In this case the main temperature dependence in the TFET is given by the change of E_g with T as long as a temperature dependence for the phonon assisted BTBT process can be neglected.

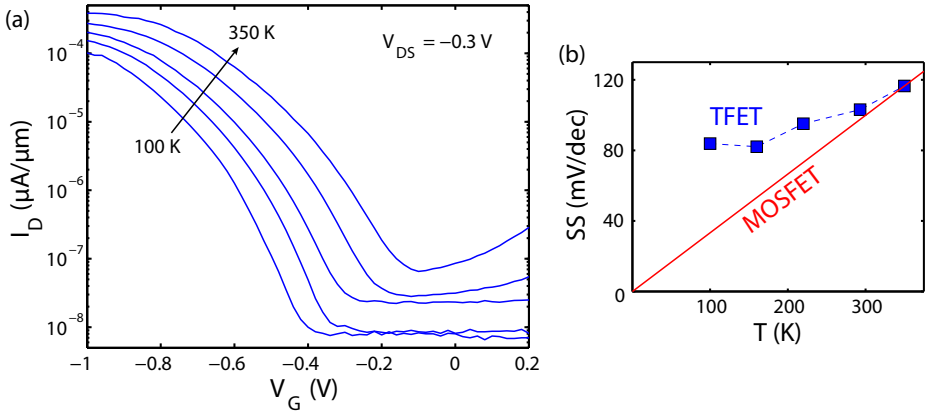

Figure 3.17: (a) Transfer characteristics of SSOI NW array TFET with gate length 100 nm and NW width 50 nm measured temperatures from 100 K to 350 K; (b) Measured inverse subthreshold swing S of a TFET as a function of T. For comparison the theoretical values for S of a MOSFET with the same initial slope as the TFET at 350 K is shown as a red line.

The temperature dependence of E_g is given by:

$$E_g(T) = E_g(T = 0\,\mathrm{K}) - \frac{\alpha T^2}{T + \beta}\,, \tag{3.5}$$

with the constants α and β. The parameters α and β are taken for Si and E_g at 0 K is corrected for uniaxial strained Si according to [62] and the discussion in section 3.2 by $\Delta E_g = -30\,\mathrm{meV}$. The corresponding temperature dependence of E_g is plotted in Fig.3.18 (b). Combining eq. (3.5) and the WKB approximation for I_D from equation (2.12) we obtain:

$$I_D = c \cdot \exp\left(-\frac{4\lambda\sqrt{2m^*}}{3\hbar} \cdot \frac{\left(E_g(T = 0\,\mathrm{K}) - \frac{\alpha T^2}{T+\beta}\right)^{3/2}}{\Delta\Phi + E_g(T = 0\,\mathrm{K}) - \frac{\alpha T^2}{T+\beta}} \right)\,, \tag{3.6}$$

where c is a constant, which is independent of T. The parameter λ can be roughly calculated by

$$\lambda = \sqrt{\frac{\varepsilon_{Si} t_{Si} \left(t_{SiO_2} + t_{HfO_2} \frac{\varepsilon_{SiO_2}}{\varepsilon_{HfO_2}} \right)}{\varepsilon_{SiO_2}}}\,, \tag{3.7}$$

assuming that λ for a $50 \times 10\,\mathrm{nm}^2$ NW is closer to the planar case. ε_{Si}, ε_{SiO_2} and ε_{HfO_2} are the dielectric constants of Si, SiO_2 and HfO_2, respectively. t_{Si}, t_{SiO_2} and t_{HfO_2} are the thicknesses of the Si substrate, the SiO_2 interfacial layer and the HfO_2, respectively. The reduced tunnel mass m^* is assumed to be $m^* = 0.087$ as for indirect BTBT in [110] direction for Si [42]. $\Delta\Phi$ denotes the energy window between source conduction band and

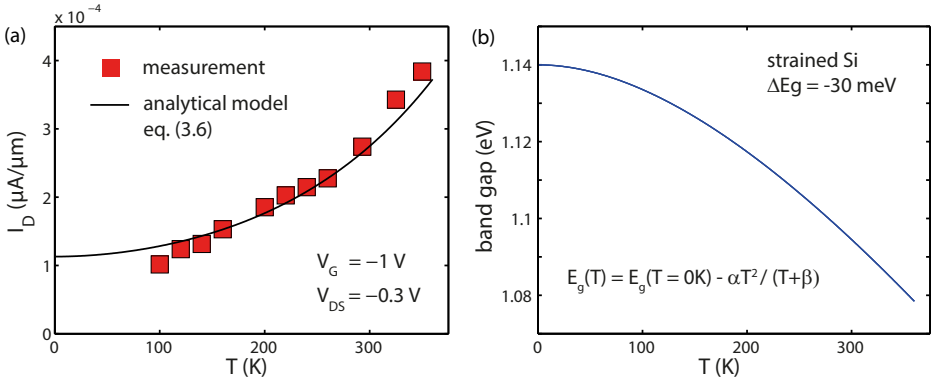

Figure 3.18: (a) Measured drain current I_D at $V_G = -1\,\mathrm{V}$ and $V_{DS} = -0.3\,\mathrm{V}$ as a function of temperature as red squares. Analytical temperature dependence according to equation (3.6) with a fitted constant c is shown as black solid line; (b) Band gap of strained Si as a function of temperature.

channel valence band and can be estimated from band structure simulations to $\Delta\Phi = 0.1\,\mathrm{eV}$ for $V_G = -1\,\mathrm{V}$. The solid black line in Fig.3.18 (a) is calculated using (3.6) and fitting the constant c to the measured values of I_D. The analytical expression is in good agreement with the measured values, indicating that the temperature dependence is in fact dominated by the temperature dependence of E_g.

Trap Assisted Tunneling

The change of S with T observed in 3.17 can be attributed to additional conduction mechanisms, such as thermally-assisted tunneling through trap states. TAT in a TFET can be modeled as a Poole-Frenkel (PF) mechanism [73]. The PF mechanism was originally used to model the field-enhanced thermal excitation of carriers in oxide traps [98]. This mechanism can be adapted for carriers in a TFET tunneling into trap states within the band gap from the source and reaching the channel by thermal excitation. Fig.3.19 illustrates this process in a p-channel TFET. The trap state is modeled as a potential well in the valence band. According to [98] the temperature dependence of a PF emission current is given by:

$$I_D \propto V_G \cdot \exp\left(\frac{q}{k_B T}(2a\sqrt{V_G} - \phi_B)\right), \tag{3.8}$$

where ϕ_B is the barrier height and $a = \sqrt{q/4\pi\varepsilon_{ox}d}$. Plotting $\ln(I_D/V_G)$ as a function of $1/k_BT$ a straight line can be fitted to the data points. The barrier height can be extracted from the slope m of the straight line according to

$$\phi_B = 2a\sqrt{V_G} - m(V_G)\,. \tag{3.9}$$

Fig.3.20 shows a plot for ϕ_B extraction at $V_G = -0.44\,\text{V}$. At this gate voltage I_D changes three orders of magnitude in the measured temperature range. In order to calculate ϕ_B the thickness d, which corresponds to the equivalent oxide thickness (EOT), was estimated to $2.8\,\text{nm}$ from TEM images in Fig.3.3. A barrier height of $\phi_B = 0.55\,\text{eV}$ was extracted, which corresponds to about $E_g/2$ of the sSi TFET. This proves that TAT through mid-gap trap states dominates the current transport at small V_G, causing a large temperature dependence in this region. The thermal emission in the TAT process limits S to the same constrictions as the MOSFET. Hence, TAT degrades S in the TFET and introduces a temperature dependence of S as shown in Fig.3.17 (b). As TAT processes freeze out at low temperature S of the TFET becomes constant at around $T = 100\,\text{K}$.

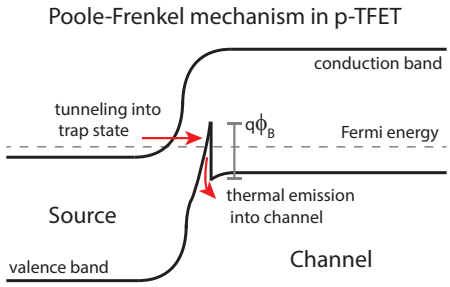

Figure 3.19: Schematic illustration of the Poole-Frenkel mechanism adapted for a trap assisted tunneling process with thermal excitation from a trap state in a p-TFET. The trap state is modeled as a potential well in the valence band.

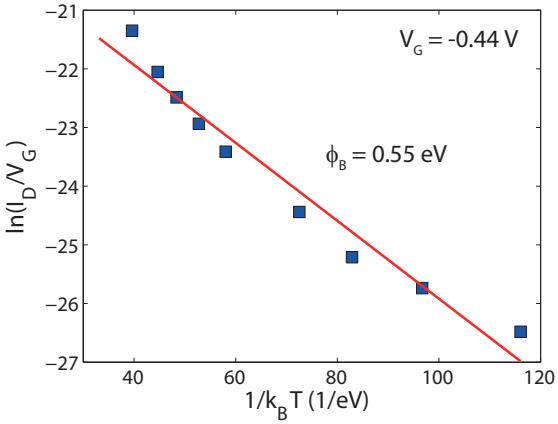

Figure 3.20: Extraction of the barrier height ϕ_B for thermal excitation from trap states in a trap assisted tunneling (TAT) process according to the Poole-Frenkel (PF) mechanism.

3.6 Conclusion

The comparison of NW array TFETs and MOSFETs fabricated on SSOI substrate in this chapter revealed distinct differences in the device characteristics. Compared to the constant close to ideal inverse subthreshold slope of the MOSFET devices S in the TFET degrades with increasing V_G. The output characteristics show S-shaped on-set and an exponential increase of I_{ON} with V_G. The decrease of E_g due to the uniaxial tensile strain in the NWs could have been estimated from SOI and SSOI NW TFETs in [23] and deformation potential calculations in [62] in good agreement to about 30 meV. Compared to SSOI NW TFETs using SiO_2/poly-Si gates in [23] the devices in this work with HfO_2/TiN gate stack exhibit two orders of magnitude higher on-current and significantly decreased S down to 76 mV/dec. Even though small NW cross-section proved good electrostatic gate control as confirmed by MOSFET devices, the formation of steep junctions by ion-implantation and spike annealing is more challenging and TFET performance can be degraded. In addition different diffusion constants for p- and n-dopants cause different performance for p- and n-channel TFETs. Furthermore, degradation of TFET performance by a hot carrier effect occurring due to high electric fields in the tunnel junction has been demonstrated.

Temperature dependent measurements of the TFET transfer characteristics showed that TAT through mid-gap trap states dominates I_D at small V_G. This leads to a degradation and temperature dependence of S. At higher V_G BTBT dominates and the temperature dependence of E_g is responsible for the change in I_D.

From these results it can be concluded that the reduction of E_g by using strained Si substrates in combination with good electrostatic gate control of a high-κ/metal gate in tri-gate configuration improves TFET performance. However the BTBT current is still orders of magnitude smaller than thermal emission current in a MOSFET with analog device processing. Further reduction of E_g seems to be the most promising way to further increase I_{ON} in a TFET. The reduction of traps in the tunnel junction is crucial for achieving steep inverse subthreshold slopes.

The exponential dependence of I_{ON} on V_G in combination with very low I_{OFF} could make TFETs interesting for low power sensing application. In this field of application high I_{ON} is less important since switching times in the range of kHz might be sufficient. Beyond that the higher temperature stability of the TFET compared to a MOSFET could make the devices suitable for high temperature application.

4 SiGe Homostructure NW TFET

As shown in the previous chapter small band gap materials are indeed advantageous to increase the TFET performance. In this chapter similar nanowire array TFETs based on the group IV compound semiconductor silicon-germanium (SiGe) are presented. SiGe allows to further decrease the band gap at the tunnel junction. The utilization of compressively strained SiGe layers due to pseudomorphic growth on Si reduces the band gap even further. Besides the reduced band gap standard CMOS compatible processes can be used to fabricate SiGe TFETs. The processing of SiGe NW TFETs as well as the $I-V$ characterization at room temperature and low temperature are presented. Furthermore the cleaning and passivation of SiGe layers prior to high-κ deposition as one of the major challenges is discussed.

4.1 Strained SiGe on SOI Substrate

The substrate, which was used for the fabrication of the SiGe NW TFETs, consists of a 15 nm thick $Si_{1-x}Ge_x$ layer grown by reduced pressure chemical vapor deposition (RP-CVD) pseudomorphically on a SOI wafer [36]. The Si(001) layer of the SOI wafer has a thickness of 15 nm. The SiGe layer is capped with 5 nm Si to prevent oxidation of the Ge. The layer stack is illustrated in Fig.4.2 (a). Two different wafer types with Ge contents of $x = 35\,\%$ and $x = 50\,\%$ have been used. The lattice constant of $Si_{1-x}Ge_x$ for different Ge contents x can be calculated with high accuracy of 10^{-4} nm by the approximation [80]:

$$a_{Si_{1-x}Ge_x} = 0.5431 + 0.01992x + 0.0002733x^2\,(\text{nm})\,. \tag{4.1}$$

For Ge mole fractions up to 80 % unstrained SiGe aloys are Si-like with an indirect Γ-Δ band gap [24]. The unstrained SiGe band gap decreases for increasing Ge mole fraction and can be calculated by:

$$E_g = 1.12 - 0.41x + 0.008x^2\,(\text{eV}) \tag{4.2}$$

for 300 K, which results in $E_g = 0.98\,\text{eV}$ and $E_g = 0.92\,\text{eV}$ for $x = 35\,\%$ and $x = 50\,\%$, respectively.

Due to the pseudomorphic growth on SOI the in-plane lattice constant of the SiGe adapts to the smaller lattice constant of the Si layer. Hence, biaxial compressive strain is introduced in the SiGe layer. The compressive strain has values of $\varepsilon = -0.98\,\%$ and $\varepsilon = -1.41\,\%$ for $x = 35\,\%$ and $x = 50\,\%$, respectively. The tetragonal lattice distortion of the SiGe causes an

increase of the out-of-plane lattice constant. The corresponding out-of-plane stress component is $\sigma_{zz} = -1.18\,\text{GPa}$ and $\sigma_{zz} = -1.64\,\text{GPa}$ for $x = 35\,\%$ and $x = 50\,\%$, respectively. The change of the effective electron mass $m^{(\Delta)}$ with Ge mole fraction in the Δ-band is negligible. Also the strain induced by pseudomorphic growth does not affect $m^{(\Delta)}$. The effective hole mass m_{v2} of the highest valence band at the Γ-point decreases by a factor of 4 from 0 % to 50 % Ge in the strained SiGe layer [24]. Fig.4.1 shows valence and conduction band energies at various symmetry points for SiGe pseudomorphically grown on Si as calculated in [24]. The biaxial compressive strain decreases E_g at 50 % Ge from $E_g = 0.92\,\text{eV}$ to about $0.67\,\text{eV}$. Hence, the biaxial compressive strain of SiGe grown on $\langle 001 \rangle$Si is beneficial for the TFET operation due to reduction of the Γ-Δ band gap and the effective hole mass, as shown in equation (2.12).

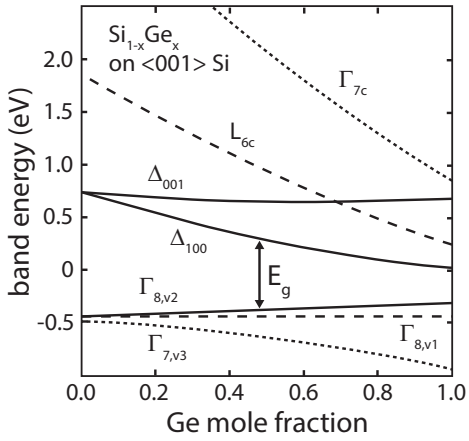

Figure 4.1: Valence and conduction band energies of $Si_{1-x}Ge_x$ pseudomorphic on Si as a function of Ge mole fraction x. Adapted from [24].

4.2 SiGe on SOI NW TFET Fabrication

Fig.4.2 (b) shows a schematic of a single SiGe on SOI NW with tri-gate configuration. The SiGe on SOI NW TFET consists of an array of 1200 NWs. The process flow is based on the process for the SSOI NW TFET introduced in section 3.1 . The important changes to the process are listed in the following:

- The dry etching of the NWs and mesa structure is changed to a Cl_2/Ar plasma, in order to achieve steeper side wall profile of the NWs for the increased etching depth of 35 nm. The NW width after etching is about 40 nm. Fig.4.3 (a) shows a top view SEM image of a SiGe NW array with $2.4\,\mu$m long NWs. The sharp bright edges of the NWs indicate steep flanks of the NWs. This is also confirmed by the tilted angle SEM

image in Fig.4.3 (b). The side wall of the NW etched into the $Si/Si_{0.5}Ge_{0.5}/Si$ stack is smooth and shows no sign of underetchning of the SiGe.

- Since the side walls of the NWs exhibit the exposed SiGe layer standard RCA cleaning cannot be applied as cleaning method prior to the gate stack deposition. The etching rates of the different cleaning solutions containing H_2O_2 is too high and results in a complete dissolution of the SiGe layer of the NWs. Instead of RCA cleaning a process of HF etch back of the native oxide and ozone oxidation for passivation in a "Semitool Raider" automated wafer cleaning tool was used. A detailed description of this process will be given in the following section.
- The gate stack consists of the gate dielectric Al_2O_3 and gate metal TiN deposited by ALD and AVD, respectively.
- Dopant activation was carried out at only 650 °C for 1 minute in order to prevent Ge diffusion.

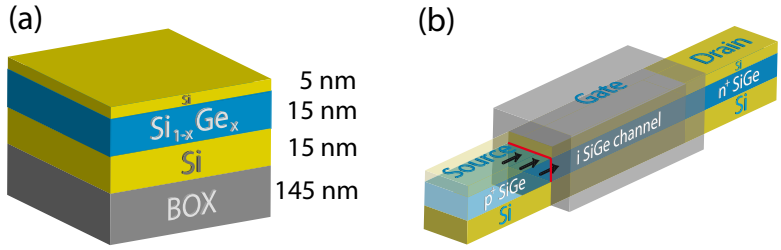

Figure 4.2: (a) Illustration of the $Si_{1-x}Ge_x$ on SOI layer stack with corresponding layer thicknesses; (b) Schematic of a single SiGe on SOI NW with tri-gate in a n-channel TFET.

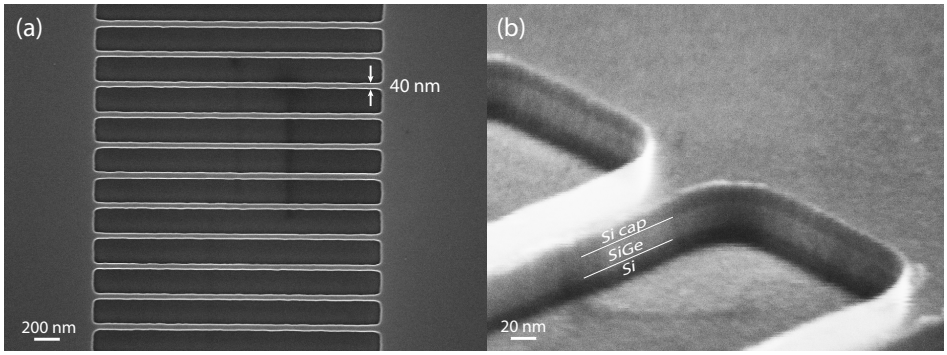

Figure 4.3: (a) Top view SEM image of a SiGe on SOI NW array with 2.4 μm long and 40 nm wide NWs; (b) Tilted angle SEM image of a NW array etched into a $Si/Si_{0.5}Ge_{0.5}/Si$ stack with Cl_2/Ar dry etching.

4.3 High-κ/Metal Gate Stack on SiGe

The cleaning process of the sample surface prior to the gate stack deposition is important in order to reduce the number of interface traps and to achieve a good electrostatic gate control in the device. Hence, an efficient process to remove particles and metallic contamination from the sample surface is needed that consumes as little material as possible. In case of high-κ deposition also the surface termination plays an important role in terms of interface layer quality. The Radio Corporation of America (RCA) cleaning process [43], which is used as a standard wet-cleaning for Si, is not suitable for SiGe alloys due to a high material consumption in the hydrogen peroxide based cleaning solutions [56]. The etching rate of $Si_{1-x}Ge_x$ increases with higher Ge content x.
A cleaning process based on an oxide removal using diluted HF (dHF) and a subsequent oxide formation by water with a few parts per million of ozone presented in [2] shows good results and reduces metallic contamination to a surface density of less than 10^{10} atoms per cm^{-2} independent of the Ge content. The thickness of the resulting oxide layer increases in this connection with the Ge content. XPS spectra confirm that the oxide layer consists mainly of SiO_2 and only to about 1 % of GeO_2 and GeO_x [1].
Based on these results the SiGe NWs in this work were cleaned by a process using dHF in combination with diluted HCl (dHCl) and a subsequent O_3 oxidation in water to form a thin SiO_2 layer. The cleaning was performed in a *Semitool Raider* automated wafer cleaning tool. The resulting oxide layer provides a passivation of the SiGe for the Al_2O_3 gate dielectric deposited by ALD.

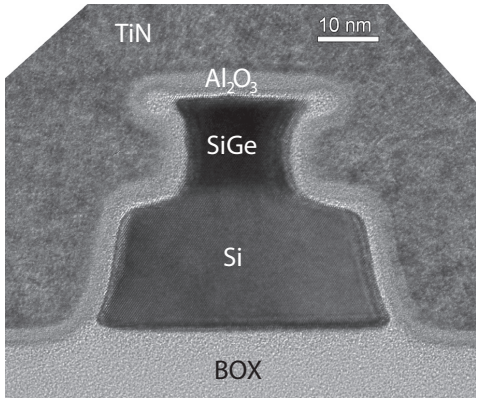

Figure 4.4: Cross-sectional TEM of a singel SiGe on SOI NW with Al_2O_3/TiN gate stack.

A cross-sectional TEM image of a single $Si_{0.5}Ge_{0.5}$ on SOI NW is shown in Fig.4.4. The bottom Si layer has a width of 40 nm, which corresponds to the NW width as patterned. The $Si_{0.5}Ge_{0.5}$ on top of the Si has a cross section of $15 \times 15\,nm^2$. Hence, the loss of SiGe due

to the dHF/O_3 cleaning is about 12 nm from each side. According to [104] the loss of SiGe could be further reduced by decreasing the ozone concentration. The 5 nm thick Si cap layer is consumed by the different cleaning steps throughout the fabrication process. Compared to the RCA cleaned SSOI NWs with HfO_2 gate dielectric in chapter 3 the thickness of the interfacial layer is decreased from about 2 nm to 1 nm.

4.4 Density of Interface States

Charge pumping measurements as described in section 2.4.3 have been performed on the SiGe on SOI NW array TFETs in order to characterize the high-κ interface layer quality. Fig.4.5 (a) shows a typical measurement of the charge pumping current (I_{cp}) as a function of the base voltage V_{base} of the applied gate voltage pulses. I_{cp} was measured with a pulse amplitude $V_{amp} = 1\,\mathrm{V}$ at a frequency of $f = 1\,\mathrm{MHz}$. A measurement at 1 kHz pulse frequency is subtracted in order to exclude gate leakage contributions to I_{cp}. Fig.4.5 (b) shows the maximum I_{cp} normalized to f, the elementary charge q and the total gate width W of the device as a function of the gate length L_g. Using the gate area $A = W \cdot L_g$ in combination with equation (3.4) yields

$$\frac{I_{cp}}{qfW} = L_g \cdot N_{it}\,, \tag{4.3}$$

and N_{it} can be extracted from the slope of a linear fit in Fig.4.5 (b). The measurement was performed on two devices of each gate length for the $Si_{0.5}Ge_{0.5}$ on SOI and the SSOI NW array TFETs from chapter 3. The RCA cleaned SSOI NWs reveal a N_{it} of $5.6 \times 10^{11}\,\mathrm{cm}^{-2}$ while the N_{it} of the SiGe on SOI NWs with dHF/O_3 cleaning reaches $2.5 \times 10^{12}\,\mathrm{cm}^{-2}$. The density of interface states D_{it} can be calculated from N_{it} by considering the total sweep of the surface potential $\Delta\phi_s$ which can be approximated by the amplitude of the applied voltage pulse V_{amp} [32].

MOS capacitors on slightly p-doped bulk Si $2 \times 2\,\mathrm{cm}^2$ pieces have been processed using the same dHF/O_3 cleaning used for the SiGe NW devices in order to measure D_{it} on Si. The gate stack on the Si test samples consists of 3.5 nm of ALD deposited HfO_2 and TiN gate metal. The measured normalized capacitance of these samples as a function of the applied voltage is shown in Fig.4.6. The maximum measured normalized capacitance corresponds to a capacitance equivalent thickness (CET) of 2.3 nm, which corresponds to an EOT= 1.9 nm when the quantum capacitance contribution of the inversion layer in Si is taken into account [96][79]. An SiO_2 interfacial layer thickness of 1.1 nm for a HfO_2 thickness of 3.5 nm and $\varepsilon_{HfO_2} \approx 18$ was calculated. A D_{it} of $3.5 \times 10^{11}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ was extracted from the measurements.

According to the TEM image in Fig.4.4 the area of the SiGe surface is 45 % of the total surface of the NW structure. Assuming that the D_{it} of the Si surface part of the NW is comparable to that of the MOS capacitors, the SiGe D_{it} is $5.1 \times 10^{12}\,\mathrm{cm}^{-2}$. This value is about one order of magnitude higher than D_{it} for the SSOI NW TFETs. However, this

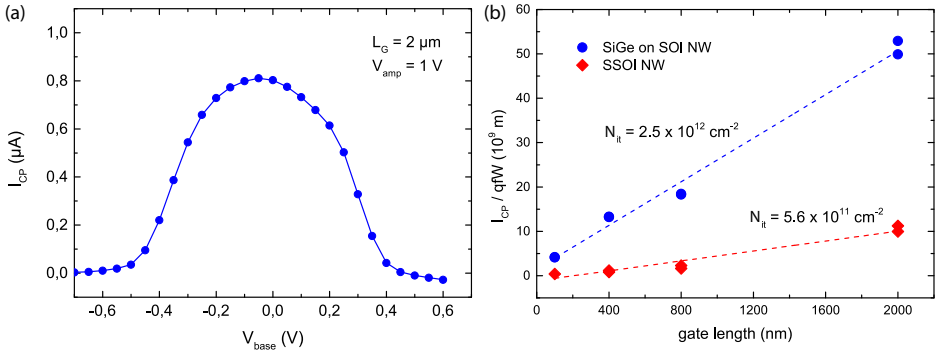

Figure 4.5: (a) Example of a charge pumping measurement in dependence of base voltage V_{base} with $V_{amp} = 1\,\mathrm{V}$ at a SiGe on SOI NW array TFET with $2\,\mu\mathrm{m}$ gate length; (b) Charge pumping current I_{cp} normalized to elextron charge q, pulse frequency f and gate width W as a function of gate length. The measurement was performed on SiGe on SOI and SSOI NW TFETs. N_{it} was extracted from the slope of a line fit.

D_{it} is at the lower end of values reported for high-κ materials grown directly on SiGe. D_{it} values for Al_2O_3 [35], HfO_2 [108] or HfAlO [39] are typically in the order of 10^{12} to $10^{13}\,\mathrm{cm^{-2}eV^{-1}}$. In SiGe the formation of GeO_x at the interface degrades D_{it} compared to Si. Recently Han *et al.* [35] achieved $D_{it} = 3 \times 10^{11}\,\mathrm{cm^{-2}eV^{-1}}$ for Al_2O_3 on $Si_{0.75}Ge_{0.25}$ by a suppression of GeO_x formation due to electron cyclotron resonance (ECR) plasma post-nitridation. However, this process results in an increase of EOT. High D_{it} levels in SiGe devices degrade the electrostatic gate control due to the screening of the gate electric field. Since TFETs exhibit high sensitivity in terms of gate control, D_{it} level can play an important role.

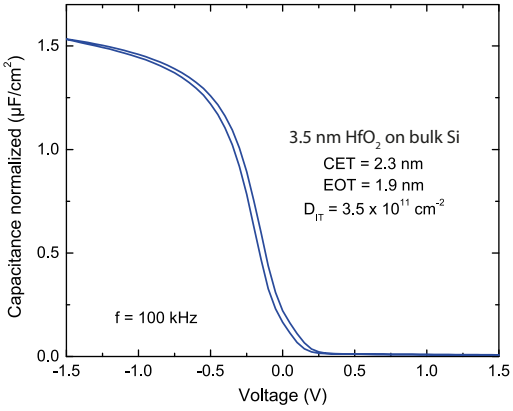

Figure 4.6: Normalized capacitance as a function of applied voltage for a bulk Si test sample with dHF/O_3 cleaning and HfO_2/TiN gate stack.

4.5 I-V Characterization

In this section transfer and output characteristics of the $Si_{1-x}Ge_x$ on SOI NW array TFETs with $x = 35\,\%$ and $50\,\%$ will be presented. The results are limited to n-channel TFET characteristics, since for the SiGe devices the n-channel outperforms the p-channel. The reason for this is the steepness of the doping profile at the junction, as discussed in section 3.4.2 for the SSOI NW TFET. In the SiGe device, however, the diffusion of the n-type dopant As is up to 7 times faster compared to that in Si [18][60]. The diffusion coefficient of B on the other hand decreases with increaing Ge content and is futher decreased for compressively strained SiGe [12].
The n-channel transfer characteristics of a $Si_{0.65}Ge_{0.35}$ and $Si_{0.5}Ge_{0.5}$ NW TFET are shown in Fig.4.7 (a). The device with higher Ge content reveals significantly higher I_D. The minimum subthreshold slope for both devices is about $200\,\mathrm{mV/dec}$. Output characteristics in Fig.4.7 (b) reveal S-shaped onset and super linear increase of I_{ON} with V_G as it was observed for the SSOI NW TFET. I_{ON} of the $Si_{0.5}Ge_{0.5}$ device is about three times higher compared to the $Si_{0.65}Ge_{0.35}$ device. This can be attributed to the smaller E_g of the SiGe alloy with higher Ge content leading to increased BTBT current. The negative differential conductance (NDC), which is visible in the output characteristics, can be attributed to a gate oxide degradation by hot carrier effects in the tunnel junction as explained in section 3.4.3 .
Besides the positive effect on I_D for higher Ge content, transfer characteristics in Fig.4.7 (a) also reveal increased I_{OFF} by one order of magnitude for $50\,\%$ Ge. I_{OFF} in a TFET is either dominated by a Shockley-Read-Hall (SRH) generation-recombination current or by tunneling processes at the channel-drain junction as a result of the ambipolar device characteristics. As explained in section 2.3.3 the separation in applied gate potential between the on-set of n- and p-branch decreases with increasing V_{DS}. Trap assisted tunneling further decreases the separation of the branches. For small V_{DS}, when the separation of n- and p-branch is large enough, SRH generation current can dominate I_{OFF} and is visible as a hump in between the two branches. SRH current increases in TFETs with smaller E_g due to the exponential dependence of the intrinsic carrier number on the band gap.
Since no SRH hump is visible in the transfer characteristics in Fig.4.7 (a) it can be assumed that channel-drain tunneling limits I_{OFF} under the applied bias conditions. Fig.4.8 shows simulated valence and conduction band energies for $35\,\%$ and $50\,\%$ Ge. The bias conditions in the simulation are $V_G = 0\,\mathrm{V}$ and $V_{DS} = 0.5\,\mathrm{V}$. The smaller E_g for the higher Ge content causes a smaller tunneling distance at the channel drain junction. The inset in Fig.4.8 shows the decrease of tunneling distance as a function of the applied V_{DS} for both Ge contents. This illustrates how a smaller E_g leads to increased I_{OFF} in the case of dominating channel-drain tunneling in the off-state.

Comparing I_D of the SiGe on SOI with the SSOI NW TFET at $\Delta V_G = 1.5\,\mathrm{V}$ from the minimum of the transfer curve (to account for the shift in threshold voltage) and $V_{DS} = 0.5\,\mathrm{V}$

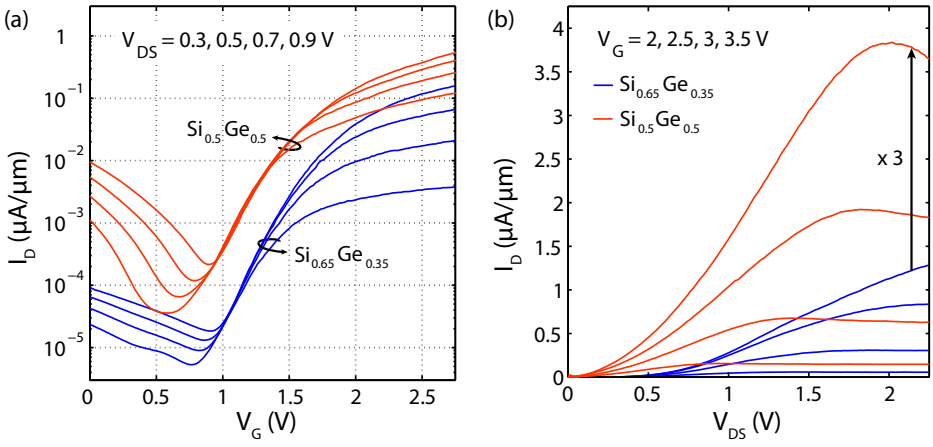

Figure 4.7: (a) Transfer and (b) output characteristics of a n-channel homostructure $Si_{1-x}Ge_x$ on SOI NW array TFETs with 2 μm gate length and $x = 35\,\%$ and $50\,\%$ Ge content, respectively.

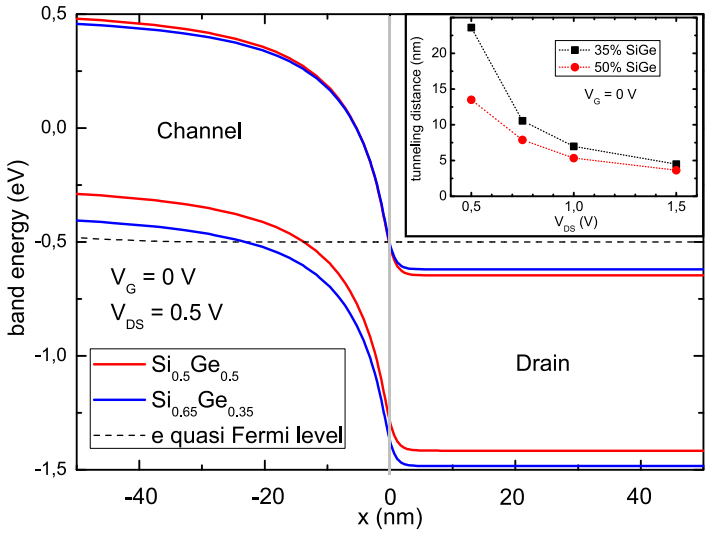

Figure 4.8: Simulated valence and conduction band energies at the channel drain junction for a $Si_{1-x}Ge_x$ TFET with $x = 35\,\%$ and $50\,\%$ Ge content. The TFET is in the off-state with $V_G = 0\,\mathrm{V}$ and $V_{DS} = 0.5\,\mathrm{V}$. The inset shows the decrease of tunneling distance for increasing V_{DS} for the different Ge contents.

a current increase from $0.02\,\mu A/\mu m$ to $0.2\,\mu A/\mu m$ is observed. The current increase can be attributed to the decrease in E_g from stained Si to the strained $Si_{0.5}Ge_{0.5}$ NWs. The EOT of the SiGe devices with 4 nm Al_2O_3 gate dielectric with a $\varepsilon_r = 9$ and 1 nm interfacial SiO_2 layer as shown in the TEM image in Fig.4.4 is approximately 2.7 nm. This value is close to the 2.8 nm EOT extracted for the HfO_2 gate dielectric with 2 nm interfacial layer of the SSOI devices. However, the electrostatic gate control in the SiGe devices is degraded by the one order of magnitude higher D_{it} level as shown in section 4.4, since interface charges screen the gate electric field. This effect causes a degradation of S in the SiGe TFET. In addition TAT has an important influence on the devices as will be discussed in the following section.

4.6 Temperature Dependent Measurements

4.6.1 Trap Assisted Tunneling

Transfer characteristics of the $Si_{0.5}Ge_{0.5}$ NW TFETs have been measured at different temperatures. The measurement results at $T = 85$, 200 and 300 K are shown in Fig.4.9. The transfer characteristics exhibit a strong temperature dependence. At $V_G = 1.3$ V the magnitude of I_D changes by 6 orders of magnitude between 85 K and 300 K. The minimum S decreases from 222 mV/dec at 300 K to 65 mV/dec at 85 K. As discussed in chapter 3 this strong temperature dependence of I_D and S at small V_G can be attributed to TAT processes dominating the current transport.
Apart from SiGe/high-κ induced D_{it} traps are also introduced at the source-channel and channel-drain junctions by ion implantation. The ion implantation energy is chosen low enough to locate the peak of implanted ions close to the top of the SiGe wire in order to allow for solid phase epitaxial regrowth (SPER) during activation. Dopant activation at only 650° C for 1 min was chosen to prevent Ge diffusion into the bottom Si layer, which would decrease Ge concentration in the SiGe NW. The low temperature activation, however, may result in a larger number of remaining defects at the source-channel and channel-drain junction, thus giving rise to TAT. TAT degrades S and increases also the channel-drain tunneling current, which in turn increases I_{OFF}. Due to the small E_g of the SiGe and the strong TAT contribution I_{OFF} is increased by more than three orders of magnitude for $Si_{0.5}Ge_{0.5}$ compared to the SSOI TFETs.

4.6.2 Band Gap Extraction from SRH Current

An estimation of the band gap E_g in the SiGe NW TFETs can be obtained from the the SRH generation-recombination current, that occurs in the off-state of the device. When the transfer curve is measured at small V_{DS} the separation of n- and p-branch of the TFET is large enough in order to observe the characteristic peak of the SRH generation in the center of the transfer characteristics. Measurements of the transfer characteristics of a SiGe

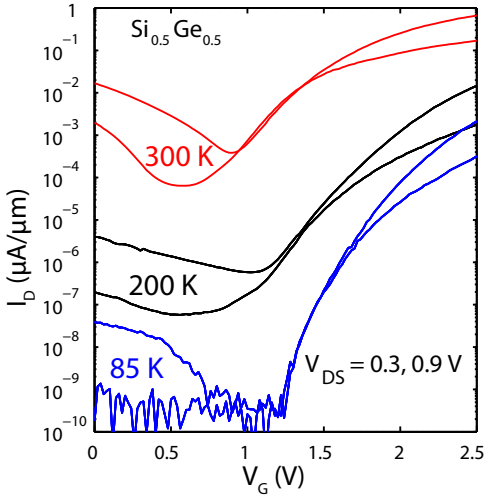

Figure 4.9: Transfer characteristics of a $Si_{0.5}Ge_{0.5}$ on SOI NW TFET measured at temperatures 85, 200 and 300 K.

NW TFET with 2 μm channel length at $V_{DS} = 50\,\text{mV}$ at temperatures between 170 K and 330 K are shown in Fig.4.10. The SRH hump is clearly visible except for the measurement at $T = 170\,\text{K}$, where the current drops below the measurement resolution of the setup.
The dependence of the SRH current on the number of intrinsic carriers in a semiconductor is given in equation (2.20). By plotting the maximum I_D of the SRH hump as a function of T in an Arrhenius plot, E_g in the channel region of the device can be extracted from the slope of a line fit according to:

$$\ln\left(I_D/T^{1.5}\right) = -\frac{1}{2k_BT} \cdot E_g\,. \tag{4.4}$$

The temperature dependence of E_g is neglected in this estimation of the band gap. In order to get a reliable estimation of E_g close to room temperature an Arrhenius plot of peak SRH currents in the temperature range from 250 K to 330 K is presented in Fig.4.11. $E_g = 0.62\,\text{eV}$ was extracted from the slope of the linear fit. This value is smaller compared to $E_g = 0.67\,\text{eV}$ calculated in [24] for biaxially compressive strained $Si_{0.5}Ge_{0.5}$. For the patterned NWs actually an increase of this value would be expected due to the strain relaxation across the NWs discussed in section 3.2. However, the TiN gate metal deposited by AVD is known to introduce compressive strain in Si layers [78]. Additional compressive strain caused by the gate stack could explain the decreased value for E_g.

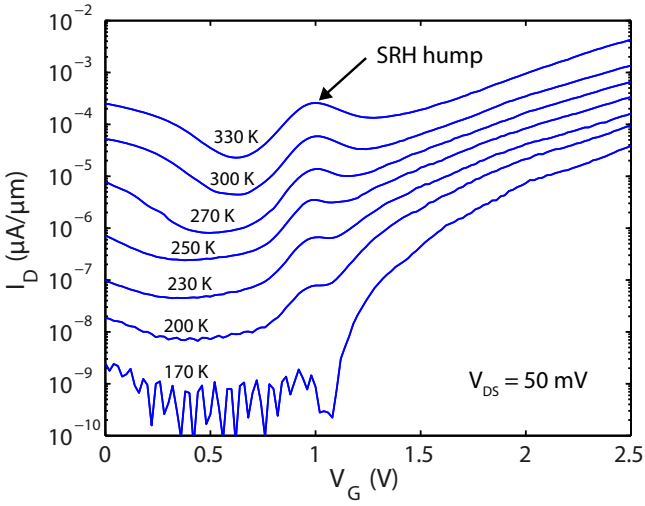

Figure 4.10: Transfer characteristics of a $Si_{0.5}Ge_{0.5}$ NW array TFET with 2 μm gate length measured at $V_{DS} = 50$ mV in a temperature range from 170 to 330 K. The SRH generation current dominates I_D in between the n- and p-branch of the TFET.

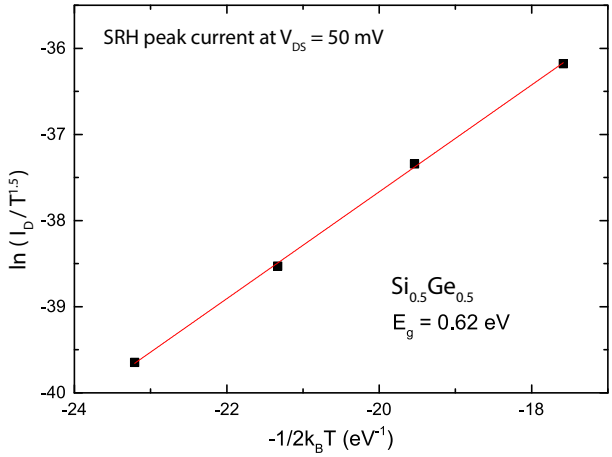

Figure 4.11: Arrhenius plot of the peak SRH current extracted from Fig.4.10 in a temperature range from 250 to 330 K.

4.7 Conclusion

The SiGe on SOI NW TFETs presented in this chapter prove the hypothesis, that materials with further reduced band gap enable higher tunneling currents. In comparison to the NW devices presented in chapter 3, I_D was increased by one order of magnitude. In the comparison of 35 and 50 % Ge content it has been shown that not only I_{ON} but also I_{OFF} increases in the homostructure SiGe TFET with smaller band gap material. Temperature dependent measurements of the transfer characteristics revealed a large contribution by TAT to I_D, which can be attributed to trap states in the tunnel junction caused by ion implatation and the lower thermal budget required by SiGe.
D_{it} values for the SiGe layer are found to be one order of magnitude higher compared to the SSOI NW TFETs. However, compared to literature values rather low D_{it} for the high-κ on SiGe gate stack was achieved. Due to a decreased interfacial layer the EOT for the SiGe devices with Al_2O_3 is even slightly better than for the HfO_2 dielectric in the SSOI devices. The gate control in the SiGe devices, however, is degraded by the larger D_{it}. Degraded gate control in combination with the large contribution by TAT causes higher S values in the SiGe devices compared to the sSi NWs.
In conclusion, it has been shown that strained SiGe NWs with a band gap of 0.62 eV, estimated from the SRH generation, can increase the current in TFETs about one order of magnitude compared to sSi, even though the gate control is inferior. Hence, a further current increase can be expected for a comparable gate control. While higher D_{it} and traps caused by ion implantation are technology issues, which could be solved by more mature processes, the increase of I_{OFF} in small band gap homostructure TFETs is a fundamental problem. A solution to this problem by a different device concept will be discussed in the following chapter.

5 SiGe/Si Heterostructure NW TFET

In this Chapter a different TFET concept is presented, which is supposed to overcome some of the limitations of the homostructure SiGe NW TFET presented in the previous section. The concept of a heterostructure tunnel junction at the interface of two semiconductors with different band gaps and band alignment offers the opportunity to employ band gap engineering for receiving high on-currents while maintaining low off-current and suppressing ambipolar behavior. The heterostructure presented combines a SiGe/Si heterojunction with an increased tunnel junction area due to step like structure with an overlap of gate and source regions in a NW design.
Subsequently to a general comparison of the homo- and heterostructure TFET concept, *I-V* characteristics of the fabricated heterostructure device are presented and compared to the homostructure SiGe TFET from chapter 4. The BTBT current dependence on the junction area as well as suppression of ambipolarity are discussed. In the last section of this chapter device simulations are presented in order to gain further inside about the influence of line tunneling in the overlapping source-gate region on device performance.

5.1 Heterostructure TFET Concept

In a heterostructure TFET different semiconductors are utilized in the source, channel and drain region. This allows for band gap engineering exploiting different band gap energies and energy offsets of valence and conduction band edges. As an example Fig.5.1 (a) shows a schematic illustration of the material composition that was used in the homojunction SiGe NW TFET in the previous chapter on the left and the material composition of the SiGe/Si heterojunction TFET which will be discussed in this chapter on the right.
The heterostructure with SiGe source and Si channel and drain is a distinct n-channel TFET, which can be understood from the simulated valence and conduction band edge energies of a homo- and heterostructure in Fig.5.1 (b). Two bias conditions in the on-state of the TFET with $V_G = 2\,\mathrm{V}$ on the left and the off-state with $V_G = 0\,\mathrm{V}$ on the right are shown. In both cases the drain is biased at $0.5\,\mathrm{V}$. An effective band gap $E_{g,eff}$ for the tunneling process can be defined, which in case of the n-channel TFET denotes the energy difference between source valence band and channel conduction band at the tunnel junction. The band gap difference from $Si_{0.5}Ge_{0.5}$ to Si is given mainly by a valence band off-set of about $0.4\,\mathrm{eV}$. Hence, $E_{g,eff}$ is basically the same for the homo- and heterostructure as shown in Fig.5.1 (b). This in turn results on one hand in a constant tunnel distance for homo- and heterojunction. On

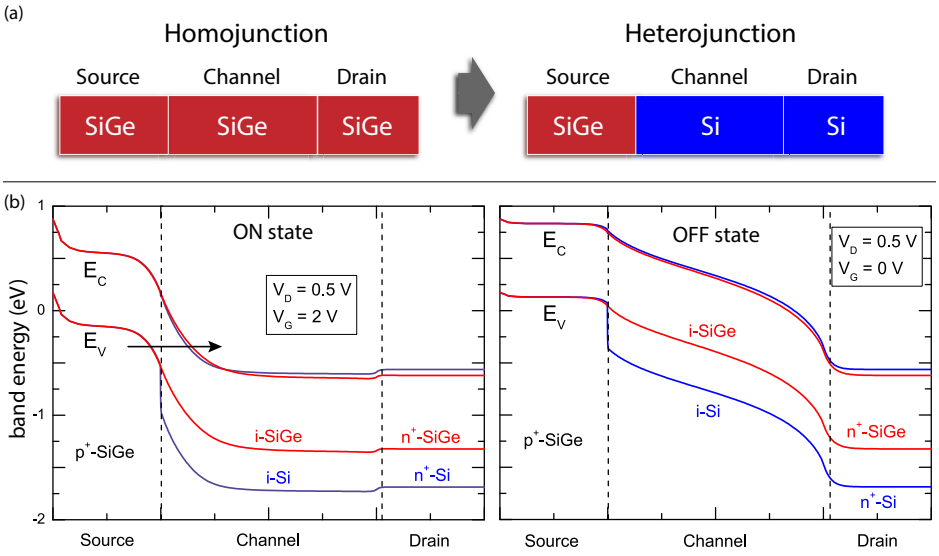

Figure 5.1: (a) Schematic illustration of source, channel and drain material configuration in SiGe homostructure and SiGe/Si heterostructure n-channel TFET. (b) Simulated valence and conduction band edge energies in a n-channel $Si_{0.5}Ge_{0.5}$ homostructure and $Si_{0.5}Ge_{0.5}$/Si heterostructure TFET in the ON-state (left) and OFF-state (right).

the other hand the band gap in channel and drain is larger in the heterojunction reducing SRH generation in the channel region and channel-drain tunneling in the off-state. Thus, the heterostructure TFET concept should maintain the I_{ON} of a $Si_{0.5}Ge_{0.5}$ TFET and reduce I_{OFF} to values which can be obtained in Si TFETs. This in turn increases the I_{ON}/I_{OFF} ratio, which is crucial for low stand-by power application.

It has to be noted that also the effective masses, which influence the tunneling probability (equation (2.12)), are different in SiGe and Si. However, in a n-channel TFET hole masses in the source valence band and electron masses in the channel conduction band have to be taken in to account. The hole mass is the same since both structures possess a $Si_{0.5}Ge_{0.5}$ source and the electron mass $m^{(\Delta)}$ is independent from the Ge content as shown in [24]. Hence, the reduced tunnel mass m^* is constant for homo- and heterostructure.

The heterostructure concept has been already studied in different theoretical and experimental publications. Simulations of SiGe source and strained Si channel TFETs shown in [77] show promising results. In [40] highly scaled gate all around (GAA) NW TFETs using Ge source and Si channel/drain are proposed and exhibit good performance in simulations. An experimental demonstration of a planar n-TFET with poly-Ge source is presented in [44]. Since the growth of lateral heterostructures is rather difficult experimental realizations with a step like structure based on epitaxially grown layers are a promising alternative [112]. Besides vertical structures fabricated in top-down approach, also bottom-up technique like

vapor-liquid-solid (VLS) growth is used to fabricate axial Ge-Si hetero nanowires used as n-channel TFET [58].
Heterojunction TFETs based on III-V semiconductors are demonstrated in [71]. One of the best performing n-channel TFETs is presented in [16] with a vertical III-V structure based on InGaAs. Using band engineering in III-V heterostructure made from InAs and GaSb even a staggered or broken gap band alignment can be achieved, which further reduces the tunneling distance and thus increases the on-current [61][54].
While heterostructures using SiGe or Ge as source and Si as channel are feasible for n-TFETs only, heterostructures employing InGaAs as source and Si as channel provide a possible concept for p-channel TFETs [103]. Such a device is realized in [76] in a vertical NW design. An integration scheme for complementary heterostructure TFETs based on vertical Si NWs with Ge and InAs top source contact for n- and p-channel TFETs, respectively, is demonstrated in [86].
In this work a new step like device structure with NW design is introduced, which allows for the combination of a SiGe/Si heterostructure tunnel junction and an increase of tunnel junction area in a NW design.

5.2 Substrate and Device Structure

The SiGe/Si heterostructure NW array TFET was fabricated using an $Si_{0.5}Ge_{0.5}$ on SOI substrate. The 12. 4 nm thick $Si_{0.5}Ge_{0.5}$ is pseudomorphically grown on a 21 nm thick SOI layer and hence biaxially compressive strained. The SiGe layer is capped with 9. 4 nm Si. The layer stack is shown schematically in Fig.5.2 (a). The $Si_{0.5}Ge_{0.5}$ layer is in situ p-doped with a boron dopant concentration of $2 \cdot 10^{20}\,cm^{-3}$.
Fig.5.2 (b) shows a schematic representation of a single NW in the heterostructure NW array. The NW exhibits a step, where the Si cap and the p^+-doped SiGe layer are removed and only the bottom Si layer remains. The p^+-doped SiGe layer acts as the source in the device, while the bottom Si layer serves as channel and drain region. A tri-gate, which covers the step and overlaps also with the SiGe source, covers the NW. The bottom Si layer sticking out of the gate is n-doped by ion implantation and acts as drain contact.
Tunneling from the p^+-SiGe to the intrinsic bottom Si occurs in the region marked with a red line in Fig.5.2 (b). The vertical tunnel direction is indicated with black arrows. BTBT processes form a highly doped source to an intrinsic layer with a tunnel direction perpendicular to the gate electric field are referred to as point tunneling as introduces in [107]. Due to the overlap of gate and source additional BTBT can occur in the source region, when a thin layer of the highly doped SiGe is inverted by the gate potential. The tunneling direction is along the electric field lines of the gate and the tunneling mechanism is referred to as line tunneling [107]. The on-set of the line tunneling mechanism is more abrupt than point tunneling offering steep subthreshold swings and high currents [102]. The occurrence of line

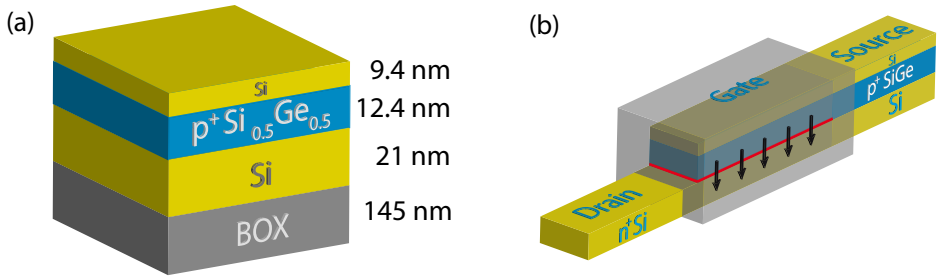

Figure 5.2: (a) Illustration of the in situ boron doped $p^+Si_{0.5}Ge_{0.5}$ on SOI layer stack with corresponding layer thicknesses. The SiGe layer is biaxially compressive strained due to the pseudomorphic growth on the SOI; (b) Schematic of a single NW of the heterostructure n-channel TFET. The tri-gate covers the the step in the nanowire. The vertical tunnel direction from the $p^+Si_{0.5}Ge_{0.5}$ in to the bottom Si layer is indicated with black arrows. The tunnel junction is marked with a red line.

tunneling strongly depends on the source doping level and gate control. It is superimposed to the point tunneling current. Further analysis of point and line tunneling contribution in the fabricated devices will be given in section 5.5.

Compared to the homostructure SiGe NW devices presented in chapter 4 the following features of the heterostructure design are supposed to increase TFET performance:

- The **$Si_{0.5}Ge_{0.5}$/Si heterojunction** offers an effective band gap at the tunneling junction that matches the SiGe homostructure NWs keeping BTBT distance small, whereas the channel and drain band gap are larger to achieve low I_{OFF}.
- The electrostatic gate control for the **Si channel** is improved compared to the SiGe channel in the homostructure due the smaller D_{it} values that can be achieved for high-κ gate dielectric on Si as shown in chapter 4.
- The **in situ doped source** features a high doping level of $2 \cdot 10^{20}\,\mathrm{cm}^{-3}$ in combination with a steep doping profile decreasing the λ_{dop} parameter. Defect formation in the tunnel junction by ion implantation, which leads to dominant TAT, is prevented and the thermal budget can be kept small since no source dopant activation is needed.
- The **tunnel junction area** is increased and scales with the gate-source overlap. In addition, the overlap of gate and source offers the possibility for line tunneling in the highly doped source adding to the current.

5.3 Device Fabrication

The fabrication process of the SiGe/Si heterostructure NW array TFET is based on the process used for devices of chapter 3 and 4. The process steps which are changed with respect to the process of the homostructure SiGe TFET are listed in the following:

- In between the marker fabrication and the patterning of the NW array an additional e-beam lithography is introduced to pattern the step for the drain region. E-beam lithography with PMMA 669.07/600K resist was used to open a window in the drain part of the NWs (which are patterned afterwards) and the drain contact pad. The Si cap and the $Si_{0.5}Ge_{0.5}$ layer are subsequently etched in this region by Cl_2/Ar dry etching. The etching was stopped at the bottom Si layer.
- After the patterning of the NW array and prior to the gate stack deposition the samples were cleaned by a dHF/O_3 process in the "Semitool Raider" cleaning tool as done for the SiGe homostructure NWs. However, the time for the ozone process was reduced to 1 min in order to reduce the SiGe consumption due to the cleaning.
- The gate stack for the devices consists of 3.5 nm HfO_2 and 40 nm TiN gate metal deposited by ALD and AVD, respectively.
- Since the source is already in situ doped no ion implantation for source doping is required. Only the e-beam lithography followed by As ion implantation to form the drain side is performed as in the homostructure TFET. RTA for dopant activation was omitted, since annealing tests at 550° C for 30 s already degraded device performance without showing positive effects on source-drain resistance.

The NWs in the array have a width of 40 nm. Four different NW lengths with corresponding gate lengths of 100, 400, 800 and 2000 nm have been patterned. The NW length is always

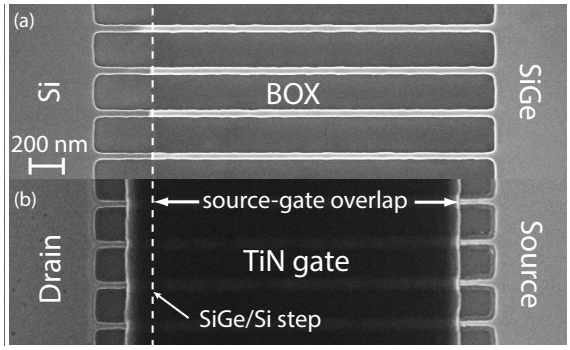

Figure 5.3: Top view SEM image of the heterostructure NW array (a) before and (b) after gate stack deposition and patterning.

400 nm in addition to the gate length. The overlap of source and gate for the different NW lengths is 75, 300, 600 and 1800 nm, respectively.
Fig.5.3 (a) shows a SEM top view image of the heterostructure NW array with the step in the NW where the p^+-doped SiGe layer ends. The patterned 2 μm gate shown in Fig.5.3 (b) covers the step in order to provide large enough separation between the p^+-doped SiGe source and the implanted n-doped Si drain.

5.4 Device Characterization

In this section I-V characteristics of the SiGe/Si heterostructure NW TFETs are presented and compared to the SiGe homostructure NW TFETs shown in the previous chapter. Since the dimensions of the NWs concerning width and length are comparable for both devices I_D is normalized to the current flow through a single NW instead of the total NW width.

5.4.1 Transfer and Output Characteristics

Fig.5.4 shows the n-channel transfer characteristics of the heterostructure and the homostructure NW TFETs both with 2 μm gate length. The heterostructure exhibits a minimum S of 90 mV/dec at $V_{DS} = 0.1$ V and $I_{ON}/I_{OFF} \approx 10^8$, while the minimum S of the homostructure is 220 mV/dec and $I_{ON}/I_{OFF} \approx 10^4$. Especially I_{OFF} is decreased in the heterostructure TFET. The heterojunction design with Si channel and drain decreases SRH generation-recombination and BTBT at the channel-drain junction compared to the homostructure. Thus lower I_{OFF} and large I_{ON}/I_{OFF} ratio could be achieved. These results demonstrate that the in situ doped heterostructure TFET clearly outperforms the ion implanted homostructure. However, both devices suffer from a substantial shift in threshold voltage towards positive gate voltage, requiring gate voltages V_G of up to 3 V to switch on the devices.
Fig.5.5 exhibits output characteristics of the heterostructure TFET for V_G from 1 V up to 3 V in steps of 0.1 V. The I_D-V_{DS} curves also show an exponential increase in I_{ON} with V_G and S-shape. However, compared to output characteristics of the homojunction TFET at $V_G = 2.5$ and 3 V also shown in Fig.5.5 the S-shape is far less pronounced and saturation of I_D is reached at much smaller V_{DS} well below 1 V. The reduction of S-shape in the heterostructure indicates a reduced DIBT presumably due to the high source doping level.
The fast saturation of I_{DS} in the output characteristics is a sign of a small λ_{dop}, which can be attributed to the steep doping profile of the in situ doped SiGe source. The current per NW in the heterostructure exceeds that of the homostructure, which is not only related to the higher junction quality, but also to the difference in device geometry, effective oxide thickness and the increased tunnel junction area in the heterostructure.

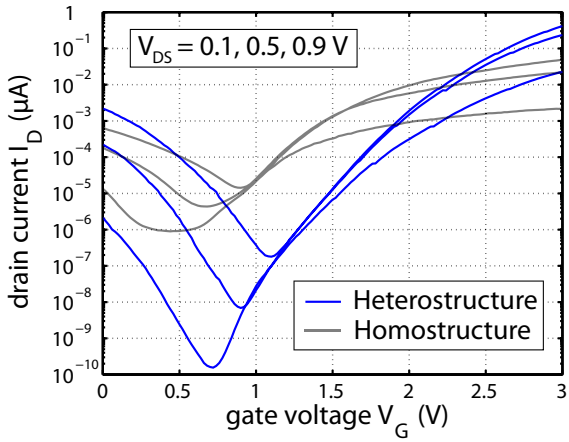

Figure 5.4: Transfer characteristics of a n-channel $Si_{0.5}Ge_{0.5}$/Si heterostructure NW TFET with 2 μm gate length (blue). In comparison transfer characteristics of the homostructure $Si_{0.5}Ge_{0.5}$ NW TFET from chapter 4 are shown in gray. Currents are normalized per NW in the array for both devices.

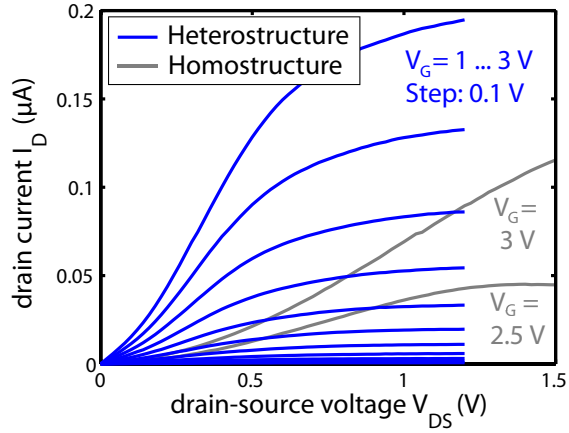

Figure 5.5: Output characteristics of a n-channel $Si_{0.5}Ge_{0.5}$/Si heterostructure NW TFET with 2 μm gate length (blue). In comparison output characteristics of the homostructure $Si_{0.5}Ge_{0.5}$ NW TFET from chapter 4 are shown in gray. Currents are normalized per NW in the array for both devices.

5.4.2 Increased Tunnel-Junction Area

In contrast to the SSOI and SiGe homostructure NW TFETs presented in chapter 3 and 4, the tunnel junction area in the SiGe/Si heterostructure TFET scales with the gate length due to the variation of the source-gate overlap. As shown in section 3.4.1 for the SSOI NW TFET, I_{ON} does not depend on the gate length since the tunnel junction is localized in a small area around the source-channel junction at the gate edge and the junction resistance is much larger than the channel resistance. In the heterostructure, in contrast, BTBT from source to drain is enabled along the line between SiGe source and bottom Si channel marked with the red line in Fig.5.2 (b). The total tunnel line length is calculated as twice the overlap of gate and source plus the width of the nanowire. The junction scaling for point and potential line tunneling is in this connection equivalent.
I_D is plotted in Fig.5.6 as a function of the tunnel line length. The current values were averaged over 10 devices of each gate length. The expected trend of increasing I_D with larger tunnel line length is apparently correct for lengths between 190 nm and 1240 nm, which corresponds to a gate-source overlap of 75 nm and 600 nm, respectively. For gate-source overlap of 1.8 μm a saturation of I_D is observed.

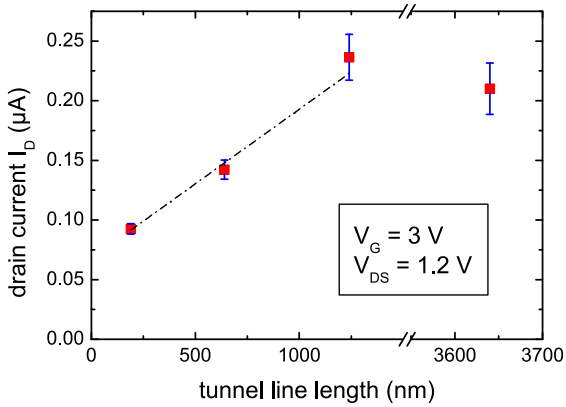

Figure 5.6: Drain current I_D as a function of tunnel line length as marked in Fig.5.2 (b) for four different gate length.

The reason for the deviation from a strictly linear dependence of I_D on the tunnel line length may be due to a drop of the applied drain potential along the source-channel junction. Morita *et al.* have shown in [74] that an overlap of source and gate in a TFET can be described with a distributed-element model for a parallel-plate capacitor. The utilized model can be adapted for the SiGe/Si heterostructure NW TFET as illustrated in Fig.5.7. Each infinitesimal section of the tunnel junction is modeled as a parallel circuit consisting of a capacitor C_T and a resistor with the conductance of the tunnel junction G_T, while each section of the channel region has the resistance R_C. It is shown in [74] that the current

in this circuit saturates at a certain length of the gate-source overlap due to the drop of V_{DS} caused by the channel resistance. According to this model I_D approaches the value of $\sqrt{G_T/R_C}V_{DS}$ for large overlap and neglected distributed source resistance R_S. When R_S is taken into account, I_D even decreases at sufficiently large gate-source overlap. Thus, this model can explain, why the current does not scale strictly linear with the gate-source overlap. The BTBT current from the junction part close to the step and especially from the front edge has a larger contribution to the overall current. Nevertheless the increase of tunneling area results in a substantial increase of I_D.

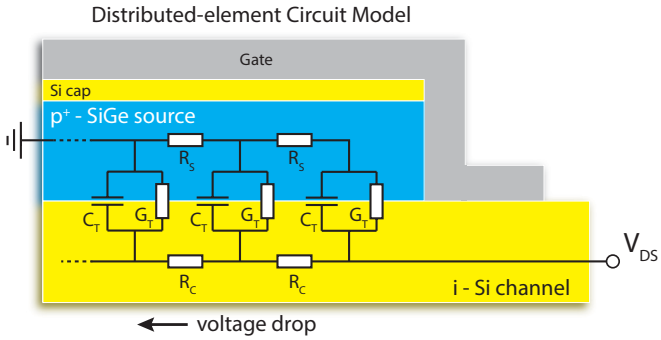

Figure 5.7: Distributed-element circuit model of a parallel-plate capacitor adapted for the drop of applied V_{DS} along the source-channel junction according to [74].

5.4.3 Temperature Dependence

Fig.5.8 exhibits transfer characteristics of the SiGe/Si heterostructure NW TFET measured at 85 and 300 K. The transfer characteristics exhibit much smaller temperature dependence compared to the SiGe homostructure devices from chapter 4. The difference in I_D at the minimum of the transfer curve at $V_{DS} = 0.9\,\mathrm{V}$ is only 2 orders of magnitude for the heterostructure compared to 6 orders of magnitude for the homostructure as shown in Fig.4.9. At $V_G = 2\,\mathrm{V}$ the current difference is about a factor of 2 to 3, which can be explained by the change of E_g with temperature and the corresponding influence on BTBT as presented in section 3.5. The small temperature dependence can be taken as an indication for a smaller TAT contribution in the heterostructure device. The in situ doped SiGe source grown pseudomorphically on the Si channel apparently exhibits less trap states in the junction than the ion implanted junction in the SiGe homostructure.

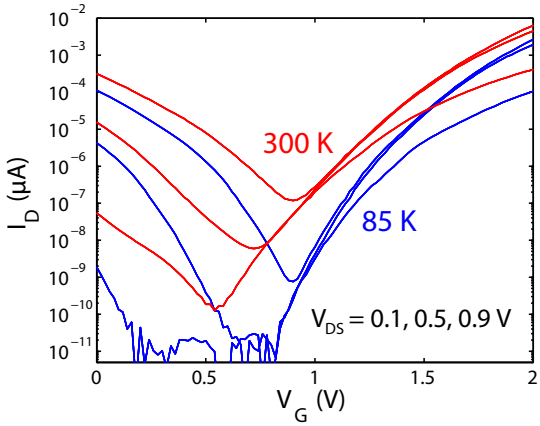

Figure 5.8: Transfer characteristics of a n-channel $Si_{0.5}Ge_{0.5}$/Si heterostructure NW TFET with 2 μm gate length measured at 85 and 300 K. Currents are normalized per NW.

5.4.4 Reduction of Ambipolarity

A reduction of the ambipolarity in the transfer characteristics of a TFET is required for logic applications, since a distinct OFF-state of the device is needed. The heterostructure device already shows an asymmetry between n- and p-branch due to the smaller $E_{g,eff}$ and larger tunneling area at the in situ doped p^+-SiGe/i-Si junction compared to the implanted n-Si/i-Si junction at channel and drain. However, the relatively high dopant fluence, in order to achieve a low resistance in the drain-side of the NW, also result in a quite good tunnel junction for the p-branch at the channel-drain side. Thus current in the p-branch is only one to two orders of magnitude smaller compared to the n-branch.

A reduction of the As fluence from 10^{15} to $10^{14}\,cm^{-2}$ results in a significant current decrease of the p-branch by 4 orders of magnitude, as shown in the transfer characteristics in Fig.5.9. The lower drain doping dose prevents tunneling at the channel-drain junction almost completely. However, also the current in the n-branch is degraded due to increasing series resistance of the NW in the drain region.

The change in dopant fluence also causes a significant threshold voltage shift of 0.5 V. A possible reason for the shift could be a work function shift of the TiN metal gate due to the ion implantation. The gate is used as a mask to perform a self aligned ion implantation with As to form the drain contact. A high drain doping may influence the metal work function of the TiN causing a shift in the transfer characteristics. This demonstrates that a reduction of drain doping is beneficial both, for reducing ambipolar behavior and shifting the threshold voltage closer to zero. The formation of a silicide at the drain junction could prevent the reduction of n-branch current due to increased drain resistance. The implications of the ambipolar behavior on logic application will be further discussed on the example of TFET inverters in chapter 6.

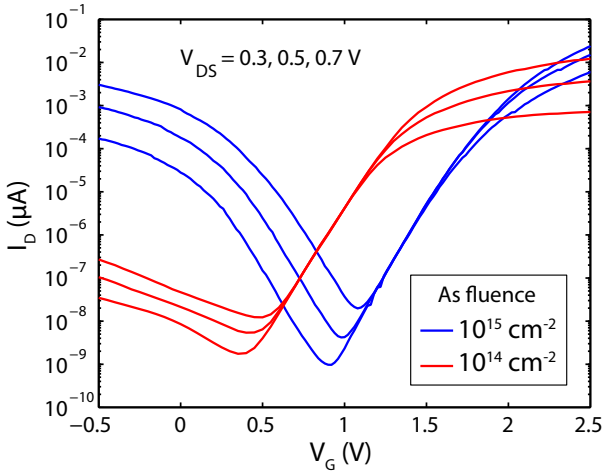

Figure 5.9: Transfer characteristics of n-channel $Si_{0.5}Ge_{0.5}$/Si heterostructure NW TFETs with different As fluence for drain implantation. Currents are normalized per NW.

5.5 Device Simulation

5.5.1 TCAD Sentaurus

Two-dimensional technology computer aided design (TCAD) device simulations were performed with Synopsys Sentaurus in order to analyze the BTBT mechanism in the SiGe/Si heterostructure TFET device in more details. The Sentaurus device simulator calculates the current flowing in the device based on a drift-diffusion model, while the tunneling process in the TFET is modeled by a non-local band-to-band tunneling model with Fermi statistics taken into account. In addition, SRH recombination and a dynamic non-local path model for trap assisted tunneling were employed.
The strain of pseudormorphically grown SiGe on Si was calculated and the corresponding effects on band gap and effective carrier masses were implemented by deformation potential models. The SiGe material parameters used for the simulations are taken from [24] and [42].

5.5.2 Point and Line Tunneling

In section 5.2 it has already been discussed, that the heterostructure design with overlapping source and channel region allows for point tunneling from source to channel as well as line tunneling in the p^+-doped SiGe source. In order to estimate the contribution of both tunnel mechanisms to I_D Sentaurus TCAD simulations have been used. The simulated vertical heterostructure with a double gate is shown in Fig.5.10. The two-dimensional vertical TFET structure resembles key features of the fabricated SiGe/Si heterostructure devices and is comparable to a cross-cut through the NW. The double gate in the simulated vertical

structure covers the channel region as well as the p^+-doped $Si_{0.5}Ge_{0.5}$ source. In comparison to the experimental structure there is no top gate in the simulated 2D structure, due to the need for a source contact. However, the influence of the top-gate is anyway small due to the additional Si cap layer in the fabricated structure. The thickness of the intrinsic Si channel corresponds to the thickness of the bottom Si layer in the experimental structure. The simulated structure has an additional n^+-doped Si layer at the bottom acting as drain region of the device.

The $Si_{0.5}Ge_{0.5}$ source layer of the simulated structure features uniaxial compressive strain along the y-direction (in plane of projection in Fig.5.10), which corresponds to the [110] channel direction of the experimental structure. The uniaxial strain stems from the initial biaxial compressive strain of a pseudomorphically grown SiGe layer on Si and the strain relaxation across patterned NWs discussed in section 3.2. Source doping and drain doping levels are $2 \times 10^{20}\,\mathrm{cm}^{-3}$ and $1 \times 10^{20}\,\mathrm{cm}^{-3}$, respectively. The doping levels fall off with a Gaussian shaped profile to the channel doping level within 4 nm. The gate dielectric consists of 1 nm SiO_2 interfacial layer and 3 nm HfO_2 with $\varepsilon_{HfO_2} = 18$. The gate work function used in the simulations is 4.5 eV.

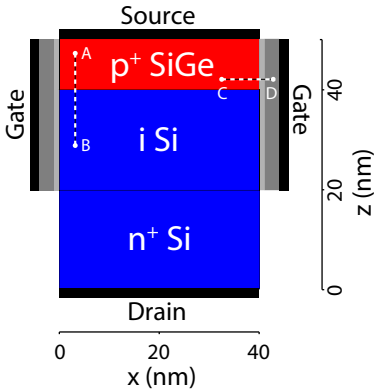

Figure 5.10: Simulated two-dimensional SiGe/Si heterostructure TFET resembling a cross-cut through the NW of the experimental heterostructure NW TFET (see Fig.5.2 (b)). Simulated band edge energies along the paths A-B and C-D are shown in Fig.5.11 demonstrating the mechanisms of point and line tunneling, respectively.

Fig.5.11 (a) and (b) exhibit the simulated band edge energies along the paths from point A to B and C to D marked in the simulated structure in Fig.5.10. Fig.5.11 (a) illustrates the point tunneling process from source to channel at $V_G = 3\,\mathrm{V}$ that occurs along the path A-B. Fig.5.11 (b) shows the line tunneling process at $V_G = 4.5\,\mathrm{V}$ that occurs along the path C-D. Here BTBT takes place in the p^+-doped SiGe layer towards a thin inversion layer at the interface to the gate dielectric.

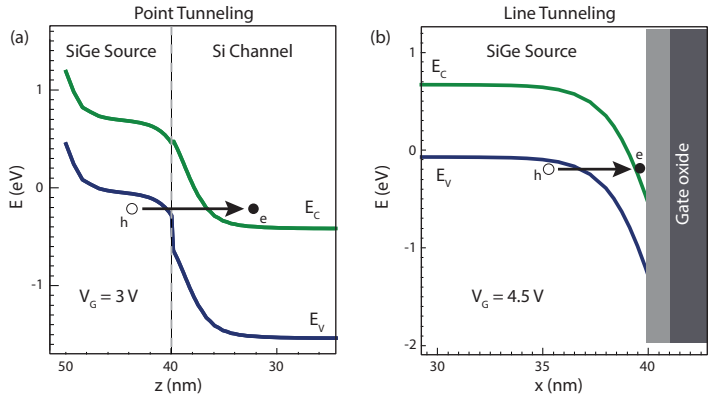

Figure 5.11: Simulated band edge energies of valence and conduction band along the paths (a) A-B at $V_G = 3\,\mathrm{V}$ and (b) C-D for $V_G = 4.5\,\mathrm{V}$ marked in Fig.5.10.

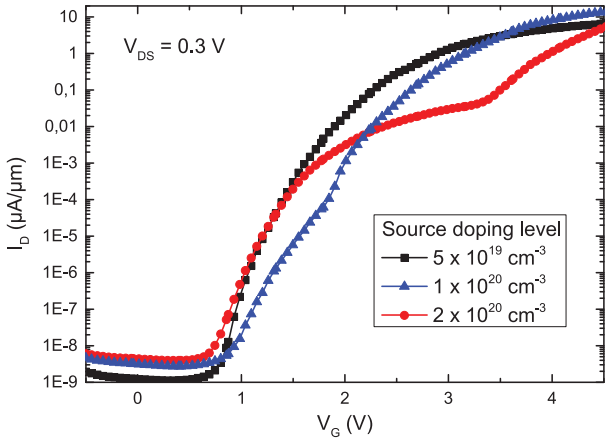

Figure 5.12: Simulated transfer characteristics of the SiGe/Si heterostructure TFET illustrated in Fig.5.10.

Fig.5.12 shows simulated transfer characteristics for three different source doping levels of $2 \times 10^{20}\,\mathrm{cm}^{-3}$, $1 \times 10^{20}\,\mathrm{cm}^{-3}$ and $5 \times 10^{19}\,\mathrm{cm}^{-3}$. The transfer characteristics for the highest source doping level, that corresponds to the value of the experimental heterostructure TFET, exhibits a round shape that is equivalent with a continuously increasing subthreshold slope up to $V_G = 3.5\,\mathrm{V}$. This behavior resembles the experimental measured transfer characteristics. At $V_G = 3.5\,\mathrm{V}$ the I_D-V_G curve exhibits a kink followed by a larger increase of I_D at $V_G > 3.5\,\mathrm{V}$. This behavior could not be observed in the experimental structure, since the break down voltage of the gate oxide was found to be below $V_G = 3.5\,\mathrm{V}$. The shape of the simulated transfer characteristics can be explained by the spatial distribution of the

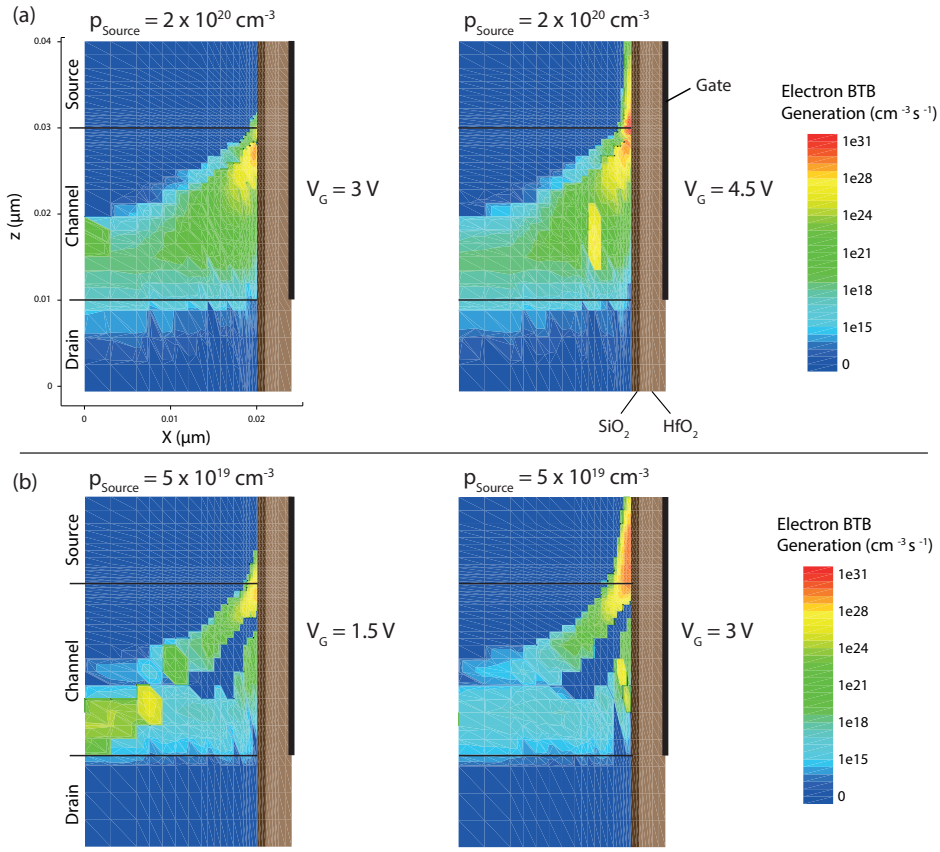

Figure 5.13: Simulated electron BTB generation in the right half of the simulated structure for (a) $p_{source} = 2 \times 10^{20}\,\mathrm{cm}^{-3}$ and (b) $5 \times 10^{19}\,\mathrm{cm}^{-3}$ at different values of V_G.

electrons generated by BTBT shown in Fig.5.13 (a). At $V_G = 3\,\mathrm{V}$ electrons are generated by point tunneling in the channel region causing the first hump in the transfer characteristics. The second hump for $V_G > 3.5\,\mathrm{V}$ is caused by line tunneling that occurs in the source region. The electron generation by line tunneling exceeds the point tunneling generation at high V_G, due to smaller tunneling distance and a larger tunnel junction area.

The gate voltage where line tunneling exceeds point tunneling can be shifted to smaller values of V_G by reducing the source doping level, since the inversion layer in the source is established for smaller gate potential. This is demonstrated in Fig.5.12 for source doping concentrations of $1 \times 10^{20}\,\mathrm{cm}^{-3}$ and $5 \times 10^{19}\,\mathrm{cm}^{-3}$. In addition, the point tunneling contribution decreases and S in this part of the transfer characteristics is degraded due to decreased

band bending at the tunnel junction, which can be observed in the transfer characteristics for $p_{source} = 1 \times 10^{20}\,\mathrm{cm}^{-3}$.
For $p_{source} = 5 \times 10^{19}\,\mathrm{cm}^{-3}$ no hump in the transfer characteristics and an improved minimum value of S are observed, indicating that line tunneling dominates the transfer characteristics. The spatial distribution of electrons generated by BTBT is shown in Fig.5.13 (b) at $V_G = 1.5\,\mathrm{V}$ and $3\,\mathrm{V}$. Line tunneling already occurs in the lower corner of the source at $V_G = 1.5\,\mathrm{V}$ and large electron BTB generation by line tunneling is observed for $V_G = 3\,\mathrm{V}$. The line tunneling contribution causes an about two orders of magnitude larger current at $V_G = 3\,\mathrm{V}$ for the smallest source doping concentration compared to the largest doping concentration. However, the decrease in source doping concentration also limits the maximum line tunnel current due to smaller band bending and thus increased tunneling distance as can be seen by comparing transfer characteristics of $p_{source} = 5 \times 10^{19}\,\mathrm{cm}^{-3}$ and $1 \times 10^{20}\,\mathrm{cm}^{-3}$ in Fig.5.12. The simulations state that the line tunneling mechanism could provide larger currents and improved subthreshold swing in a similar heterostructure device with reduced source doping level.

5.6 Conclusion

The SiGe/Si heterostructure TFET proved to be beneficial in terms of maintaining low I_{off} in combination with a small effective band gap at the tunneling junction. Thus, excellent I_{on}/I_{off} ratio up to eight orders of magnitude could be achieved in the heterostructure TFET. In comparison to the SiGe homostructure NW TFETs, shown in chapter 4, also the on-current per nanowire was increased due to the improved tunnel junction quality by in situ source doping and increased tunnel junction area due to the gate source overlap. The increased tunnel junction quality furthermore resulted in reduced TAT, superior output characteristics with decreased S-shape and fast current saturation at small V_{DS}. The latter two points are especially important in terms of utilizing the devices for logic application as will be discussed in the following chapter.
Furthermore, it has been demonstrated that the TFET on-current can be scaled by an enlarged tunnel junction area due to an expanded overlap of source and gate region. A drop of the applied drain voltage along the channel, however, limits the ability to scale I_{on} for large overlap lengths.
TCAD device simulations revealed that line tunneling could be employed as a tunnel current booster in the SiGe/Si heterostructure device with gate-source overlap. In order to achieve maximum device performance the source doping concentration needs to be adapted to the gate control and dimensions of the structure.

6 Logic Application

TFETs are supposed to be integrated in digital logic circuits for low power application. In order to reach this aim, not only the transfer characteristics of single transistors have to be studied, but also the characteristics of the basic components in integrated circuits performing logic operations need to be investigated. In this chapter the operation of a TFET inverter is compared to the same logic device built from complementary MOSFETs and the impact of progress in TFET I-V characteristics on inverter structures is demonstrated. The implications concerning power dissipation and field of application for the TFET will be discussed.

6.1 The Inverter

One essential logic operation in integrated circuits is turning a logic "1" into a logic "0". This operation is performed by an inverter, which is also called "NOT"-gate in electronics. The inverter consists of two complementary transistors and has one input and one output terminal plus two contacts which are connected to the supply voltage V_{DD} and ground potential, respectively. A logic "1" at the input gives a logic "0" at the output and vice versa.
Fig.6.1 (a) and (b) show a schematics of complementary MOSFETs and TFETs connected to a MOSFET and TFET inverter, respectively. The p-channel device of an inverter is also referred to as the pull-up transistor, since it connects V_{out} to V_{DD}, while the n-channel device is denoted pull-down transistor, since it connects V_{out} to the ground. For both kinds of inverters the input voltage V_{in} is applied to the connected gates, while the output voltage V_{out} is measured at the connected drain pads. In the TFET inverter the supply voltage V_{DD} is applied to the n-doped source region of the p-TFET and the p-doped source of the n-channel TFET is connected to ground potential. In the MOSFET inverter V_{DD} is connected to the source of the p-MOSFET and the source of the n-MOSFET is connected to ground.
Fig.6.2 exhibits a schematic graph of V_{out} as a function of V_{in}, which is called the voltage transfer characteristics (VTC) of an inverter. The switching threshold voltage V_M is defined as $V_{in} = V_{out}$. V_{IL} and V_{IH} denote the input voltages where the voltage gain of the inverter is $g = dV_{out}/dV_{in} = -1$. The corresponding output voltages are V_{OL} and V_{OH}. The noise margins for the "low" and "high" state are defined as $NM_L = V_{IL}$ and $NM_H = V_{DD} - V_{IH}$,

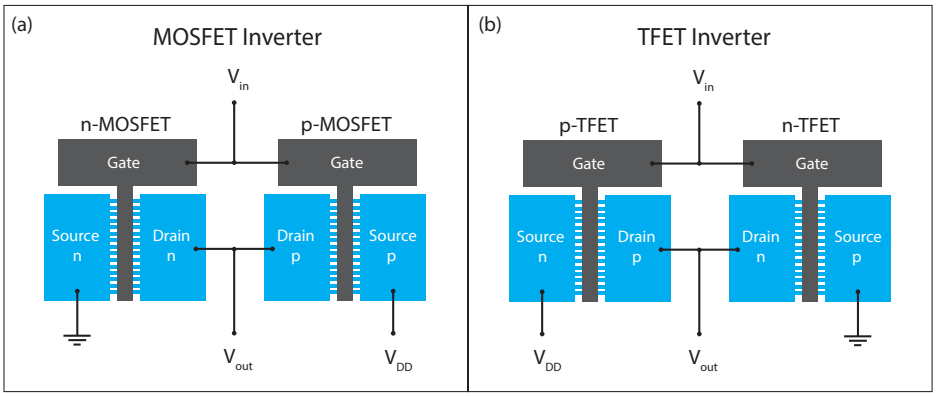

Figure 6.1: Schematic representation of (a) MOSFET and (b) TFET inverter from complementary NW transistors. The gate and drain pads are short-cut and used as input and output terminal, respectively, for measuring the voltage transfer characteristics (VTC). The source contacts are connected to supply voltage V_{DD} and ground.

respectively [82]. The average voltage gain of the inverter can be defined as:

$$g_{av} = \frac{V_{OH} - V_{OL}}{V_{IL} - V_{IH}} \,. \tag{6.1}$$

For a simplified VTC where V_{OL} and V_{OH} are close to zero and V_{DD}, respectively, the noise margins are given by:

$$NM_H = V_{DD} - V_{IH} = V_{DD} - \left(V_M - \frac{V_M}{g_{av}} \right) \tag{6.2}$$

and

$$NM_L = V_{IL} = V_M + \frac{V_{DD} - V_M}{g_{av}} \,. \tag{6.3}$$

According to these equations it is obvious that V_M should be as close to $V_{DD}/2$ as possible and g_{av} should be large in order to achieve the maximum noise margins.

The total power consumption P of an inverter can be calculated as the sum of static power P_{stat} when the inverter is either permanent in the "high" (logic "1") or "low" (logic "0") state and the dynamic Power P_{dyn} when the inverter switches from one state to the other. The static power consumption is given by

$$P_{stat} = I_{DD,0} \cdot V_{DD} \,, \tag{6.4}$$

where $I_{DD,0}$ is the short-circuit current through the transistors between V_{DD} and ground in the static case. $I_{DD,0}$ is determined by the off-current in the n- or p-channel transistor

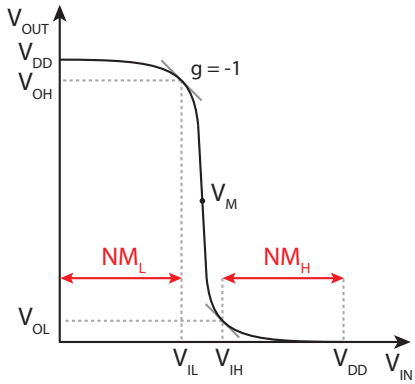

Figure 6.2: Schematic voltage transfer characteristics of an inverter.

in the "high"- or "low"-state, respectively. The dynamic power depends on the charge that needs to be transferred when the inverter is switched. The total capacitance is given by:

$$C_{out} = C_{Dp} + C_{Dn} + C_L \,, \tag{6.5}$$

where C_{Dp} and C_{Dn} are the drain capacitance of p- and n-channel transistor, respectively, and C_L is the load capacitance connected to the output terminal. Since the output of an inverter in integrated circuits is usually connected to the input of further logic elements, C_L depends on the gate capacitance of the transistors in these logic circuits and the capacitance of the interconnects. The total charge that is transferred during switching can be calculated as $Q = C_{out} \cdot V_{DD}$. The dynamic power can be expressed as:

$$P_{dyn} = V_{DD} \cdot Q \cdot f = C_{out} \cdot V_{DD}^2 \cdot f \,, \tag{6.6}$$

where f is the frequency of the signal change. Hence, the total power is given by:

$$P = C_{out} \cdot V_{DD}^2 \cdot f + I_{DD,0} \cdot V_{DD} \tag{6.7}$$

This equation states that the power consumption depends strongly on V_{DD} and that the frequency has a strong influence whether static or dynamic power dominate P.

The MOSFET and TFET inverters, which are compared in this chapter, were realized using the SSOI NW array devices presented in chapter 3. In the chip layout of these devices two transistors were placed close to each other and thus could be utilized for building inverter structures. In case of the TFET the transistors next to each other are identical, since symmetric TFETs can work as p- or n-channel devices. In case of the MOSFET inverter one n-channel device was placed next to a p-channel device. Fig.6.3 (a) exhibits a SEM top

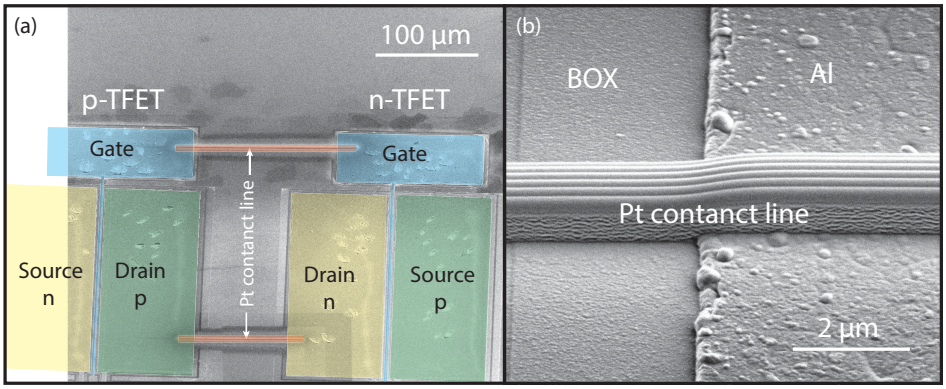

Figure 6.3: (a) Top view SEM image of two SSOI NW array TFETs connected by Pt contact lines to an inverter structure. (b) SEM image of a Pt contact line with a cross-section of $1 \times 1\,\mu\text{m}^2$ at the edge of an Al contact pad.

view of two TFETs connected to an inverter. The devices were connected using platinum (Pt) deposition in a focused ion beam (FIB) tool. Fig.6.3 (b) shows a magnification of the Pt connection line with a cross-section of $1 \times 1\,\mu\text{m}^2$ at the edge of an Al contact pad. The Pt lines connect the gates of both transistors as well as the two drain pads.

6.2 Voltage Transfer Characteristics

6.2.1 MOSFET Inverter

The voltage transfer characteristics (VTC) of MOSFET and TFET inverters were recorded by varying V_{in} from 0 V up to V_{DD} and measuring V_{out}. This measurement was repeated for different supply voltages V_{DD}. Fig.6.4 shows the I_D-V_G characteristics of n- and p-channel NW array MOSFETs with $10 \times 10\,\text{nm}^2$ NW cross-section and $2\,\mu$m gate length. The devices were connected and the inverter characteristics were measured according to the setup shown in Fig.6.1 (a). Fig.6.5 (a) shows the VTC of the MOSFET inverter at $V_{DD} = 1.5\,\text{V}$ and $2.0\,\text{V}$. For a symmetric characteristic of both transistors it is expected that V_{out} switches from V_{DD} to 0 V at $V_{in} = V_{DD}/2$. In the measured VTC of the MOSFET inverter, however, the switching occurs at $V_{in} < V_{DD}/2$. The transfer characteristics in Fig.6.4 suggest two reasons for the shift of the switching:

- The **threshold voltage** V_t of p- and n-MOSFET is asymmetric, which can be seen in the transfer characteristics. Thus the center of the transfer characteristics is shifted to negative V_G. This means that the p-MOSFET, which is switched on at $V_{in} = 0\,\text{V}$ switches off at a too small value of V_{in} and the switching point in the VTC moves to the left.

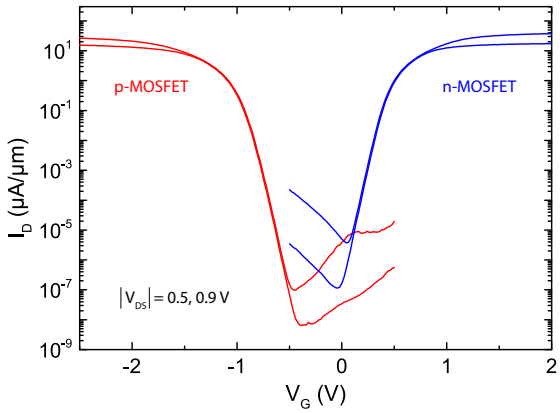

Figure 6.4: I_D-V_G characteristics of p-channel and n-channel SSOI NW array MOSFETs with 2 μm gate length.

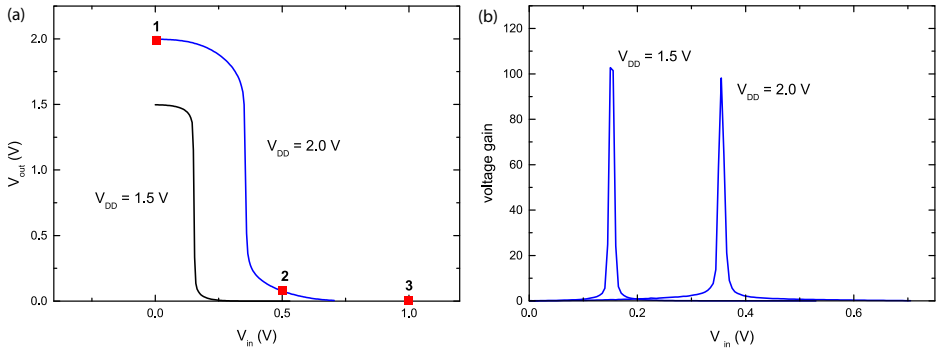

Figure 6.5: (a) Voltage transfer characteristics (VTC) of SSOI NW MOSFET inverter; (b) Voltage gain of the MOSFET inverter calculated from the derivative of VTC.

- The different **mobilities of electrons and holes** result in in a larger on-current in the n-MOSFET compared to the p-MOSFET, as shown in the transfer characteristics. The mobility of electrons in the channel is larger compared to the one of holes, causing a difference in on-current. Due to the smaller current in the p-MOSFET the switching point in the VTC moves to the left.

Both effects shift the switching point in the VTC to smaller values of V_{in}. For achieving a switching at $V_{in} = V_{DD}/2$ current levels as well as threshold voltages need to be matched at the same time. The current level of n- and p-MOSFET can be matched relatively easy by scaling the width of the devices to level out the difference in mobility. Hence, in standard CMOS design the p-MOSFET has three times the width of a n-MOSFET. Adapting V_t, however, can be achieved by tuning the gate work function, which depends on the gate metal. Realizing $V_{in} = V_{DD}/2$ is important in order to achieve high noise margins in the

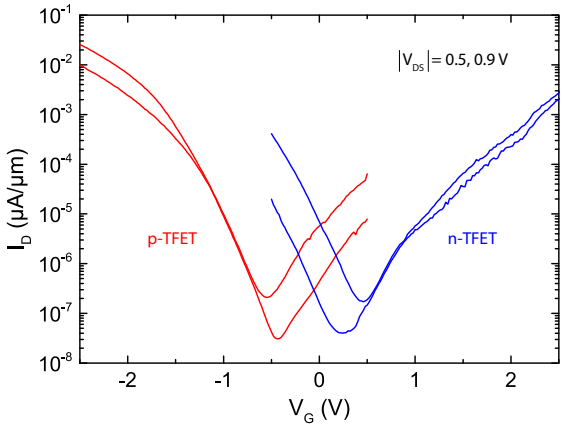

Figure 6.6: I_D-V_G characteristics of p-channel and n-channel SSOI NW array TFETs with 2 μm gate length..

logic circuits as previously shown. However, for the analysis of basic differences of MOSFET and TFET inverters the shift is of minor concern.
Fig.6.5 (b) exhibits the voltage gain of the MOSFET inverter as a function of V_{in}, which is calculated as the absolute value of the derivative of the VTC. A maximum voltage gain of 103 is observed at $V_{DD} = 1.5$ V. This large gain value is possible due to the subthreshold swing close to 60 mV/dec of the NW MOSFETs. At $V_{DD} = 2.0$ V the voltage gain decreases slightly. The VTC at this voltage shows a more pronounced decrease of V_{out} prior to the switching point, which can be explained by a degraded saturation of I_D at higher V_G.

6.2.2 TFET Inverter

The VTC of the TFET inverter was measured according to the setup shown in Fig.6.1 (b). Fig.6.6 exhibits the I_D-V_G characteristics of n- and p-channel NW array TFETs with $10 \times 10\,\text{nm}^2$ NW cross-section and 2 μm gate length. The on-current in the p-TFET is larger compared to the n-TFET and S is smaller due to the steeper doping profile of the tunnel junction as discussed in section 3.4.2. The minima of the transfer characteristics are almost symmetric to $V_G = 0$ V, with a small shift to the left. The VTC of the TFET inverter fabricated from these devices are shown in Fig.6.7 (a) for $V_{DD} = 1.5$ V to 3 V. In contrast to the MOSFET inverter the switching from V_{DD} to 0 V occurs close to $V_{DD}/2$ for all VTC. This is achieved since the larger on-current of the p-TFET and the shift of I_D-V_G curves cancel each other out with respect to the shift of the VTC.
It is noticeable that V_{out} in the TFET VTC does not reach V_{DD} and zero for low and high V_{in}, respectively. The MOSFET inverter VTC (Fig.6.5 (a)) in contrast do not exhibit this degradation of V_{out}. The reason for this effect in the VTC can be found in the strong ambipolarity of the I_D-V_G characteristics in Fig.6.6 and will be discussed in detail in the

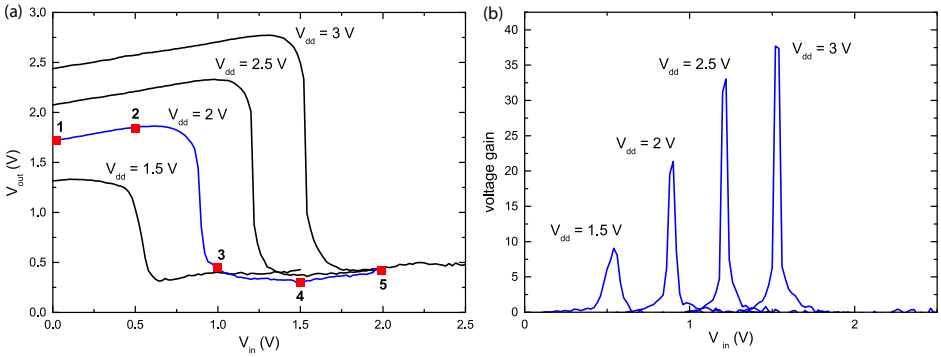

Figure 6.7: (a) Voltage transfer characteristics (VTC) of SSOI NW TFET inverter; (b) Voltage gain of the TFET inverter calculated from the derivative of VTC.

following section by analyzing the inverter supply currents.
The voltage gain of the TFET inverter calculated from the VTC is shown in Fig.6.7 (b). The maximum voltage gain increases from 9 at $V_{DD} = 1.5\,\mathrm{V}$ to 38 at $V_{DD} = 3\,\mathrm{V}$. Compared to the MOSFET inverter the gain values are smaller due to the larger S of the NW array TFETs. However, the gain of the TFET inverter at $V_{DD} = 1.5\,\mathrm{V}$ is still large enough to achieve acceptable noise margins.

6.3 Inverter Supply Current

In order to analyze the origin of the differences in the VTC of TFET and MOSFET inverter and compare the power consumption, the load lines, which correspond to the output curves of a single transistor, were measured for both transistors in the inverter. In order to analyze the current flow through each transistor at different points in the VTC, V_{in} was varied from $0\,\mathrm{V}$ to V_{DD} in steps of $0.5\,\mathrm{V}$. The current at the source of n-channel and p-channel transistor was measured as a function of V_{out}, which was swept from $0\,\mathrm{V}$ up to V_{DD} at each value of V_{in}. Fig.6.8 exhibits the results of this measurement for the TFET inverter at $V_{DD} = 2\,\mathrm{V}$. The point where the load curves of n- and p-channel device intersect for a certain value of V_{DD} gives the corresponding value of V_{out} in the VTC, since the current flow through both transistors has to be equal in the static case. The intersections of the load lines of both transistors are marked and numbered from one to five in Fig.6.8. These markers correspond to the markers shown in the VTC at $V_{DD} = 2\,\mathrm{V}$ in Fig.6.7.
The load line plot in Fig.6.8 reveals that the p-TFET is in the on-state at $V_{in} = 0\,\mathrm{V}$ and turns off for increasing V_{in}, while the n-TFET switches on. However, the current of the n-(p-)channel device in the off-state starts to increase when V_{out} increases (decreases). This is caused by the ambipolarity of the TFET transfer characteristics. The turn-on of the ambipolar branch in the off-state leads to an increased current flow in the transistor that is

supposed to be in the off-state and to the degradation of V_{out} in the high and low state of the inverter, as can be seen by comparing the markers in Fig.6.7 and Fig.6.8.
The current flow in the static "high" and "low" states, which refer to the markers one and five in Fig.6.8, is on the order of 10^{-8} A. Due to the ambipolarity the current flow in the static case is actually larger than the short circuit current at the switching point from marker two to three in Fig.6.8. Assuming the ambipolar branch in n- and p-TFET would be successfully suppressed, by an asymmetric design of both TFETs, $I_{DD,0}$ in the static case could be as low as 10^{-13} A.

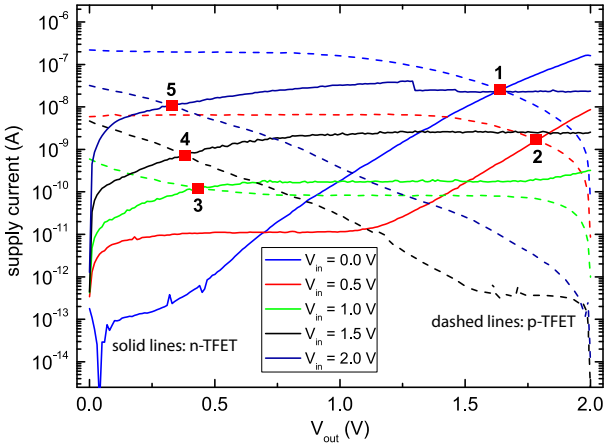

Figure 6.8: Measured load lines of the n-TFET (solid lines) and p-TFET (dashed lines) in the TFET inverter.

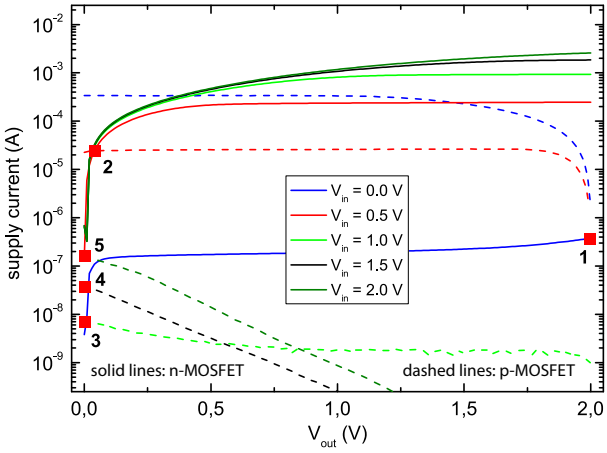

Figure 6.9: Measured load lines of the n-MOSFET (solid lines) and p-MOSFET (dashed lines) in the MOSFET inverter.

From the supply current plot it is obvious that a small inverse subthreshold slope, which means a rapid change of I_D with V_{in} is necessary to enable steep switching inverters. Additionally, a good saturation of the output curves at small values of V_{out} is crucial. This could be an important advantage of TFETs, since short channel effects in MOSFETs lead to DIBL which deteriorates the saturation of I_D, whereas TFETs are known to show less short channel effects and hence better current saturation.

Fig.6.9 shows the load line measurement of the MOSFET inverter at $V_{DD} = 2\,\mathrm{V}$. Again, the intersections of p- and n-MOSFET I_D curves at corresponding V_{in} are numbered and the markers are also shown in the MOSFET inverter VTC in Fig.6.5 (a). Note that markers 4 and 5 are not shown in the VTC due to choice of scale. The shift in V_t of p-MOSFET and n-MOSFET reflects in an asymmetry in the load line curves that causes the shift of the VTC. The transition from high to low state already occurs between $V_{in} = 0\,\mathrm{V}$ and $0.5\,\mathrm{V}$. The current in the low state increases for increasing V_{out} (from marker 3 to 5), since the potential difference from drain to channel increases and BTBT from channel to drain is enabled, also known as GIDL.
Taking the shift of the VTC into account, the current level for $I_{DD,0}$ in the MOSFET inverter is in the range between marker three and four in Fig.6.9 on the order of $10^{-8}\,\mathrm{A}$, which is comparable to $I_{DD,0}$ measured for the TFET. Hence, a TFET inverter with suppressed ambipolarity and possible $I_{DD,0} \approx 10^{-13}\,\mathrm{A}$ could offer a huge benefit in terms of static power consumption.

6.4 Emulated Heterostructure TFET Inverter

As seen in the previous section, the reduction of the ambipolarity is crucial in order to achieve a good TFET inverter performance. The SiGe/Si heterostructure NW TFETs presented in chapter 5 introduced a concept for reducing the ambipolarity in TFET devices and proved reduction of the p-branch in n-channel TFETs due to a larger band gap at the drain-channel tunnel junction as well as improved device performance. In order to analyze how the improved TFET characteristics of this device would effect the inverter performance, an inverter is modeled using the measured transfer and output characteristics of the n-channel SiGe/Si heterostructure TFET. The p-channel TFET is emulated by mirroring the n-channel transfer and output characteristics. Fig.6.10 exhibits the measured n-channel transfer characteristics and the emulated p-channel transfer characteristics. The threshold voltage of the transfer characteristics was adjusted to optimize the inverter performance.

In order to extract an inverter VTC from the measured n-TFET and emulated p-TFET, the I_D-V_{DS} dependence of the n-channel device was measured for small steps of V_G, which corresponds to V_{in} of the inverter. V_{DS}, which corresponds to V_{out}, was swept continuously

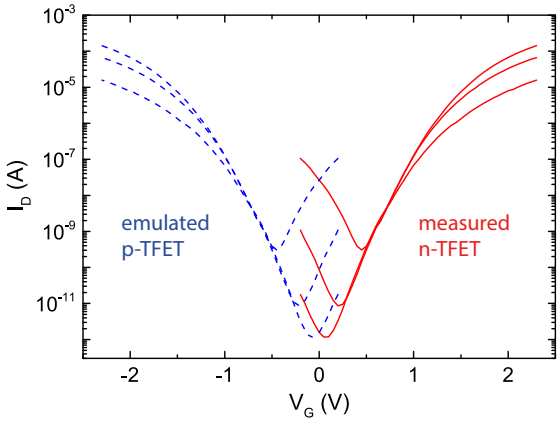

Figure 6.10: Measured transfer characteristics of an n-channel SiGe/Si nanowire array TFET and emulated p-channel transfer characteristics.

and V_G was stepped up to the corresponding supply voltage V_{DD}. The steps of V_G were 5 mV close to the inverter switching threshold and 40 mV else. The values for V_{out} of the VTC were extracted from the intersections of measured n-channel and emulated p-channel output characteristics at corresponding V_{in}. Fig.6.11 shows the output curves for $V_{DD} = 1\,\mathrm{V}$ and $0.5\,\mathrm{V}$. The VTC extracted from these curves are shown in Fig.6.12 for $V_{DD} = 1\,\mathrm{V}$, $0.5\,\mathrm{V}$ and $0.2\,\mathrm{V}$. The VTC exhibit high voltage gain of 44 at $V_{DD} = 1\,\mathrm{V}$ and even at V_{DD} as low as $0.2\,\mathrm{V}$ still a gain of 8 is achieved.
Compared to the measured SSOI NW TFET inverter (Fig.6.7), the VTC of the SiGe/Si heterostructure inverter show no degradation of V_{out} at high and low V_{in}, respectively. Fig.6.11 reveals that the load line curves of the devices in the off-state still increase with V_{out}, however, the suppression of the p-branch in the measured n-TFET in combination with the adjusted V_t is sufficient to prevent a degradation of V_{out}. The comparison of supply voltages $V_{DD} = 1\,\mathrm{V}$ and $0.5\,\mathrm{V}$ in Fig.6.11 also demonstrates that the degradation due to the ambipolarity is less severe at decreased V_{DD}. Furthermore the static power consumption is decreased due to the V_{DD} scaling by a factor of two and also by the reduction of $I_{DD,0}$ by a factor of 500 from $10^{-8}\,\mathrm{A}$ to $2 \times 10^{-11}\,\mathrm{A}$. This results in a reduction of P_{stat} by three orders of magnitude according to eq.(6.4).

A drawback of reducing V_{DD} from 1 V to $0.5\,\mathrm{V}$ is of course the reduction of the maximum on-current, that decreases by a factor of 300, resulting in a decrease of the maximum switching frequency f_{max} of the inverter. f_{max} is given by the inverse of the overall propagation delay t_p, which can be calculated from the charging and discharging times of the RC-circuit consisting of C_{out} and the resistance of the n- and p-channel transistor in the on-state R_n and R_p, respectively [82]. Since the propagation delay in an RC-circuit is given by $t_p = \ln(2)RC$,

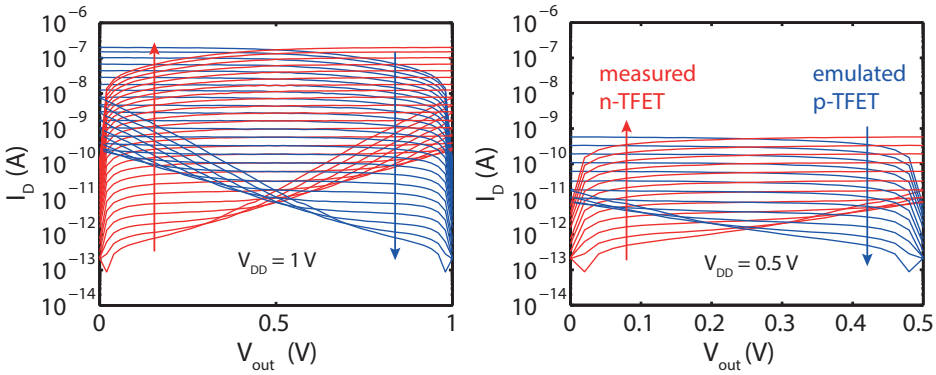

Figure 6.11: Load line plot with measured n-channel SiGe/Si heterostructure TFET and emulated p-TFET for $V_{DD} = 1\,\mathrm{V}$ (left) and $V_{DD} = 0.5\,\mathrm{V}$ (right). V_{in} increases in direction of the arrows from 0 V to V_{DD} in steps of 40 mV.

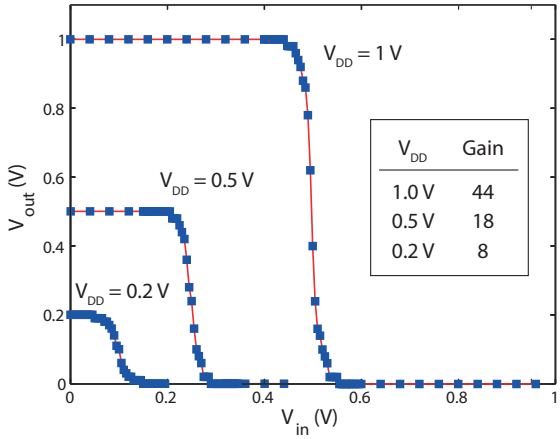

Figure 6.12: VTC extracted from measured n-channel SiGe/Si heterostructure and emulated p-channel characteristics at various V_{DD}. The table shows the corresponding maximum voltage gain extracted from the VTC.

t_p of the inverter can be calculated as the average propagation delay of n- and p-channel transistor, assuming that C_{out} is the same in both cases:

$$t_p = \ln(2) C_{out} \frac{(R_n + R_p)}{2} . \tag{6.8}$$

Thus, f_{max} decreases by a factor of 150 when V_{DD} is reduced from 1 V to 0.5 V, while the dynamic power consumption is decreased by a factor of 4 and the static power consumption by three orders of magnitude.
The improved VTC of the SiGe/Si heterostructure inverter can be attributed to the improved TFET device characteristcs. Especially the reduced S-shape in the output characteristics and saturation at small V_{DS} (see Fig.5.5) enable sufficient gain at voltages down to $V_{DD} = 0.2$ V. Also adjusting V_t is important to optimize TFET inverter characteristics. Since p- and n-branch in a TFET are separated by the potential difference depending on band gap, doping level and drain bias as shown in section 2.3.3 for a symmetric homojunction TFET, two different gate metals with adjusted work function for p- and n-channel device are required. A corresponding p-channel heterostructure TFET that would be required to build an heterostructure TFET inverter was already realized with a InGaAs based source and Si channel in [76]. Also an integration scheme for n- and p-channel heterostructures has recently been demonstrated [86].

6.5 Conclusion

In conclusion, inverters based on SSOI NW TFETs and MOSFETs have been demonstrated and compared. The analysis of the inverter supply currents revealed that a strong ambipolar behavior of TFETs is disadvantageous for the inverter VTC. The ambipolarity degrades the output voltage and increases the static power consumption. Nevertheless, high voltage gain of 44 was observed in the fabricated TFET inverter. The SSOI NW MOSFET inverter with close to ideal subthreshold swing shows a voltage gain exceeding 100. The static power consumption in the measured load line plots of the inverters is similar for MOSFETs and TFETs. However, a TFET structure with suppressed ambipolarity could offer a five orders of magnitude smaller P_{stat}.
The calculated VTC of an inverter built from the SiGe/Si heterostructure TFET presented in chapter 5 and a corresponding emulated p-TFET with equal performance, revealed large improvement compared to the SSOI TFET inverter. The reduced ambipolarity in the heterostructure TFET prevents the degradation of V_{out} and sufficiently large voltage gain was obtained down to very low V_{DD} of 0.2 V. The reason for the improvement can be found in the superior TFET output characteristics with reduced S-shape and saturation at smaller V_{DS}. Current saturation could be an important advantage of TFETs, since short channel effects in MOSFETs lead to DIBL which deteriorates the saturation of I_D, whereas TFETs are known to show less short channel effects and hence better current saturation.

A reduction of V_{DD} further reduces the influence of the ambipolar branch, and thus decreases the static power consumption by several orders of magnitude. The corresponding drop in on-current causes a drop in the maximum switching frequency. However, in many low power applications such as sensing, f_{max} is of minor importance, since frequencies in the kHz range are sufficient. Especially in passive systems without external power supply and in systems where P_{stat} dominates the total power consumption TFET logic elements with very low P_{stat} could be beneficial.

7 Low Frequency Noise

The analysis of electrical noise in electronic devices helps to understand the transport mechanism and to detect possibilities for improving the devices. Some noise sources can hereby be reduced by device improvement such as generation-recombination noise by reducing the number of traps. Other noise sources such as thermal noise are unavoidable since they are based on fundamental physical laws [38]. Despite the fact that various TFET devices have been studied experimentally, there are only very few publications reporting on low frequency noise (LFN) measurements [106] [8] [105]. In this chapter LFN in TFET devices presented in chapter 3 is measured and compared to LFN in MOSFET reference devices. The implications of the different transport mechanisms of thermal emission over a potential barrier in a MOSFET and BTBT in a TFET on the LFN are studied. Furthermore the influence of different device concepts and tunnel junction quality is discussed by comparing noise characteristics of SSOI NW TFET devices with ion implanted tunnel junction in chapter 3 and in-situ doped SiGe/Si heterostructure TFETs from chapter 5.

7.1 Measurement Setup

A schematic of the measurement setup for LFN analysis is shown in Fig.7.1. A battery in combination with an adjustable voltage divider is used as voltage source to apply gate bias (V_G) and source-drain bias (V_{DS}). The battery enables stable voltage bias conditions with minimal circuit fluctuations. The battery voltage supply for V_G is not shown in Fig.7.1 for simplicity. The capacitor connected to the battery and the voltage divider has a large capacitance of $9400\,\mu$F, which provides stable DC bias conditions and is at the same time transparent for AC signals due to a small AC resistance $R = 1/(\omega C)$. Hence, for AC signals such as electrical noise the load resistance R_{load} and sample resistance R_s of the device under test are connected in parallel to each other. The voltage noise spectral density S_V is measured with a combination of preamplifier, amplifier and signal analyzer connected to a computer. Preamplifier and amplifier have a gain of 128 and 100, respectively. The noise contribution by the amplifiers is calibrated and subtracted from the measured S_V. The voltage drop at the sample V_s and the total voltage drop V_{total} at sample and R_{load} are measured before and after each noise measurement. During the noise measurement the voltmeters are disconnected. The DC current through the sample is calculated by

$$I = \frac{V_{total} - V_s}{R_{load}}\,. \tag{7.1}$$

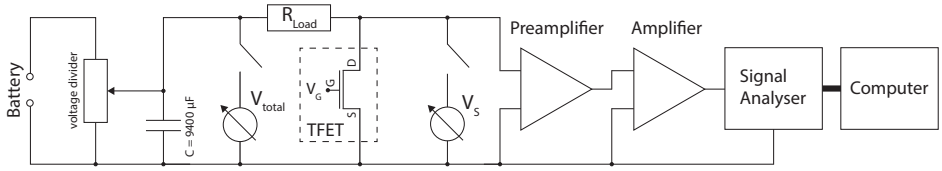

Figure 7.1: Schematic of the setup for low frequency measurements.

A larger load resistance enables the measurement of smaller currents. However, the intrinsic capacitance of the preamplifier on the order of 100 pF and R_{load} build up an RC circuit, which acts as a low-pass filter reducing S_V spectra at higher frequency. Hence the load resistance is chosen according to

$$\frac{R_{load}}{R_s} < \frac{1}{10}\,. \tag{7.2}$$

The cut-off frequency at 3 dB damping can be calculated by

$$f_c = \frac{1}{2\pi \cdot R \cdot C}\,. \tag{7.3}$$

For cut off frequencies in the order of the frequencies where the noise spectral density is measured the spectra need to be corrected for the damping of the RC circuit.

7.2 LFN Measurements

In order to compare LFN in TFETs and MOSFETs the p-channel SSOI NW array devices with NW diameter of $10 \times 10\,\mathrm{nm}^2$ and 400 nm gate length, which were already discussed in section 3.3, were used. These devices have the advantage that the process for TFET and MOSFET fabricated on the same chip, is exactly the same except from the implantation in source and drain. This excludes process related differences in LFN measurements and limits the comparison to the noise caused by the different transport mechanisms in the devices. The LFN spectra were measured at 300 K in a frequency range of 1 Hz to 2 kHz. The setup illustrated in Fig.7.1 records the voltage noise spectral density $S_V(f)$. The Current noise spectral density $S_I(f)$ can be derived from $S_V(f)$, when the current through the channel of the device increases linearly with the applied drain voltage V_{DS}. For such ohmic behavior $S_I(f)$ and $S_V(f)$ meet the relation [38]:

$$\frac{S_I(f)}{I^2} = \frac{S_V(f)}{V^2}\,. \tag{7.4}$$

$S_I(f)$ can be calculated according to

$$S_I(f) = S_V(f) \cdot \frac{I^2}{V^2} = \frac{S_V(f)}{R_{total}^2}\,, \tag{7.5}$$

with the total resistance of R_s and R_{load} in parallel:

$$R_{total} = \left(\frac{1}{R_s} + \frac{1}{R_{load}}\right)^{-1}. \tag{7.6}$$

7.2.1 MOSFET

In a MOSFET ohmic behavior can be assumed for small V_{DS} and sufficiently large V_G, which is apparent from I_D-V_{DS} characteristics in Fig.3.9 (a). $V_{DS} = -0.1\,\mathrm{V}$ was chosen to measure noise spectra as a function of V_G. The normalized current spectral density of the NW array MOSFET is shown in Fig.7.2 for V_G from $-1.05\,\mathrm{V}$ to $-1.3\,\mathrm{V}$. The spectra were measured with $R_{load} = 10\,\mathrm{k\Omega}$. The thermal noise, given by

$$S_{V,thermal} = 4k_BTR_{total} \tag{7.7}$$

was subtracted from the spectra in order to investigate the excess noise contribution only. The noise spectra show a $1/f$ behavior, which can be attributed either to channel mobility fluctuations $\Delta\mu$ or to carrier number fluctuations ΔN due to trapping at the oxide interface. Fig.7.3 shows the dependence of the normalized noise spectral density for $f = 10\,\mathrm{Hz}$ on I_D. Since fS_I/I_D^2 is basically proportional to $1/I_D$ and shows no strong correlation with $(g_m/I_D)^2$ Hooge mobility fluctuations can be assumed as origin of the MOSFET current noise [26][81]. Furthermore, the $1/I_D$ dependence of normalized flicker noise proves that the contribution of the contacts to the transistor noise is small [101]. In Fig.7.2 the noise level in the MOSFET decreases for increasing V_G since the number of carriers in the channel rises for increasing gate potential. The dependence of the normalized current noise on the number of carriers N is expressed by the Hooge empirical relation [38]:

$$\frac{S_I(f)}{I^2} = \frac{1}{f}\frac{\alpha_H}{N}\,, \tag{7.8}$$

where α_H is a dimensionless Hooge parameter and f the frequency where the noise is measured. The dimensionless parameter α_H can be used to compare noise characteristics in different materials and devices and has a value between 10^{-6} and 10^{-4} in high quality epitaxial layers [101]. However, it is degraded in devices due to surface effects and interface traps. In order to calculate α_H of the fabricated MOSFETs, N can be extracted by measuring the channel resistance [81]

$$R_{ch} = L^2/(q\mu N)\,, \tag{7.9}$$

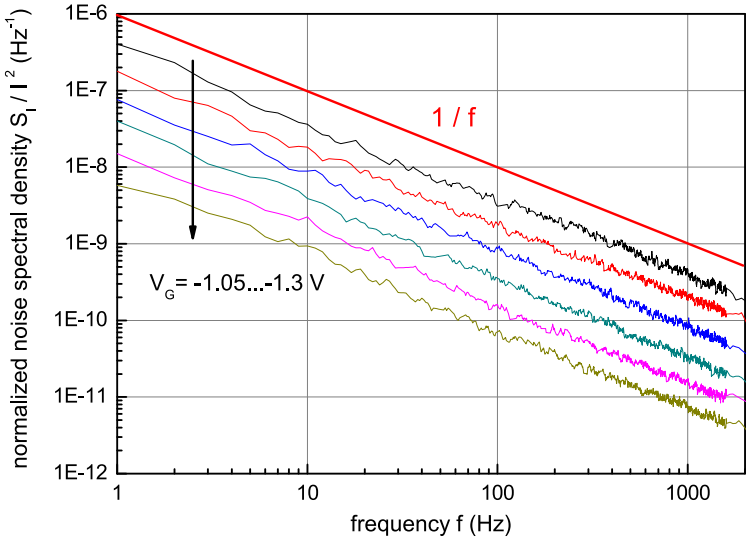

Figure 7.2: Normalized current noise spectra of a SSOI NW array MOSFET with 400 nm gate length at $V_{DS} = -0.1\,\mathrm{V}$ for different gate voltages. The red line represents a $1/f$ noise behavior.

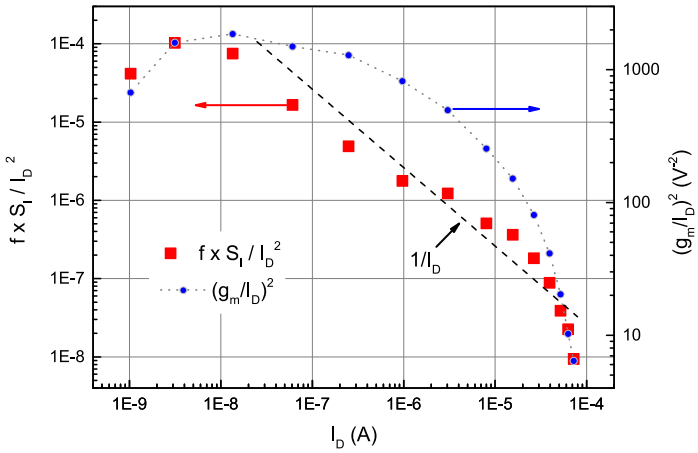

Figure 7.3: Normalized noise spectral density at $f = 10\,\mathrm{Hz}$ and $(g_m/I_D)^2$ as a function of the drain current I_D. The dashed black line resembles a $1/I_D$ dependence.

where q is the electron charge, L the channel length and μ the effective hole mobility. The effective hole mobility of the MOSFET was calculated using the I_D-V_G characteristics at $V_{DS} = -0.1\,\mathrm{V}$ and

$$\mu_h = \frac{1}{C_{ox}} \cdot \frac{L}{W} \cdot \frac{1}{(V_G - V_{th})} \cdot \frac{I_D}{V_{DS}}\,, \tag{7.10}$$

where W is the gate width, C_{ox} the oxide capacitance and V_{th} the threshold voltage of the MOSFET. C_{ox} was calculated for an equivalent oxide thickness (EOT) of $2.8\,\mathrm{nm}$ estimated from the thicknesses of the interfacial layer and HfO_2 in Fig.3.3. I_D was corrected for a source drain resistance of $1049\,\Omega$ extracted from additional MOSFET devices with different gate length presented in [84]. The resulting hole mobility is $\mu_h = 47\,\mathrm{cm}^2/\mathrm{Vs}$. This value is notable degraded compared to the universal hole mobility $\mu_0 = 170\,\mathrm{cm}^2/\mathrm{Vs}$ for (001) bulk Si MOSFETs at corresponding inversion carrier density. The reduction of mobility results from increased scattering at the surface of the tri-gated NWs with very small cross-section of $10 \times 10\,\mathrm{nm}^2$. Reduced mobility in Si NW structures for decreasing diameter is also reported in [17]. Furthermore it has been demonstrated that hole mobility in uniaxially strained NWs along [110] direction is reduced compared to unstrained NWs [57]. Increased Coulomb scattering due to the high-κ gate dielectric [64] and the coupling of carriers to surface soft-optical phonons [25] lead to further degradation of the mobility.
Using (7.9) and (7.8) α_H can be calculated as:

$$\alpha_H = \frac{S_I f L^2}{q \mu I_D V_D} \tag{7.11}$$

With S_I for $f = 10\,\mathrm{Hz}$, $V_{DS} = -0.1\,\mathrm{V}$ and $V_G = -1.15\,\mathrm{V}$ the extracted Hooge parameter is $\alpha_H = 7.3 \times 10^{-3}$. This value for α_H is in the typical range for MOSFET devices employing high-κ gate dielectrics with values between 10^{-3} and 2×10^{-2} [101],[28],[94]. The processed NW MOSFETs are used as reference devices for the LFN measurements on the TFETs in the following section. Both devices were processed on the same chip. Only the source doping type was varied to fabricate the TFET devices. This enables a direct comparison of LFN in MOSFET and TFET without distortion by process related effects.

7.2.2 TFET

Since the I_D-V_{DS} characteristics of the TFET shown in Fig.3.9 (b), exhibit a distinct S-shape, ohmic behavior can not be assumed for the whole range of V_{DS}. In order to find bias conditions meeting eq. (7.4) voltage noise spectral densities were measured at a constant $V_G = -1.8\,\mathrm{V}$ and V_{DS} from $-0.01\,\mathrm{V}$ to $-1\,\mathrm{V}$. Fig.7.4 shows S_I for $f = 10\,\mathrm{Hz}$ plotted as a function of I_D in a double logarithmic plot. The red line reflects I_D^2 proportionality. From the region fitting best to this relation $V_{DS} = -0.1\,\mathrm{V}$ was chosen to measure noise spectra as a function of V_G. The normalized current noise spectra of the p-TFET at $V_{DS} = -0.1\,\mathrm{V}$ and $V_G = -1.6\,\mathrm{V}$ to $-2.1\,\mathrm{V}$ are shown in Fig.7.5. The spectra were measured

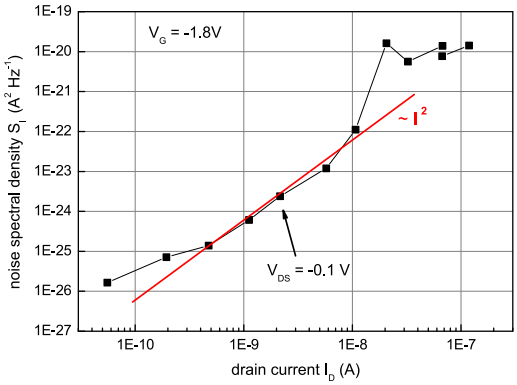

Figure 7.4: Dependence of current noise spectral density on drain current I_D as V_{DS} is changed for constant $V_G = -1.8\,\mathrm{V}$.

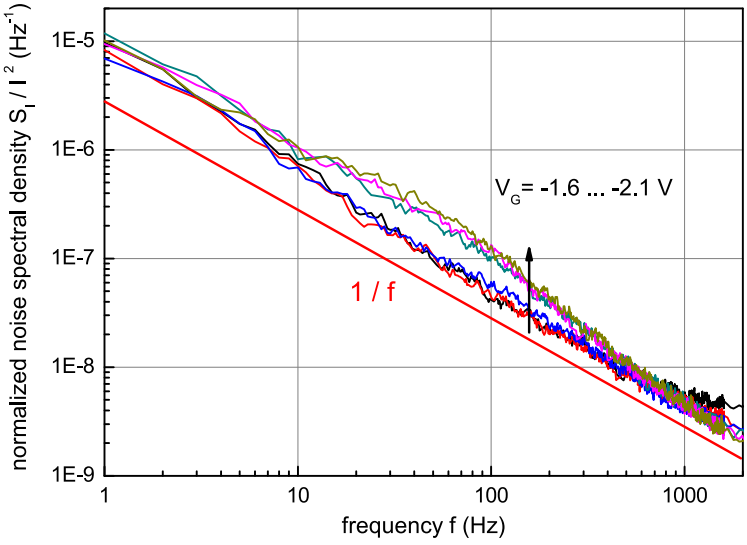

Figure 7.5: Normalized current noise spectra of a SSOI NW array TFET with 400 nm gate length at $V_{DS} = -0.1\,\mathrm{V}$ for different gate voltages. The red line represents a $1/f$ noise behavior.

with $R_{load} = 500\,\mathrm{k\Omega}$. Due to the large load resistance the cut-off frequency of the spectra is in the range of kHz and therefore the spectra were corrected for the damping at higher frequencies. In addition, the thermal noise was subtracted. The TFET noise spectra show a deviation from the clear $1/f$ behavior for the MOSFET. Also the gate voltage dependence of the spectra differs from the MOSFET. The normalized current noise is at least one order of magnitude larger compared to the MOSFET and is not decreasing with increasing V_G. The channel quality and the quality of the gate dielectric interface can be assumed to be equal for MOSFET and TFET because of the same processing. Based on this assumption the noise contribution from the channel region should be the same in both devices. The larger noise level of the TFET and the independence of the inversion carrier density indicate the existence of an additional noise source in the TFET. This additional contribution is presumably introduced by the spatially confined tunnel region at the source-channel junction, which acts as the dominant resistance in the device as shown in section 3.3.

An additional Lorentzian shaped component appears on the TFET noise spectra when V_G is changed from $-1.8\,\mathrm{V}$ to $-1.9\,\mathrm{V}$. This change in spectral shape can be explained by analyzing the time trace of the drain current using an oscilloscope. At gate voltages $\mid V_G \mid \geq 1.9\,\mathrm{V}$ a random telegraph signal (RTS) noise is observed in the time domain record of the drain current shown in Fig.7.6 (a) for $V_G = -2\,\mathrm{V}$. Characteristic for the RTS noise is the change of current between two or more discrete current levels at random times [111][45]. RTS noise in MOSFETs is caused by random trapping and de-trapping of carriers in slow traps located within the oxide [51]. When a certain V_G is reached charge carriers can tunnel into these slow oxide traps [85][66]. In a MOSFET I_D is than affected by fluctuations of the channel mobility due to the slow oxide trap. In a TFET the BTBT probability can be reduced when a trap is localized close to the tunnel junction and screens the electrical potential. The exponential dependence of the tunnel probability on the gate potential causes significant fluctuations of I_D [105].
The random switching between different discrete current levels results in a Lorentzian noise component with a $1/f^2$ dependence in the spectrum [65]. The sum of Lorentzians with homogeneously spread time constants results in a $1/f$ spectrum [97]. Hence, Lorentzian $1/f^2$ noise spectra are observed for devices with small gate area where only a few slow oxide traps occur. In a MOSFET this is usually the case for a gate area below $1\,\mu\mathrm{m}^2$ [105]. Due to the confined tunnel junction ($< 10\,\mathrm{nm}$) in the TFET, the total effective gate area is $< 0.3\,\mu\mathrm{m}^2$ considering the total width of all NWs in the array. Hence, the number of slow oxide traps in the device is supposed to be small. Fig.7.6 (b) exhibits a histogram of the drain current variation from the average I_D for a time trace of one second. The histogram exhibits two peaks, which correspond to two levels of the RTS caused by a single trap. A Gaussian function is fitted to each peak in order to extract the current difference and occupation time of each level. The current difference ΔI of the RTS levels is $0.9\,\mathrm{nA}$, which corresponds to $1.1\,\%$ of the total current. The current is $36\,\%$ of the time in the upper and $64\,\%$ of the time

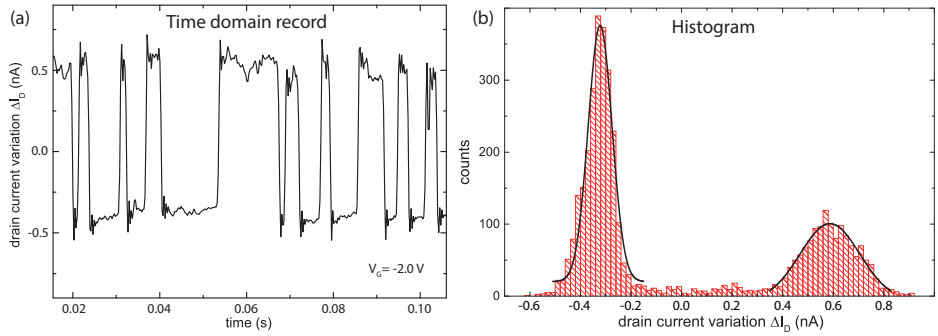

Figure 7.6: (a) Time domain record of the drain current variation from the average I_D at $V_G = -2\,\mathrm{V}$ showing random telegraph signal noise; (b) Histogram of drain current variation for a period of 1 second.

in the lower state of the RTS and the state changes 250 times in one second. According to this the average lifetimes are $\tau_{up} = 2.88\,\mathrm{ms}$ and $\tau_{down} = 5.12\,\mathrm{ms}$ for the upper and lower RTS state, respectively. The power spectral density of a two-level RTS signal is given by [111]:

$$S_I(f) = 4\Delta I^2 \frac{(\tau_{up}\tau_{down})^2}{(\tau_{up}+\tau_{down})^3} \frac{1}{1+4\pi f^2/f_c^2}\,. \tag{7.12}$$

The corner roll-off frequency f_c is given by $f_c = \tau_{up}^{-1} + \tau_{down}^{-1} = 542\,\mathrm{Hz}$. Since the noise spectra in Fig.7.5 are basically constant from $V_G = -1.6\,\mathrm{V}$ to $-1.8\,\mathrm{V}$, the spectrum of the RTS noise at $V_G = -2.0\,\mathrm{V}$ can be extracted by subtracting an average of the constant spectra from the spectrum with RTS. This RTS spectrum extracted from the measurements is compared in Fig.7.7 to a two-level noise spectrum calculated by equation (7.12) for the previously extracted lifetimes. The extracted spectrum is in good agreement with the calculated RTS noise from the time trace for frequencies above 10 Hz and shows the expected $1/f^2$ behavior of a Lorentzian noise contribution. This proves that the change in the TFET noise spectra in Fig.7.5 is caused by the on-set of an additional RTS noise.

Due to the small cross section of the NWs and the exponential dependence of the BTBT probability on the gate potential it seems likely that a slow trap in the oxide can degrade I_D in a single NW by orders of magnitude and turn it basically off. The measured relative change of I_D between the two RTS states, however, seems to be quite large with 1.1 %. Since the NW array consits of 1000 NWs in parallel and the trap causing the RTS can only affect a single wire, a maximum relative current change of 0.1 % is expected. However, process variations in width and doping profile of the $10 \times 10\,\mathrm{nm}^2$ NWs cause large variation in the performance of different NWs in the array. Hence, the current difference of the RTS levels is an indication that variation in the current contribution of single wires to I_D is large. This could also give a further explanation why the performance of the smaller NWs does not exceed that of the wider NWs as shown in section 3.4.1.

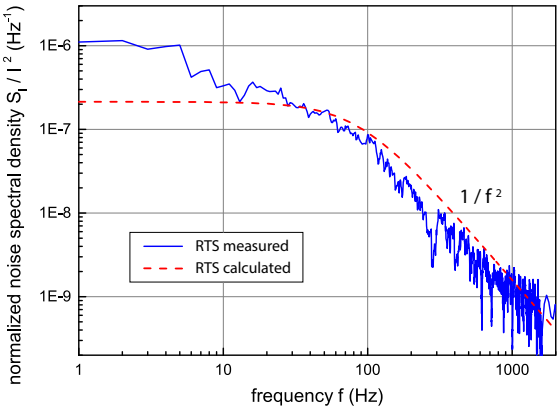

Figure 7.7: Current noise spectrum of the RTS noise calculated by subtracting an average of spectra without RTS noise from the spectrum at $V_G = -2\,\mathrm{V}$ (blue solid line). Calculated two level RTS noise spectrum for lifetimes extracted from the measured RTS (red dashed line) shows good agreement with measured RTS spectrum.

Noise at same current level

Fig.7.8 compares normalized current noise spectra of TFET and MOSFET for the same current level. For both devices spectra at $I_D = 3.1\,\mathrm{nA}$ are shown. Under these current conditions electrical noise in the MOSFET is about one order of magnitude higher compared to the TFET. Since the current in the MOSFET is up to three orders of magnitude higher in the on-state compared to the TFET the bias conditions for same I_D are quite different in both devices. V_G in the MOSFET is at $-0.7\,\mathrm{V}$ still slightly below the threshold voltage (see Fig.3.6 (a)). At the same current V_G in the TFET is at $-1.6\,\mathrm{V}$ and BTBT is switched on. Noise characteristics cannot be measured in the off-state of the TFET devices since the setup used for the measurements can only measure the excess noise for currents above 1 nA. For smaller currents the spectra are dominated by the thermal noise of the load resistance. However, at small current levels and for this reason presumably also in the off-state the noise level in the TFET can be below the noise level in a MOSFET. This could be related to the different mechanisms how the charge transport is suppressed in the off-state. In a MOSFET the current is blocked by the finite potential barrier, while a reverse biased p-i-n junction prevents the current flow in the TFET.

7.2.3 In-situ Doped Tunnel Junction

From the results of the previous sections it could be deduced that the tunnel junction adds the major noise contribution in a TFET. In order to study the influence of different TFET concepts on the noise level the SSOI TFET with ion implanted tunnel junction from chapter 3 is compared to the SiGe/Si heterostructure TFET with in-situ doped SiGe source from

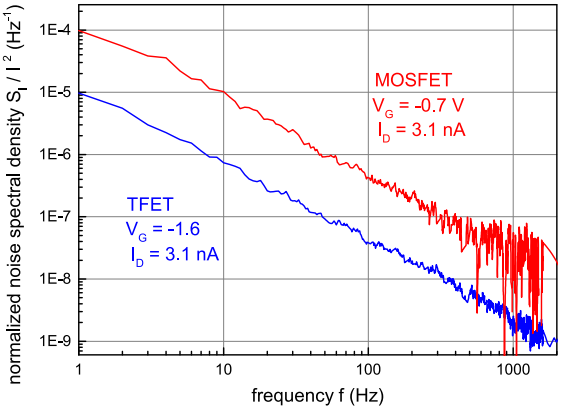

Figure 7.8: Normalized current noise spectra of MOSFET and TFET at the same current level of $I_D = 3.1\,\text{nA}$.

chapter 5. The compared devices both have a gate length of 400 nm, however, the tunnel junction area in the heterostructure TFET is much larger due to the overlap of source and drain (see Fig.5.2). Fig.7.9 shows the comparison of normalized current noise spectra from the p-channel SSOI and n-channel SiGe/Si heterostructure TFET. The spectra are measured at $V_{DS} = -0.1\,\text{V}$ and $0.1\,\text{V}$ for the p-channel and n-channel device, respectively. V_G is varied for both devices over a range of $0.6\,\text{V}$ starting at the same $\Delta V_G = 1.4\,\text{V}$ relative to the minimum of the transfer characteristics, which is at $V_{G,min} = -0.2\,\text{V}$ in case of the p-channel SSOI TFET and $V_{G,min} = 0.7\,\text{V}$ in case of the n-channel SiGe/Si TFET. At the smallest V_G both devices exhibit similar noise characteristics. However, the noise in the SSOI TFET is constant with increasing V_G until the additional Lorentzian contribution caused by RTS noise leads to an increase of the noise level, as previously shown. The current noise level in the SiGe/Si heterostructure device on the other hand decreases by a factor of three over the difference in V_G of $0.6\,\text{V}$. The decrease in noise level reminds of the SSOI MOSFET, which however was more pronounced and at smaller noise levels. The direct comparison of these devices is difficult though due to the differences in device structure as well as gate stack. The decrease of noise in the heterostructure TFET could be related to a smaller contribution by TAT in the in-situ doped tunnel junction, since it has been shown in [8] that the noise level decreases at low temperature (77 K) when trap assisted tunneling is suppressed and current is limited by BTBT.

Furthermore, the current noise spectra of the SiGe/Si heterostructure are close to $1/f$ behavior and show no indication of Lorentzian contributions by RTS noise. This could be related to the enlarged tunnel junction region all along the overlap of source and gate. Compared to the SSOI NW array TFETs with confined tunnel junction at the source channel junction, single oxide traps are less likely to suppress BTBT by orders of magnitude in this structure.

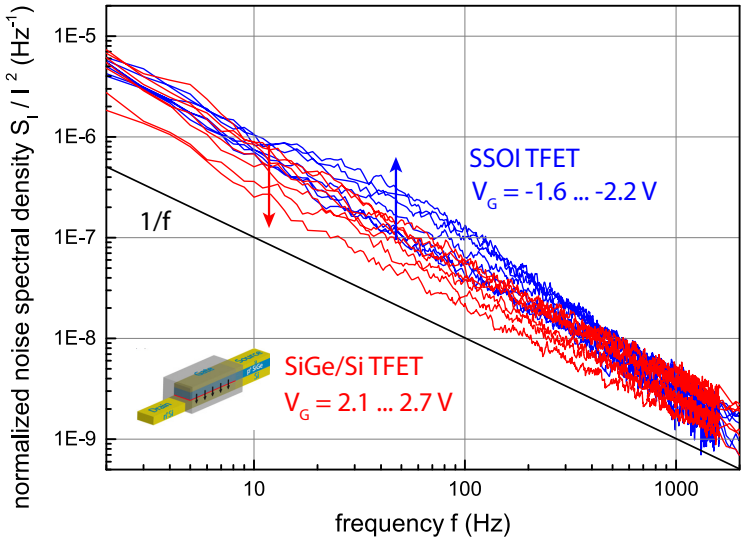

Figure 7.9: Normalized current noise spectra of SSOI NW TFET with ion implanted tunnel junction (blue) and SiGe/Si heterostructure NW TFET with in-situ doped SiGe source (red).

7.3 Literature Comparison

The results on the LFN noise in TFETs of this chapter can be compared to the few published LFN measurements in literature. In contrast to results on n-type planar FD-SOI TFETs with 6 nm SiO_2 gate dielectric and ion implanted junctions [105], [106], which showed distinct $1/f^2$ behavior, TFETs in this work show close to $1/f$ noise spectra and only additional Lorentzian contributions by RTS noise. On-currents of the TFETs in [105], [106] are very small and gate voltages up to 6 V are applied. In these devices RTS noise was recorded, which presumably dominates the spectra causing the $1/f^2$ behavior. More mature devices as the SSOI and SiGe/Si heterostructure TFETs presented in this work seem to exhibit close to $1/f$ noise characteristics as it was also shown by measurements on vertical III-V TFET structures with in situ doped junctions reported in [8]. The vertical InGaAs n-TFET structure with in-situ doped junction showed normalized noise current levels of $10^{-6}\,\mathrm{Hz}^{-1}$ at $f = 10\,\mathrm{Hz}$, which matches the noise level of both TFET devices presented in this work. However, the drain current level where the LFN was measured ($2\,\mu\mathrm{A}/\mu\mathrm{m}$) for devices in [8] is three orders of magnitude larger compared to LFN measurements on the SSOI NW TFETs in this work.

7.4 Conclusion

In conclusion, it was observed that LFN in SSOI NW TFETs exceeds the noise level of MOSFETs fabricated with the same process by at least one order of magnitude in the on-

state. The absence of a gate voltage dependence on the noise level indicates that the tunnel junction acts as the dominant noise source in the TFET, rather than the channel as in MOSFETs. Due to the spatial confined tunnel junction TFETs are more likely to exhibit RTS noise, comparable to MOSFETs with very small channel area. Hence, oxide traps close to the tunnel junction as well as defects in the tunnel junction caused by ion implantation play an important role for noise characteristics in a TFET with small tunnel junction. The concept of an enlarged tunnel junction area due to the overlapping source and gate as in the presented SiGe/Si heterostructure TFET may reduce the influence by traps on the BTBT. Furthermore, TFET devices exhibit current noise spectra with close to $1/f$ dependence as long as no dominant RTS is observed in the drain current. Literature comparison reveals similar normalized current noise levels measured at 300 K for TFET devices with essential differences in semiconductor material as well as in structure. Low temperature measurements in [8], however, indicate that reduction of trap assisted tunneling can lower the noise level.

8 Conclusion and Outlook

Within the framework of this thesis possibilities of improving TFET performance have been experimentally demonstrated based on design rules deduced from physical BTBT probability relations. The aim was to increase the on-current and to reduce the subthreshold swing of TFETs by realizing devices with decreased λ, E_g and m^*. Hence, the fabricated TFETs consisted of arrays of NWs to allow for tri-gate architecture to maximize electrostatic gate control by minimizing λ_{ch}. Strained Si on insulator substrates have been employed to process uniaxial tensile strained NWs with E_g reduced by about 30 meV. SSOI NW TFETs in combination with high-κ/metal gate stack proved to have 20 times improved current at $V_{DS} = 0.5\,\mathrm{V}$ and $V_G = 1.5\,\mathrm{V}$ and reduced S compared to similar TFET devices using SiO_2/poly-Si gate stack presented in [89].
In comparison to NW MOSFET fabricated with the same process typical TFET characteristics like the increase of subthreshold slope with V_G and small temperature dependence of S have been demonstrated. By comparison to an analytical model it has been shown that the temperature dependence of the band gap causes the dominating effect in the temperature dependence of the on-current. Furthermore, charge pumping measurements revealed that hot carrier effects in the large electric field of the tunnel junction can cause degradation of the gate oxide resulting in a decrease of tunneling current.
Further reduction of E_g and m^* was achieved by the fabrication of NW TFETs based on strained SiGe on SOI substrates. Enhanced on-current was demonstrated by increasing the Ge content in the SiGe layer from 35 % to 50 %. For 50 % Ge content the BTBT current could be increased by one order of magnitude compared to the SSOI NW TFETs. However, also an off-current increase due to larger SRH generation and channel-drain tunneling was observed. The analysis of the density of interface states by charge pumping experiments revealed an one order of magnitude larger D_{it} level limiting the electrostatic gate control an degrading S. A relatively large temperature dependence of the transfer characeristics indicated that trap assisted tunneling is a dominant process in the SiGe NW TFET, leading to further degradation of S and increased current in the off-state. The high impact of TAT is correlated to the damage caused by ion implantation and the need for a low thermal budget to prevent Ge diffusion in the device resulting in a higher trap density in the junction.
In order to prevent off-current degradation, occurring for TFETs based on small band gap materials, while maintaining the advantageous small band gap at the tunneling junction a heterostructure TFET based on the NW array design has been conceived and fabricated. An in-situ boron doped $Si_{0.5}Ge_{0.5}$ source provided superior tunnel junction quality compared to

the implanted SiGe homojunction NWs. The TAT contribution to I_D was small as proven by temperature dependent measurements. A small I_{OFF} was achieved by the larger band gap of the Si channel and drain. The increased tunnel junction area due to overlapping source and drain in combination with the high quality tunnel junction resulted in enhanced I_{ON} per NW compared to the SiGe homostructure device. Thus, a high I_{ON}/I_{OFF} ratio of up to eight orders of magnitude was achieved in the heterostructure TFET. Furthermore, the ambipolar branch could be reduced due to the asymmetric design of the heterostructure. A suppression of the p-branch in the n-channel heterostructure TFET was successfully demonstrated. However, for ion implanted drain contacts a trade-off between low ohmic resistance and decreased channel-drain tunneling was observed.
The feasibility of TFETs for logic application has been studied by the fabrication of inverters based on the SSOI NW TFETs. Voltage transfer characteristics with maximum gain of 40 at $V_{DD} = 3\,\mathrm{V}$ and sufficient gain down to $1.5\,\mathrm{V}$ have been measured for the TFET inverters. It has been observed that the ambipolar characteristics of the TFETs cause a degradation of the inverter output voltage. The comparison to MOSFET inverters fabricated from SSOI NW MOSFETs revealed that an equivalent TFET inverter with suppressed ambipolarity could offer an up to five orders of magnitude reduced current flow in the off-state of the inverter. Thus, the TFET could provide a substantial reduction of static power consumption. An emulated TFET inverter build from the n-channel SiGe/Si heterostructure TFET and a corresponding p-channel TFET under optimized threshold voltage conditions, revealed sufficient voltage gain at ultra-low supply voltages down to $V_{DD} = 0.2\,\mathrm{V}$. This enhanced performance is enabled by the improved output characteristics of the heterostructure TFET with in-situ doped source, providing reduced S-shape and current saturation at small values of V_{DS}. Additionally the degradation of V_{out} is prevented by the reduced ambipolarity of the heterostructure. The demonstration of logic operation at very small values of V_{DD} proves the feasibility of reduced dynamic power consumption with the application of TFET inverters. A drawback of the very low supply voltage in the TFET inverter, however, is the limited on-current that results in a limited maximum switching speed of the inverter.
Low frequency noise characterization of SSOI NW TFETs in comparison to MOSFET devices revealed that the dominant noise contribution is generated in the tunnel junction of the TFET. The spatially confined tunnel junction of the TFET, which provides the main resistance in the device, is more likely to exhibit RTS noise. Single traps screening the gate potential can have large influence on I_D due to the exponential dependencies of BTBT on the applied potential. An enlarged tunnel junction as in the SiGe/Si heterostructure could provide an effective mean to reduce RTS noise in the TFET.
Continuous progress was achieved for the TFETs fabricated in this work. However, further improvements of on-current as well as subthreshold swing are necessary to fulfill requirements for bringing TFETs into application. Smaller band gap materials like strained SiGe proved to be beneficial for increasing the BTBT current. Further improvement in the SiGe

homostructure NW devices could for example be achieved by enhancing the tunnel junction quality. Forming highly doped source regions with small trap densities, for example, was achieved in Si TFET devices by silicidation and dopant segregation in [50]. This process could be adapted for the SiGe NWs and offer improved performance in combination with the smaller SiGe band gap. A silicided drain region in the SiGe/Si heterostructure could likewise suppress the ambipolar branch, as was demonstrated by the reduced doping concentration, while providing small series resistance, thus enabling high on-current. Further decrease of the NW width and a reduction of the interfacial oxide layer would scale down λ_{ch} with an exponential effect on I_{ON}. The structure could also benefit from an Ω-shaped gate or GAA architecture to increase the gate control at the bottom Si layer.

In conclusion, TFET devices fabricated in this work proved to have high potential for reducing static as well as dynamic power consumption in integrated circuits. Especially in systems which are in stand-by mode most of the time and where switching frequency of transistors is moderate static power consumption is the most important issue. In this field of application TFETs could provide a substantial asset. Since static power consumption scales linearly with I_{OFF}, reduction by several orders of magnitude seems possible by utilizing TFETs. The exponential dependency of the BTBT current on gate control makes TFETs also interesting, for example for sensing application. The exponential dependencies of the BTBT current on design and material parameters also leaves much room for further improvement of I_{ON} and further research could increase performance in order to make TFETs also feasible for applications with a higher demand on switching speed.

Bibliography

[1] A. Abbadie, J. Hartmann, P. Besson, D. Rouchon, E. Martinez, P. Holliger, C. Di Nardo, Y. Campidelli, and T. Billon. Wet cleaning and surface characterization of Si1-xGex virtual substrates after a CMP step. *Applied Surface Science*, 254 (21):6793–6798, Aug 2008.

[2] A. Abbadie, J. Hartmann, C. D. Nardo, T. Billon, Y. Campidelli, and P. Besson. An efficient wet-cleaning of SiGe virtual substrates and of thick, pure Ge layers on Si(001) after a chemical mechanical planarization step. *Microelectronic Engineering*, 83(10): 1986–1993, Oct 2006.

[3] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris. Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors. *Physical Review Letters*, 93(19):1–4, Nov 2004.

[4] U. Avci, R. Rios, K. Kuhn, and I. Young. Comparison of Performance, Switching Energy and Process Variations for the TFET and MOSFET in Logic. *Symposium on VLSI Technology (VLSIT) 2011*, page 124–125, 2011.

[5] S. Banerjee, W. Richardson, J. Coleman, and A. Chatterjee. A new three-terminal tunnel device. *IEEE Electron Device Letters*, 8(8):347–349, Aug 1987.

[6] S. Baudot, F. Andrieu, F. Rieutord, and J. Eymery. Elastic relaxation in patterned and implanted strained silicon on insulator. *Journal of Applied Physics*, 105(11):114302, 2009.

[7] S. Bergmann and C. Schaefer. *Lehrbuch der Experimentalphysik, Bd.6 Festkörper*. De Gruyter, 3rd edition, 1992. Abb.1.19 pp.

[8] R. Bijesh, D. Mohata, and S. Datta. Flicker noise characterization and analytical modeling of homo and hetero-junction III–V tunnel FETs. *DRC Conference 2012*, page 6–7, 2012.

[9] D. Buca, S. Feste, B. Holländer, S. Mantl, R. Loo, M. Caymax, R. Carius, and H. Schaefer. Growth of strained Si on He ion implanted Si/SiGe heterostructures. *Solid-State Electronics*, 50(1):32–37, Jan 2006.

[10] D. Buca, R. A. Minamisawa, H. Trinkaus, B. Holländer, S. Mantl, R. Loo, and M. Caymax. Si ion implantation for strain relaxation of pseudomorphic Si(1-x)Ge(x)/Si(100) heterostructures. *Journal of Applied Physics*, 105(11):114905, 2009.

[11] W. Chen, V. G. Dubrovskii, X. Liu, T. Xu, R. Larde, J. Philippe Nys, B. Grandidier, D. Stievenard, G. Patriarche, and P. Pareige. Boron distribution in the core of Si nanowire grown by chemical vapor deposition. *Journal of Applied Physics*, 111(9): 094909, 2012.

[12] J. S. Christensen. *Dopant diffusion in Si and SiGe*. PhD thesis, KTH, 2004.

[13] J. Colinge. Novel gate concepts for MOS devices. *Solid-State Device Research conference 2004*, pages 45–50, 2004.

[14] N. C. Das and V. Nathan. Hot carrier degradation in MOSFETs: a charge pumping study. *Semiconductor science and technology*, 549, 1993.

[15] S. Datta. Exclusion principle and the landauer-büttiker formalism. *Physical Review B*, 45(3):1347–1362, 1992.

[16] G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, and N. Mukherjee. Fabrication, characterization, and physics of III–V heterojunction tunneling Field Effect Transistors (H-TFET) for steep sub-threshold swing. *2011 International Electron Devices Meeting*, 3:33.6.1–33.6.4, Dec 2011.

[17] J. Dura, F. Triozon, D. Munteanu, S. Barraud, S. Martinie, and J. L. Autran. Electronic transport in GAA silicon nanowire MOSFETs: From Kubo-Greenwood mobility including screening remote coulomb scattering to analytical backscattering coefficient. *2012 15th International Workshop on Computational Electronics*, page 1–4, May 2012.

[18] S. Eguchi, J. L. Hoyt, C. W. Leitz, and E. A. Fitzgerald. Comparison of arsenic and phosphorus diffusion behavior in silicon–germanium alloys. *Applied Physics Letters*, 80(10):1743, 2002.

[19] T. Elewa, H. Haddara, S. Cristoloveanu, and M. Bruel. Charge pumping in silicon on insulator structures using gated p-i-n diodes. *JOURNAL DE PHYSIQUE*, 49(9): 137–140, 1988.

[20] T. Ernst, S. Cristoloveanu, A. Vandooren, T. Rudenko, and J.-P. Colinge. Recombination Current Modeling and Carrier Lifetime Extraction in Dual-Gate Fully-Depleted SOI Devices. *Transactions on Electron Devices, IEEE*, 46(7):1503–1509, 1999.

[21] L. Esaki. New Phenomenon in Narrow Germanium p-n Junctions. *Physical Review*, 109(2):603–604, 1958.

[22] I. Ferain, C. a. Colinge, and J.-P. Colinge. Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors. *Nature*, 479(7373):310–6, Nov 2011.

[23] S. Feste, J. Knoch, S. Habicht, D. Buca, Q.-T. Zhao, and S. Mantl. Silicon nanowire FETs with uniaxial tensile strain. *Solid-State Electronics*, 53(12):1257–1262, Dec 2009.

[24] M. Fischetti. Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys. *Journal of Applied Physics*, 80(4), 1996.

[25] M. V. Fischetti and S. E. Laux. Long-range Coulomb interactions in small Si devices. Part I: Performance and reliability. *Journal of Applied Physics*, 89(2):1205, 2001.

[26] G. Ghibaudo, O. Roux, C. Nguyen-Duc, F. Balestra, and J. Brini. Improved Analysis of Low Frequency Noise in Field-Effect MOS Transistors. *Physica Status Solidi (a)*, 124(2):571–581, Apr 1991.

[27] B. Ghyselen, J.-M. Hartmann, T. Ernst, C. Aulnette, B. Osternaud, Y. Bogumilowicz, A. Abbadie, P. Besson, O. Rayssac, and A. Tiberj. Engineering strained silicon on insulator wafers with the Smart Cut(TM) technology. *Solid-State Electronics*, 48(8): 1285–1296, Aug 2004.

[28] G. Giusi, E. Simoen, G. Eneman, P. Verheyen, F. Crupi, K. De Meyer, C. Claeys, and C. Ciofi. Low-frequency (1/f) noise behavior of locally stressed HfO_2/TiN gate-stack pMOSFETs. *IEEE Electron Device Letters*, 27(6):508–510, Jun 2006.

[29] E. Gnani, P. Maiorano, S. Reggiani, A. Gnudi, and G. Baccarani. Investigation on Superlattice Heterostructures for Steep-Slope Nanowire FETs. *Device Research Conference (DRC), 2011*, page 201–202, 2011.

[30] E. Gnani, S. Reggiani, a. Gnudi, and G. Baccarani. Drain-conductance optimization in nanowire TFETs. *2012 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, (2):105–108, Sep 2012.

[31] K. Gopalakrishnan, P. Griffin, and J. Plummer. I-MOS: a novel semiconductor device with a subthreshold slope lower than kT/q. *Digest. International Electron Devices Meeting (IEDM) 2002*, page 289–292, 2002.

[32] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. D. Keersmaecker. A Reliable Approach to Charge-Pumping Measurements in MOS Transistors. *IEEE Transactions on Electron Devices*, 31(1):42–53, 1984.

[33] S. Guha and V. Narayanan. High-κ /Metal Gate Science and Technology. *Annual Review of Materials Research*, 39(1):181–202, Aug 2009.

[34] R. N. Hall and J. H. Racette. Diffusion and Solubility of Copper in Extrinsic and Intrinsic Germanium, Silicon, and Gallium Arsenide. *Journal of Applied Physics*, 35 (2):379, 1964.

[35] J. Han, R. Zhang, T. Osada, M. Hata, M. Takenaka, and S. Takag. Reduction in Interface Trap Density of Al2O3/SiGe Gate Stack by Electron Cyclotron Resonance Plasma Post-nitridation. *Applied Physics Express*, 6:1–4, 2013.

[36] J. M. Hartmann, Y. Bogumilowicz, P. Holliger, F. Laugier, R. Truche, G. Rolland, M. N. Séméria, V. Renard, E. B. Olshanetsky, and O. Estibals. Reduced pressure chemical vapour deposition of SiGe virtual substrates for high mobility devices. *Semiconductor Science and Technology*, 19(3):311–318, Mar 2004.

[37] B. Holländer, S. Lenk, S. Mantl, H. Trinkaus, D. Kirch, M. Luysberg, T. Hackbarth, H.-J. Herzog, and P. F. P. Fichtner. Strain relaxation of pseudomorphic SiGe/Si (100) heterostructures after hydrogen or helium ion implantation for virtual substrate fabrication. *Nuclear instruments and methods in physics research / B*, 177:357–367, 2001.

[38] F. N. Hooge, T. G. M. Kleinpenning, and L. K. J. Vandamme. Experimental studies on 1/f noise. *Rep. Prog. Phys.*, 44:479, 1981.

[39] J. Huang, J. Fu, C. Zhu, A. A. O. Tay, Z.-Y. Cheng, C. W. Leitz, and A. Lochtefeld. A Study of compressively strained Si0.5Ge0.5 metal-oxide-semiconductor capacitors with chemical vapor deposition HfAlO as gate dielectric. *Applied Physics Letters*, 90 (4):023502, 2007.

[40] S. Huang, X. Guan, J. Zhang, V. Moroz, V. Wang, and Z. Yu. Design of Complementary GAA-NW tunneling-FETs of Axial Si-Ge Heterostructure. *IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC), 2010*, pages 6–9, 2010.

[41] A. M. Ionescu and H. Riel. Tunnel field-effect transistors as energy-efficient electronic switches. *Nature*, 479(7373):329–37, Nov 2011.

[42] K. Kao, A. S. Verhulst, W. G. Vandenberghe, and K. De Meyer. Optimization of Gate-on-Source-Only Tunnel FETs With Counter-Doped Pockets. *IEEE Transactions on Electron Devices*, 59(8):2070–2077, 2012.

[43] W. Kern and D. A. Puotinen. Cleaning solutions based on hydrogen peroxide for use in silicon semiconductor technology. *RCA Rev.*, 31:187–206, 1970.

[44] S. Kim, H. Kam, C. Hu, and T. Liu. Germanium-source tunnel field effect transistors with record high I_{ON}/I_{OFF}. *VLSI 2009*, page 178–179, 2009.

[45] M. Kirton and M. Uren. Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/ f) noise. *Advances in Physics*, 38(4):367–468, Jan 1989.

[46] J. Knoch and J. Appenzeller. A novel concept for field-effect transistors - the tunneling carbon nanotube FET. *Device Research Conference (DRC) Digest, 2005*, 2005.

[47] J. Knoch, M. T. Bjork, H. Riel, H. Schmid, and W. Riess. One-Dimensional Nanoelectronic Devices - Towards the Quantum Capacitance Limit. *2008 Device Research Conference*, page 173–176, Jun 2008.

[48] J. Knoch, S. Mantl, and J. Appenzeller. Impact of the dimensionality on the performance of tunneling FETs: Bulk versus one-dimensional devices. *Solid-State Electronics*, 51(4):572–578, Apr 2007.

[49] J. Knoch, S. Mantl, and R. Waser (Editor). *Nanoelectronics and Information Technology*. Wiley-VCH, 3rd edition, 2012. 347 pp.

[50] L. Knoll, Q.-t. Zhao, A. Nichau, S. Trellenkamp, S. Richter, A. Schäfer, D. Esseni, L. Selmi, K. K. Bourdelle, and S. Mantl. Inverters With Strained Si Nanowire Complementary Tunnel Field-Effect Transistors. *Electron Device Letters, IEEE*, 34(6): 813–815, 2013.

[51] J. Kolhatkar, L. Vandamme, C. Salm, and H. Wallinga. Separation of random telegraph signals from 1/f noise in MOSFETs under constant and switched bias conditions. *33rd Conference on European Solid-State Device Research (ESSDERC) 2003*, page 549–552, 2003.

[52] E. Koren, N. Berkovitch, and Y. Rosenwaks. Measurement of active dopant distribution and diffusion in individual silicon nanowires. *Nano letters*, 10(4):1163–7, Apr 2010.

[53] S. Koswatta and M. Lundstrom. Performance comparison between pin tunneling transistors and conventional MOSFETs. *Transactions on Electron Devices, IEEE*, 56(3): 456–465, 2009.

[54] S. O. Koswatta, S. J. Koester, and W. Haensch. On the Possibility of Obtaining MOSFET-Like Performance and Sub-60-mV/dec Swing in 1-D Broken-Gap Tunnel Transistors. *IEEE Transactions on Electron Devices*, 57(12):3222–3230, 2010.

[55] S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov. Influence of phonon scattering on the performance of p-i-n band-to-band tunneling transistors. *Applied Physics Letters*, 92(4):043125, 2008.

[56] K. Koyama, M. Hirai, T. Tatsumi, and H. Hirayama. Etching characteristecs of SiGe alloy in ammoniac wet cleaning. *Applied Physics Letters*, 57(November):2202–2204, 1990.

[57] M. Koyama, M. Casse, and R. Coquand. Study of carrier transport in strained and unstrained SOI tri-gate and omega-gate Si-nanowire MOSFETs. *Proceedings of the European Solid-State Device Research Conference (ESSDERC), 2012*, page 73–76, 2012.

[58] S. T. Le, P. Jannaty, X. Luo, A. Zaslavsky, D. E. Perea, S. a. Dayeh, and S. T. Picraux. Axial SiGe Heteronanowire Tunneling Field-Effect Transistors. *Nano letters*, 12:5850–5855, Oct 2012.

[59] C.-W. Lee, S.-R.-N. Yun, C.-G. Yu, J.-T. Park, and J.-P. Colinge. Device design guidelines for nano-scale MuGFETs. *Solid-State Electronics*, 51(3):505–510, Mar 2007.

[60] M. L. Lee, E. a. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld. Strained Si, SiGe, and Ge channels for high-mobility metal-oxide-semiconductor field-effect transistors. *Journal of Applied Physics*, 97(1):011101, 2005.

[61] W. Li, Q. Zhang, O. A. Kirillov, R. Bijesh, Y. Liang, D. Mohata, B. Tian, X. Liang, S. Datta, and C. A. Richter. Complete Band Alignment Determination of InAs-GaSb Broken-Gap Tunneling Field-effect Transistor Hetero-Junction. *Device Research Conference (DRC) 2013*, page 1–2, 2013.

[62] J. Lim and S. Thompson. Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs. *Electron Device Letters,*, 25(11):731–733, 2004.

[63] M. Luisier and G. Klimeck. Simulation of nanowire tunneling transistors: From the Wentzel–Kramers–Brillouin approximation to full-band phonon-assisted tunneling. *Journal of Applied Physics*, 107(8):084507, 2010.

[64] G. Lujan, S. Kubicek, S. De Gendt, M. Heyns, W. Magnus, and K. De Meyer. Mobility degradation in high-k transistors: the role of the charge scattering. *33rd Conference on European Solid-State Device Research (ESSDERC) 2003*, page 399–402, 2003.

[65] S. Machlup. Noise in Semiconductors: Spectrum of a Two-Parameter Random Signal. *Journal of Applied Physics*, 25(3):341, 1954.

[66] Y. Maneglia, D. Bauza, and T. Ouisse. Extraction of the slow oxide trap density in MOS transistors using the charge pumping method. *Semiconductor Conference (CAS), 1995*, pages 155–156, 1995.

[67] G. E. McGuire. *Semiconductor Materials and Process Technology Handbook*. Noyes Publication, 1988. 501–504 pp.

[68] L. D. Michielis, L. Lattanzio, and A. Ionescu. Understanding the superlinear onset of tunnel-FET output characteristic. *IEEE Electron Device Letters*, 33(11):1523–1525, 2012.

[69] R. A. Minamisawa, S. Habicht, D. Buca, R. Carius, S. Trellenkamp, K. K. Bourdelle, and S. Mantl. Elastic strain and dopant activation in ion implanted strained Si nanowires. *Journal of Applied Physics*, 108(12):124908, 2010.

[70] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, and R. Chau. A 45nm logic technology with high-k+ metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100% Pb-free packaging. *IEDM Meeting 2007*, page 247–250, 2007.

[71] D. K. Mohata, R. Bijesh, Y. Zhu, M. K. Hudait, R. Southwick, Z. Chbili, D. Gundlach, J. Suehle, J. M. Fastenau, and D. Loubychev. Demonstration of improved heteroepitaxy, scaled gate stack and reduced interface states enabling heterojunction tunnel FETs with high drive current and high on-off ratio. *2012 Symposium on VLSI Technology (VLSIT)*, page 53–54, Jun 2012.

[72] S. Mookerjea and S. Datta. Band-gap engineered hot carrier tunnel transistors. *Device Research Conference (DRC) 2009*, pages 8–9, 2009.

[73] S. Mookerjea, D. Mohata, T. Mayer, and S. Datta. Temperature-Dependent I–V Characteristics of a Vertical In0.53Ga0.47As Tunnel-FET. *IEEE Electron Device Letters*, 31(6):564–566, 2010.

[74] Y. Morita, T. Mori, S. Migita, W. Mizubayashi, A. Tanabe, K. Fukuda, M. Masahara, and H. Ota. First Demonstration of Drain Current Enhancement in SOI Tunnel FET with Vertical-Tunnel-Multiplication. *Proceedings of SOI Conference 2012*, 2012.

[75] K. Moselund, M. Bjork, and H. Schmid. Silicon Nanowire Tunnel FETs: Low-Temperature Operation and Influence of High-k Gate Dielectric. *IEEE Transactions on Electron Devices*, 58(9):2911–2916, 2011.

[76] K. E. Moselund, H. Schmid, C. Bessire, M. T. Björk, H. Ghoneim, S. Member, H. Riel, and S. Member. InAs – Si Nanowire Heterojunction Tunnel FETs. *Electron Device Letters, IEEE*, 33(10):1453–1455, 2012.

[77] O. M. Nayfeh, C. N. Chleirigh, J. Hennessy, L. Gomez, J. L. Hoyt, D. A. Antoniadis, and A. Heterojunction. Design of Tunneling Field-Effect Transistors Using Staggered Heterojunctions. *IEEE Electron Device Letters*, 29(9):2008–2011, 2008.

[78] A. Nichau. *Characterization, integration and reliability of HfO_2 and $LaLuO_3$ high-κ/metal gate stacks for CMOS application.* PhD thesis, RWTH Aachen, 2013.

[79] Y. Ohkura. Quantum effects in Si n-MOS inversion layer at high substrate concentration. *Solid-State Electronics*, 33(12):1581–1585, Dec 1990.

[80] D. J. Paul. Si/SiGe heterostructures: from material and physics to devices and circuits. *Semiconductor Science and Technology*, 19(10):R75–R108, Oct 2004.

[81] D. Pogany, C. Zeiner, S. Bychikhin, T. Burchhart, A. Lugstein, and L. K. J. Vandamme. RTS and 1/f noise in Ge nanowire transistors. *21st International Conference on Noise and Fluctuations*, page 368–371, Jun 2011.

[82] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic. Digital integrated circuits : a design perspective. In *Digital Integrated Circuits (2nd Edition)*, pages 144–192. Upper Saddle River, Prentice Hall, 2008, 2008.

[83] S. Richter, C. Sandow, A. Nichau, S. Trellenkamp, M. Schmidt, R. Luptak, K. K. Bourdelle, Q. T. Zhao, and S. Mantl. Ω-Gated Silicon and Strained Silicon Nanowire Array Tunneling FETs. *IEEE Electron Device Letters*, 33(11):1535–1537, 2012.

[84] S. Richter, S. Trellenkamp, M. Schmidt, A. Schäfer, K. K. Bourdelle, Q. T. Zhao, and S. Mantl. Strained silicon nanowire array MOSFETs with high-k/metal gate stack. *Proceedings of 13th Ultimate Integration on Silicon (ULIS) Conference 2012*, 1:53–56, 2012.

[85] R. Rofan and C. Hu. Stress-induced oxide leakage. *IEEE Electron Device Letters*, 12 (11):632–634, Nov 1991.

[86] R. Rooyackers, A. Vandooren, A. Verhulst, K. Walke, A. Devriendt, S. Locorotondo, M. Demand, G. Bryce, R. Loo, A. Hikavyy, T. Vandeweyer, C. Huyghebaert, N. Collaert, and A. Thean. A New Complementary Hetero-Junction Vertical Tunnel-FET Integration Scheme. *IEDM 2013*, 2013.

[87] C. Sah and W. Shockley. Electron-Hole Recombination Statistics in Semiconductors through Flaws with Many Charge Conditions. *Physical Review*, 109(4):1103–1115, 1958.

[88] C. Sandow, J. Knoch, C. Urban, Q.-T. Zhao, and S. Mantl. Impact of electrostatics and doping concentration on the performance of silicon tunnel field-effect transistors. *Solid-State Electronics*, 53(10):1126–1129, Oct 2009.

[89] C. P. Sandow. *Modeling, Fabrication and Characterization of Silicon Tunnel Field-Effect Transistors*. PhD thesis, RWTH Aachen, 2010.

[90] A. Schenk. Rigorous Theory and Simplified Model of the Band-to-Band Tunneling in Silicon. *Solid-State Electronics*, 36(1):19–34, 1993.

[91] A. C. Seabaugh and Q. Zhang. Low-Voltage Tunnel Transistors for Beyond CMOS Logic. *Proceedings of the IEEE*, 98(12):2095–2110, Dec 2010.

[92] S. Selberherr. *Analysis and Simulation of Semiconductor Devices*. Springer-Verlag, 1984.

[93] C. Shen, J. Lin, E. Toh, K. Changt, P. Bait, C. Heng, G. S. Samudra, and Y. Yeo. On the Performance Limit of Impact-Ionization Transistors. *Digest. International Electron Devices Meeting (IEDM) 2007*, page 117–120, 2007.

[94] E. Simoen, A. Mercha, C. Claeys, and E. Young. Correlation between the 1/f noise parameters and the effective low-field mobility in HfO2 gate dielectric n-channel metal–oxide–semiconductor field-effect transistors. *Applied Physics Letters*, 85(6):1057, 2004.

[95] J. T. Smith, C. Sandow, S. Das, R. A. Minamisawa, S. Mantl, and J. Appenzeller. Silicon Nanowire Tunneling Field-Effect Transistor Arrays: Improving Subthreshold Performance Using Excimer Laser Annealing. *IEEE Transactions on Electron Devices*, 58(7):1822–1829, Jul 2011.

[96] F. Stern. Quantum properties of surface space-charge layers. *C R C Critical Reviews in Solid State Sciences*, 4(1-4):499–514, Dec 1973.

[97] M. Surdin. Fluctuations de courant thermionique et le Flicker effect. *Journal de Physique et le Radium*, 10(4):188–189, Apr 1939.

[98] S. M. Sze. *Physics of Semiconductor Devices (3rd edition)*. Hoboken, NJ: Wiley, 3rd edition, 2007. 227–228 pp.

[99] E. Takeda, H. Matsuoka, Y. Igura, and S. Asai. A band to band tunneling MOS device (B2T-MOSFET) - A kind of "Si quantum device". *Technical Digest. International Electron Devices Meeting (IEDM) 1988*, page 402 – 405, 1988.

[100] M. Toledano-Luque, R. Degraeve, M. B. Zahid, L. Pantisano, E. S. Andrés, G. Groeseneken, and S. D. Gendt. New developments in charge pumping measurements on thin stacked dielectrics. *IEEE Transactions on Electron Devices*, 55(11):3184–3191, 2008.

[101] L. K. J. Vandamme and F. N. Hooge. What Do We Certainly Know About 1/f Noise in MOSTs? *IEEE Transactions on Electron Devices*, 55(11):3070–3085, 2008.

[102] W. Vandenberghe, A. Verhulst, G. Groeseneken, and B. Sor. Analytical model for point and line tunneling in a tunnel field-effect transistor. *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD) 2008*, page 137–140, 2008.

[103] A. Verhulst, W. Vandenberghe, K. Maex, S. De Gendt, M. Heyns, and G. Groeseneken. Complementary silicon-based heterostructure tunnel-FETs with high tunnel rates. *IEEE Electron Device Letters*, 29(12):1398–1401, 2008.

[104] M. Wada, H. Takahashi, J. Snow, R. Vos, T. Conard, P. W. Mertens, and H. Shirakawa. Cleaning and Surface Preparation for SiGe and Ge Channel Device. *Solid State Phenomena*, 187:19–22, Apr 2012.

[105] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu. Low-frequency noise behavior of tunneling field effect transistors. *Applied Physics Letters*, 97(24):243503, 2010.

[106] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu. Tunneling FETs on SOI: Suppression of ambipolar leakage, low-frequency noise behavior, and modeling. *Solid-State Electronics*, 65-66:226–233, Nov 2011.

[107] P. Wang. *Complementary tunneling-FETs (CTFET) in CMOS technology*. PhD thesis, Technische Universität München, 2003.

[108] O. Weber, J.-F. Damlencourt, F. Andrieu, F. Ducroquet, T. Ernst, J.-M. Hartmann, A.-M. Papon, O. Renault, B. Guillaumot, and S. Deleonibus. Fabrication and mobility characteristics of SiGe surface channel pMOSFETs with a HfO/sub 2//TiN gate stack. *IEEE Transactions on Electron Devices*, 53(3):449–456, Mar 2006.

[109] G. D. Wilk, R. M. Wallace, and J. M. Anthony. High-κ gate dielectrics: Current status and materials properties considerations. *Journal of Applied Physics*, 89(10):5243, 2001.

[110] www.ericsson.com. *Ericsson Mobility Report - November 2013*.

[111] Y. Yuzhelevski, M. Yuzhelevski, and G. Jung. Random telegraph noise analysis in time domain. *Review of Scientific Instruments*, 71(4):1681, 2000.

[112] Q. T. Zhao, W. J. Yu, B. Zhang, M. Schmidt, S. Richter, D. Buca, R. Luptak, A. Fox, K. K. Bourdelle, and S. Mantl. Tunneling Field-Effect Transistor with a Strained Si Channel and a SiGe Source. *Proceedings of ESSDERC 2011*, pages 3–6, 2011.

List of Publications

Journal Papers

- S. Richter, S. Trellenkamp, A. Schäfer, J. M. Hartmann, K. K. Bourdelle, Q. T. Zhao, and S. Mantl, "Improved Tunnel-FET Inverter Performance with SiGe/Si Heterostructure Nanowire TFETs by Reduction of Ambipolarity," Solid-State Electronics (accepted for publication), 2014.

- S. Richter, S. Blaeser, L. Knoll, S. Trellenkamp, A. Fox, A. Schäfer, J. M. Hartmann, Q. T. Zhao, and S. Mantl, "Silicon-Germanium Nanowire Tunnel-FETs with Homo- and Heterostructure Tunnel Junctions," Solid-State Electronics, vol. 98, pp. 75-80, 2014.

- L. Knoll, S. Richter, A. Nichau, S. Trellenkamp, A. Schäfer, S. Wirths, S. Blaeser, D. Buca, K. K. Bourdelle, Q.-T. Zhao, S. Mantl, "Strained silicon based complementary tunnel-FETs: Steep slope switches for energy efficient electronics," Solid-State Electronics, vol. 98, pp. 32-37, 2014.

- L. Knoll, S. Richter, A. Nichau, S. Trellenkamp, A. Schäfer, K. K. Bourdelle, J. M. Hartmann, Q. T. Zhao, and S. Mantl, "Strained Si and SiGe Tunnel-FETs and complementary Tunnel-FET inverters with minimum gate lengths of 50 nm," Solid-State Electronics, vol. 97, pp. 76-81, 2014.

- L. Knoll, Q. Zhao, A. Nichau, S. Trellenkamp, S. Richter, A. Schäfer, D. Esseni, L. Selmi, K. K. Bourdelle, and S. Mantl, "Inverters With Strained Si Nanowire Complementary Tunnel Field-Effect Transistors," IEEE Electron Device Letters, vol. 34, no. 6, pp. 813-815, 2013.

- M. Schmidt, R. A. Minamisawa, S. Richter, A. Scha?fer, D. Buca, J. M. Hartmann, Q.-T. Zhao, and S. Mantl, "Unipolar behavior of asymmetrically doped strained Si0.5Ge0.5 tunneling field-effect transistors," Applied Physics Letters, vol. 101, no. 12, p. 123501, 2012.

- S. Richter, C. Sandow, A. Nichau, S. Trellenkamp, M. Schmidt, R. Luptak, K. K. Bourdelle, Q. T. Zhao, and S. Mantl, "Ω-Gated Silicon and Strained Silicon Nanowire Array Tunneling FETs," IEEE Electron Device Letters, vol. 33, no. 11, pp. 1535-1537, 2012.

- D. Grützmacher, Q. T. Zhao, S. Richter, L. Knoll, J. Moers, J. Gerharz, G. Mussler, D. Buca, and S. Mantl, "Strained Nanoscaled Devices," ECS Transactions, vol. 50, no. 9, pp. 727-736, 2012.

- Q. T. Zhao, W. J. Yu, B. Zhang, M. Schmidt, S. Richter, D. Buca, J.-M. Hartmann, R. Luptak, A. Fox, K. K. Bourdelle, and S. Mantl, "Tunneling field-effect transistor with a strained Si channel and a Si0.5Ge0.5 source," Solid-State Electronics, vol. 74, pp. 97-101, Aug. 2012.

- M. Schmidt, R. A. Minamisawa, S. Richter, R. Luptak, J.-M. Hartmann, D. Buca, Q. T. Zhao, and S. Mantl, "Impact of strain and Ge concentration on the performance of planar SiGe band-to-band-tunneling transistors," Solid-State Electronics, vol. 71, pp. 42-47, May 2012.

Conference Contributions

- C. Schulte-Braucks, S. Richter, L. Knoll, L. Selmi, Q.-T. Zhao, and S. Mantl, "Experimental Demonstration of Improved Analog Device Performance in GAA-NW-TFETs," ESSDERC, 2014.

- S. Richter, C. Schulte-Braucks, L. Knoll, G. V. Luong, A. Schäfer, S. Trellenkamp, Q.-T. Zhao, and S. Mantl, "Experimental Demonstration of Inverter and NAND Operation in p-TFET Logic at Ultra-low Supply Voltages down to VDD = 0.15 V," Device Research Conference (DRC), 2014.

- S. Richter, S. Trellenkamp, A. Schäfer, J. M. Hartmann, K. K. Bourdelle, Q. T. Zhao, and S. Mantl, "Tunnel-FET Inverters for Ultra-low Power Logic with Supply Voltage down to VDD = 0.2 V," ULIS Conference 2014, pp. 13-16, 2014.

- L. Knoll, Q. T. Zhao, A. Nichau, S. Richter, G. V. Luong, S. Trellenkamp, A. Schäfer, L. Selmi, K. K. Bourdelle, and S. Mantl, "Demonstration of Improved Transient Response of Inverters with Steep Slope Strained Si NW TFETs by Reduction of TAT with Pulsed I-V and NW Scaling," International Electron Device Meeting (IEDM) 2013.

- S. Richter, S. Vitusevich, S. Pud, J. Li, L. Knoll, S. Trellenkamp, A. Schäfer, S. Lenk, Q. T. Zhao, A. Offenhäusser, and S. Mantl, "Low Frequency Noise in Strained Silicon Nanowire Array MOSFETs and Tunnel-FETs," European Solid State Device Research Conference (ESSDERC) 2013.

- S. Mantl, L. Knoll, S. Richter, M. Schmidt, S. Wirths, A. Nichau, A. Schäfer, S. Blaeser, S. Trellenkamp, J.-M. Hartmann, K. K. Bourdelle, D. Buca, and Q.-T. Zhao,

"Si compatible Tunneling Field Effect Transistors and Inverters," Device Research Conference (DRC), 2013.

- Q.-T. Zhao, L. Knoll, S. Richter, M. Schmidt, S. Wirths, A. Nichau, A. Schäfer, S. Blaeser, S. Trellenkamp, J.-M. Hartmann, K. K. Bourdelle, D. Buca, and S. Mantl, "Strained Si nanowire TFETs and Inverters," Third Berkeley Symposium on Energy Efficient Electronic Systems, 2013.

- S. Richter, S. Blaeser, L. Knoll, S. Trellenkamp, J. M. Hartmann, A. Schafer, Q. T. Zhao, and S. Mantl, "SiGe on SOl Nanowire Array TFETs with Homo- and Heterostructure Tunnel Junctions," ULIS Conference 2013, pp. 25-28, 2013.

- L. Knoll, S. Richter, A. Nichau, A. Schafer, K. K. Bourdelle, Q. T. Zhao, S. Mantl, P. Grunberg, I. P.- Iit, and F. Julich, "Gate-all-around Si nanowire array tunnelling FETs with high on-current of 75 μA/μm at VDD=1.1 V," ULIS Conference 2013, pp. 97-100, 2013.

- S. Mantl, L. Knoll, M. Schmidt, S. Richter, N. Alexander, S. Trellenkamp, A. Schäfer, S. Wirths, S. Blaeser, D. Buca, and Q.-T. Zhao, "Si based tunnel field effect transistors: recent achievements," ULIS Conference 2013, pp. 15-20, 2013.

- S. Richter, L. Knoll, A. Schäfer, S. Trellenkamp, J. M. Hartmann, Q. T. Zhao, and S. Mantl, "Strained SiGe on Si Nanowire Array TFETs," EUROSOI 2013, pp. 2-3, 2013.

- L. Knoll, S. Richter, A. Nichau, S. Trellenkamp, A. Schäfer, K. K. Bourdelle, Q. T. Zhao, and S. Mantl, "Complementary-Tunnel FET Inverters with ultrathin Strained Si," EUROSOI 2013, pp. 8-9, 2013.

- S. Richter, L. Knoll, M. Schmidt, A. Nichau, A. Schäfer, S. Trellenkamp, K. K. Bourdelle, J. M. Hartmann, D. Buca, Q. T. Zhao, and S. Mantl, "Strained Si and SiGe Nanowire TFETs," STEEPER Workshop, ESSDERC 2012.

- D. Grützmacher, Q. T. Zhao, S. Richter, L. Knoll, J. Moers, J. Gerharz, G. Mussler, D. Buca, and S. Mantl, "Strained Nanoscaled Devices," PRiME 2012, p. 100, 2012.

- Q. T. Zhao, L. Knoll, S. Richter, S. Trellenkamp, A. Schäfer, K. K. Bourdelle, and S. Mantl, "Si Nanowire Tunnel FETs with Epitaxial NiSi2 Source/Drain and Dopant Segregation," IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2012.

- L. Knoll, Q. Zhao, S. Richter, S. Trellenkampl, A. Schafer, K. K. Bourdelle, and S. Mantl, "Si Nanowire tunnel FETs with epitaxial NiSi 2 source/drain and dopant segregation," IEEE 11th International Conference on Solid-State and Integrated Circuit Technology (ICSICT), pp. 2-5, 2012.

- S. Richter, S. Trellenkamp, M. Schmidt, A. Schäfer, K. K. Bourdelle, Q. T. Zhao, and S. Mantl, "Strained silicon nanowire array MOSFETs with high-k/metal gate stack," Proceedings of 13th Ultimate Integration on Silicon (ULIS) Conference, pp. 53-56, 2012.

- M. Schmidt, L. Knoll, S. Richter, A. Schäfer, J. M. Hartmann, Q. T. Zhao, and S. Mantl, "Si/SiGe hetero-structure tunneling field effect transistors with in-situ doped SiGe source," 13th ULIS Conference, pp. 191-194, 2012.

- Q. T. Zhao, W. J. Yu, B. Zhang, M. Schmidt, S. Richter, D. Buca, R. Luptak, A. Fox, K. K. Bourdelle, and S. Mantl, "Tunneling Field-Effect Transistor with a Strained Si Channel and a Si0.5Ge0.5 Source," ESSDERC 2011, vol. 41, pp. 251-254.

- M. Schmidt, R. A. Minamisawa, S. Richter, J.-M. Hartmann, R. Luptak, A. Tiedemann, D. Buca, Q. T. Zhao, and S. Mantl, "Impact of strain and Ge concentration on the performance of planar SiGe band-to-band-tunneling transistors," ULIS 2011 Ultimate Integration on Silicon, 2011.

- Q. T. Zhao, C. Sandow, M. Schmidt, S. Richter, and S. Mantl, "Planar and Nanowire Si-TFETs," China Semiconductor Technology International Conference (CSTIC), Shanghai, 2011.

- S. Richter, M. Schmidt, S. Habicht, R. Luptak, and S. Trellenkamp, "Nanowire Tunnel Field Effect Transistor (TFET)," JARA-FIT Science Days 2011.

- C. Sandow, C. Urban, M. Schmidt, S. Richter, Q. T. Zhao, and S. Mantl, "Silicon and Strained Silicon Nanowire Array Tunneling FETs," Nanoelectronic Days 2010.

Curriculum Vitae

Personal Information

Name	Simon Richter
Date of birth	May 18th, 1983
Place of birth	Dinslaken, Germany
Nationality	German

Education and professional experience

2/2014 – today	Forschungszentrum Jülich, Peter Grünberg Institute 9, *PostDoc position*
6/2010 – 1/2014	Forschungszentrum Jülich, Peter Grünberg Institute 9, *PhD student in the group of Prof. Siegfried Mantl*
9/2006 – 6/2007	Chalmers University of Technology, Sweden, *Studies on Nanoscale Science and Technology*
2003 – 2009	RWTH Aachen University, Germany, *Diploma in Physics*

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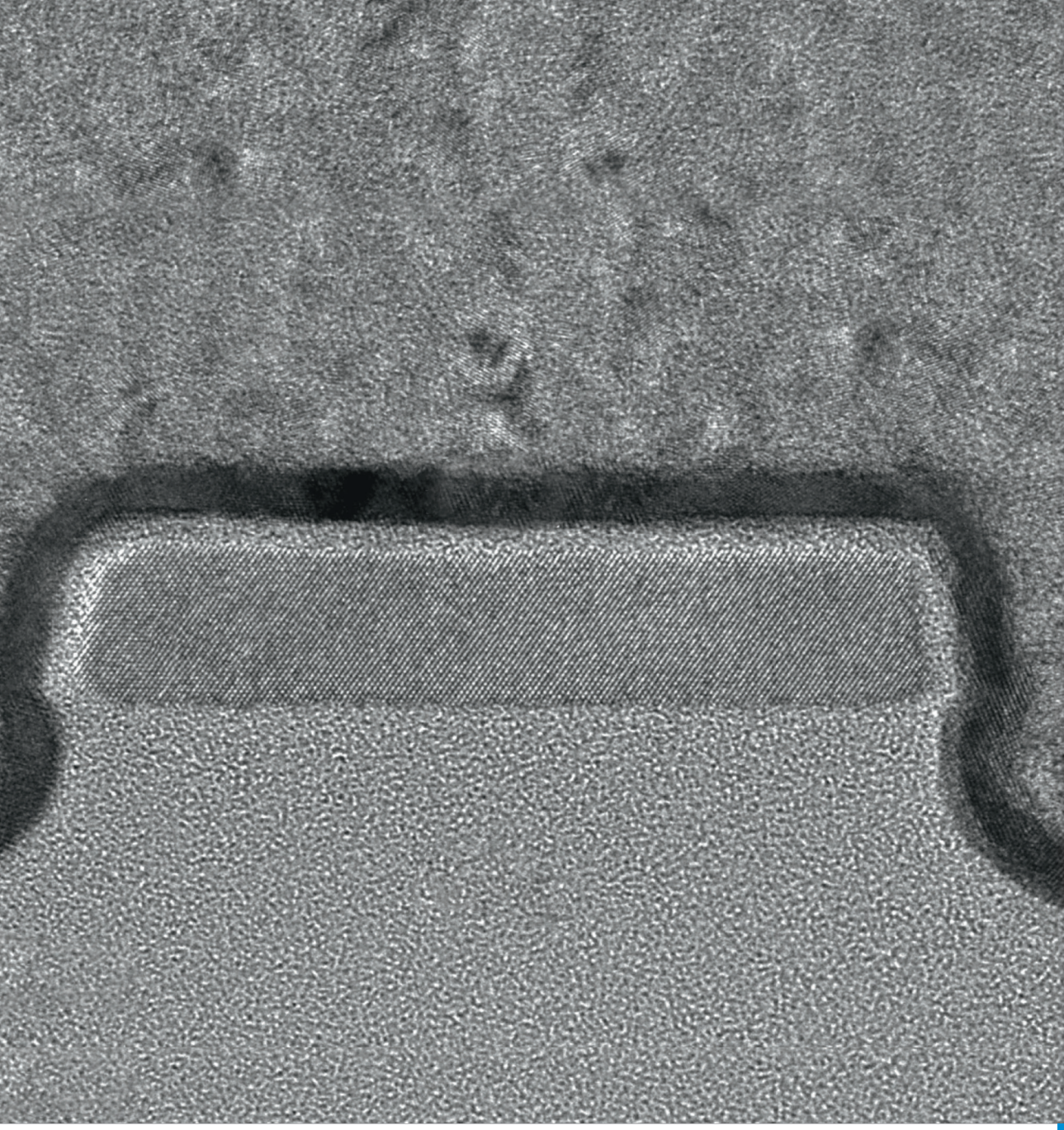

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