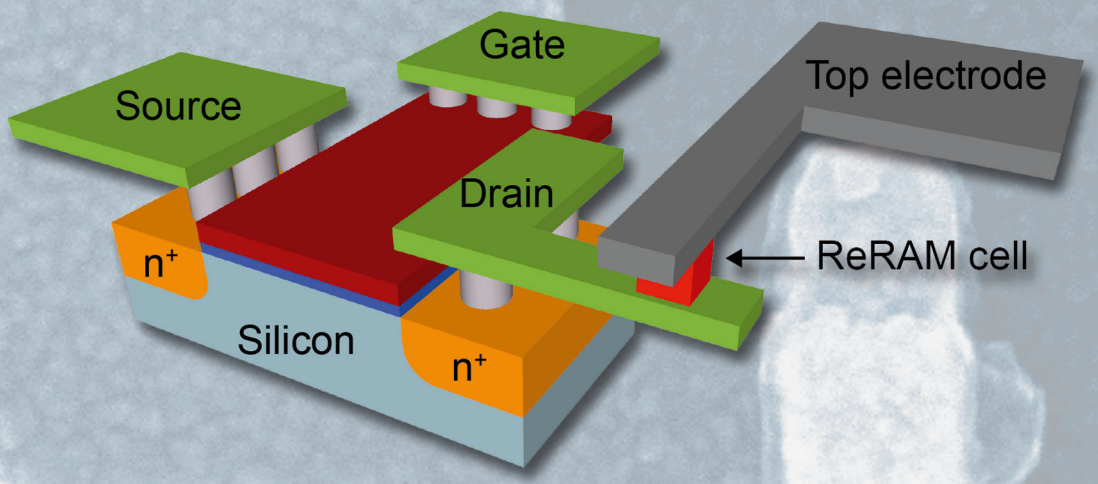

Integration of Redox-Based Resistive Switching Memory Devices

Florian Lentz

JÜLICH
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Schriften des Forschungszentrums Jülich
Reihe Information / Information Band / Volume 41

Forschungszentrum Jülich GmbH
Peter Grünberg Institute (PGI)
Electronic Materials (PGI-7)

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Schriften des Forschungszentrums Jülich
Reihe Information / Information Band / Volume 41

ISSN 1866-1777 ISBN 978-3-95806-019-7

Bibliographic information published by the Deutsche Nationalbibliothek.
The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data are available in the Internet at http://dnb.d-nb.de.

Publisher and Distributor:	Forschungszentrum Jülich GmbH Zentralbibliothek 52425 Jülich Tel: +49 2461 61-5368 Fax: +49 2461 61-6103 Email: zb-publikation@fz-juelich.de www.fz-juelich.de/zb
Cover Design:	Grafische Medien, Forschungszentrum Jülich GmbH
Printer:	Grafische Medien, Forschungszentrum Jülich GmbH
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Schriften des Forschungszentrums Jülich
Reihe Information / Information, Band / Volume 41

D 82 (Diss., RWTH Aachen University, 2014)

ISSN 1866-1777
ISBN 978-3-95806-019-7

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Abstract

The steadily growing market for consumer electronics and the rapid proliferation of mobile devices such as tablet computers, MP3 players and smart phones make high demands for the nonvolatile memory. Present FLASH memory technology approaches to the end due to physical scalability limits. Therefore, an alternative technology must be developed. For memory technology, not only the storage density and cost are important factors but the power consumption and the writing/reading speed must also be taken in account. Redox-based resistive memory (ReRAM) offers a potential alternative to the FLASH technology and presently is in the focus of research activities. The operating principle of the ReRAM is based on the non-volatile reversible change in resistance by electrical stimuli in a simple metal-insulator-metal (MIM) device architecture. This simple structure enables the integration of ReRAM in passive crossbar arrays, in which each crosspoint consumes only $4F^2$ (F- feature size) device area. This leads to an ultra-high storage density at reduced cost.
Research on the ReRAM memory elements requires a technology platform that ensures a cost-effective fabrication of the crossbar devices with nanometer feature size. In this thesis, the fabrication processes have been developed based on the nanoimprint lithography, which facilitates both the high resolution (<50nm) and the high throughput at low cost. The stamp for the UV-nanoimprinting is developed with plasma etching and electron-beam lithography. This process facilitates the fabrication of the ReRAM devices sizes ranging from 40x40 nm^2 to 100x100 nm^2. The fabricated nano-crosspoint ReRAM of different switching layer thickness and different device areas are electrically characterized. In order to toggle the resistance state in the ReRAM device, an electroforming step is generally required. In this work, a systematic analysis of the electroforming process is carried out on TiO_2 and WO_3-based ReRAM cells and the respective switching characteristics are investigated. The switching mechanism is explained by the filamentary conduction model. The forming voltage decreases with decreasing oxide layer thickness whereas it increases for the smaller device size. Due to overshoot phenomena during the electroforming process, these devices show a significant increased switching current, lower non-linearity, and lower endurance. The ReRAM device performance is improved by integration in the backend of a 65nm CMOS process. In the integrated 1T-1R stack, the electroforming is performed by controlling the current flow with the gate electrode. By employing this approach, the switching current in the ReRAM devices is reduced to 1 μA. In order to lower the sneak path current in the passive crossbar arrays, a high degree of nonlinearity is required. This nonlinearity parameter has been investigated with 100 ns transient pulses in the nano-crossbar devices and in the 1T-1R structures. This parameter depends on the switching current and switching material properties. The lower switching current in the TiO_2 ReRAM leads to the higher nonlinearity.
Furthermore, the ReRAM nanodevices inherently exhibit open clamp voltage in the switching characteristics. This phenomenon is explained by the electromotive force (EMF). The amplitude of the generated EMF voltage depends on the nature of the switching materials and can be several hundred mV. This degrades the conducting filament and thereby limits the ON state retention properties of the ReRAM devices. Additionally, the non-zero crossing of the I-V characteristics, caused by the EMF voltage demands the refinement of the memristor theory.

Kurzfassung

Der stetig wachsende Markt für Unterhaltungselektronik und die rasche Verbreitung von mobilen Geräten wie Tablet-Computer, MP3-Player und Smartphones stellen hohe Anforderungen an den verwendeten nichtflüchtigen Speicher. Aufgrund physikalischer Beschränkungen der aktuellen FLASH-Speichertechnologie, nähert sich die Skalierbarkeit dem Ende und daher muss eine alternative Technologie entwickelt werden. Für die Speichertechnologie spielt dabei nicht nur die Speicherdichte und die damit verbundenen Kosten eine wichtige Rolle, sondern vor allem auch die Leistungsaufnahme sowie die Schreib- und Lesegeschwindigkeit sind zu berücksichtigen. Redox-basierte Resistive Speicher (ReRAM) bieten eine mögliche Alternative zur FLASH-Technologie und stehen derzeit im Fokus der Forschungsaktivitäten. Das Funktionsprinzip des ReRAM beruht auf der nichtflüchtigen reversiblen Veränderung des Widerstandes einfacher Metall-Isolator-Metall Bauelemente durch elektrische Signale. Dieser einfache Aufbau ermöglicht den Einsatz in passiven Crossbar-Arrays, in denen jeder Kreuzungspunkt nur eine Fläche von $4F^2$ (F-Strukturgröße) benötigt. Dies führt zu einer extrem hohen Speicherdichte bei reduzierten Kosten.
Die Erforschung von ReRAM Speicherelementen erfordert eine Technologie Plattform, welche eine kosteneffiziente Herstellung von Crossbar-Strukturen im nm-Bereich gewährleistet. In dieser Arbeit wurden Herstellungsprozesse basierend auf der Nanoimprint Lithographie entwickelt, welche sowohl die erforderlichen Auflösungen ($<$50 nm) als auch einen hohen Durchsatz bei geringen Kosten ermöglichen. Diese Verfahren ermöglichen die Untersuchung von ReRAM Elementen mit deutlich reduzierten Strukturgrößen von 40x40nm^2. Sowohl der Einfluss der Oxidschichtdicke als auch der lateralen Ausmaße der Speicherelemente auf die elektrischen Eigenschaften wurden untersucht. Der im Allgemeinen benötigte Elektroformierschritt und die damit einhergehenden Schalteigenschaften wurden in dieser Arbeit systematisch für TiO_2 und WO_3 basierte ReRAM Zellen analysiert. Die Formierspannung skaliert mit der Oxidschichtdicke und erhöht sich bei reduzierten Zellgrößen. Das Überschwingen der Schaltströme während des Elektroformierschritts von passiven Speicherelementen führt zu erhöhten Schaltströmen, niedrigen Nichtlinearitäten und geringen Lebensdauern. Die Eigenschaften des ReRAM wurden durch Integration in das Backend eines 65-nm-CMOS-Prozess verbessert. In den integrierten 1T-1R Elementen wird der Formierschritt durch die Regelung des Stromflusses mittels angelegter Gate-Spannungen gesteuert wodurch die Schaltströme des ReRAM auf 1 µA reduzieren lassen. Um parasitäre Ströme in passiven Crossbar-Arrays zu reduzieren ist ein hoher Grad an Nichtlinearität erforderlich. Dieser Parameter wurde mit 100 ns Spannungspulsen sowohl in Nanocrossbar als auch in 1T-1R Speicherelementen untersucht. Die Nichtlinearität hängt von den Schaltströmen und Materialeigenschaften des Oxids ab. Reduzierte Schaltströme in TiO_2 ReRAMs führen zu höheren Nichtlinearitäten.
Darüber hinaus weisen ReRAM Elemente von Natur aus offenen Klemmspannungen auf. Dieses Phänomen wird durch das Vorhandensein der elektromotorischen Kraft (EMK) erklärt. Die Amplitude der erzeugten EMK-Spannung hängt von den involvierten Materialien ab und kann mehrere hundert mV betragen. Dies degradiert das leitende Filament und begrenzt die Stabilität der eingeschriebenen Zustände der ReRAM Elemente. Die durch die EMK hervorgerufene Verschiebung der Hysteresekurven erfordert eine Anpassung der Memristor Theorie.

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Chapter 1

Introduction

Non-volatile memory plays a very important role in data storage because of the ubiquitous presence of portable devices such as digital still cameras, MP3 players, tablet computers and especially smartphones. Non-volatile memory (NVM) functionality refers to the ability of an electronic system to retain the stored information even when the power of the system is switched off.
In the last two decades, FLASH memory has dominated the NVM market due to merits such as ultra-low cost and excellent reliability. The memory density of NAND FLASH has been continually increased over the recent years. However, the scaling of conventional floating-gate FLASH memory is limited by the thickness of the tunneling oxide and the channel length. The further scaling of FLASH memory technology is expected to reach its physical limit in the near future. Thus, there is an increasing demand for new NVM technologies to overcome the increasing challenges like the reliability, data retention issues and the loss of multi-level capability that FLASH faces.
Recently, Redox-based Resistive Random Access Memory (ReRAM) attracts more and more attention. It is a potential candidate for next generation NVM due to its superior performance. The resistive switching effect describes the reversible change of the resistance of simple metal-insulator-metal (MIM) devices by voltage stimuli. MIM structures based on binary oxides like TiO_2 or WO_3 exhibit excellent properties in terms of scalability, data operation speed and retention [1–3]. These properties open a tremendous potential to become a so-called "universal memory". The universal memory has to combine the fast data operation comparable to DRAM while storing the information for

years like current FLASH technology. In addition, the ReRAM has attracted attention due to its memristive behavior which makes it a candidate to mimic the functionality of neurons in the human brain [4, 5].

1.1 Scope of this work

The focus of this work is the integration and electrical characterization of redox-based resistive switching memory elements. Two resistive switching materials are mainly investigated: The polycrystalline TiO_2 and the amorphous WO_3. This thesis is divided into seven chapters. In the following chapter, an overview on the redox-based resistive switching, the utilized materials and the challenges regarding the integration into passive crossbar-arrays is given.
The integration of ReRAM into passive and active nano-crossbars is a major part of this work. The required patterning techniques, the physical characterization methods employed and also the measurement technology for electrical characterization are introduced in chapter 3. The development of the patterning processes to structure passive crossbars by the combination of nanoimprint and electron beam lithography will also be explained in this chapter. The chapter is concluded with the development of integrated memory devices with MOSFET selectors.
In chapter 4, it will be demonstrated that the MIM structures exhibit an electromotive force (EMF) and therefore can be considered as nanobatteries. The analysis of the EMF in various memory elements is carried out in this chapter and its impact on ReRAM integration will be discussed.
The electrical characteristics of the fabricated passive nano-crossbar devices with respect to the quasi-static electroforming, resistive switching and the AC nonlinearity will be discussed in chapter 5.
This is followed by the investigation of the influence of the current limitation by the integrated MOS transistors on the electrical characteristics of the resistive switching elements in chapter 6.
Finally, chapter 7 gives the conclusion of the performed work and suggests future work.

Chapter 2

Redox-Based Resistive Switching RAM

The redox-based resistive random access memory (ReRAM) is one of the most promising emerging memory concepts to succeed in the memory market. The current dominating non-volatile memory is FLASH which is based on MOSFET devices and is extensively used in mobile devices, eg. digital cameras, digital audio players, smart-phones but also in solid state drives [6]. However, this success is based on the aggressive scaling of the MOSFET device, which approaches its physical limits. The strive for an alternative memory technology that comprises fast data operation, low energy consumption, non-volatility, infinite endurance and low cost offers the chance for the ReRAM to enter the memory market. In this chapter the redox-based resistive switching mechanisms and the integration concepts of ReRAM devices for future non-volatile memory will be introduced.

2.1 Mechanisms and Materials

The fundamental mechanism that constitutes the basis of this work is the redox-based resistive switching effect. Research on the switching of the resistance in transition metal oxides can be traced back to the 1960s and was reviewed by Dearnaley, Oxley and Pagnia [7–9]. Due to the limitations in the analytical tools and the great success of the CMOS based FLASH memory technology, the interest and thereby the research activities on the resistive

switching effects faded. However, Asamitsu *et al.* [10], Kozicki *et al.* [11], and Beck *et al.* [12] rediscovered the resistive switching effect in the late 1990s. Since then, the research on the resistive switching phenomena has regained considerable interest. The ReRAM technology has also stepped into the industry's R&D focus [13] and has been considered as an emerging memory technology in the ITRS roadmap [14].

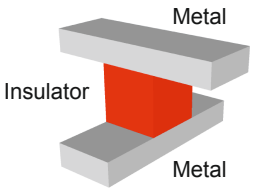


Figure 2.1: ReRAM crossbar element consisting of the metal-insulator-metal stack.

In principle, the ReRAM device consists of simple capacitor-like metal-insulator-metal (MIM) structures (Fig. 2.1), which offer the prospect of ultimate scalability and low cost. The functionality of ReRAM devices is based on the switching of the resistance state of the functional layer, sandwiched between the two electrodes, by electrical stimuli. The transition to the ON or low resistance state (LRS) is known as the SET process. The RESET process switches the device back to the OFF or high resistance state (HRS). The Boolean "1" and "0" are attributed to the ON and OFF state respectively.

Among the numerous resistive switching effects considered for the non-volatile memory applications, the group of materials exhibiting redox-related chemical effects is particularly interesting. Therefore, the classification shown in Figure 2.2 accounts for the involved material systems and the switching mechanism. Within this material group, three different effects are observed: electrochemical metallization effect (ECM), valence change mechanism or memory effect (VCM) and thermochemical memory effect (TCM) [15]. They can be classified according to different features like the switching polarity and the dominating material.

First of all, two basic operation schemes of the ReRAM devices are distinguished: The *unipolar* and the *bipolar* resistive switching [16]. As illustrated in Figure 2.3 (a), the *unipolar* switching does not depend on the polarity of the applied electrical voltage but rather on the voltage amplitude. Unipolar switching is usually found in the ReRAM devices with the symmetric cell design like Pt/NiO/Pt [17]. Starting in the OFF state, the applied voltage is

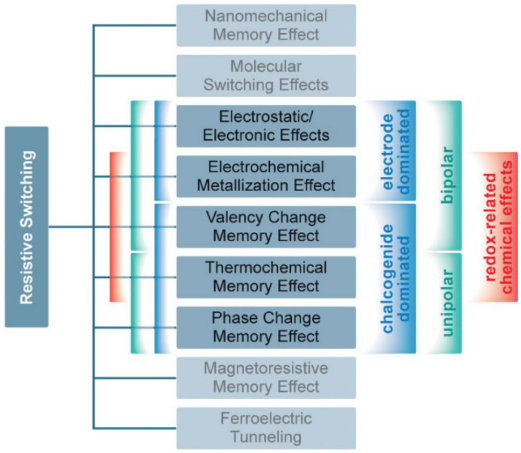


Figure 2.2: Classification of resistive switching phenomena by their physical effects, their material, and their switching polarity. From [15]

increased until the set voltage V_{SET} is reached. At this point, a controlled soft breakdown process occurs that results in the formation of a conductive filament (CF) inside the functional layer. The current during the SET process has to be limited by the current compliance (I_{CC}) to prevent the destruction of the device for both unipolar and bipolar switching. This is indicated by the dashed lines in the I-V plot. The RESET process is carried out with a voltage of the same polarity as the SET but without the I_{CC}. The high currents

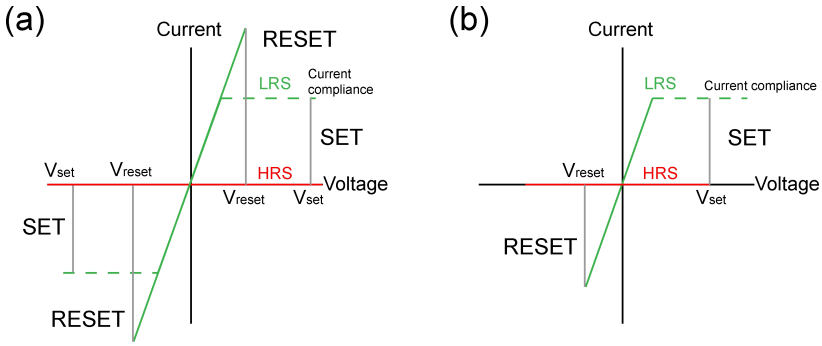


Figure 2.3: Schematic I-V traces of (a) the unipolar and (b) the bipolar redox-based resistive switching modes. [16]

during the RESET process cause joule heating and thereby the rupture of the

filament by thermochemical processes [18]. The unipolar switching is therefore attributed to the TCM type ReRAM. The required voltage for the RESET is generally smaller than the set voltage.
In contrast to the unipolar switching, the ReRAM device is considered to be *bipolar* when the SET occurs at one voltage polarity and the RESET at the opposite polarity (Fig. 2.3 (b)). This is generally observed for unsymmetrical cells such as $Pt/TiO_2/Ti/PT$ [19]. The ECM and the VCM effects exhibit the bipolar resistive switching.
Besides the switching modes discussed before, the resistive switching effects can further be classified by the material that dominates their electrical characteristics. In case of the ECM systems, the electrochemically active electrode metal such as Ag or Cu is crucial for the resistive switching. Here, the insulating solid electrolyte material can be seen as a matrix for the transport of the involved metal ions and is therefore of secondary importance in these systems. In contrast, the oxides or higher chalcogenides are the dominating material for the switching mechanism of VCM and TCM systems. Due to the high endurance, the ECM and VCM type systems are considered to be promising candidates for future non-volatile memory [14] and constitute the basis for this research work. Therefore, these effects will be discussed in more detail in the following subsections.

2.1.1 Electrochemical Metallization Memory

The ReRAM devices in which the oxidation, migration and reduction of the electrode material is the dominating factor for the resistive switching are called electrochemical metallization cells. They are also referred to as Atomic Switch or Conductive Bridging RAM (CBRAM) [20, 21] and have been peer-reviewed [22, 23].
In general, the device consists of an electrochemically active electrode metal (e.g. Cu, Ag), an electrochemically inert electrode, such as Pt or Ir, and a thin solid electrolyte (e.g. SiO_2, WO_3, Ge_xSe_y). Figure 2.4 sketches the operation principle of an ECM memory cell with the layer stack of $Cu/WO_3/Pt$. Initially, the device is in the high resistance state and no electrodeposited Cu is present on the Pt electrode (Fig 2.4 (a)).
For the SET process a positive bias voltage V is applied to the electrochemi-

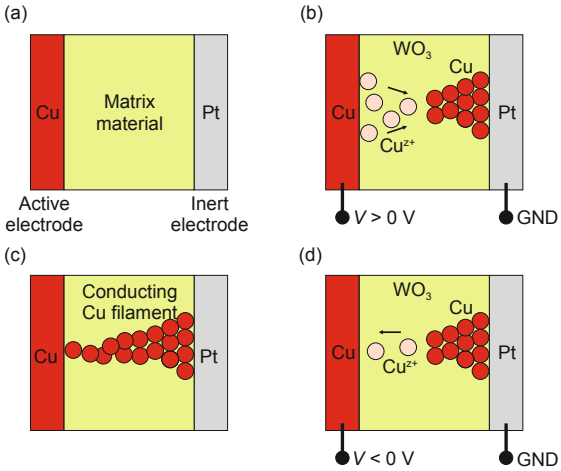


Figure 2.4: Working principal of ECM type memory elements: (a) Initial state, (b) Formation of a metallic filament under positive bias, (c) Filament connecting both electrodes resulting in the low resistive ON state, (d) Dissolution of the filament under negative bias reverting the cell back the high resistance OFF state shown in (a).

cally active Cu electrode (Fig 2.4 (b)). In consequence, the metal is oxidized and an anodic dissolution of the Cu according to equation 2.1 takes place:

$$\mathrm{Cu} \rightarrow \mathrm{Cu}^{z+} + ze^{-} \tag{2.1}$$

In this equation, Cu^{z+} denotes the mobile metal cations in the solid electrolyte while e^{-} denotes the required electron counter charge. Afterwards, the dissolved cations drift along the high electric field towards the inert electrode. When the cations reach the Pt electrode, a reduction and electro-crystallization process takes place (equation 2.2):

$$\mathrm{Cu}^{z+} + ze^{-} \rightarrow \mathrm{Cu} \tag{2.2}$$

This results in the formation of a metal filament growing from the inert electrode to the active electrode (Fig 2.4 (c)). Since the filament is highly conducting, a sudden decrease in the resistance is observed once it completely bridges the solid electrolyte. The cell has switched to the ON state. Generally, the

first SET cycle requires a higher voltage and is known as electroforming. Valov *et al.* proposed that this could be explained by mechanical stress induced by the formation of the nano-channel which persists after the RESET and acts as the template for subsequent switching cycles [22].
The RESET process is carried out with a voltage of opposite polarity (Fig 2.4 (d)). In this process, the filament is ruptured and dissolved again. Further physical details regarding the ECM switching mechanism can be found in the cited literature.

2.1.2 Valence Change Memory

The valence change memory (VCM) effect is dominated by local changes inside the transition metal oxide of the MIM structure. The observed changes in the electronic conductivity are related to intrinsic defects that act as charged dopants. In contrast to the cation based switching mechanism of the ECM systems, the resistive switching effect in VCM systems (e.g. TiO_2 [19], HfO_2 [24], ZrO_x [25] and WO_3 [26]) is explained by the localized drift of oxygen anions (or equivalently the positive charged oxygen vacancy). This is based on the fact that cation defects, that could contribute to the resistive switching, exhibit low mobilities at the operating temperatures of ReRAM [27,28]. Consequently, oxygen vacancies play the most important role since they exhibit much larger mobilities at moderate temperatures. The resulting stochiometry changes can lead to a redox reaction that causes a change in the valence state of the cation lattice.
The VCM type systems generally require an *electroforming* step to enable the resistive switching. This is achieved by applying a forming voltage which is usually larger than the subsequent SET voltages to the ReRAM element. During this procedure the formation of oxygen deficient Magnéli-phase filaments with the stochiometry of Ti_4O_7 have been observed in TiO_2 based ReRAM elements [29]. These highly n-conducting filaments result in the change of the resistance state.
The schematic SET and RESET process of a VCM type switching memory element is shown in Figure 2.5. The I-V characteristic is sketched in the center of the figure. The green and purple elements in the insets represent oxygen vacancies and Zr ions in a lower valence state respectively. In the OFF state,

the oxygen vacancy concentration at the Pt/ZrO_x interface (disc) is low (Fig. 2.5 (A)). Upon applying a negative voltage to the Pt electrode, the oxygen vacancies are attracted from the filament region (plug) into the Schottky-type barrier (Fig. 2.5 (B)). Due to a local reduction process, the height of this barrier is significantly lowered and the memory element switches to the ON state (Fig. 2.5 (C)). The RESET Process is carried out by applying a positive voltage to the active interface (Fig. 2.5 (D)). In this process, the oxygen vacancies are repelled from the disc region and drift back into the plug region. As the result, the original height of the Schottky-barrier is re-established.

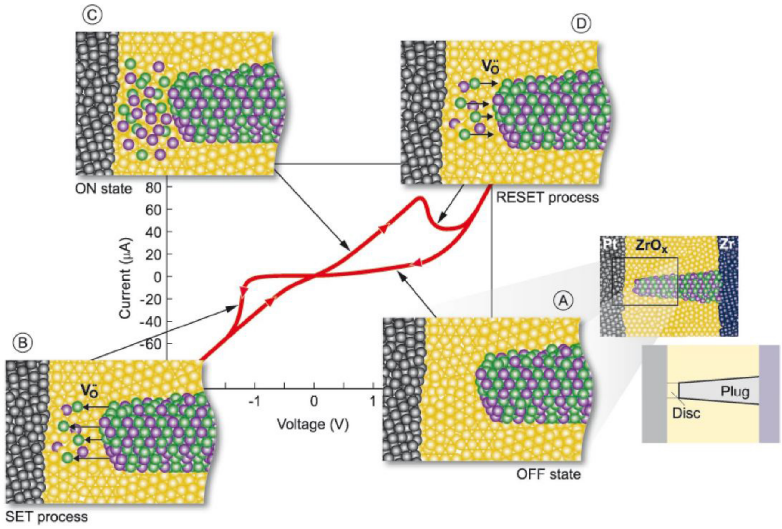


Figure 2.5: Schematic of the VCM type switching of a Pt/ZrO_x/Zr memory element. (A) OFF state, (B) SET process, (C) ON state, (D) RESET process. [30]

2.2 ReRAM Crossbar-Array Integration

In order to compete with current memory technologies like FLASH and DRAM, the ReRAM has to be integrated with high memory density at low cost. The preferred integration scheme is the purely passive crossbar-array concept, i.e., arrays without select transistors at the storage nodes [31]. The main reason is

the inherently high density with cell sizes of $4F^2$, in which F is the minimum feature size and thus the width of the electrodes at the integration technology node (Fig. 2.6). In addition, the passive crossbar-arrays offer the prospect

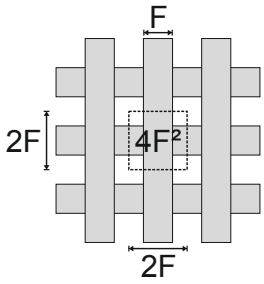


Figure 2.6: Passive crossbar-array with the minimum feature size F determining the width of the electrodes. The memory device size amounts to $4F^2$.

of 3-D integration by simple stacking of multiple crossbar layers [32, 33]. This can further increase the integration density of ReRAM crosspoint devices. The prototypical realization of this approach by means of nanoimprint has been demonstrated [34].

The passive crossbar-arrays however suffer from the sneak path problem. This occurs due to the unwanted voltage drop across the non-addressed memory cells. The sneak path in the passive array disturbs the memory operation, i.e. read and write [35]. The disturbance of the read operation in a crossbar-array is shown in Figure 2.7. The detected read current I_{read} consists of two

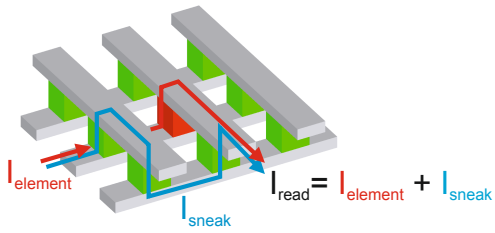


Figure 2.7: Sneak path problem during the readout. The shown configuration represents a worst case pattern where the major part of the read current does not flow through the selected memory element (HRS) but through adjacent cells in the LRS. This makes the detection of the resistance state extremely difficult [35].

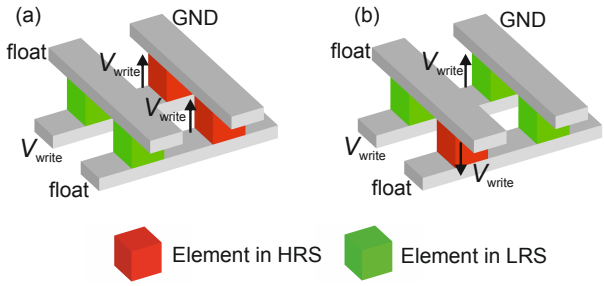


Figure 2.8: Unintended writing caused by the sneak path problem in passive crossbar-arrays for two worst case patterns (a) and (b). In both cases, the addressed memory element is located in the right side at the back. When the non-addressed lines are left floating, the writing voltage will drop at cells neighboring the addressed memory element leading to the unintended writing [31].

parts; the current through the selected memory element I_{element} and the current through non-addressed cells I_{sneak}. In the shown case, the cell to be read out is in the HRS and the surrounding cells are in the LRS, only a minor part of the read current stems from addressed element.

The disturbance of the writing operation of passive crossbar arrays is shown in Figure 2.8. When row and column are biased with the write voltage V_{write} and ground respectively while the surrounding electrodes are left floating unintended writing can occur. Because of the large resistance ratio between the OFF and ON state a parasitic path is formed and almost the entire V_{write} drops across the non-selected cell.

The issue of unintended writing can be circumvented by the application of dedicated biasing schemes like the $V/3$ and the $V/2$ schemes shown in Figure 2.9. Both schemes have in common that the potential of the non-addressed word- and bitlines is fixed. This effectively limits the unwanted voltage drop across the not selected memory elements to $1/3$ or $1/2$ of the writing voltage. The drawback of these addressing schemes is the static power losses.

Beside the addressing schemes, several solutions to overcome the sneak-path issue have been proposed. First, the complementary resistive switches (CRS) proposed by Linn *et al.* consisting of two antiserial memristive elements that allow the construction of large passive crossbar arrays and the reduction of the power consumption [35]. The second approach is based on selector ad-

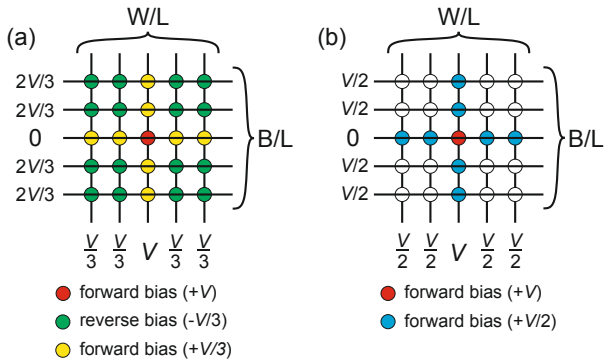


Figure 2.9: Schematic plot of the applied voltages and bias schemes for passive crossbar arrays. (a) In the $V/3$ scheme, all memory elements except the addressed cell are biased with $\pm V/3$. This leads to increased static power loss. (b) In the $V/2$ scheme, only the ReRAM cells in the same word and bit line as the addressed cell are biased with $V/2$. Redrawn from [36]

dressed memory elements. The selector can be a diode resulting in an 1D-1R configuration [37, 38]. The scalability of such devices has not been proven yet. Another proposed selector device is the MOSFET resulting in an 1T-1R configuration. However, the integrated devices consume a larger area than the 1D-1R configuration. The third approach uses the inherent nonlinearity in the I-V characteristics of the ReRAM devices such as $Pt/TiO_2/Ti/Pt$ cells. This approach will be analyzed in chapter 5 and chapter 6.

Since non-volatile memory based on the ReRAM devices will be operated by voltage pulses, the nonlinearity of the ON state in this work is analyzed with pulses of 100 ns width. This is especially important to minimize the static power losses imposed by the fixed voltage schemes. The nonlinearity parameter (NL) of the ReRAM devices is calculated from the transient current responses to the voltage pulses by equation 2.3:

$$\mathrm{NL} = \frac{I(V_{\mathrm{RESET}})}{I(V_{\mathrm{RESET}}/2)} \tag{2.3}$$

In this equation, the V_{RESET} is the voltage required for the RESET at the given pulse period while $V_{\mathrm{RESET}}/2$ represents the voltage drop across non-addressed cells in a crossbar-array. This definition is deducted from the V/2 addressing

scheme for the passive crossbar-arrays [36].

Chapter 3

Fabrication of ReRAM Devices

3.1 Equipment and Experimental Methods

3.1.1 Thin Film Deposition Techniques

This section focuses on the thin film deposition methods utilized in this work. The controlled deposition of layers in the low nanometer range is a necessity to enable research on resistive switching devices. The fabrication process of metal-insulator-metal structures requires the deposition of metal layers as electrodes and also metal oxides as the switching material. In the present work, two deposition techniques, plasma-related sputter deposition and thermal evaporation of metals were used. These techniques are generally classified as Physical Vapor Deposition (PVD). In the following section,the working principle of both techniques will be described.

3.1.1.1 Sputter Deposition

The physical sputter deposition process does rely on the creation of an electrically induced non-thermal plasma between two parallel electrodes. The plasma is generated by electrons with high kinetic energies colliding with the gas atoms leading to an ionization of the latter. The achievable kinetic energies of the electrons are directly influenced by their mean free path. Resulting from this fact, a vacuum chamber with low pressure (10^{-3} to 1 mbar) is necessary to enable the ignition of the plasma at low power. The generated Ar-ions inside the plasma are accelerated towards the target and bombard the surface. The

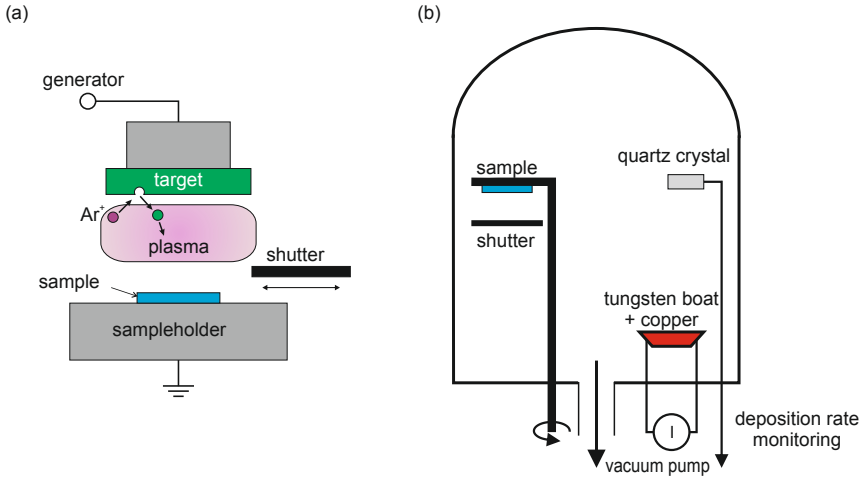


Figure 3.1: Physical vapor deposition (PVD): Schematic of a sputter deposition tool (a) and a thermal evaporation chamber (b). [40]

momentum transfer causes an ablation of the target material into the vapor phase. Then, the sputtered particles fly from the target to the sample and deposit on the surface. Due to the relatively high energy of the particles and the isotropic nature of deposition resulting in coverage of the resist flanks, sputtering processes are not suitable for lift-off metallization [39].

The simplified schematic of the sputtering tool is shown in Figure 3.1 (a). In general, the sample is mounted at the grounded electrode while the generator is connected to the target. Depending on the target material either a direct current (DC) voltage source or a radio frequency (RF) generator, typically at $f = 13.56$ MHz, is used for the thin film deposition. The ion bombardment causes static charging of insulating target materials. This can disrupt the plasma and therefore DC sputtering is not applicable to insulation targets. For further information regarding plasma processes and the sputter deposition, the reader is referred to literature [41].

The TiO_2 investigated in this research work was deposited by using a reactive DC sputter process from a metallic Ti target with a gas mixture of Ar and O_2 in an Univex 450C cluster tool from Oerlikon-Leybold. Depositions of the different layers can be performed in-situ with this machine since it has several

sputter chambers with different target materials connected to a transfer chamber. The deposition of Ti and Pt was carried out in pure Ar gas atmosphere. The complete list of the sputtering parameters are presented in table 3.1. Further descriptions of the sputtering processes are given by Hermes [42] and Nauenheim [39] and the detailed physical characterization of the as-deposited TiO_2 layers is described by Jeong [43].

Sputter Parameter	**TiO_2**	**Ti**	**Pt**
Gas flow [sccm]	46/14 of Ar/O_2	60 Ar	60 Ar
Power [W]	300	300	375
Presputter time [s]	120	180	20
Pressure [mbar]	$2.24x10^{-2}$	$2.24x10^{-2}$	$1.44x10^{-2}$
Deposition rate [Å/s]	0.29	4.2	17.6

Table 3.1: Sputter deposition parameters for the TiO_2, Ti and Pt

RF sputtering of the WO_3 films was carried out at room temperature in pure Ar atmosphere at a pressure of $9.9 \cdot 10^{-2}$ mbar with an applied RF power of $P = 121$ W. Under these conditions, the deposition rate was 1 nm/minute. The sputtered WO_3 was physically characterized with atomic force microscopy, x-ray diffraction and Rutherford back-scattering spectroscopy. The deposited layer was amorphous with a rms roughness of 0.5 nm and a slight excess of oxygen [40].

3.1.1.2 Thermal Evaporation

In this research work, thermal evaporation processes were used for lift-off metallization of the top electrode structures as well as the deposition of Cr for the fabrication of imprint stamps. This process is usually carried out at room temperature in a high vacuum (HV) chamber with a pressure of about 10^-7 mbar. The reasons for using the HV conditions are on the one hand the low vapor pressure of the materials and on the other hand the elongation of the mean free path of the evaporated material. The longer mean free path is an important parameter to achieve an undisturbed trajectory of the evaporated atoms from the point-like source to the sample. This enables the anisotropic deposition. In order to evaporate the target materials, two type of sources are

used in the thermal evaporation process:

1. Resistively heated sources
2. Electron beam heated sources

In the first case the material to be evaporated is placed inside a W boat (cf. Fig. 3.1 (b)) that is heated by passing current through the material. This method was used to evaporate copper. In the second case a high energy electron beam (e-beam) is guided to a water cooled crucible to melt the material inside. The evaporation rate is monitored by a quartz crystal placed next to the sample surface and can be controlled either by the current through the boat or by the e-beam current. The advantages of the thermal evaporation in comparison to sputtering are the low kinetic energy of the vaporized metal atoms and the lack of sidewall deposition of resist masks. Therefore, the e-beam evaporation was employed for the deposition of Ti and Pt for lift-off metallization of the top electrode structures. In this thesis, the Cr thin layer deposition for the imprint stamp fabrication was also carried out by thermal evaporation. Additional information regarding the thermal evaporation processes can be found in [41].

3.1.2 Lithography Methods

The success of the semiconductor industry can be linked to the technological developments in patterning techniques. One of the most prominent tools to fulfill the everlasting demand for the reduction of device sizes and improvements in performance are lithography processes. The word lithography stems from the Greek words *lithos*, "stone" and *graphein*, "to write". Classic lithography was invented in 1796 and utilizes stone or metal plates modified by chemical processes to exhibit hydrophobic and hydrophilic regions to either accept or reject ink. The images or text on the plate can than be printed to a sheet of paper by a press.
In modern lithography used for micro- and nano-electronic fabrication, the information of the mask is generally transferred to the wafer by means of light or charged particle beams. The medium to pattern the desired structures is a resist, whose solubility in special developers is altered by the exposure to those beams. The development and improvement of patterning processes including lithography for the integration of resistive switching elements into passive crossbars and 1T-1R devices was a major part of this work. The different kinds of employed lithography methods as well as some standard processes will be addressed in this section.

3.1.2.1 Optical Lithography

Structures with lateral sizes in the micrometer range (≥ 1 μm) were patterned by means of optical photo lithography. The name of this type of lithography refers to the use of (visible) light to illuminate a suitable resist that is sensitive to the wavelength of the applied radiation. In this research work the AZ 5214E image reversal photoresist from MicroChemicals GmbH was used. This special photoresist comprised of a novolak resin and naphthoquinone diazide as photoactive compound is capable of featuring negative as well as positive angle resist wall profiles depending on the process flow [44]. Figure 3.2 illustrates the corresponding positive an negative processes. The initial steps for both processes were essentially the same. First, the sample had to be cleaned in an acetone bath to remove organic contamination followed by an isopropanol bath to prevent striations. Both cleaning steps were carried out for 5 minutes with

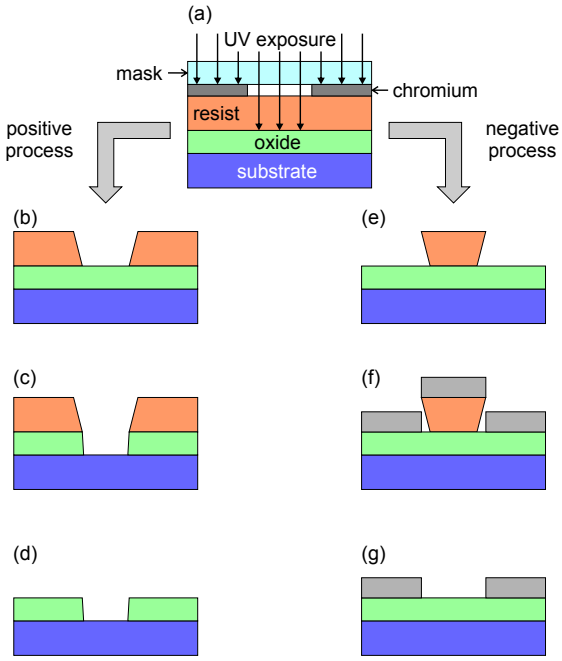


Figure 3.2: Process flow for optical lithography illustrating the positive process utilized for the creation of etch masks (left) and negative or image reversal process for lift-off metallization (right).

ultrasonic agitation. After blow-drying the sample with nitrogen it was placed on a hotplate at 120 °C to eliminate any remaining water and solvent from the surface. The photoresist was then spun onto the substrate with 500 rpm for 5 s and subsequently 4,000 rpm for 30 s. This resulted in a homogeneous film thickness of 1.5 μm. Afterwards, the sample was baked for 5 minutes on a hotplate at 90 °C. The baking step was necessary to diffuse solvent out of the resist to avoid mask contamination or sticking to the mask and blistering by N_2 created during exposure [45].

Next, the substrate was mounted on the MA6 mask alignment tool from Süss MicroTec and exposed with UV light through a photo-mask. The photo-mask consists of a UV transparent glass plate which carries a layer of chromium patterned by electron beam lithography and an etching step (Fig. 3.2 (a)).

There are three modes to transfer the information of the mask to the sample,

contact lithography, proximity lithography and projection lithography. In the *contact lithography*, the mask is brought into direct contact to the resist. The theoretical critical dimensions (CD) depend on the wavelength λ and the resist thickness d, given by equation 3.1:

$$\mathrm{CD} = \sqrt{d \cdot \lambda} \tag{3.1}$$

In case of the MA6 with a Hg-arc light source emitting at the I-line (λ = 356 nm) and the 1.5 μm resist thickness the smallest achievable structures had a size of approximately 740 nm. However, due to an imperfect contact between the mask and the resist and other factors, the maximum achievable resolution averaged at 1 μm.
The main drawback of the contact lithography is the deterioration of the mask caused by the physical stress during processing. This can be overcome by the introduction of a gap g between the mask and the sample, and is known as *proximity lithography*. This advantage of the proximity lithography is traded in for a reduction in the resolution to:

$$\mathrm{CD} = \sqrt{(g + d) \cdot \lambda} \tag{3.2}$$

The *Projection lithography* is the standard technology in semiconductor industry. In this case, the optical system transfers the image of the mask to the resist offering the chance to shrink the image in order to achieve smaller structures. Based on the Rayleigh Criterion the critical dimension results in:

$$\mathrm{CD} = k_1 \frac{\lambda}{NA} \tag{3.3}$$

with the technology constant k_1 summarizing non ideal conditions e.g. lens errors, resist behavior and shape of the structures. The numerical aperture (NA) of the optical system is given by $NA = \sin(\alpha) \cdot n$, with the refractive index n of the material between the last optical element and the substrate and α half the opening angle of the lens.
In this research work, the structures with micrometer dimensions were patterned with the contact lithography. The first exposure was a distinctive feature to differentiate between the positive and negative process. For the positive

process (Fig. 3.2(b)-(d)) an exposure of 41 s with an intensity of approximately 2.3 - 2.4 mW/cm^2 in constant power mode (350 W) was applied. The resist in the illuminated area became soluble by the AZ 326 developer (70 s) leaving a mask with positive wall profiles for structuring the oxide or metal layer with an etching step .
For the negative process (Fig. 3.2(b)-(d)), a shorter first exposure for 17 s was carried out. Then the image reversal bake step at 120 °C for 40 s was performed after a waiting period of at least 2 minutes to give the generated nitrogen some time to diffuse out of the resist. During the baking step, the exposed areas were crosslinked making them resistant to the developer. Next, a flood exposure of 90 s without a mask alters the before unexposed resist with still active photo compound to be soluble. The resulting resist mask exhibits an undercut which is necessary to perform the lift-off process.

3.1.2.2 Electron Beam Lithography

The investigation of the resistive switching properties of metal-insulator-metal structures requires a reduction of the device size into the nanometer regime. This is necessary on the one hand to prove the scaling potential of this kind of memory technology and on the other hand to explore the switching kinetics without large RC-times arising from the ReRAM cells, which are essentially capacitors. While advanced optical lithography like immersion lithography is used by the semiconductor industry for the sub-50 nm node, this technology is not applicable in a laboratory environment because of cost. However, the cost efficient conventional UV based optical lithography, as described in section 3.1.2.1, faces resolution constraints. Therefore, an alternative patterning method must be selected to create prototypes in the sub-100 nm regime. The most flexible method available at the Forschungszentrum Jülich is the Electron Beam Lithography (EBL). In this section the basics of EBL will be introduced and also the employed machine and writing strategy will be explained.
The main reason for the usage of electron beam lithography is based on the relation between the smallest feature size and the radiation wavelength as described in equation 3.3. In case of electrons as radiation source the de Broglie hypothesis states that all matter has a wave-like nature with the wavelength

λ related to its momentum p in the following way:

$$\lambda = \frac{h}{p} = \frac{h}{m_\mathrm{e} \cdot v} \tag{3.4}$$

with h the Planck constant, m_e the mass of an electron and its velocity v. The momentum $p = m_\mathrm{e} \cdot v$ is determined by the acceleration voltage V_acc applied to the electrons by the electron beam column:

$$\begin{aligned} E_\mathrm{kin} &= E_\mathrm{el} \\ \Rightarrow \frac{1}{2} m_\mathrm{e} v^2 &= e V_\mathrm{acc} \\ \Rightarrow m_\mathrm{e} \cdot v &= \sqrt{2 m_\mathrm{e} e_0 V_\mathrm{acc}} \end{aligned} \tag{3.5}$$

Equations 3.4 and 3.5 combine to

$$\lambda = \frac{h}{\sqrt{2 m_e e_0 V_\mathrm{acc}}} \tag{3.6}$$

This is an adequate non-relativistic approximation of the wavelength of the electron beam radiation for the acceleration voltage of $V = 50$ kV, that was used during this work. The resolution of electron beam lithography is in general not limited by the wavelength, which amounts to $\lambda \approx 5.5$ pm, but by several other effects inherent to the writing system and described by Nauenheim [39].

The employed EBL system employed is a Leica EBPG 5000 from Vistec Electron Beam GmbH. The working principle of this electron beam column is schematically shown in Figure 3.3. The electrons required to form the beam are generated by thermal field emission from the Schottky emitter, which in the case of the EBPG 5000 is a sharp tungsten tip coated with ZrO_2 with a radius smaller than 1 μm. The ZrO_2 coating reduces the work function. The emitter is heated up to to 1800 °C and an electric field is generated by a positive voltage bias of $V = 6622$ V on the extractor to lower the surface barrier that electrons have to overcome by thermal excitation to escape from the metal. In order to prevent contamination of the emitter, the electron source is located in ultra high vacuum with a pressure of $3.5 \cdot 10^{-10}$ mbar while the pressure at the wafer stage chamber averages at $5 \cdot 10^{-7}$ mbar. Backward emis-

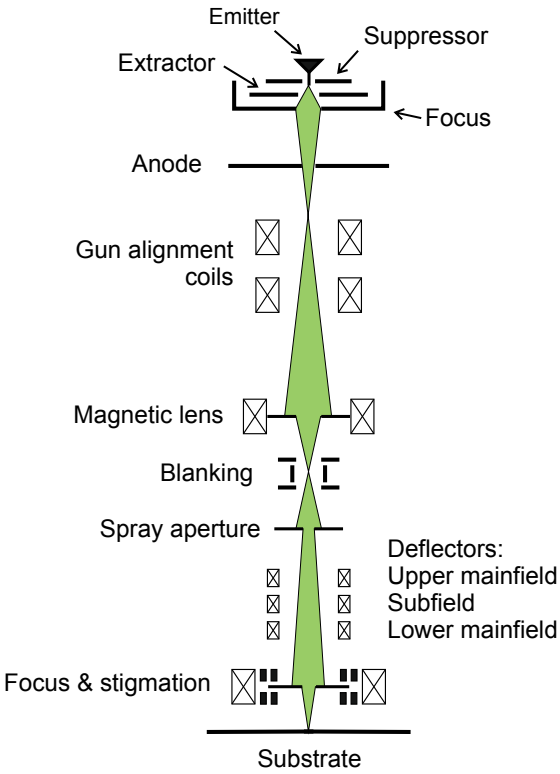


Figure 3.3: Schematic diagram of an electron beam writing system. Redrawn from [46]

sion is shadowed and suppressed by feeding the tip of the filament by 0.24 mm through the suppressor with a negative applied potential. Subsequently, the electron beam is focused by a Wehnelt cylinder and the electrons receive their kinetic energy from the electric field generated by applying the acceleration voltage to the anode. The lenses which focus the beam by electrostatic forces are only placed in the electron gun region because they have worse aberration than magnetic lenses but can sustain bake-out temperatures.

On their way down the electron beam column to the sample stage, the electrons are focused by several magnetic lenses. In these lenses the magnetic flux diverging along the optical axis from two circular symmetric high permeability material pole pieces wrapped around copper windings, focuses the

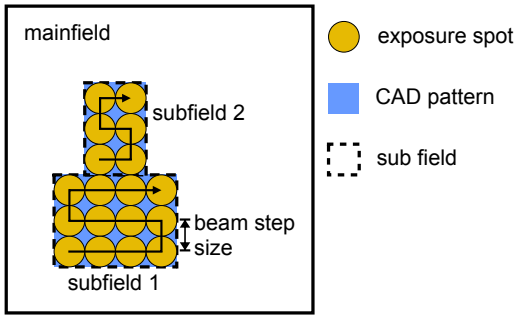


Figure 3.4: Vector scan electron beam writing scheme.

electrons towards this axis. Furthermore, there are two kinds of apertures that the electron beam has to pass. First, a beam blanking aperture is placed at a focal point of the beam to turn the beam off and on. This is accomplished by deflecting the beam so that is does not hit the hole in the aperture but is intercepted. Second, the spray aperture obstructs any stray electrons.
Before the final set of lenses controlling the focus and stigmation, a deflector cascade consisting of the upper and lower mainfield deflector and the subfield or trapezium deflector is placed to scan the electron beam over the sample.
The EBPG 5000 is vector scan system. This means that the beam is only scanned in areas of the substrate that have been defined by a CAD mask file to be written. First of all, the CATS software from Synopsis translates the pattern to fit to the writing strategy of the EBL system. A schematic of this writing strategy is shown in Figure 3.4. The area that the deflector cascade can scan the electron beam over is limited and therefore, the substrate is mounted to a moveable wafer stage that steps through the pattern to extend the possible pattern sizes. This stage can hold up to 6 inch wafers and its movement is controlled by laser interferometers with sub nm precision. Since samples with different thicknesses can be mounted, the height of the sample surface must be controlled by a reflected laser beam to adjust the focus of the beam.
At a give stage position, the square area that the upper and lower mainfield deflectors can cover by deflecting the electron beam to the required position is defined as a *mainfield*. Therefore, the pattern is divided into blocks whose size is a function of the beam step size because each pixel needs to be addressed

and the available address space is limited (see Table 3.2). The mechanical movement of the stage itself has limited accuracy, so writing structures that span over more than one mainfield can result in so called stitching errors, as described by Nauenheim [39].
Part of the writing strategy is to segment the pattern, that is to be written in one mainfield, into *subfields* of trapezoid shape. Then, the mainfield deflectors guide the electron beam to one corner of a subfield before unblanking the beam. From there, the scanning is performed by the trapezoid deflector in a meander type movement through the subfield. The trapezoid deflector has a smaller scan area as compared to the mainfield deflectors but has a higher scanning speed. Since EBL is a direct write process and every pixel will be exposed sequentially it has very low throughput and is not suitable for industry applications except mask creation.

Beam step size [nm]	12.5	5	2.5	2	1
Main field [μm^2]	$800 \cdot 800$	$320 \cdot 320$	$160 \cdot 160$	$260 \cdot 260$	$180 \cdot 180$

Table 3.2: Mainfield size as a function of beam step size

In reality, the electron beam spot has a circular shape with a Gaussian intensity distribution. However, the exposure dose D of one pixel with a square area, depending on the beam step size d_{step}, is calculated for the chosen beam current I_{beam} and the stepping frequency f_{step}:

$$D = \frac{I_{beam}}{d_{step}^2 \cdot f_{step}} \tag{3.7}$$

The resist is not only exposed by the incident beam but also a significant dose amount results from the interactions of electrons with the resist and especially the layers underneath it. This so called proximity effect is generated by large angle scattering of the electrons in the substrate [47–50]. These electrons can return to the substrate surface and expose the resist as far as some μm away from the incident beam. Besides this, the electrons will also undergo inelastic scattering inside the resist which broadens the beam. The proximity effect and the beam broadening need to be especially considered when patterning dense structures like lines and spaces but also very small structures because they

limit the resolution.

3.1.2.3 Nanoimprint Lithography

Nanoimprint lithography (NIL) is based on the replication of the nano-structured surface of a stamp (mold) into a resist by mechanical pressure and three dimensional displacement of the material. Hence, the possible resolution is essentially not limited by the wavelength of the employed light source like in optical lithography but by the pattern in the mold. The main advantage of NIL in comparison to conventional lithography methods is the high resolution patterning potential as accomplished by electron beam lithography without the constraint of low throughput [51–53]. The resulting contrast in local thickness of the imprinted resist can be used as a means to pattern an underlying layer by etching but the resist can also be applied as a functional material e.g. to create micro lenses [54, 55] or micro-fluidic channels [56]. NIL achieves high efficiency because imprinting offers parallel patterning and can be carried out on a wafer scale. In general, two types of NIL can be distinguished:

1. Thermal NIL
2. UV-NIL

The first publications on nanoimprint lithography by Stephen Y. Chou *et al.* in 1995 [57–59] deal with the *thermal NIL*. In thermal NIL, thermoplastic polymers, e.g. polymethyl-methacrylate (PMMA), are utilized as moldable resists. The PMMA is frequently used because it can easily be spin-coated onto the substrate to form highly uniform layers with resist thicknesses tunable by the solid contents of the resist and the spin-rate. Thermoplastic materials basically undergo three different states depending on temperature that are essential for the application as imprint resists. Below the material's glass transition temperature $T_g \approx 100°C$, the resist is in a hard elastic glassy state while it becomes viscoelastic for temperatures above T_g. Until reaching the flow temperature T_f the viscosity of the material is almost constant. At T_f, which was empirically identified to be approx. 80 °C above the T_g, the viscosity again drops by several orders of magnitude and the polymer enters the flow state [55]. Therefore, the resist flows into the cavities of the mold while applying the imprint pressure and heating the system above T_f. Once the cavities in the stamp are filled, the

temperature is decreased below T_g and the resist solidifies, leaving a negative image of the stamp in the polymer after demolding.
The *UV-NIL* was first reported by Haisma *et al.* from Philips Research Laboratories in 1996 [60]. In the Forschungszentrum Jülich the UV based nanoimprint technology was introduced by Meier and Gilles *et al.* [61–65]. Its name is derived from the usage of monomers that are curable by UV light and, in contrary to the thermal NIL, have a low viscosity and can be deformed at room temperature. These resists are first deposited on the wafer by spin-coating (Fig. 3.5 (a)). An UV transparent mold consisting of quartz glass is then pressed into the liquid monomer (Fig. 3.5 (b)). The UV light exposure triggers the polymerization and linking of the oligomers in the resist (Fig. 3.5 (c)). This step leads to an irreversible solidification of the resist. Once this process step is completed, the mold and substrate are separated by mechanical forces just as in the thermal NIL process.
The thermal and the UV-NIL share the fact that after imprinting an unwanted resist layer remains in between the patterned resist structures (Fig. 3.5 (d)). This so called residual layer has to be removed by a plasma etching step (breakthrough etch) (Fig. 3.5 (e)) to expose the surface of the wafer for the subsequent transfer of the resist pattern into the functional layer. Finally the remaining resist has to be removed either by a plasma process or by wet chemical etching with either solvents like acetone or acids depending on the applied resist (Fig. 3.5 (f)).

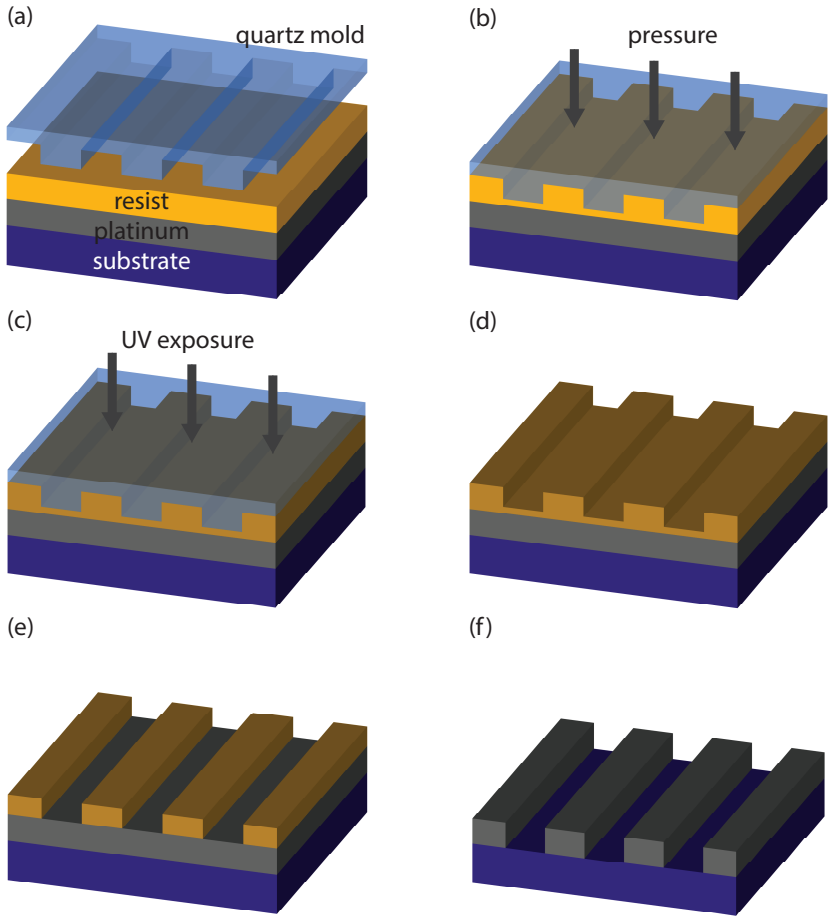


Figure 3.5: UV-nanoimprint process flow. A silicon wafer with a titanium/platinum layer is cleaned by oxygen plasma and spin-coated with the imprint resist (a). Next, the quartz stamp is pressed into the resist, that flows into the cavities of the mold (b). An exposure with UV light cures the resist (c), leaving a negative image of the quartz wafer in the polymer after demolding (d). The residual layer is removed by an etching step (e) before the pattern is transferred into the platinum layer (f).

3.1.3 Etching

Etch methods are an essential tool for the semiconductor industry to realize micro- and nano-structure patterning. The two methods used in this work to transfer the information of the resist masks into functional layers were wet chemical etching and dry etching. Therefore, both methods and their suitable applications will be introduced in this section.

3.1.3.1 Wet Etching

The wet chemical etching is based on the exposure of a surface to an etching fluid by immersion in a bath of etchant. Diffusion plays in important role in wet chemical etching since the reactive components in the liquid-phase etchant have to diffuse to the surface and the etch products have to be transported away from the surface. Wet etching is usually isotropic which leads to an undercut under the resist mask and results in broadening of the structures (Fig. 3.6 (c)). This drawback impedes the usage of wet chemical etching for the patterning of nano-structures. However, the wet etching offers very high selectivity meaning that the etch rate of the material to be structured is higher than the etch rate of other layers. During this research work the wet etching was employed for pad opening processes for instance to remove the WO_3 from the platinum bottom electrode contact pads with a KOH etch. The chemical removal of the WO_3 followed the reaction equation:

$$WO_3(s) + 2OH^- \rightarrow WO_4^{2-}(aq) + H_2O \tag{3.8}$$

Because of the high selectivity of this process the WO_3 was completely removed from the pads by performing an overetching while the underlying Pt was not

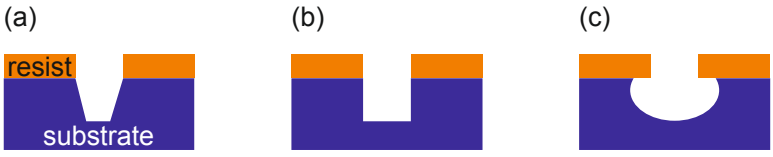


Figure 3.6: Etch characteristics: sputtering (a), physically assisted chemical etching (b), chemical etching (c)

affected. This technique is especially advantageous if the electrodes are very thin.

3.1.3.2 Dry Etching

The fabrication of the nano-structures requires advanced dry etching processes. The pattern transfer was primarily performed with an Ionfab300plus tool from Oxford Instruments which is shown in Figure 3.7. This Reactive Ion Beam Etching (RIBE) machine offers various process gases like Ar, O_2, CF_4 and SF_6. Depending on the nature of the processing gas, the etching process can be physical or physically assisted chemical (Figure 3.6). For example, Ar gas etches the material physically whereas O_2 and CF_4 exhibit a chemical etch component. Pure chemical etching, which can achieve undercuts, is not possible with the employed machine.

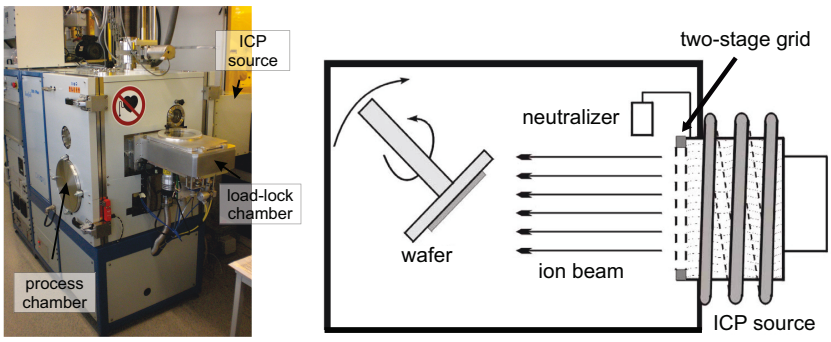


Figure 3.7: Reactive ion beam etching tool Ionfab300plus with process and load-lock chamber. The plasma source is located outside the main chamber as well as a mass spectrometer on the top of the machine (a). Schematic of the internal setup of the machine (b). [66]

Up to 6 inch wafers can be transferred from the load-lock into the process chamber which is kept under HV conditions ($1 - 2 \cdot 10^{-6}$ mbar). Inside the main chamber, the wafer is mechanically clamped with a clamp ring onto a temperature-controlled chuck, which is referred to as platen. The backside cooling of the platen by fluid circulation from an external chiller and the helium cushion between the wafer and the chuck stabilizes the processing temperatures. The chuck can be tilted from 0 ° to 90 ° in relation to the beam axis

to enable trimming of sidewalls. To ensure homogeneous etching, especially for tilted wafers, the chuck can be rotated with up to 20 rpm.
In this tool, the plasma is generated outside the reactor chamber by an inductively coupled plasma (ICP) source in which the energy is supplied by time-varying electric currents through a coil causing electromagnetic induction. The ions are extracted from the source, accelerated and focused by a two-stage grid. Namely the inner (screen) grid and the front (accelerator) grid with the respective potentials V_{B} (Beam Voltage) and V_{A} (Acceleration Voltage). The beam voltage is measured between ground potential and the walls of the source. The plasma bulk is kept slightly positive with respect to V_{B}. The accelerator grid is kept negative with respect to ground to prevent a backstreaming of electrons into the source. Thus, the total extraction potential (V_{ext}) accelerating the ions out of the source is the difference of $V_{\mathrm{B}} - V_{\mathrm{A}}$ [63].
In order to prevent the charge up of insulating surfaces caused by impinging ions, the ion beam is neutralized. Otherwise the surface of the wafer would repel ions and the etch characteristics would be changed. Neutralization is done by generation of an intense plasma in a cylindrical metal cup inside the filament bridge neutralizer (FBN) feeding electrons to the ion beam.
There are two main regulation parameters to tune the etch characteristics:

- V_{B} - Beam Voltage
- I_{B} - Beam Current

Both parameters have an almost linear impact on the etch rate. The beam voltage determines the kinetic energy of the ions while the beam current effects the amount of ions impinging on the wafer surface.
In summery the RIBE offers great adaptability for the patterning in the nanometer scale required for the creation of imprint molds and nano-crossbar memory elements.

3.1.4 Physical Characterization Methods

Physical characterization methods are required in process development as well as the structural analysis of redox-based resisting switching devices. It is crucial to monitor the quality of each process step and also the final ReRAM cells. The standard means to control micrometer scale features like contact pad structuring, pad opening processes or resist stripping were optical microscopes. However, the fabricated nano-structures are analyzed by scanning electron microscopy (SEM) since it offers nanometer scale resolution. Another important tool to quickly check for resist thicknesses or etched steps was the surface profilometry.

3.1.4.1 Scanning Electron Microscopy

The nano-structural characterization is primarily carried out with a Hitachi SU8000 scanning electron microscope. The general working principle of the SEM is similar to the electron beam writing system described before [67, 68]. As the name states, the SEM is based on scanning a focused electron beam over the specimen. This electron beam is generated by field emission from an electron gun comparable to Figure 3.3 and accelerated by an electric field generated by an applied acceleration voltage of up to 30 kV. Depending on the kinetic energy of the electrons and the material properties, the penetration depth and therefore the interaction volume can extend from less than 100 nm to several μm into the surface. Two distinct interactions of the electrons with the matter of the sample occur. First, secondary electrons (SE) are released from the atoms by inelastic interaction with the incident high energy primary electrons (PE) from the beam [69]. The secondary electrons have energies of less than 50 eV and can therefore only leave the surface if they are created within the first 10 nm -30 nm of the specimen. Second, elastic scattering gives rise to the high-energy back scattered electrons (BSE).

The image acquisition of the SEM is based on the detection of these secondary and backscattered electrons. The detector configuration of the SU8000 is shown Figure 3.8. The SU8000 in-lens detectors offer the advantage of a possible decrease of the working distance which results in a better resolution because of the reduction of the spherical aberration that is due to the geom-

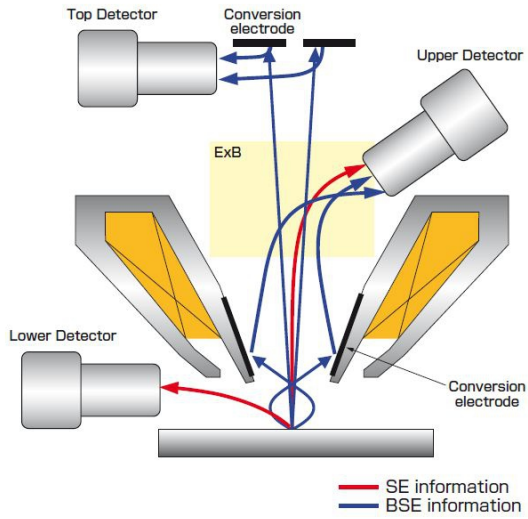


Figure 3.8: Hitachi SU8000 scanning electron microscope detector configuration. [70]

etry of electromagnetic lenses. The detection of high angle BSE with the top detector exhibits a material contrast depending on the Z-number with less topographical information while the main purpose of the upper detector is to display the topography image gained from the SE. The lower detector is used for longer working distance (less resolution) SE imaging of surface topography. The determination of layer thicknesses or structure heights required a tilt of the sample so that the flanks become visible. Because of the viewing an-

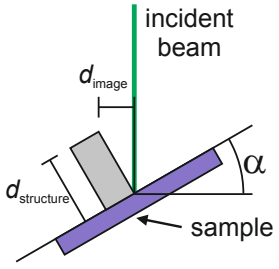


Figure 3.9: Determination of structure height or layer thickness for a tilted sample in SEM.

gle, the height of a structure measured in an SEM image is compressed and needs correction. The real layer thickness $d_{\text{structure}}$ is calculated with simple trigonometry (Fig. 3.9):

$$d_{\text{structure}} = \frac{d_{\text{image}}}{\sin \alpha} \tag{3.9}$$

3.1.4.2 Surface Profilometry

Surface profilometry is carried out with a Veeco Dektak 150. These measurements are very expedient as they offered a quick feedback when performing consecutive processing steps. The surface profile is obtained by scanning a thin stylus over the surface of the specimen with a vertical resolution of approximately 5 nm. In contrast to atomic force microscopy which offers a better resolution, the Dektak can measure larger step heights of up to 1 mm and is therefore suited to check for the correct thickness of photoresist masks. The surface profilometry is also used to determine etch rates. This is done by covering a part of the sample with resist or by clamping of a piece of silicon on the surface and exposing the sample to the etch process. After removing the cover from the surface, the step can be measured with the Dektak. Although the shadowing during the etching does not produce steep edges, the long scan distance of the Dektak enables a determination of the different heights of the sample surface and the etched layer. Due to the limited lateral resolution, this method does not give an insight into the quality of the etched flank. However, this offers a good solution for etch rate and step height determination.

3.1.5 Electrical Characterization Setup

The resistive switching behavior of the different fabricated ReRAM devices was electrically characterized over a large dynamic range from nanosecond voltage pulses to quasi-static modes where the ramp rate is in the range of volt per seconds and even minutes. The large range of encountered resistances and the resulting currents make the characterization of the performance of the memory elements challenging. Most of the employed setups are standard laboratory equipment and will therefore only shortly be described in the following subsection.

3.1.5.1 Automated Quasi-Static IV-Characterization

The *B1500A Semiconductor Parameter Analyzer* from Agilent Technologies was used for the quasi-static characterization during this research work. Quasi-static in the context of ReRAM measurements means that the applied voltage or current sweeps have a slow ramp rate to ensure that parasitic capacitances are loaded. This is necessary in order to suppress the impact of capacitive effects and RC times on the memory element. The semiconductor parameter analyzer offers four source-measurement units (SMUs), which are required for the characterization of integrated MOSFET and ReRAM devices where, in contrast to standard two-terminal ReRAM devices, at least 3 electrodes need to be electrically contacted. The input impedance for voltage measurements is lager than 1 TΩ [71]. Two SMUs in the system are high resolution SMUs capable of detecting currents down to 1 fA and voltages as low as 0.5 µV. They are connected to the probe holders via triaxial cables. These SMUs have limited output capabilities of 100 V or 100 mA with a powerlimit of 2 W. The two other SMUs offer the higher output of 200 V and 1 A with a power limit of 20 W and are therefore referred to as high power SMUs. The Agilent B1500A SMUs are capable of relatively slow voltage pulse measurements with a minimum pulse width of 100 ms. The quasi-static measurements were the method of choice to determine the figures of merit like forming, set and reset voltages as well as the corresponding currents. Also the measurements of the electromotive force in ReRAM cells were performed with the Agilent B1500A. Further details regarding the quasi-static measurement system can be found

in [39].

In order to test the device to device variability of the switching characteristics like the forming voltages, a large number of devices has to be measured. Hence, the Agilent B1500A is connected to a semi-automatic probe station. The SUESS Microtec PA-200 (see Fig. 3.10) has a thermal wafer chuck, enabling temperature dependent measurements from room temperature up to 200 °C. The samples are placed on the chuck that steps through a predefined grid. This is done by lowering the chuck to separate the probe tips from the sample surface, moving to the next position and raising the chuck again to bring the probe tips back into contact with the pad structures.

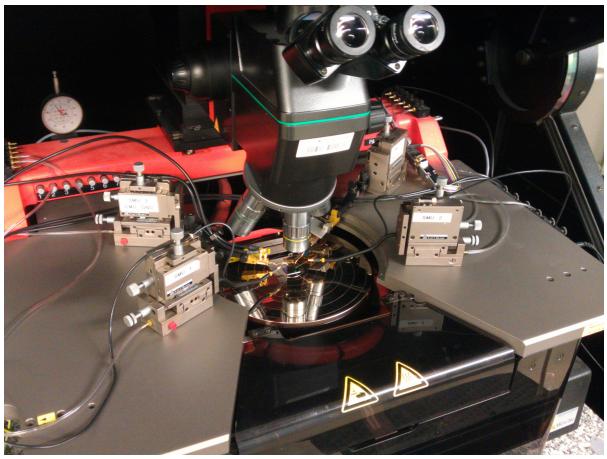


Figure 3.10: Semi-automatic probe station SUESS Microtec PA-200 with 4 probe holders. The position of the probe tips is fixed by micro-manipulators while the sample position can be changed by the movable chuck.

3.1.5.2 Voltage Pulse Measurement Setup

Next generation memory elements do not only have to be non-volatile, maintaining the written state for at least 10 years, but also the capability of switching by means of short voltage pulses in the regime of 100 ns or shorter has to be proven [72]. The pulse switching experiments in the scope of this work were primarily performed with a specialized fast pulse measurement setup (Fig. 3.11) developed by Rösgen and Hermes [42, 73]. In this setup, the voltage

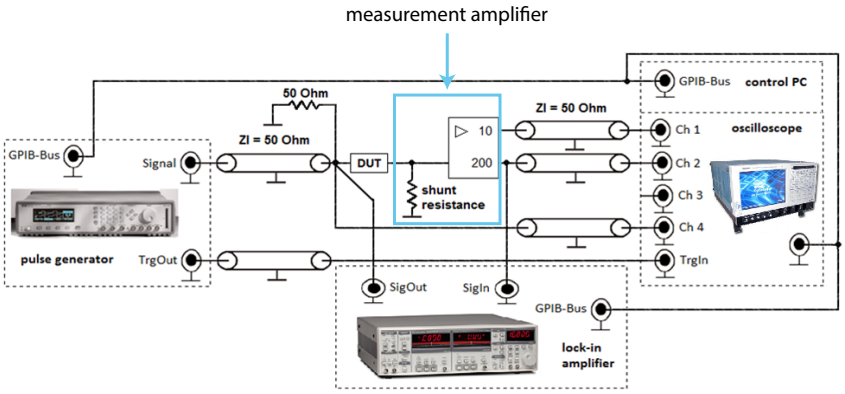


Figure 3.11: Schematics of the measurement setup. Taken from [42]

pulse signals are sourced by an Agilent 81110A 165 MHz pulse pattern generator. This generator is capable of delivering voltage pulses with a width of 3 ns up to 999.5 s with rise and fall times of down to 2 ns. The available voltage amplitudes of ±100 mV up to ±10 V are well suited for the resistive switching applications. The resistance state of the memory elements can be determined before and after applying a voltage pulse by a Stanford Research SR830 lock-in amplifier with a sinusoidal signal (described by Bruns *et al.* [74]) generating a voltage drop of 26.5 mV over the cell.

For the measurement of the transient current response of the memory el-

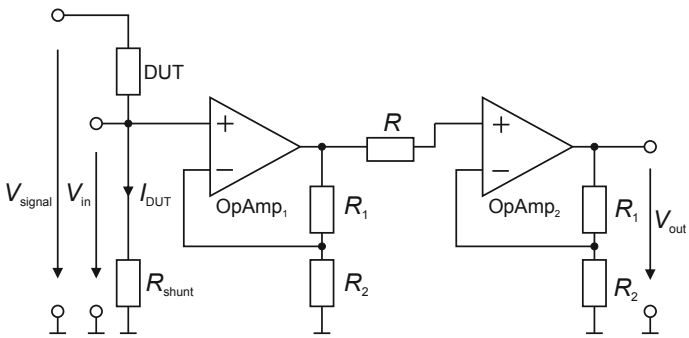


Figure 3.12: Simplified circuitry of the two-stage non-inverting amplifier

ements, a self build measurement amplifier was used. A simplified circuit diagram is depicted in Figure 3.12. The current I_{DUT} through the device under test (DUT) causes a voltage drop over a shunt resistor (50 Ω). It must be noted that the shunt resistor should have a reasonable small resistance so that it does not affect the measurement. The voltage signal fed to the two-stage non-inverting is defined as:

$$V_{\mathrm{in}} = I_{\mathrm{DUT}} \cdot R_{\mathrm{shunt}} \tag{3.10}$$

The closed loop gain of the two stages is calculated to:

$$G_{1/2} = 1 + \frac{R_1}{R_2} \tag{3.11}$$

This results in the total output voltage of

$$V_{\mathrm{out}} = V_{\mathrm{in}} \cdot G_1 \cdot G_2 \tag{3.12}$$

$$= I_{\mathrm{DUT}} \cdot R_{\mathrm{shunt}} \cdot \left(1 + \frac{R_1}{R_2}\right)^2 \tag{3.13}$$

The measurement of this output voltage is performed by a Tektronix TDS6804b oscilloscope with a maximum sample rate of 20 GSample/s for 4 channels. The bandwidth of this tool is 8 GHz with an input range of ±100 mV to ±5 V. In summery this setup is capable of measuring currents responses as low as 2 µA during the 5 ns voltage pulses. This is suitable to detect the currents during write pulses. However, there is a tradeoff between the achievable bandwidth and the possible current resolution. Since the system is designed for maximum bandwidth, the current resolution is limited and the detection of currents in the nA range is impossible. Therefore, determining the resistance of memory elements in the OFF state with read voltage pulses is not possible. This impedes endurance measurements where the readout of the state with the lock-in amplifier is to slow. For further information on the development of the amplifier as well as its characteristics the reader is referred the works of Hermes and Rösgen [42, 73].

The most versatile measurement system used for this work is the *Model 4200-SCS Semiconductor Characterization System* from Keithley Instruments [75]. It is equipped with 4 medium power SMUs for quasi-static measurements where

the focus is on the precision of the current and voltage measurements. The performance of the 4200-SCS SMUs is comparable to the B1500A's SMUs. They have a maximum output voltage of 210 V and a maximum current of 100 mA with a power limitation of 2 W. The shunt resistance is specified to be $> 10^{12}$ Ω. The current and voltage measurement resolutions amount to 100 fA and 1 μV respectively. In addition to the quasi-static measurement capabilities, the 4200-SCS offers the measurement of transient currents with the two installed Pulse Measurement Units (PMU). Each PMU has two channels for sourcing of voltage pulses with a minimum duration of 60 ns with simultaneous current measurement. The main advantage of this system in comparison with the B1500A and the described self-built setup for the fast pulse measurements is that it combines quasi-static and fast pulse measurements. This is achieved by the systems 4225-RPM remote amplifier/switch. First of all, the remote amplifier can be placed in close vicinity of the sample which shortens the wire length and provides an extended measurement range for transient currents shown in Table 3.3. Since the RPM also acts as a switch, quasi-static measurements with the SMUs and pulse measurements with the PMUs can be carried out without rewiring or movement of the sample. Therefore, the system is capable of performing fast endurance measurements.

Current measurement range:	**100** nA	**1** μA	**10** μA	**100** μA	**1** mA	**10** mA
Recommended minimum pulse width	134 μs	20.4 μs	8.36 μs	1.04 μs	370 ns	160 ns
Recommended minimum measure window	10 μs	1.64 μs	1 μs	130 ns	40 ns	20 ns
Recommended minimum transition time (10 to 90%)	1 μs	360 ns	360 ns	40 ns	30 ns	20 ns
Settling time	100 μs	15 μs	6 μs	750 ns	250 ns	100 ns

Table 3.3: Keithley 4200-SCS measurement timing with Model 4225-RPM [75]

3.2 Nano-Crossbar Device Fabrication

The integration of the redox-based resistive switching memory elements into passive crossbars offers the prospect of achieving the smallest possible footprint of the memory devices of $4F^2$. Research technology platforms for this integration have been developed in the work of Nauenheim [39], who focused on the array fabrication by e-beam lithography and lift-off metallization. The UV-nanoimprint patterning developed by Meier [63] offers the advantage of parallel fabrication which is highly efficient in reducing the e-beam writing time. Subsequently, Rosezin changed the patterning process of the imprint stamps which he explained by reliability issues regarding the fabrication [31]. The minimum reproducible feature size of electrically functional devices in the mentioned works was limited to 100 nm x 100 nm. However, the shrinking of the device dimensions is highly demanded to prove the scaling potential of the ReRAM devices. Furthermore the impact of device sizes on the resistive switching characteristics has to be analyzed. The improvement of the processes to scale the fabricated electrodes is comparable to a new development. The development of the imprint process including the mold fabrication and the pattern transfer as well as the e-beam lithography for top electrode patterning is described in this section.

3.2.1 Development of the Imprint Mold

One key to obtain smaller device sizes with the nanoimprint lithography is the mold fabrication process. This fabrication process is based on the patterning by the electron beam lithography and dry etching techniques. The e-beam lithography is utilized to define the structures in a resist on the stamp. These nano-structures are later transferred into the mold by means of ion beam etching and reactive ion beam etching. The schematic processing scheme of the UV-nanoimprint stamps is shown in Figure 3.13.

The fabrication process starts with a quartz wafer with a diameter of 100 mm. The used quartz substrates from Plan Optik AG with a thickness of 525 ± 25 µm have a transmission of 92% for the desired UV light wavelength. They are double side polished and have an average roughness of 0.5 nm. As a first step, a 15-nm-thick chromium layer is deposited on the wafer by electron

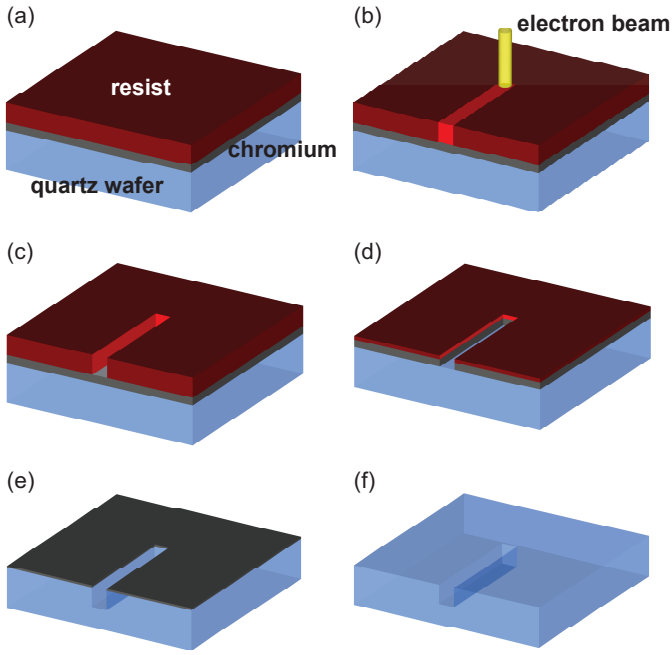


Figure 3.13: Processing scheme of the UV-nanoimprint mold. (a) Deposition of the Cr layer and spin coating of the PMMA resist on a quartz wafer. (b) E-beam exposure. (c) Development of the written pattern. (d) Structuring of the Cr layer by Ar plasma etching. (e) Reactive ion beam etching with CF_4 into the substrate. (f) Wet chemical removal of the remaining Cr.

beam evaporation (Fig. 3.13(a)). The reason for using the chromium layer is threefold:

1. The metal layer serves as a conductor to remove the impinging electrons during the e-beam writing. This prevents charge up of the insulating substrate that would deflect electrons and make the writing of fine structures impossible.

2. In the utilized EBPG5000, the focus height is measured by a laser beam. Therefore, an opaque material like the chromium layer is required.

3. The chromium layer acts as a hard mask in subsequent patterning by dry etching.

Next, the PMMA (AR-P 679.02, 950K, 2% solid matter from ALLRESIST GmbH) is spun on the wafer at 3000 rpm for 60 s. This results in a 80-nm-thick resist [76]. The reduced resist film thickness enables smaller structures because of the lower aspect ratios. The high molecular weight resist was chosen because it offers higher contrast [77]. The used material stack is on the contrary to the layer sequence proposed in [31] where the chromium layer is located on top of the PMMA resist. This is necessary to fulfill the demand for smaller structure sizes. As described in section 3.1.2.2, the interaction between the electrons and solid matter during the e-beam lithography causes a broadening of the beam and limits the patterning resolution. To compare the two layer stacks with respect to the beam broadening, a simulation with the *sceleton - scattering of electrons in matter* software was carried out. The results are shown in Figure 3.14. The trace of 10^7 electrons with an injection

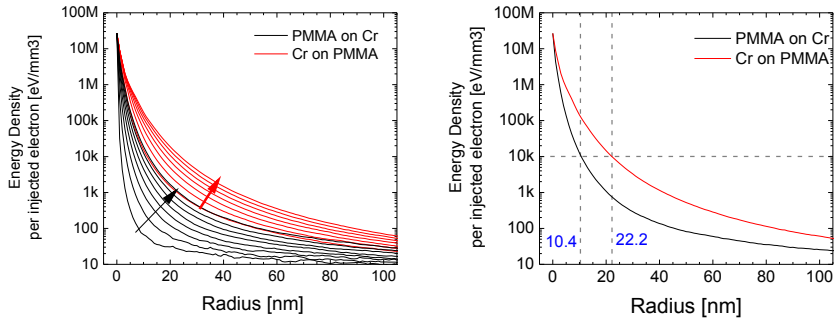


Figure 3.14: Simulation of scattering effects during e-beam writing. (a) Simulation results of the two layer stacks for different penetration depth. The depth increases in direction of the arrows in 10 nm steps. Panel (b) compares the extracted energy densities at a penetration depth of 60 nm in the resist. The layer sequence with the Cr on top of the PMMA resist results in a 113 % larger beam broadening.

energy of 50 keV was calculated. The energy density at a given radius from the point of injection is a decisive factor to determine the solubility of the resist during development. An identical quartz layer representing the wafer material was chosen as bottom layer for both simulations. The black lines in Figure 3.14 represent the layer sequence of 15-nm-thick Cr on the quartz followed by

the 80-nm-thick PMMA resist. The reversed layer sequence is shown in red. It should be noted that the 15-nm-thick Cr on top of the PMMA will produce lesser scattering than the 50-nm-thick, used by Rosezin. The layer sequence of PMMA/Cr reduces the electron scattering by a factor of two shown in Figure 3.14. The focus height measurement issues during the e-beam writing encountered by Rosezin have not been observed in this work. However, it was crucial to ensure stable electrical contact to the chrome layer. Therefore, the area of the wafer where it was clamped during the e-beam writing was covered by adhesive tape during spin coating. This ensures the resist-free conducting surface.

The next fabrication step is the exposure by the electron beam (Fig. 3.13(b)). The suitable dose of 600 $\mu C/cm^2$ for the nano-structures was determined by dose tests. The micro-structures and contact pads require a smaller dose of 240 $\mu C/cm^2$. After the exposure, the development in the AR 600-55 developer from ALLRESIST GmbH for 75 s was performed.

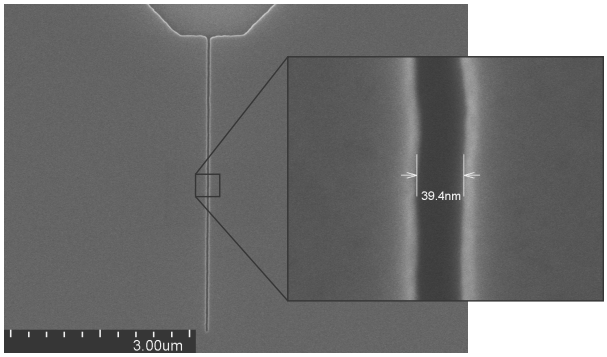


Figure 3.15: SEM image of a designed 20 nm line in the mold. The image was taken before the removal of the Cr layer.

The information contained in the resist was then transferred into the stamp by a two step etch process. First, the Cr layer was physically etched with an Ar ion beam for 3 minutes (Fig. 3.13(d)). The selectivity between Cr (6 nm/min) and PMMA (21 nm/min) in this process determines the minimum thickness of the PMMA for reliable patterning of the Cr layer. The patterned Cr film was afterwards used as a hard mask to etch into the quartz (SiO_2) with a CF_4

RIBE step of 2 minutes (Fig. 3.13(e)). The selectivity of the SiO_2 to the Cr is approximately 15 which enables an etch depth of at least 150 nm in the mold. The smallest line in the mold has a width of 40 nm (Fig. 3.15). Finally, the remaining Cr is removed by a wet chemical etch process (Fig. 3.13(f)).
After the imprint process, the mold has to be separated from the substrate (demolding) by mechanical forces. In this process, the resist patterns will be destroyed or peeled-off from the substrate, if the sticking force between the resist and the quartz mold is stronger than the resist strength or the adhesion to the substrate. The reduction of the separation force is achieved by the application of a self-assembled monolayer (SAM) often referred to as mold releasing layer or anti-adhesion layer. The most commonly used materials in combination with SiO_2 stamps are fluorinated silanes [78–80]. In the Forschungszentrum Jülich the SAM treatment was introduced by Schwaab, Gilles and Meier [61, 65,81,82]. In this work trichloro(1H,1H,2H,2H-perfluorooctyl)-silane molecules from ABCR as shown in Figure 3.16 were used.

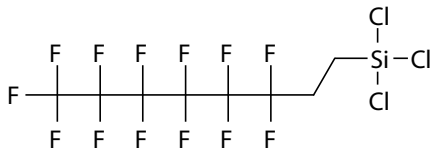


Figure 3.16: Schematic of the trichloro(1H,1H,2H,2H-perfluorooctyl)-silane molecule used for the anti-adhesion treatment of the UV-nanoimrint mold.

Before the SAM treatment was carried out, the mold was cleaned in piranha etch solution for 10 minutes followed by an oxygen plasma cleaning (300 W for 10 minutes). This activates the surface of the mold by creating -OH termination on the silicon oxide. Afterwards, the wafer was placed in a desiccator inside a glove-box (Fig. 3.17) for the vapor deposition of the silane. 200 μl of the liquid silane solution were poured into a petri-dish located next to the mold. Then, the desiccator was evacuated to a pressure of 45 mbar and kept at this pressure for one hour to perform the silanization. The silane molecules link covalently to surface exposed silanol groups so that a self-assembled monolayer of hydrophobic silane was formed. The detailed chemical and physical processes during the silanization are described in [82].

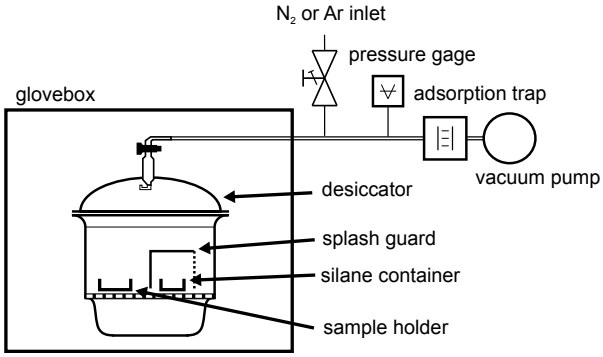
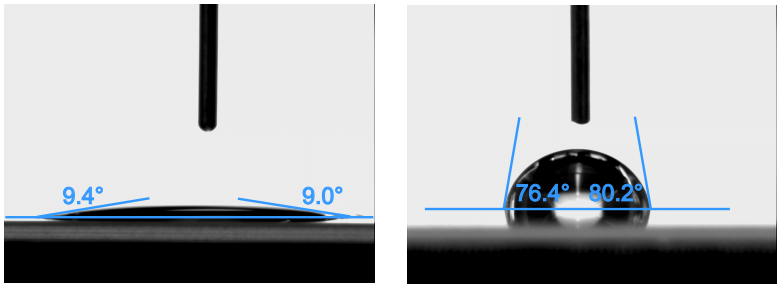


Figure 3.17: Setup for vapor deposition of silane. Redrawn from [81]

A method to estimate the surface properties like the wettability is the contact angle measurement. A smaller contact angle (<20°) between the oxide surface and the water drop represents the hydrophilic surface of the oxide. The contact angle of the mold after the activation of the surface was measured to be <10° (Fig. 3.18(a)). This represents a very clean SiO_2 surface. The contact angle after silanization amounted to approximately 115° which is considered to be a high quality hydrophobic surface.



(a) (b)

Figure 3.18: Water contact angles: (a) Quartz wafer before silane treatment. (b) Imprint mold after approximately 20 imprints.

A degradation of the anti-adhesion layer was observed after more than 20 imprints as revealed by the contact angle measurement (Fig. 3.18(b)). This phenomena can be explained by a loss of fluorine as shown by Houle [83]. How-

ever, the anti-adhesion properties were still good enough to have a successful demolding.

In order to check the shape and the depth of the structures in the UV-nanoimprint mold a cross-sectional SEM investigation was performed with H. Bochem from the PGI-8 Bioelectronics at the Forschungszentrum Jülich. Since the quartz wafer cannot be broken in a controlled way, a focused ion beam (FIB) preparation was necessary. This was done with the FEI Helios NanoLab 600 which offers Ga^+ ion milling and high resolution SEM imaging. The sample preparation as well as the imaged trenches in the mold are shown in Figure 3.19. During the preparation a Pt layer was deposited on the sample to avoid damage from the Ga^+ ions (Fig. 3.19(a)). Then, a cavity was milled into the mold. Subsequent polishing steps were performed to reveal the areas of interest (Fig. 3.19(c),(e)). The SEM inspection proves that the cavities in the mold have a homogeneous depth of approx. 150 nm (Fig. 3.19(d),(f)) for both the micro-structures as well as the nano-structures. This is in good agreement with the determined etch-rate of 50 nm/min with CF_4 and the etch duration of 3 minutes for this mold. The inspection proves, that a successful execution of nanoimprints with enough resist thickness to pattern metal layers is possible with this stamp.

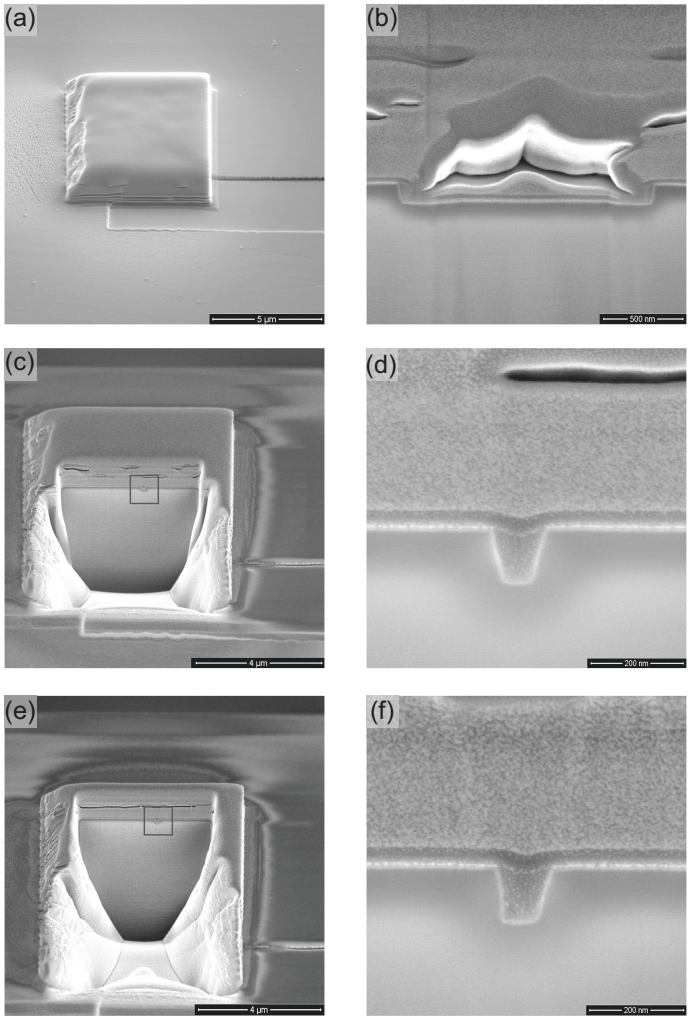


Figure 3.19: Focused ion beam preparation of the imprint mold to determine the structure depth of an 80 nm single line at different positions. (a) A platinum blanket is deposited to protect the structure during Ga^+ ion milling. (b) The depth of the micro-structure amounts to 148 nm. (c),(e) Further polishing by the ion beam along the nano-structure is performed. (d),(f) A uniform depth of the nano-structure of 146 nm is measured.

3.2.1.1 Mask Design

In this work a new design for the imprint stamp as well as the mask for the e-beam patterning of the top electrodes and the corresponding optical mask for the pad opening process was developed. In order to perform studies on the impact of the deposition parameters of the oxide layers on the resistive switching behavior of the memory elements a large amount of samples is generally required. On these samples mostly single nano-crossbar devices are demanded. The designed mask has a reduced die size of 2 cm x 2 cm which results in an improved yield of 12 samples per imprinted wafer in comparison with 6 1 x 1 inch^2 samples in the work of Meier [63].
The CAD mask of a single die is shown in Figure 3.20 on page 50. The mask consist of 72 blocks, 12 in x-direction and 6 in y-direction that are denoted on their top left corner (green numbers in Fig. 3.20). Each block contains 25 electrodes that are organized in columns. The structures of each of the columns have the same lateral size starting form 100 nm in the very left column and reaching down to 20 nm the the right column in steps of 20 nm. This enables cell size dependent measurements of the electrical properties on every area of the sample to detect possible inhomogeneities of the oxide deposition methods. The 360 devices of each size are sufficient to acquire enough measurement data to perform statistical analysis.
Besides the structures for nano-crossbar memory elements, the mask contains 4-point measurement devices of different line width to check the resistance of the fabricated lines. This becomes especially interesting to evaluate the impact of the electrode resistance on the ReRAM element if alternative bottom electrode materials are used or if the thickness of the Pt layer is shrunken.

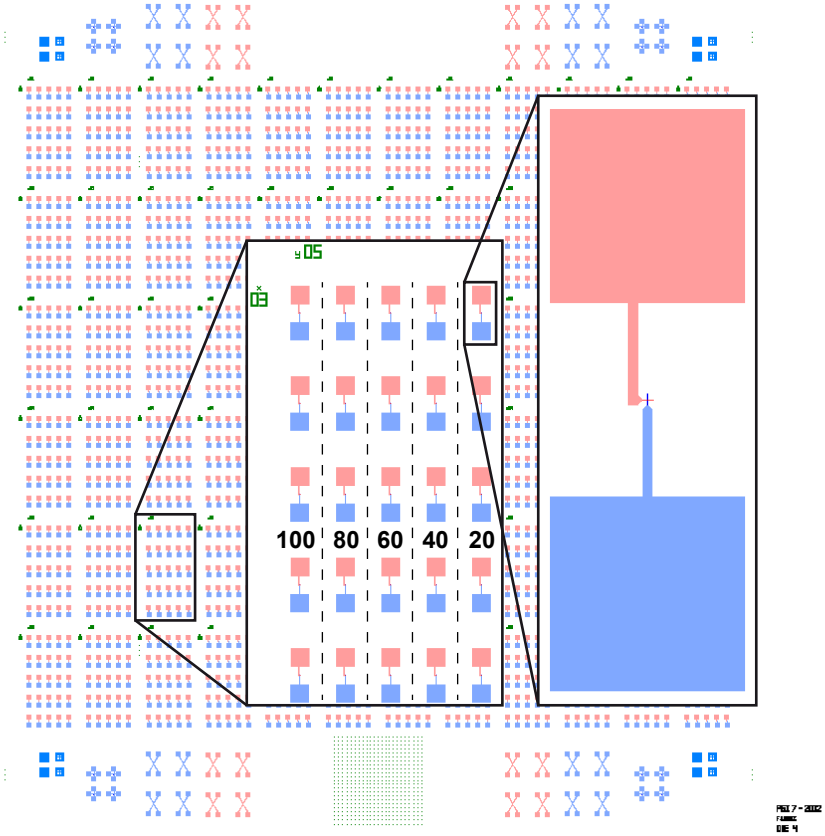


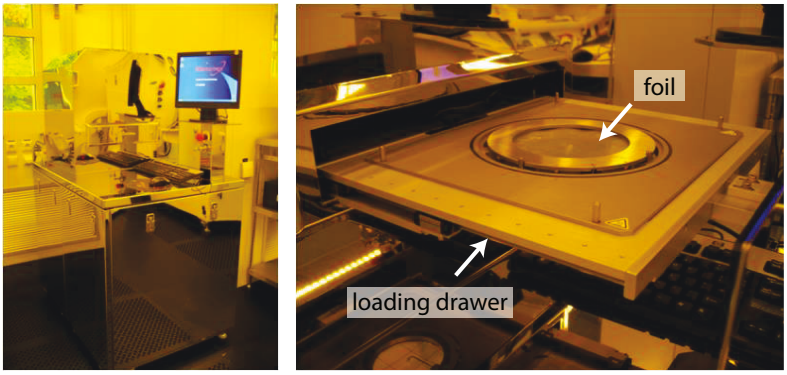
Figure 3.20: Mask design of the 2 cm x 2 cm nano-crossbar sample. The blue structures are contained in the imprint mold for the bottom electrodes while the red structures belong to the e-beam mask for top electrode patterning. The sizes in nm of the nano-structures for each column are denoted in black.

3.2.2 Pattern Transfer

The pattern transfer in the UV-nanoimprint lithography can be divided into two processes. The nanoimprint, which casts the information of the stamp into the resist and the etching process to transfer the resist pattern into the functional layer. Both processes will be dealt with in this subsection.

3.2.2.1 UV-Nanoimprint Process

The imprints in this work were carried out with the NX2000 nanoimprint tool from Nanonex (Fig. 3.21). This machine is capable of performing temperature NIL as well as UV NIL. However, only the UV light based nanoimprint lithography has been performed in this work. Wafers with a diameter of up to 100 mm can be imprinted with the NX2000. The system employs the air-



(a) (b)

Figure 3.21: (a) The Nanonex NX2000 nanoimprint tool. (b) Up to 4 inch wafers can be placed between 2 foils in the loading drawer. [63]

cushion technique to apply the maximum pressures of 550 psi [84]. In the air-cushion technique, depicted in Figure 3.22, the mold is placed on top of the spin-coated wafer between two transparent foils. After the wafer has been transferred into the imprinter with the sample drawer, the process chamber is closed by air pressure. A vacuum is applied to remove any remaining air between the two foils and also between the mold and the wafer (Fig. 3.22(a)). Next, air pressure is introduced in the chamber to perform the molding. The main advantage of the air-cushion technique in comparison with conventional

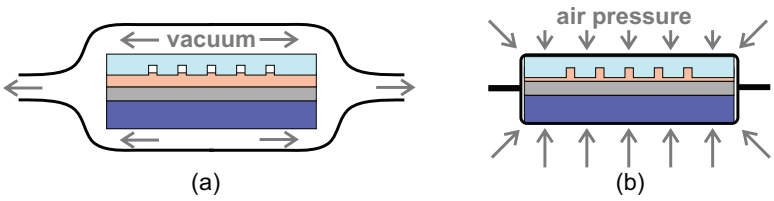


Figure 3.22: The air-cushion press employed in the NX2000 imprinter. (a) The chamber is evacuated before (b) air pressure is introduced to perform the nanoimprint process. [84]

parallel plate pressure systems is the uniformity of the press. This is especially important to achieve homogenous residual layer thicknesses. It was experienced in this work that a high imprint pressure of 500 psi did reduce the size and number of defects. The pressure and temperature conditions that produced the best NIL results are shown in Figure 3.23. First the pre-imprint

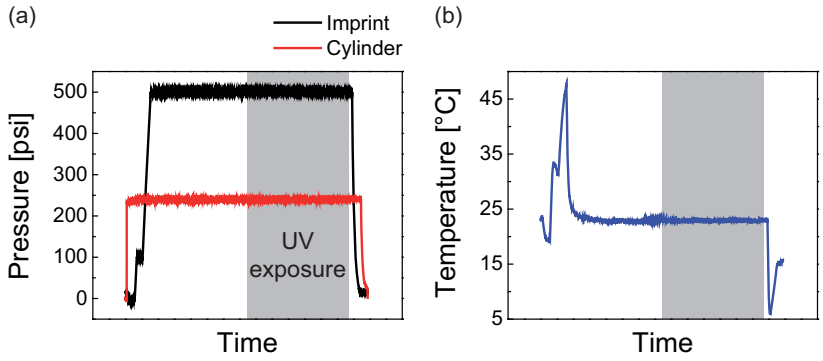
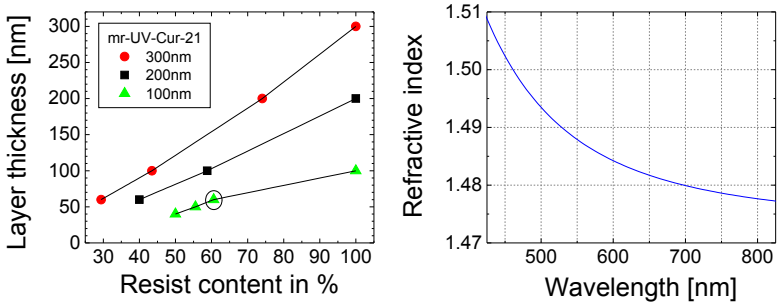


Figure 3.23: (a) Pressure and (b) temperature conditions of the UV-nanoimprint process.

pressure of 100 psi is applied for 20 s. Afterwards, the full pressure of 500 psi is applied. This is followed by a waiting time of 5 minutes to give the resist enough time to flow into the cavities of the mold and for the resin to absorb any air trapped in the cavities [85]. Then, the resist is cured by UV light exposure for 4 minutes. The temperature changes in the system that can be observed in Figure 3.23(b) are caused by the adiabatic change of the pressure

and not by an external heating or cooling.

The established NXR-2010 resist from Nanonex is not sold anymore and therefore the UV-nanoimprint resist *mr-UVCur21* from micro resist technology GmbH was chosen. Several publications have shown that this resist can be applied for single digit nano-fabrication [86–88]. It offers several advantages in comparison with the nanonex resist. In fact, it has the longer shelf life, can be stored at room temperature and does not require an adhesion promoter for spin coating on Pt. In addition, the resist does not contain any inorganic components like silicon and can be removed by an oxygen plasma treatment after the patterning processes.



(a) (b)

Figure 3.24: Properties of the mr-UVCur21 resist: (a) Film thickness dependence of the resist for different dilutions spun at 3000 rpm. (b) Refractive index after softbake. [89]

Tuning the resist thickness is necessary to achieve sufficiently thin residual layers for a successful break-through etch after imprinting. This can either be done by changing the spin-rate during coating or by dilution of the resist. The resulting resist thickness for different resist dilutions spin-coated at 3000 rpm for 60 s is shown in Figure 3.24(a). The ratio of 8:5 of the mr-UVCur21 to the diluent mr-T 1070 results in a resist thickness of 60 nm after the softbake at 80°C for 60 s. This resist thickness was measured by ellipsometry. The required refractive index n of the resist is given by equation 3.14 and shown in

Figure 3.24 (b) [89].

$$n(\lambda) = 10^3 \cdot n_0 + 10^2 \cdot n_1/\lambda^2 + 10^7 \cdot n_2/\lambda^4 \quad (3.14)$$
$$\text{with: } n_0 = 1473;\ n_1 = 16;\ n_2 = 88$$

The residual resist layer thickness after the UV NIL is almost equal to the initial resist thickness because only a small fraction of the total area of the mold contains cavities that have to be filled by the resist. Also the residual layer does show high homogeneity because of the regular placement of the structures and the high imprint pressure. In conclusion, the employed UV NIL resist in combination with the imprint process are suitable to fabricate sub 100 nm structures.

3.2.2.2 Development of the Etch-Processes

The pattern transfer of the molded structures in the resist is a two steps process as described in the subsection 3.1.2.3:

1. Break-through etch of the residual layer.
2. Sputter etching of the metal layer.

The residual layer remaining in the recessed areas of the polymer film after the imprint is recommended to be removed by oxygen reactive ion etching (RIE) in order to open the window to the substrate. In this work, reactive ion beam etching (RIBE) was applied since it offers higher anisotropy which in turn results in lower trimming of the resist flanks. In general, the wafer was positioned perpendicular to the ion beam and rotated at 10 rpm during the etching. The backside cooling ensured stable temperatures of 15°C. With the standard parameters of V_B = 450 V, V_A = 187 V and I_B = 125 mA the etch rates of the mr-UVCur21 resist were estimated to be:

Process Gas	Ar	CF_4	O_2
Etch rate [nm/min]	14	42	103

Table 3.4: Etch rates of the mr-UVCur21 resist for different process gases.

The mr-UVCur21 showed a good etch resistance against the Ar^+ ion beam which is necessary to transfer patterns into metal layers. However, the etch resistance of the mr-UVCur21 against the O_2 ion beam with standard parameters is comparably small and therefore a high etch rate of 103 nm/minute is observed. This high etch rate makes the process control difficult.A short exposure to the O_2 ion beam can reduce the resist structure height significantly. To prevent this issue, etch tests with different ion beam currents were carried out to tune the etch rate (Fig. 3.25).

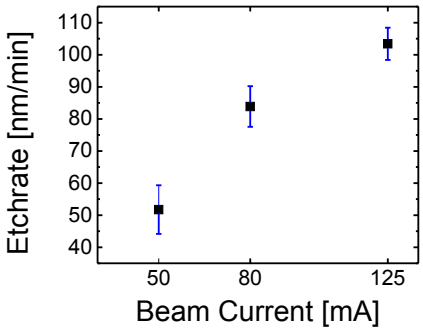


Figure 3.25: Etch rate of the mr-UVCur21 resist with O_2 as a function of the ion beam current

It can be concluded from the experiments that the reduction of the ion beam current from 125 mA to 50 mA lowers the etch rate by a factor of two. This is explained by the smaller amount of impinging ions on the wafer surface. An etching time of 65 seconds was sufficient to reliably remove the residual layer (55 nm) without damaging the pattern in the resist.
The second step in the pattern transfer process is the Ar^+ ion beam etching of the Pt film. The patterning process of Pt is known to be challenging because Pt does not react with the available process gases like Ar, CF_4, O_2 and SF_6 during plasma etching [90,91]. Therefore, the sputtered material is nonvolatile and tends to redeposit on the flanks of the resist mask as shown in Figure 3.26. This parasitic process is called *fencing*. The fences at the edges of the metal structures need special consideration because they can lead to short circuits between the bottom and the top electrode in the MIM device rendering the memory element useless. Meier proposed an Ar^+ RIBE step under a flat angle

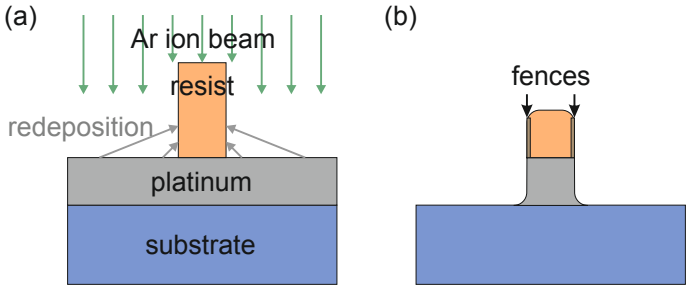
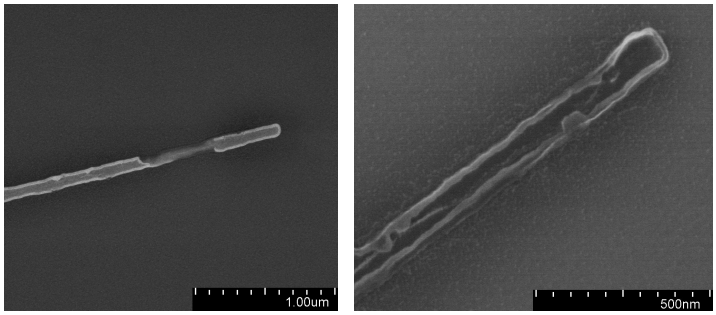


Figure 3.26: Fencing during the Ar^+ ion beam etching of Pt: (a) The removed Pt is redeposited on the resist flanks. (b) Parasitic protrusions at the edges of the metal structures remain after the etch process.

between the wafer and the ion beam of 10° for 30 seconds to reduce the fencing [63]. During this fence removal etch the wafer was rotated at 10 rpm to have homogeneous etching of the redeposited material. The proposed fence removal step was applied to the structures created with the mr-UVCur21 resist and the new mold design but did not solve the fencing issues. Even extending the etching time to 90 seconds did not remove the fences.

Two alternative methods for the fence removal were investigated in this work. First, a wet chemical etching step with *aqua regia* after the resist stripping has been tested. Aqua regia is a mixture of concentrated nitric acid and hydrochloric acid with a volume ratio of 1:3 (HNO_3 + 3 HCl). It is known to dissolve noble metals like gold and platinum [92]. Since the thin fences are standing free, they have a large surface in comparison with their volume. Therefore, the fences (Fig. 3.27(a)) should be etched a lot faster than the electrodes. The etch tests were carried out at room temperature and at 80°C. For short etch durations of 10 s and 60 s for both temperatures no effect on the fences or the electrodes could be observed. The SEM image after an etch duration of 10 minutes at 80° is shown in Figure 3.27(b). The SEM image demonstrates that the platinum electrode has been completely removed by the etch process but only the fences remain. This could be explained by the high energy of the Ar sputter process that can lead to a mixture of the resist and the Pt at the resist flank. In this case the Pt would be passivated by the resist and not get attacked by the HNO_3 + 3 HCl solution. Anyways, the wet chemically aqua

regia etching turned out to be not suitable for the fence removal.



(a) (b)

Figure 3.27: Fence removal by aqua regia etching: (a) The bright contrast at the edges of the Pt nano-structures before the aqua regia etching is attributed to the fences. (b) After the 10 min aqua regia wet etching at 80°C the Pt is completely removed but the fences remain

Second, dry etching for the fence removal with reactive gases has been examined. This offers a physical as well as a chemical component to remove the material mix that the fences presumably consist of. The CF_4 reactive ion beam process with standard beam parameters was employed. The angle between the sample surface and the ion beam was configured to be 45° in order to affect not only the fences that are still standing but also the ones that have collapsed on the surface of the electrode. The sample was rotated at 10 rpm during the fence removal.

The SEM image of the 25-nm-thick nano-electrode (40 nm lateral size) before the RIBE process is shown in Figure 3.28. Especially at the nano-structure but also on the micro-structure a thin bright line at the edges of the structure indicates fencing. In the SEM image of the same structure after the 25 s long etch step the fences are completely removed (Fig. 3.29). It is here worth mentioning that longer etching generally removes the bottom Ti adhesion layer especially underneath the smaller structures (<40 nm). This results a deformation in the structures.

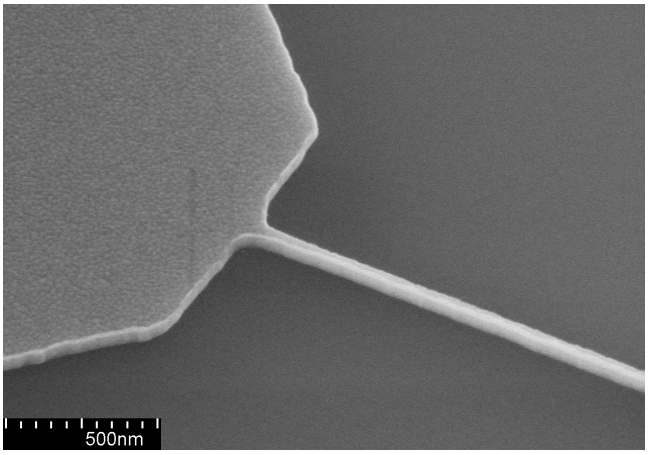


Figure 3.28: The 40 nm Pt electrode exhibits fencing before the CF_4 RIBE treatment

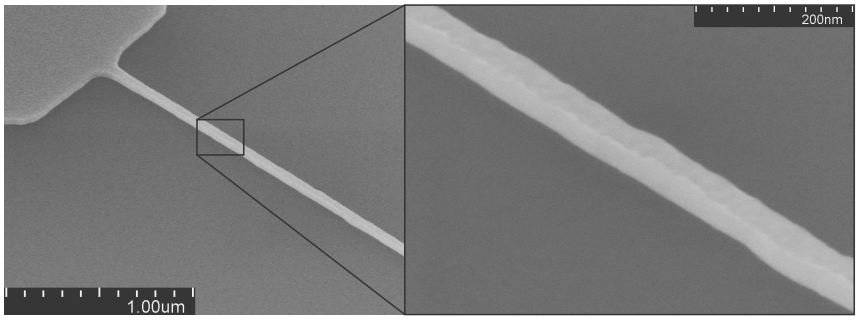


Figure 3.29: The CF_4 RIBE treatment has successfully removed the fences

The process flow for the fabrication of the Pt bottom electrodes by UV NIL can be summarized as follows:

1. Sputter deposition of Ti/Pt on an oxidized 100 mm silicon wafer.
2. Cleaning of the wafer by O_2 plasma for 10 minutes at 300 W.
3. Spin-coating of the of the mr-UVCur21 resist at 3000 rpm for 60 s.
4. UV nanoimprint.
5. Break-through etch with the developed O_2 RIBE process.
6. Patterning of the Ti/Pt layer by Ar sputtering in the RIBE tool.
7. Fence-removal with the CF_4 RIBE process with an angle of 45°.

The photograph of the wafer after the completed nano-patterning process is shown in Figure 3.30. Afterwards, the wafer is diced into 12 dies for further processing.

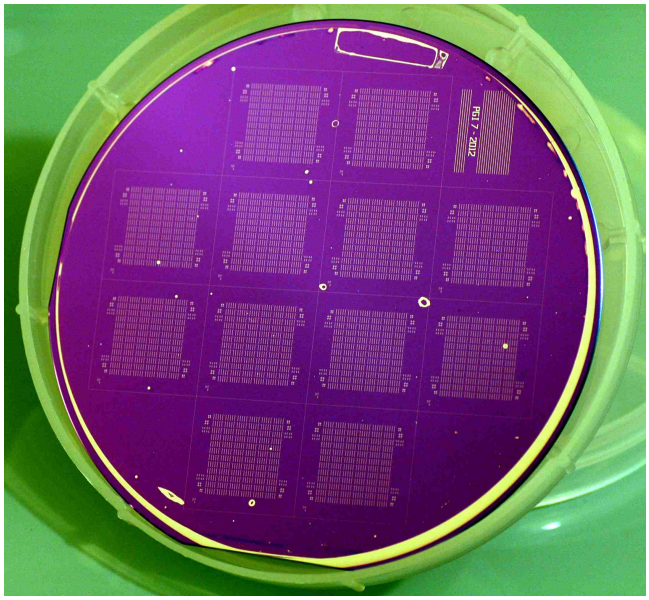


Figure 3.30: Imprinted 100 mm wafer after completed patterning processes

3.2.2.3 Electrical Characteristics of the Nano-Electrodes

The fabricated metal lines with thicknesses and lateral sizes in the nanometer regime were electrically characterized to evaluate their suitability for the application as electrodes in the resistive switching MIM structures. In order to perform the high precision resistance measurements, four-point structures were integrated in the design. Figure 3.31 shows the SEM image of the smallest reproducibly fabricated nano-structure with a with of 23 nm ± 2 nm. These bridge-like structures have proven to enable reliable resistance measurements on metal lines [93]. The used four-point measurement setup with the CAD

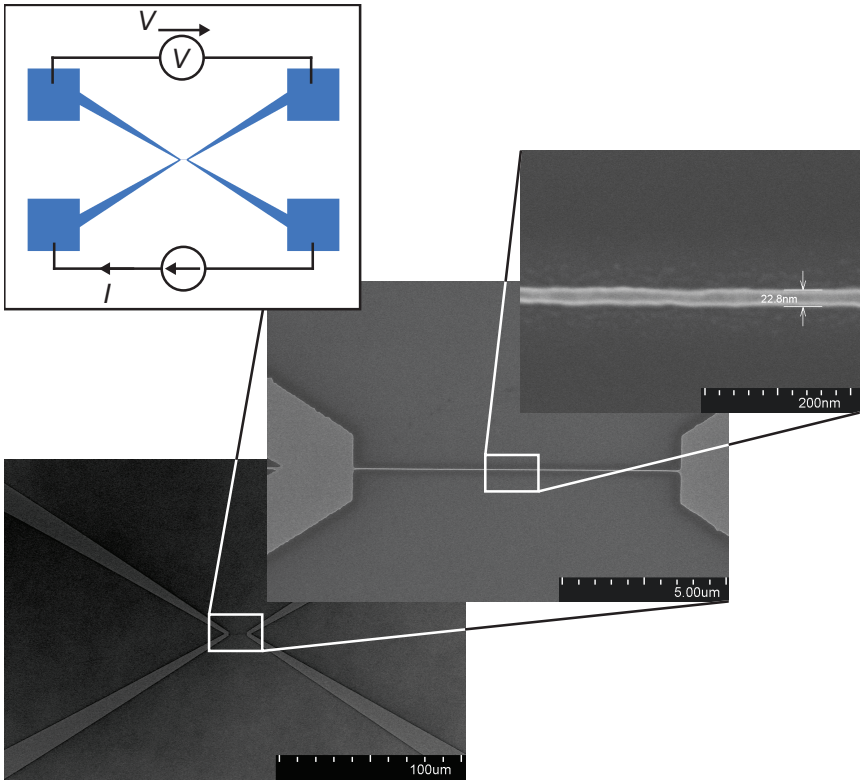


Figure 3.31: SEM micrograph of a 23 nm wide Pt line in a four-point configuration for the determination of the sheet resistance. The CAD design of the four-point structure with the measurement circuit are shown in the inset.

mask are illustrated in the inset of Figure 3.31. Two contacts are utilized

as supply lines to force a current sweep starting at 0 A and increasing up to 20 µA through the 10 µm long nano-electrode. The other two contacts are used as sense contacts where the voltmeter is connected to. Because of the high input impedance of the used parameter analyzer almost no current flows into the measurement system and therefore no voltage drop occurs in the sense lines. This enables the differentiation of the resistance contribution of the nano-structure and the micro-structure feed lines. For the current range below 20 µA the resistance of the nano-structures was constant. Above this current level the resistance increased, which can be attributed to Joule heating (also called self-heating) of the metal line. The results shown in Figure 3.32 were measured on devices structured by UV-NIL from a 5 Ti / 15 nm Pt film. The characterized lines had a width of 20 nm, 60 nm and 100 nm in the design.

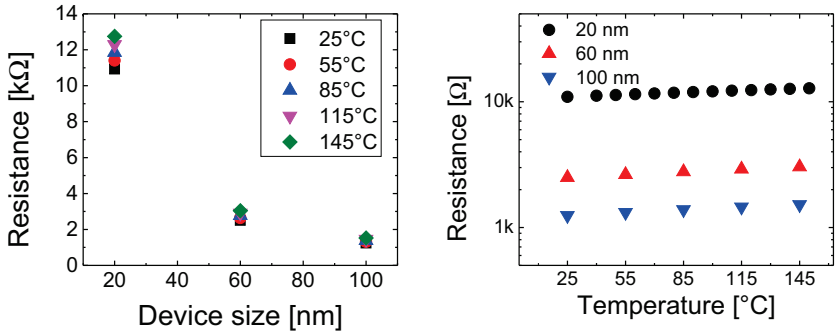


Figure 3.32: Size and temperature dependence of the resistance of the patterned 15-nm-thick Pt nano-structures

The measured resistances do not follow the linear dependency on the wire width as expected from an ohmic resistor as given by equation 3.15:

$$R = \rho \frac{l}{A} \tag{3.15}$$

In this equation, ρ is the specific resistivity of the material, l the length of the conductor and A the cross-section area. To explain the drastic increase of the resistivity for the 20-nm-wide electrode two additional effects have to

be considered that contribute to the resistivity of the nano-wire. Since the dimensions of the Pt wire are scaled down to an extent where they match the mean free path of an electron of 23 nm in bulk Pt [94], the scattering of the electrons at the surfaces [95] and the grain boundaries within the material [96] strongly increase the resistivity. Similar size effects of rectangular shaped copper wires in the nanometer regime have been addressed by Steinhoegl *et al.* [97–99].

Platinum wires are also commonly used as resistance thermometers [100]. The temperature dependence of the resistance of the fabricated Pt nano-structures is shown in Figure 3.32 (b). In the temperature range of 0°C to 100°C it is reasonable to assume a linear resistance-temperature characteristic with an error of less than 0.4°C at 50°C [100]. The extracted resistance-temperature dependence of three different sized nano-structures is given by the following equations:

$$R_{20\text{ nm}} = 10678\ \Omega + 14.9\ \Omega/^{\circ}\text{C} \cdot T \tag{3.16}$$

$$R_{60\text{ nm}} = 2391\ \Omega + 5.5\ \Omega/^{\circ}\text{C} \cdot T \tag{3.17}$$

$$R_{100\text{ nm}} = 1189\ \Omega + 2.3\ \Omega/^{\circ}\text{C} \cdot T \tag{3.18}$$

Hence, the fabricated four-point nano-structures can be utilized to measure the temperature on the sample surface. This is especially useful for the electrical characterization under vacuum or cryogenic conditions to check the thermal coupling between the stage and the sample by the resistance of the Pt line.

In summery, the 15-nm-thin Pt electrodes with lateral sizes down to approximately 20 nm are generally suitable for the integration of ReRAM elements. Though, it must be noted that the line resistance of the nano-structures increases nonlinear with the device dimensions. This has to be considered if the resistance of the metal electrodes is in the resistance range of the memory element. In this case, it represents a non negligible series resistance and can influence the switching characteristics.

3.2.3 Top Electrode Patterning

The patterning approach for the top electrodes consists of the electron beam lithography and a lift-off process. Lift-off processes generally require resist masks that exhibit an undercut. For these resist masks, the flanks with negative slopes are not covered by the evaporated material to be structured. This allows the solvent to remove the resist, starting from the uncovered surfaces and lifting the excess metal of the sample surface. For the lift-off patterning, a two layer resist systems was applied [93, 101]. Nauenheim and Rosezin used a resist stack consisting of a PMMA (polymethyl methacrylate) top layer and a PMMA-MAA (MAA: methyl methacrylic acid) bottom layer. The PMMA-MAA resist has a higher sensitivity to the electrons than the top PMMA layer and is therefore dissolved faster and wider by the developer. This leads to the required undercut for the lift-off process.

In this work, the PMMA/PMMA-MAA double layer resist system was found to produce unreliable patterning when applied for different resistive switching oxides. Therefore, the two layer resist system was changed. The idea of having different sensitivity resist layers was adopted by implementing a resist system consisting of two layers of PMMA resist with different molecular weights. First, the AR-P 639.04 (50K molecular weight) resist from Allresist GmbH was spincoated with a spin-rate of 6000 rpm and baked on a hotplate at the temperature of 180°for 10 minutes. This results in the layer thickness of 70 nm. Second, the AR-P 679.01 (950k molecular weight) was spincoated and baked at 180°for 5 minutes. The spin-rate of 2000 rpm produces a layer of 40 nm thickness. The polymer 50K bottom layer has about 20% higher sensitivity as the polymer 950K top layer [76]. This enables the creation of the undercut.

The electron beam exposure was carried out in a two step process. The adjusted dose for the nano-structures was determined to be 350 $\mu C/cm^2$ and written with a beam current of 1 nA with a beam step size (bss) of 5 nm. The micro-structures were written with a broader beam of 150 nA beam current and a 50 nm bss. Because of the proximity effect, a smaller nominal dose of 280 $\mu C/cm^2$ was used in this step.

The development was performed by an AR-600-55 developer bath for 75 s and stopped in isopropanol for 30 s. Afterwards, the 5-nm-thick Ti and the 25-

nm-thick Pt layers defining the top electrode were evaporated. For the lift-off process, the sample was immersed in the acetone bath with low power ultrasonic agitation followed by cleaning in isopropanol.
The fabrication process-flow of the nano-crossbar ReRAM elements shown in Fig. 3.33 is summarized as follows:

1. First, the sputter deposition of the Ti (5 nm) and Pt (25nm) layers on an oxidized Si wafer is performed.

2. Then, the bottom electrodes are patterned by UV nanoimprint lithography and dry etching steps (3.33 (a)).

3. Next, the resistive switching TiO_2 layer is deposited by reactive sputtering (3.33 (b)).

4. Afterwards, the top electrodes are defined by the e-beam lithography in combination with the metal evaporation and the lift-off process (3.33 (c)).

5. In order to enable electrical measurements on the MIM device, the oxide on the bottom electrode contact pad has to be removed. This is done by optical lithography and RIBE process. The process is referred as pad opening (3.33 (d)).

In summary, the developed patterning processes provide a technology platform for the integration of ReRAM devices with different resistive switching oxide and top electrode materials with cell sizes down to 40 x 40 nm^2. These structures have also been utilized in the works of Reiners for studies on ALD grown TiO_2 [102] and Tappertzhofen for research on nanobattery effects in SiO_2 based ECM cells [103].

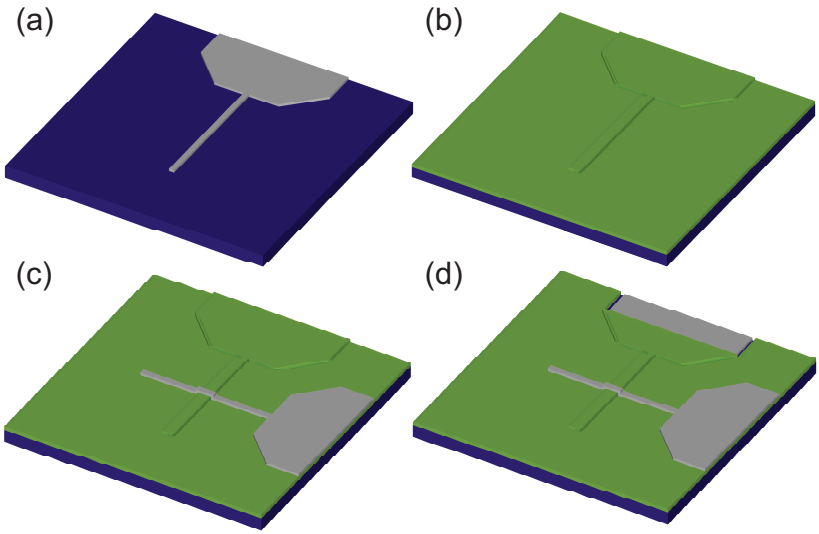


Figure 3.33: Fabrication route of the nano-crossbar devices. (a) First, the bottom electrode is structured by UV-NIL. (b) This is followed by the sputter deposition of the resistive switching oxide layer. (c) Then, the top electrode is structured by EBL and a lift-off process. (d) Finally, optical lithography and a RIBE process is performed for the pad opening.

3.3 Integration of ReRAM Devices with MOSFETs

Redox-based resistive switching memory devices (ReRAM) require a limitation of the maximum current during the electroforming and the SET process to prevent permanent damage of the memory element by excessive currents in the ON state. This limitation is referred to as current compliance I_C. The conventional ReRAM devices, consisting of the MIM structure (1R), the current compliance is realized by the semiconductor parameter analyzer during the electrical characterization. This gives rise for overshoot phenomena caused by the discharging of parasitic capacitances through the memory element as well as the settling time of the measurement tool during which current higher than the I_C is sourced. The overshoot phenomena are known degrade the memory element performance with regard to low current operation and endurance [104–106]. In order to suppress these parasitic effects, n-channel MOS transistors have been integrated with the ReRAM devices in this work (1T-1R). The schematic of this setup is shown in Figure 3.34.

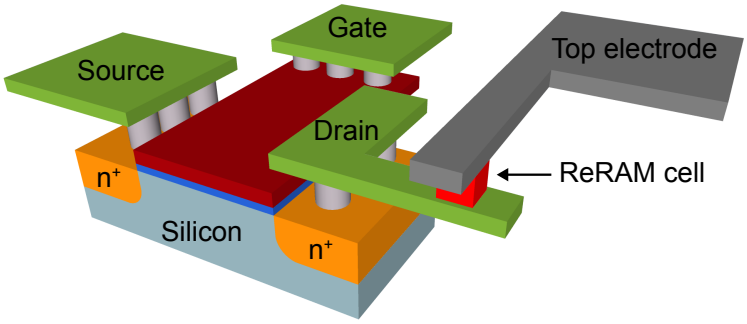


Figure 3.34: Schematic of the ReRAM element integrated with a n-channel MOS transistor. The resistive switching cell (red) is realized on top of the nano-electrode extending from the drain contact (green).

The integration starts with pre-structured wafers at the transistor level provided by IMEC Belgium. A 65 nm CMOS process is used to fabricate the n-channel MOSFETs on 300 mm wafers. During the back-end processing,

40-nm-thick PVD TiN electrodes are patterned on top of W-filled via's contacting the transistor source, gate and drain regions [107, 108]. The ReRAM element is then realized at the junction of the nano-electrode extending from the drain contact region of the n-channel transistor and the top electrode nanostructure.

3.3.1 Mask Layout

The mask of the 1T-1R sample contains different functional areas that are denoted as modules. An image of the CAD mask is shown in Figure 3.35. The blue structures in this image are patterned from the TiN layer and contain to contact pads of the transistors and the bottom electrodes of the ReRAM devices. The red structures are created during the top electrode patterning and define the active area of the memory elements at the junctions with the TiN structures.

There are three modules of interest for this research work that are labeled as BE, FE and FR. First, the BE module contains TiN crossbar micro- and nano-structures without MOSFETs for the fabrication of 1R devices. Second, transistors with variable length and width of up to 1 µm are located in the FE module. The connected TiN bottom electrodes for the memory elements also exhibit different sizes from 55 nm to 3 µm. Therefore, the specific combination of one transistor size and one footprint of the memory element is only present once in this module. This renders the comparison of the electrical characteristics of the structures in this module with only one sample impossible. Third, the FR module contains transistors with a constant length and width of 1 µm. A total of 84 1T-1R devices are located in this module organized in columns of 6 devices of the same size. The smallest memory element size is 55 x 55 nm^2 in the design while the largest cells have an active area of 335 x 335 nm^2.

Each column contains transistors with and without direct access to the drain contact through the monitor pad. This enables separate electrical characterization of the transistor as well as the ReRAM cell.

For the e-beam patterning, two sets of marker structures consisting of 5 x 5 μm^2 squares are located in the scribe line of each die.

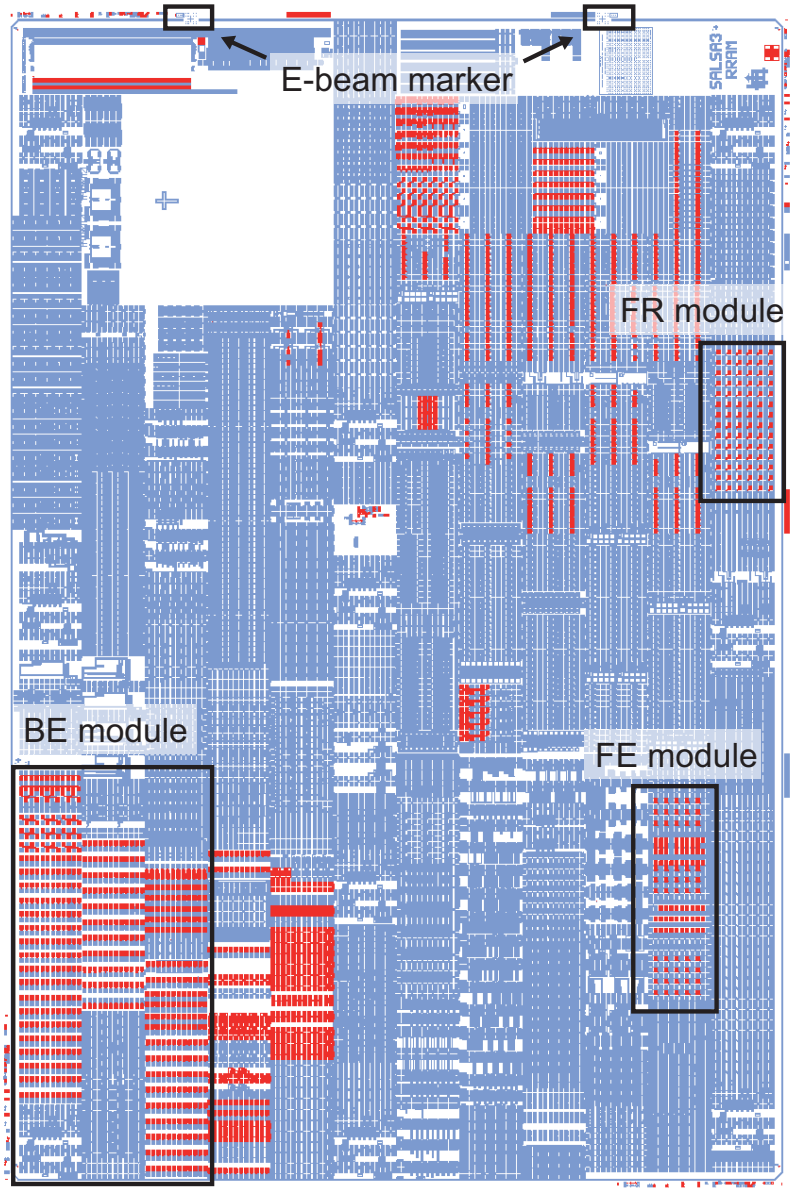


Figure 3.35: Mask design of the 1T-1R sample. The integrated MOS transistors with ReRAM devices are located in the FR and FE modules. The BE module offers memory elements without a transistor.

3.3.2 Development of the Process Flow

The mask design shown in Figure 3.35 represents one die on the 300 mm wafer. In the Forschungszentrum Jülich most of the deposition and patterning tools are not capable of handling such large wafers. The wafer is therefor diced with a Disco DAD3350 Automatic Dicing Saw. Since the marker structures for e-beam patterning are contained in the scribe line of the dies, the wafer cannot be cut along these lines. It is rather cut 2 mm to the sides of the left and right scribe line of the die. The most important FR module is located at the edge of the dies in the original design. This location is prone to edge bead effects. To improve the yield of working devices, the horizontal cutting line was shifted 7 mm from the scribe line so that the FR module is placed in the center of the diced sample. The photograph of a single die is shown in Figure 3.36.

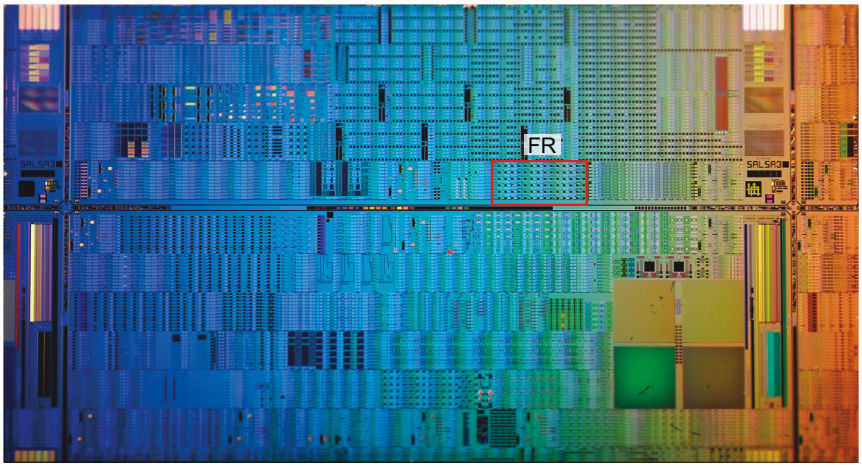
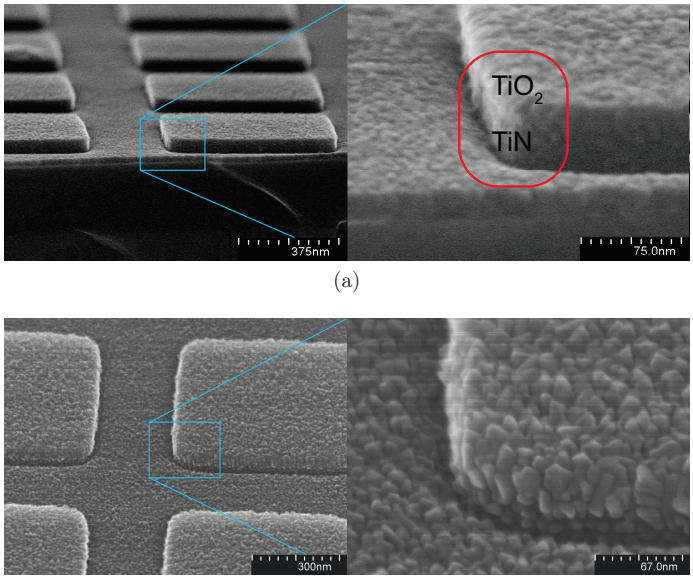


Figure 3.36: Photograph of the 1T-1R sample. The FR module with the 1T-1R devices is marked with the red rectangle

3.3.2.1 Oxide Deposition

The provided wafer for the integration of 1T-1R devices contains the MOS transistors and the patterned TiN electrodes, as described in the introduction of this section. Two generations of this technology platform can be distinguished. The wafers from the first generation are not planarized while the

second generation wafers are planarized with a layer of SiO_2/SiN [109]. When fabricating ReRAM devices on the first generation substrates, the edge coverage of the deposition process for the oxide layer on the flanks of the TiN electrodes needs special consideration. The comparison of the edge coverage of two TiO_2 layers of different thicknesses, sputtered with the standard deposition process described in section 3.1.1.1, is shown in Figure 3.37.



(a)

(b)

Figure 3.37: Comparison of the edge coverage of (a) 25-nm-thick and (b) 50-nm-thick reactively sputtered TiO2 on 40-nm-thick TiN structures

The 25-nm-thick TiO_2 layer is shown in Figure 3.37 (a) while the 50-nm-thick layer is depicted in Figure 3.37 (b). In the images, the rectangular shaped structures are the TiN pillars of 40 nm height. The area of special interest is highlighted in the red box. The 25-nm-thick TiO_2 layer shows a poor edge coverage that is not suitable for ReRAM integration. The columnar structure and a comparable roughness, as reported by Nauenheim [39], is found in the SEM cross section of the TiO_2 film. For the 50-nm-thick TiO_2 layer shown in Figure 3.37 (b), a more pronounced roughness and the presence of nano-crystals is observed. The increased roughness at the edges of the TiN structures leads to the conclusion that they are also covered with TiO_2. The electrical character-

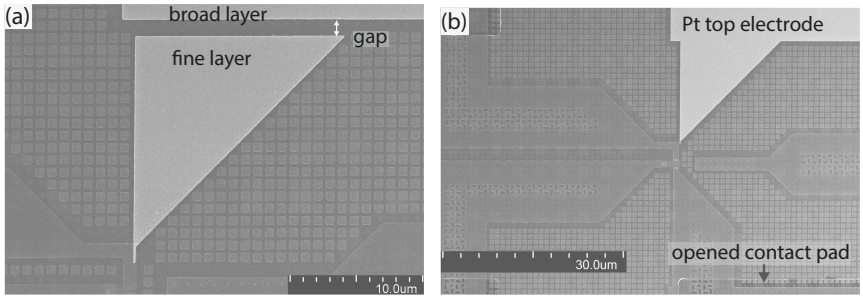


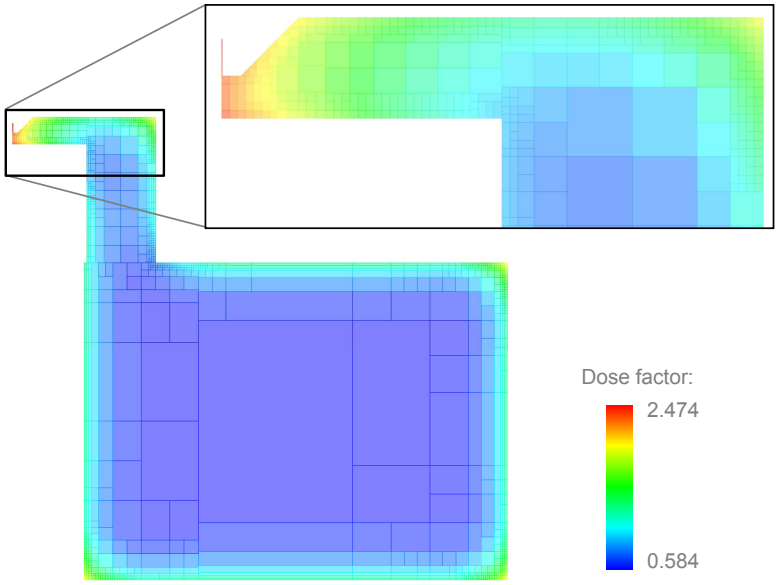
Figure 3.38: Comparison of the two and one layer e-beam patterning. (a) The two layer patterning results in a gap between the nano- and the micro-structures. (b) The one layer approach prevents the gap and yields better alignment.

ization proves that the 50-nm-thick TiO_2 yields functional integrated ReRAM devices. However, considering the edge coverage, the first generation samples are not suitable for the integration of ultra-thin sputtered resistive switching oxides. This drawback is circumvented by the planarization in the second generation sample. That enables ultra-thin oxide layer integration.

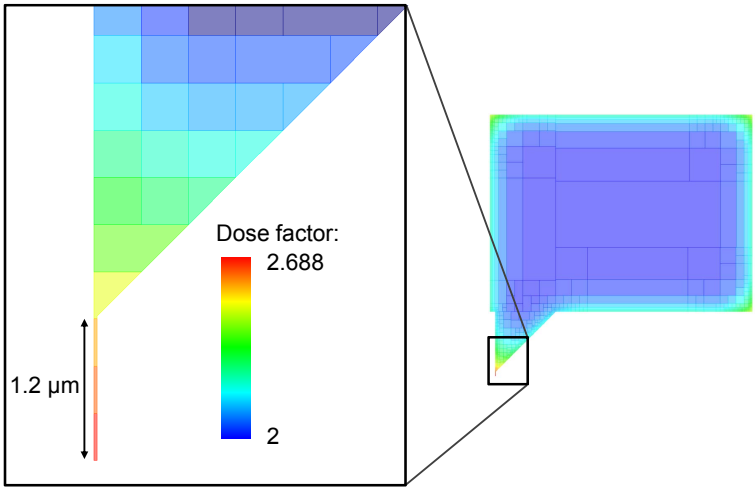
3.3.2.2 Top Electrode Patterning by E-Beam Lithography

The patterning of the top electrodes was performed by the combination of electron beam lithography, metal evaporation and the lift-off process. In the first approach the top electrode mask design provided by IMEC was split into two layers. One layer containing the structures smaller than 1 µm and the other layer containing the larger structures. This strategy offers the prospect of achieving the resolution for small structures by using a fine beam of 500 pA beam current in the first step. The larger structures, like the contact pads, are patterned with a broader beam (I_{beam} = 50 nA) that yields higher writing speeds in the second step.

The alignment of the sample is the crucial step in the e-beam patterning. For this purpose, marker structures are patterned during the definition of the TiN bottom electrodes. During the alignment procedure, the tool is operated in the SEM mode to capture an image of the marker area. The image quality depends on the used beam current and was especially poor for the fine beam. Therefore, the two layer writing strategy often resulted in insufficient align-



(a)



(b)

Figure 3.39: Proximity effect correction by dose modulation for (a) the FR-modules and (b) the FE-modules.

ment and even gaps between the nano- and the microstructures (Fig. 3.38 (a)).
In order to improve the alignment precision and prevent the gap between the nano- and micro-structures a second approach to pattern the top electrodes was selected. In this e-beam writing strategy, the structures are defined in one layer in the CAD file. This layer is then written in one step. The beam current of 8 nA and a beam step size of 12.5 nm was chosen since it offers a reasonable compromise between achievable resolution and writing speed. The suitable e-beam exposure base dose of 260 $\mu C/cm^2$ was determined by writing test patterns of variable doses. In addition, simulations were carried out to calculate dose factors that the base exposure dose is multiplied with, in order to account for the proximity effect. These dose factors are shown in Figure 3.39. They range from 0.58 to 2.47 for the structures in the FR module. In this case the nano-structure is exposed with a nominal dose of more than 600 $\mu C/cm^2$ while the middle of the pad has the lowest dose of 150 $\mu C/cm^2$.
For the resist, a two layer system comparable to the system utilized for the imprint based nano-crossbar integration is applied. The bottom layer consists of a PMMA resist with a molecular weight of 50K that is spincoated at 2000 rpm and softbaked on a hotplate at 180 °C for 5 minutes. This results in a layer thickness of 120 nm. Afterwards the less sensitive PMMA 950K resist is spincoated at 4000 rpm to achieve a 30-nm-thick film. Again, the softbake at 180 °C is performed for 5 minutes. The two layer resist is applied to achieve the required undercut in the resist profile for the successful lift-off. The development of the resist after the afore-mentioned exposure is carried out in an AR-P 600-55 developer bath for 75 seconds and is stopped in isopropanol for 30 seconds.

The developed process flow for the fabrication of the memory element on the transistor platform is summarized as follows:

1. First, the wafer is cut and diced into single dies.

2. Next, a standard cleaning in acetone and isopropanol (5 minutes each) is performed.

3. The TiO_2 sputtering is carried out in the next step.

4. Afterwards, the e-beam resist is coated on the sample and the top electrode pattern is exposed.

5. The Ti and Pt metal deposition for the top electrodes is then performed by thermal evaporation.

6. This is followed by the lift-off process in acetone.

7. Finally, the source and gate contact pads are opened with optical lithography and dry etching.

The optical microscope image of the patterned FR module is shown in Figure 3.40. The corresponding SEM image of the 1T-1R device is depicted in Figure 3.41 as well as the image of the 1T-1R device from the FE module in Figure 3.42.

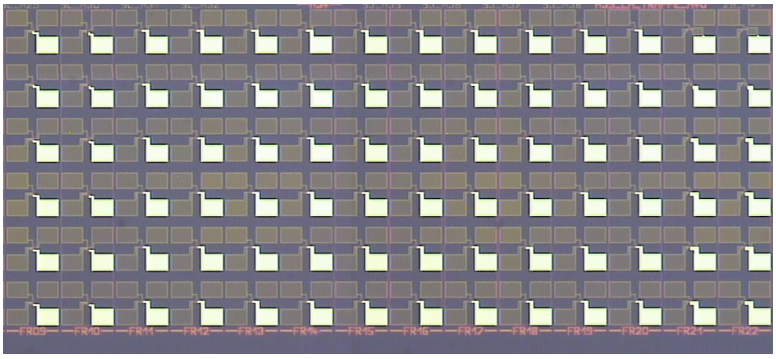


Figure 3.40: Microscope image of the FR-module. The Pt top electrodes of the memory elements have a white color while the TiN transistor contact pads are grey.

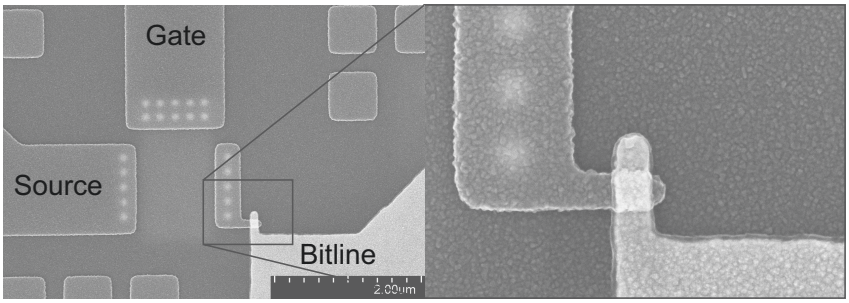


Figure 3.41: SEM image of a 1T-1R device in the FR module

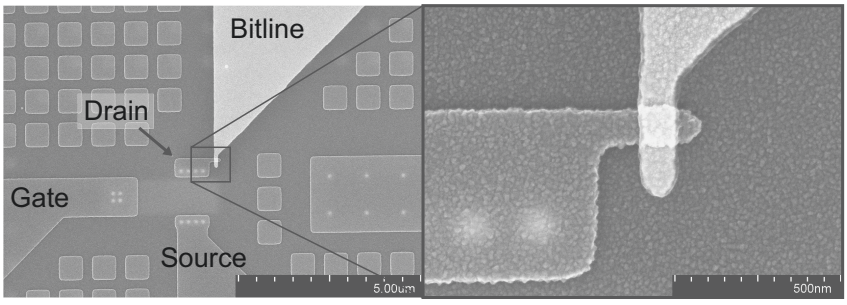


Figure 3.42: SEM image of a 1T-1R device in the FE module

Chapter 4

Electromotive Force in ReRAM Devices

It has recently been shown that redox-based resistive switching memory elements can be considered as nanobatteries since they exhibit an open clamp voltage of up to 800 mV [110]. The reason for the detected voltages is the electromotive force (EMF). In this chapter the theoretical background for the origin of the EMF will be presented. This will be followed by the performed measurements of the EMF. The chapter will be concluded with the impact of the nanobattery effect on the ReRAM devices.

4.1 Theory

Three origins for the nanobattery effect in metal (M) / solid-electrolyte (I) / metal (M) structures of the ReRAM devices can be distinguished:

1. The Nernst EMF.
2. The diffusion potential.
3. The Gibbs-Thomson potential.

First, the potential difference determined by the half-cell reactions at the two electrode/electrolyte interfaces is known as the Nernst potential V_{N}. It is described by the Nernst equation (Eq. 4.1):

$$V_{\mathrm{N}} = V_{\mathrm{s}'} - V_{\mathrm{s}''} = V^0 + \frac{kT}{e} \ln \frac{(a_{\mathrm{Ox}})_{\mathrm{s}'} \cdot (a_{\mathrm{Red}})_{\mathrm{s}''}}{(a_{\mathrm{Red}})_{\mathrm{s}'} \cdot (a_{\mathrm{Ox}})_{\mathrm{s}''}} \tag{4.1}$$

with $V_{s'}$ and $V_{s''}$ being the half-cell potentials at the active electrode/electrolyte (s') and the inert electrode/electrolyte (s") interface with the difference in standard potentials of these reactions V^0. The activity of the denoted processes (oxidation or reduction) are expressed as a_{Ox} or a_{Red} respectively.
Second, inhomogeneous distribution of charge, like Ag^+ ions, OH^- ions or electrons across the solid-electrolyte layer may be present. These are either caused by the resistive switching processes of the ReRAM device or by chemical dissolution of the electrode material. The gradient in the charge distribution gives rise for the diffusion potential V_{diff} in Equation 4.2:

$$V_{\mathrm{diff}} = -\frac{kT}{e}\sum_{\mathrm{i}}\int_{s''}^{s'}\frac{t_{\mathrm{i}}}{z_{\mathrm{i}}}d\ln a_{\mathrm{i}} = -\frac{kT}{e}\left(\bar{t}_{\mathrm{Me^+}}\ln\frac{(a_{\mathrm{Me^+}})_{s'}}{(a_{\mathrm{Me^+}})_{s''}} - \bar{t}^{-}\ln\frac{(a^-)_{s'}}{(a^-)_{s''}}\right) \quad (4.2)$$

here t_{i} is the transference number of the involved charged species (metal cations, anions or electrons) and z_{i} the charge number.
The third contribution to the measured open clamp voltage is generated by the increased surface energy of the non-contacting nanofilament inside the ReRAM device in comparison to the macro-electrode. This possibly generates the potential V_{GT} (Gibbs-Thomson effect) described by equation 4.3 [111]:

$$V_{\mathrm{GT}} = -\frac{\mu_{\mathrm{Ag}}^{\mathrm{macro}} - \mu_{\mathrm{Ag}}^{\mathrm{nano}}}{ze} = -\frac{2\gamma}{zer}V_{\mathrm{m}} \quad (4.3)$$

In this equation μ_{Ag} is the chemical potential of Ag, r is the radius of the particle and γ the surface tension. V_{m} stands for the molar volume.
The measured EMF is usually a combination of the three contributions. In case of a formed metallic filament inside the ReRAM device that connects both electrodes, no voltage is measurable. This is due to the short circuit caused by the filament.

4.2 EMF in ECM Systems

In this research work, the EMF was measured on memory elements based on $Ge_{0.3}Se_{0.7}$ and WO_3 with Ag and Cu as active electrode material and Pt for the inert electrode. They are categorized as ECM type ReRAM elements.
The $Ge_{0.3}Se_{0.7}$ based ReRAM devices were fabricated by RF sputtering using

silicon wafers with the platinum layer as substrate. The sputter process of the chalcogenite material is described elsewhere [112]. The 100-nm-thick Ag top electrodes were deposited by RF sputtering and patterned by UV lithography. The resulting micro-structures had diameters between 10 µm and 100 µm.
It is reported that Ag is chemically dissolved in $Ge_{0.3}Se_{0.7}$ chalcogenide material [113]. Therefore, the Ag/Ag-$Ge_{0.3}Se_{0.7}$/Pt ReRAM element contains a significant amount of Ag^+ ions. In this case the chemical activities at both interfaces are approximately the same and equation 4.1 can be simplified to:

$$V_N = \frac{kT}{e} \ln \frac{(a_{Me})_{s"}}{(a_{Me})_{s'}} \tag{4.4}$$

The optical microscope image of the initial state (Fig. 4.1 (a)) was recorded after a SET/RESET cycle. Afterwards, the negative voltage of 1 V was applied to the Ag electrode. This removes the residual Ag atoms from the inert Pt electrode interface (s"). In addition, a dendrite formation is observed at the Ag interface (s') (Fig. 4.1 (b)). At $t_1 = 0$ s the voltage measurement over time was started. From t_1 to t_2 the increasing highly negative $V_{cell} \approx 450$ mV was detected. This was accompanied by the fading of the dendrites in the optical image (Fig. 4.1 (c)). This is explained by the vanishing contribution of the diffusion potential (positive) and the dominating Nernst potential (negative) between the electrodes. In parallel to the dissolution of the dendrites (t_2), the EMF increases to positive values again (Fig. 4.1 (d)) with a diffusion potential as the remaining component of the EMF owing to the different activity of Ag+ ions at the both s', s" surfaces (t>t_3).

EMF measurements were also performed on Cu/WO_3/Pt micro-crossbars with a size of 2 x 2 μm^2. They were fabricated by RF sputtering of the 30-nm-thick WO_3 film in Ar atmosphere on the Pt bottom electrodes that were defined by optical lithography and etching of the Pt layer. The 70-nm-thick Cu top electrodes were structured by thermal evaporation and a lift-off process.
The as deposited WO_3 based ReRAM device exhibits a measured cell voltage of $V_{EMF} = 10$ mV (Fig. 4.2 (a)). After the first time dependent voltage measurement, the memory element was formed and switched to the ON state by applying 3 consecutive voltage sweeps (Fig. 4.2 (b)), to determine the impact of the resistive switching process on the cell voltage. The limitation

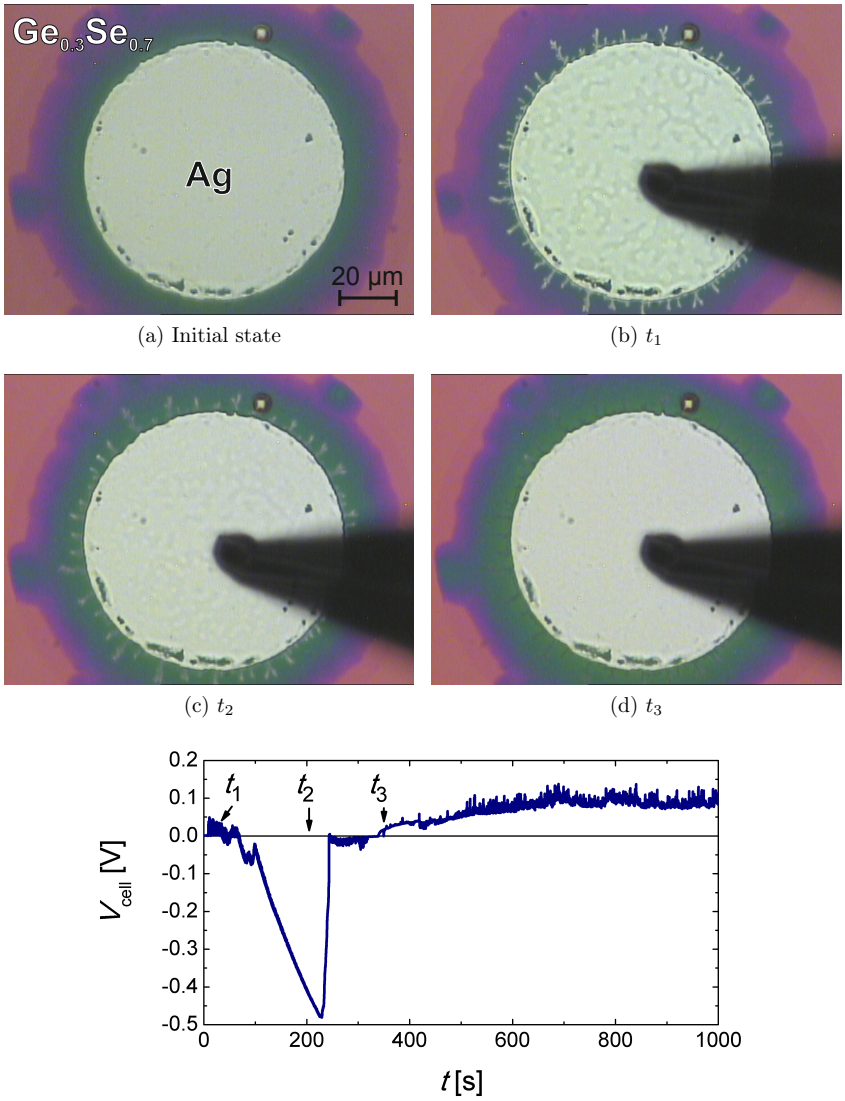


Figure 4.1: Time-dependent EMF measurements for $Ag/Ge_{0.3}Se_{0.7}/Pt$ based ECM cells. [110]

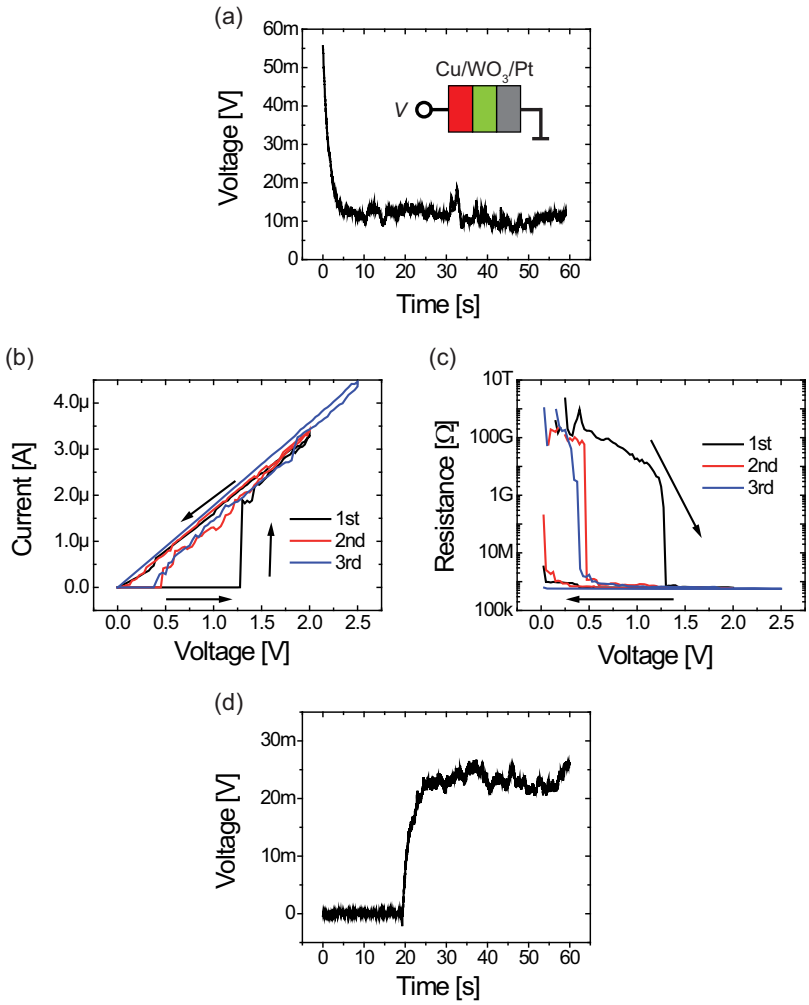


Figure 4.2: EMF measurement on $Cu/WO_3/Pt$ micro-structures. (a) The virgin cell exhibits an EMF of $V_{\mathrm{EMF}} = 10$ mV. (b) The ReRAM cell is then switched to the ON state by 3 consecutive I-V sweeps with a series resistance (500 kΩ), (c) shows the corresponding R-V plot. (d) Immediately after the SET, there is no detectable EMF. During the measurement the voltage increases to $V_{\mathrm{EMF}} = 25$ mV. A control measurement reveals that the cell has switched back to the OFF state.

of the switching current during the SET was achieved by a series resistance of 500 kΩ, which shows in the $R(V)$ plot in Figure 4.2 (c). Then, the EMF of the cell in the ON state was measured (Fig. 4.2 (d)). During the first phase of the EMF measurement the ReRAM device remains in the ON state with no detectable cell voltage. This is explained by the conducting metal filament inside the ECM that short circuits the EMF. After 20 s, a sudden increase in the measured cell voltage was observed. Another 5 s later, the EMF reaches a steady state of $V_{\mathrm{EMF}} = 25$ mV with only small fluctuations. The control measurement with an applied voltage sweep reveals that the ECM cell has switched to the high resistive OFF state. The increased value of the measured cell voltage in comparison to the initial EMF can be explained by the higher ion concentration inside the ReRAM element induced by the switching cycles.

4.3 Impact of the EMF on ReRAM Devices

The nanobattery effect in ReRAM devices caused by the electromotive force has been demonstrated for ECM type systems in the previous section. However, it was shown that the nanobattery effect also exists in VCM type memory elements. It is even suggested that in principal EMF voltages are present in all bipolar ReRAM devices [110]. An overview of the EMF for different types of ReRAM cells is depicted in Figure 4.3 (a).

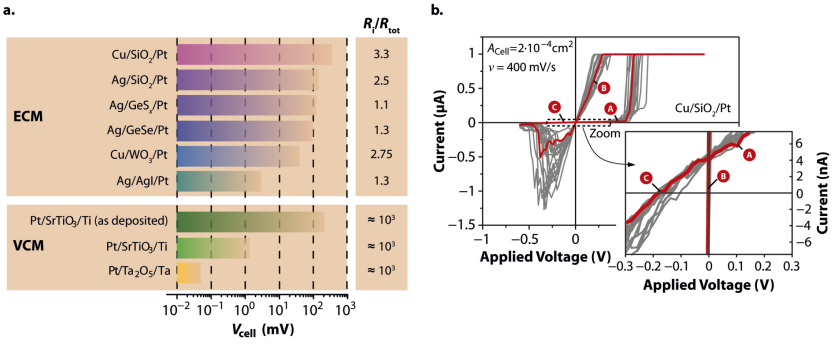


Figure 4.3: Varying EMF from the microvolts range to some hundred millivolts have been measured depending on the type of cell (a). The EMF results in the non-zero-crossing I-V characteristics for the $Cu/SiO_2/Pt$ system (b). [110]

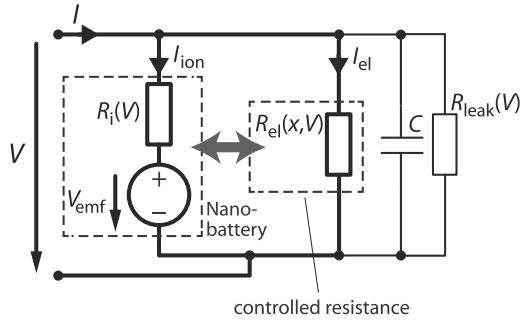


Figure 4.4: Equivalent circuit of the extended memristive element that accounts for the presence of the inherent nanobattery. [110]

There are several consequences of the inherent EMF that need to be considered for the integration of ReRAM devices into future non-volatile memory. First of all, it is interesting to note that by measuring the EMF, a conclusion about the resistance state of the cell can be drawn. This offers the possibility for a non-destructive readout of complementary resistive switches (CRS) besides the capacity based readout proposed by Tappertzhofen *et al.* [114]. In fact, Rosezin has shown that the EMF can be used to determine the state of a single CRS cell [31].

In addition, the non-zero-crossing I-V characteristics shown in Figure 4.3 (b) caused by the EMF necessitate a correction of the memristor theory [110]. The original memristive model from Strukov *et al.* [115] postulates that memristive devices are passive elements with no current flow for zero applied voltage. However, this does not hold true with the presence of the EMF in ReRAM elements. The ionic current caused by the nanobattery is accounted for in the extended memristive circuit model shown in Figure 4.4. It adds the nanobattery in parallel to original memristive model. Further details regarding the extended memristive element are explained in [110].

The WO_3 based ECM ReRAM devices showed limited retention during the electrical characterization. This can be explained by the presence of the EMF inside the memory element that leads to a self-dissolution of the conducting filament. Similar effects have been shown Tappertzhofen *et al.* for SiO_2 based ECM systems [103]. In addition the nanobatery effect has an impact on the

switching characteristics by causing a decrease of the observed set voltages of the ReRAM devices. This limits the endurance since the memory element gets stuck in the ON state if the set voltage decreases to zero.

Chapter 5

Electrical Characterization of Nano-Crossbar Memory Elements

The fabricated passive nano-crossbar devices based on TiO_2 and WO_3 will be electrically characterized in this chapter. The impact of external series resistances and layer stacks on the electroforming behavior of the ReRAM elements and the corresponding RESET characteristics will be elucidated. In addition, the impact of device areas on the ReRAM behavior will also be demonstrated by using the passive crossbar technology platform.

5.1 TiO_2 Based Nano-Crossbar ReRAM

The analysis of the reactively sputtered TiO_2 in passive nano-crossbar ReRAM with the standart layer stack shown in Figure 5.1 (a) will be carried out in this section. During the electrical characterization, the signal was always applied to the top electrode (5-nm-thick Ti/ 25-nm-thick Pt) while the Pt bottom electrode of the memory element was grounded.

ReRAM elements in passive crossbar structures are prone to current overshoot phenomena that degrade the device characteristics like endurance and low power switching [106]. This is due to the response time of the semiconductor parameter analyzer's (SPA) current compliance and the parasitic capacitances from the MIM structure and the wiring. The current overshoot linked to the response time of the SPA can be minimized by implementing an external series resistance for the current limitation in the measurement tip [40]. Therefore,

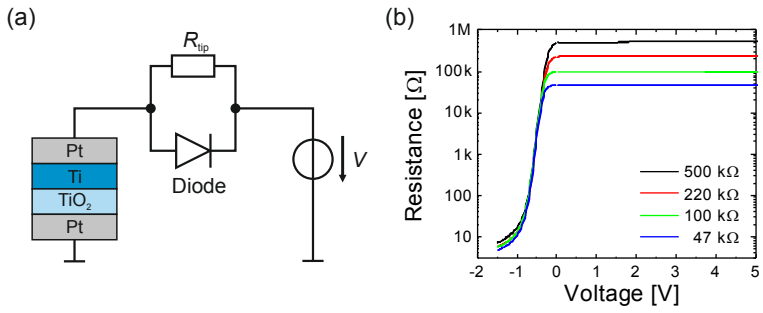


Figure 5.1: Tailored measurement tip for passive current compliance. (a) The tip consists of a series resistance R_{tip} to the ReRAM element with a diode in parallel. (b) It only limits the current through the ReRAM element for positive voltages. Different compliance levels are realized by variation of the built-in series resistance.

the electroforming and SET were carried out with different series resistances. The circuit diagram of the tailored tip as well as the corresponding resistance graph are depicted in Figure 5.1.

The voltage drop over the memory element (V_{cell}) and the cell resistance (R_{cell}) are calculated from the simple voltage divider and Ohm's law by Equation 5.2:

$$V_{\text{cell}} = V_{\text{total}} - V_{\text{tip}} = V_{\text{total}} - I_{\text{meas}} \cdot R_{\text{tip}} \tag{5.1}$$

$$R_{\text{cell}} = \frac{V_{\text{cell}}}{I_{\text{meas}}} \tag{5.2}$$

with V_{total} being the applied voltage, I_{meas} the measured current and R_{tip} the used series resistance. This enables the detection of the intrinsic behavior of the ReRAM element that is otherwise hidden in the current compliance of the SPA. The diode in parallel to the series resistance enables higher reset currents.

5.1.1 Electroforming Characteristics

To enable the resistive switching, the fabricated TiO_2 based nano-crossbar ReRAM devices require an electroforming step. This is a common requirement for redox-based resistive switching devices and the applied forming routine is known to have an impact on the switching behavior [107, 116, 117]. The negative current driven electroforming into the OFF state was reported to be

the most reliable routine for ReRAM devices based on sputtered TiO_2 films [117, 118]. However, the electroforming approach described by Nauenheim *et al.* [117] caused structural damage to the devices examined in this work. This can be explained by the high initial resistances (>1 TΩ) of the TiO_2 based memory elements and the fact that the SPA has to apply a high voltage in the first step of the sweep to drive any current through these devices.
The electroforming was therefore carried out by applying a positive voltage sweep to the top electrode of the memory element with a series resistance as current limiter. The typical I-V and R-V electroforming characteristics of the 10-nm-thick TiO_2 based ReRAM cell is shown in Figure 5.2 (a). In this case the $R_{\mathrm{tip}} = 100$ kΩ was utilized and the device formed into the ON state at the forming voltage $V_{\mathrm{form}} = 4.6$ V.

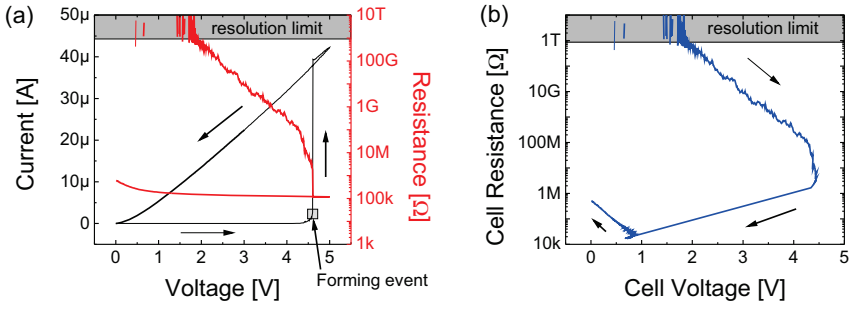


Figure 5.2: Electroforming of a 10-nm-thick TiO_2 based memory element with the 100 kΩ series resistance. (a) I-V and R-V characteristics of the quasi-static electroforming process. The box marks the electroforming event. The forming power is calculated from the corresponding I-V values at that point. (b) Calculated cell resistance over the cell voltage.

The calculated resistance of the ReRAM element over the voltage drop across the nano-crossbar device is illustrated in Figure 5.2 (b). At the forming event, a sudden decrease in the cell resistance with the drastic reduction of voltage drop across the device is observed. The analysis of the electroforming parameters will be elucidated in the following subsections.

5.1.1.1 TiO_2 Layer Thickness Dependence

In order to facilitate the analysis of the impact of the oxide layer thickness on the electroforming process, the samples with 10-nm-thick and 25-nm-thick TiO_2 were fabricated. They are both based on imprint structured 15-nm-thick Pt bottom electrodes and the top electrodes consist of Ti/Pt with layer thicknesses of 5 nm and 25 nm respectively.

The electroforming process of the TiO_2 based ReRAM is known to be affected by electric field and the increased local temperature inside the ReRAM element due to joule heating effects [116, 119]. Therefore, the electroforming voltage should scale in proportion to the oxide layer thickness. In total, 40 ReRAM elements with 4 different device sizes were measured for each TiO_2 layer thickness and the average forming voltage is illustrated in Figure 5.3 (a). The measurements were all carried out at room temperature with the external series resistance $R_{\text{tip}} = 100\ \text{k}\Omega$. In average, the 25-nm-thick TiO_2

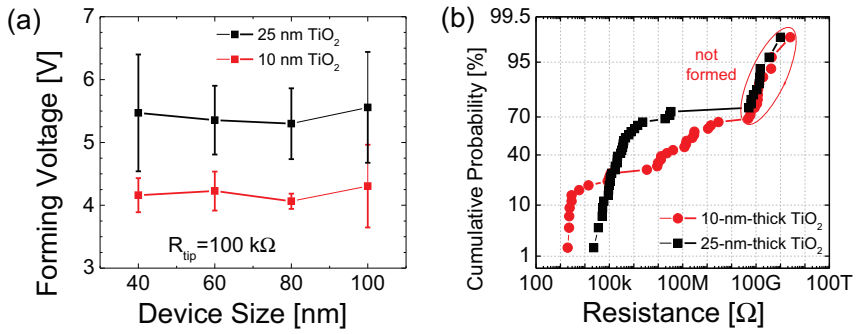


Figure 5.3: Impact of the TiO_2 layer thickness on the electroforming process. (a) Comparison of the average forming voltages for 10 devices of each size of the 10-nm-thick (red) and 25-nm-thick (black) TiO_2 based ReRAM device. (b) Comparison of the resistance state after the electroforming process for the two oxide layer thicknesses.

based ReRAM devices require voltages of 5.4 V $\pm$ 0.7 V for the electroforming, whereas the devices with 10-nm-thick TiO_2 exhibit lower forming voltages of $V_{\text{form}} \approx 4.2\ \text{V} \pm 0.3\ \text{V}$. This is in good agreement with the expected scaling of the forming voltage. In addition, the deviation in the V_{form} is considerably lower for the 10-nm-thick TiO_2 ReRAM devices. For both samples the forming

voltage seems to be constant over the different device areas.
The cumulative probability of the ON state resistances of the electroformed ReRAM elements is shown in Figure 5.3 (b). The 10-nm-thick TiO_2 based devices exhibit the lower minimum resistance values ($\approx$ 2 kΩ) as compared to the thicker TiO_2 (>20 kΩ). However, a large variability of more than 3 orders of magnitude in the resistance state after the electroforming process is observed for both TiO_2 layer thicknesses with the thinner TiO_2 film having the larger spread. In addition, approximately 30 % of the devices have not formed and exhibit resistance states >100 GΩ. In summery, the scaling of the TiO_2 layer thickness of the ReRAM devices is beneficial to reduce the forming voltage.

5.1.1.2 Impact of the External Series Resistance

The proper control over the resistance states is mandatory for the industrial application of the ReRAM. In this research work, the external series resistance in the measurement probe was applied to limit the current and also the voltage drop and thereby the electric field across the ReRAM elements during the electroforming and SET process. It is expected that the external serial resistor will influence the resistance state after the electroforming process. Figure 5.4

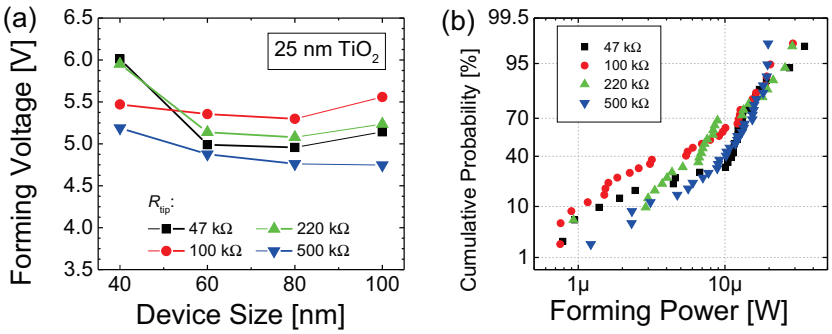


Figure 5.4: Impact of the series resistance on the electroforming characteristics of the Pt/25-nm-thick TiO_2/Ti/Pt. (a) Electroforming voltage over device size and (b) the distribution of the required power for the different R_{tip}.

shows the electroforming characteristics of the Pt/25-nm-thick TiO_2/Ti/Pt based ReRAM devices with the external series resistances of 47 kΩ (black),

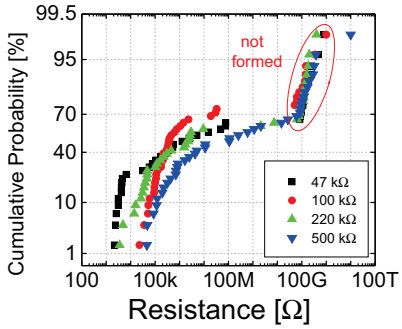


Figure 5.5: ReRAM resistance states after the electroforming with different external series resistances.

100 kΩ (red), 220 kΩ (blue) and 500 kΩ (green). The electroforming voltages exhibit a deviation for the different applied series resistances (Fig. 5.4 (a)). However, the difference in the V_{form} is smaller than the standard deviation of the plotted mean values. In addition, the devices measured with 47 kΩ and 500 kΩ series resistances have smaller forming voltages than the devices with 100 kΩ and 220 kΩ series resistance. From these facts, it can be concluded that the different series resistances do not significantly affect the forming voltages. Similar behavior is observed in the power that is required for the forming event to take place (Fig. 5.4 (b)). Most of the devices electroform between 1 µW and 30 µW while the impact of the external series resistance is not clearly visible.

The comparison of the resistance states (read at $V_{\text{read}} = 0.1$ V) after the electroforming with the different R_{tip} is illustrated in Figure 5.5. Here a clear difference between the devices formed with $R_{\text{tip}} = 47$ kΩ and $R_{\text{tip}} = 500$ kΩ is observed. The insertion of the $R_{\text{tip}} = 47$ kΩ enables higher currents during the electroforming process and therefore the resulting resistance states of the ReRAM elements are lower as compared to the $R_{\text{tip}} = 500$ kΩ. The graphs of the resistance states of the devices formed with $R_{\text{tip}} = 100$ kΩ and $R_{\text{tip}} = 220$ kΩ have a similar distribution and are located between the two other graphs. Based on the filamentary model, the current limitation influences the resistance state of the ReRAM device by controlling the diameter and/or shape of the conducting filament inside the memory element [120].

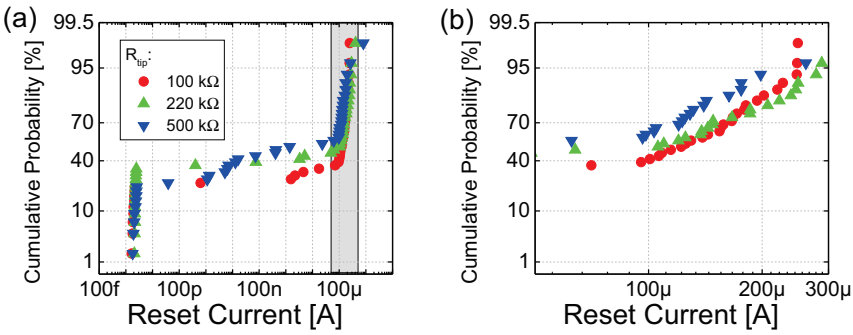


Figure 5.6: RESET characteristics of the 25-nm-thick TiO_2 based ReRAM devices in dependence of the different R_{tip} during the electroforming. (a) Cumulative probability plot of the maximum current during the RESET process. (b) Enlarged view of the data marked with the gray box in (a).

The large deviation in the resistance states after the electroforming process might be explained by the stochastic nature of the electroforming and resistive switching in general [121, 122].
The cumulative probability of the observed maximum RESET currents (I_{RESET}) for the devices formed with the different R_{tip} are shown in Figure 5.6. It shows that approximately 30% of the devices have not formed into the ON state as the respective I_{RESET} is in the pA range. The devices, that have formed into the ON state ($\approx$ 60%), require between 100 µA and 300 µA for the RESET process (Fig. 5.6 (b)). Because of the current limitation to lower values for the $R_{\text{tip}} = 500\ \text{k}\Omega$, the maximum measured I_{RESET} is lower in comparison to the I_{RESET} of the devices which were formed with the lower series resistances. This indicates the control of the filament formation process during the electroforming by the external series resistance.

5.1.1.3 Influence of the Top Electrode Layer Material

The VCM type switching is generally to be dominated by the active oxide layer. A high work function metal electrode and the oxide form the active interface, at which the switching takes place, while the interface at the counter electrode exhibits an ohmic behavior. The material of the counter electrode, also referred to as buffer layer, is known to play an important role in the elec-

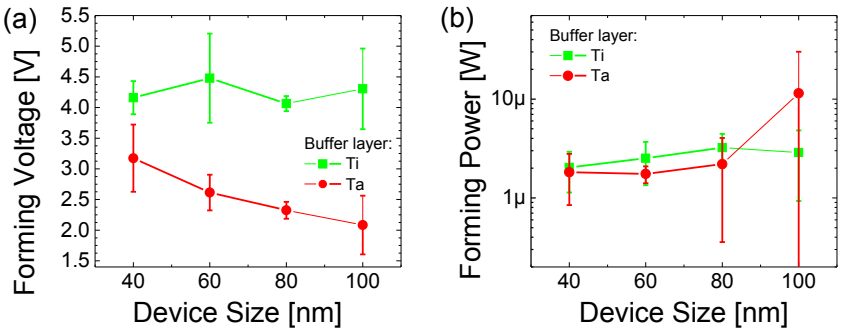


Figure 5.7: Impact of the buffer layer material on the electroforming voltage (a) and power (b) of 10-nm-thick TiO_2 based ReRAM (R_{tip} = 100 kΩ) for different device sizes.

troforming and switching characteristics of the ReRAM devices [123–126]. The impact of the buffer layer material on the TiO_2 based nano-crossbar devices will be analyzed in this section. For this purpose, the samples with Ti and Ta buffer layer were fabricated. The thickness of the switching TiO_2 layer was kept at 10 nm for both type of devices.

The electroforming characteristics of the samples are compared in Figure 5.7. Distinctly lower electroforming voltages are observed for the ReRAM devices with the Ta buffer layer as compared to the Ti buffer layer (Fig. 5.7 (a)). Furthermore, the Pt/TiO_2/Ta/Pt sample exhibits a clear cell size dependence of the forming voltage whereas the Pt/TiO_2/Ti/Pt devices have constant forming voltages. The required power for the electroforming is nearly the same for both samples (Fig. 5.7 (b)). The physical explanation for the observed difference in the electroforming voltages is yet unknown.

The reduced electroforming voltages of the ReRAM devices with the Ta top electrode material result in a smaller scatter of the resistance state after the electroforming. This is shown in Figure 5.8. While the ReRAM devices with the Ti buffer layer exhibit resistances between 2 kΩ and 1 GΩ, the resistances of the Ta buffer layer devices are narrowly distributed around 100 kΩ. In general, the smaller electroforming and switching voltages result in a smaller amount of stored charge in the parasitic capacitance and are therefore beneficial to reduce the overshoot phenomena caused by the discharge of the capacitance.

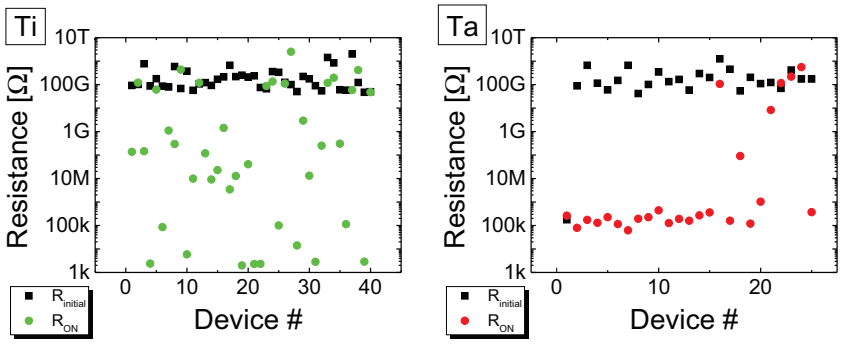


Figure 5.8: Comparison of the resistance states of ReRAM devices with Ti and Ta buffer layer.

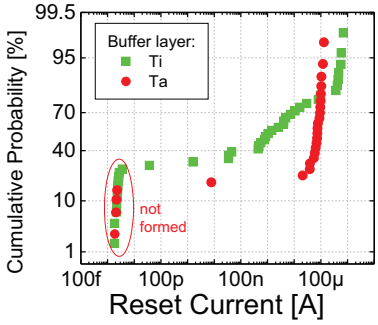


Figure 5.9: Impact of the buffer layer material on the RESET process. The majority of the ReRAM devices with the Ta buffer layer require higher currents as compared to the Ti buffer layer devices.

This could explain the improved characteristics of the ReRAM devices with the Ta buffer layer.
Since the ReRAM devices with Ta buffer layer form into the comparably lower resistance state, the conducting filament inside these devices is assumed to be larger. Higher maximum reset currents I_{RESET}, shown in Figure 5.9, are therefore required to dissolve the conducting path. In addition, the I_{RESET} of the $Pt/TiO_2/Ta/Pt$ devices exhibit much smaller scatter in comparison to the $Pt/TiO_2/Ti/Pt$ devices.

5.1.1.4 Electroforming at Elevated Temperature

The electroforming of ReRAM devices at elevated temperatures (150°) introduced by Butcher *et al.* as hot forming is beneficial for the ReRAM performance of HfO_x based devices [127]. The reduction of the relatively high forming voltages of more than 5 V of the 25-nm-thick TiO_2 based ReRAM devices at room temperature, as described in section 5.1.1.2, is highly desirable. Therefore, the electroforming process is carried out at an elevated temperature of 150°C. Both measurements were carried out with identical sweep-rates and

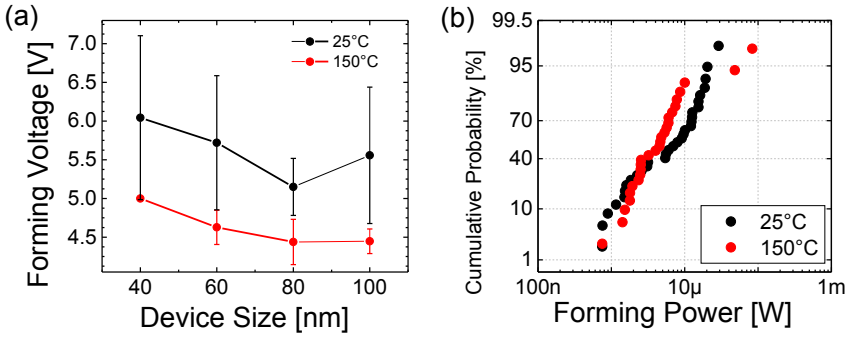


Figure 5.10: Temperature dependence of the electroforming characteristics for the $Pt/25$-nm-thick $TiO_2/Ti/Pt$ based ReRAM. 10 devices of each size were measured. (a) The cells formed at 150°C exhibit lower forming voltages as compared to 25°C. (b) The required power is comparable for both temperatures.

external series resistances. The extracted forming voltages and the required power are shown in Figure 5.10. At the elevated temperature the forming voltages reduce to 4.5 V for the 100 x 100 nm^2 ReRAM devices. The electroforming

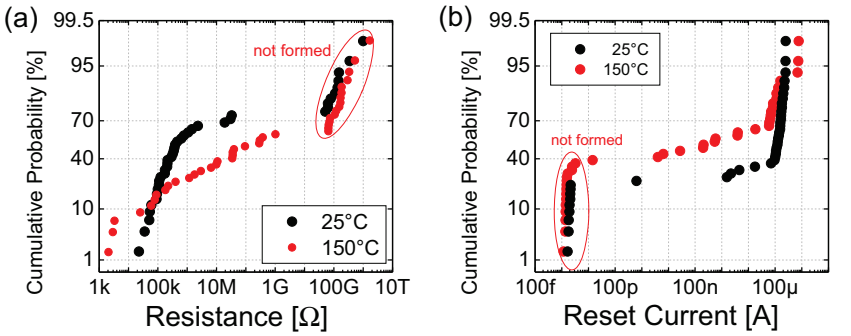


Figure 5.11: Impact of the ambient temperature on (a) the resistance state and (b) the maximum current during the first RESET after the electroforming process.

process is known to be electric field and temperature dependent [128]. The elevated temperatures are therefore beneficial for the filament formation during the initial phase of the electroforming. Once, the current through the ReRAM element is large enough to create the joule heating effect, the defect generation is strongly accelerated, thus triggering a positive feedback that quickly leads to the formation of the conducting filament [128]. The joule heating is therefore the dominating heat source for the electroforming event. This is why there is no distinguishable difference in the power consumption during the forming process at different temperatures.

The hot forming is beneficial for the reduction of the forming voltage, the positive effect for the resistive switching characteristics reported in [127] is not observed for the TiO_2 based nano-crossbar devices. The resistance state after the forming at 150°C shows the larger scatter as compared to the room temperature electroforming (Fig. 5.11). In addition, the decrease in the maximum reset currents for the hot formed devices is negligible.

5.1.2 Transient Pulse Characterization

The integration of ReRAM into future non-volatile nano-crossbar memory requires a high degree of nonlinearity in the I-V characteristics of the individual memory elements to overcome the sneak path problem [129]. The impact of different applied series resistances during the electroforming on the resistance

state of the TiO_2 based ReRAM elements was demonstrated in section 5.1.1.2. In this subsection, the nonlinearity parameter (NL), introduced in section 2.2, of the different achieved ON states in the 10-nm-thick TiO_2 based ReRAM devices with the layer stack of $Pt/TiO_2/Ti/Pt$ will be analyzed. The memory elements were electroformed and SET with series resistances of 100 kΩ, 220 kΩ and 500 kΩ respectively. Afterwards, the analysis of the nonlinearity parameter was carried out with voltage pulses of 100 ns width without the series resistance. The quasi-static SET process and the transient RESET voltage pulses are shown in Figure 5.12 - 5.14.

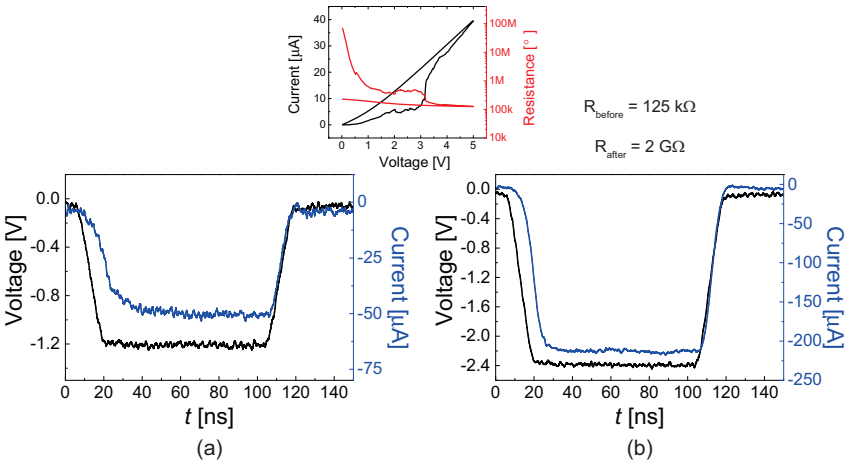


Figure 5.12: AC nonlinearity of the 1Pt/10-nm-thick TiO_2/Ti/Pt device which is toggled to the SET state with 100 kΩ external series resistance.

First, voltage pulses with an amplitude of $V_{\mathrm{RESET}}/2 = -1.2$ V were applied to the top electrode of the ReRAM devices. The transient currents $I(V_{\mathrm{RESET}}/2)$, shown in panel (a), were analyzed with the specialized measurement amplifier, described in section 3.1.5.2. The resistance state of the nano-crossbar devices was measured before and after each voltage pulse with the lock-in amplifier to verify that the $V_{\mathrm{RESET}}/2$ pulses did not change the resistance of the ReRAM device. Next, the RESET process was induced by the application of a voltage pulse of $V_{\mathrm{RESET}} = -2.4$ V and measuring the transient current response. Again, the resistance state was measured with the lock-in amplifier. The de-

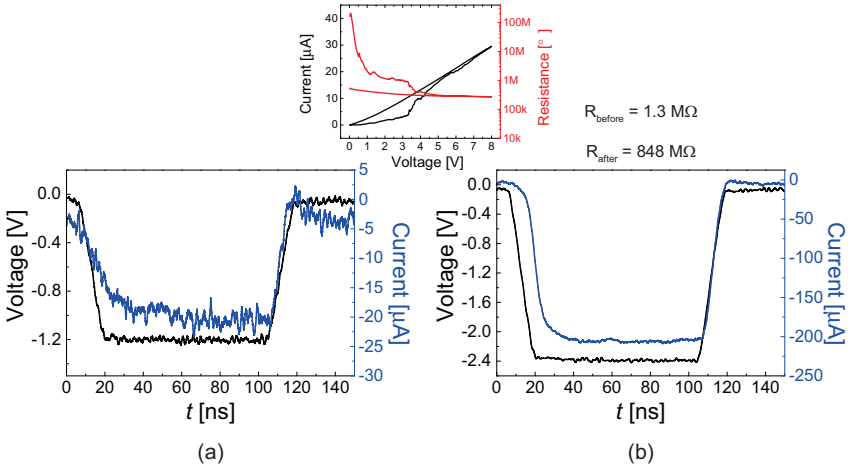


Figure 5.13: AC nonlinearity of a Pt/10-nm-thick TiO_2/Ti/Pt based memory element with 220 kΩ external series resistance.

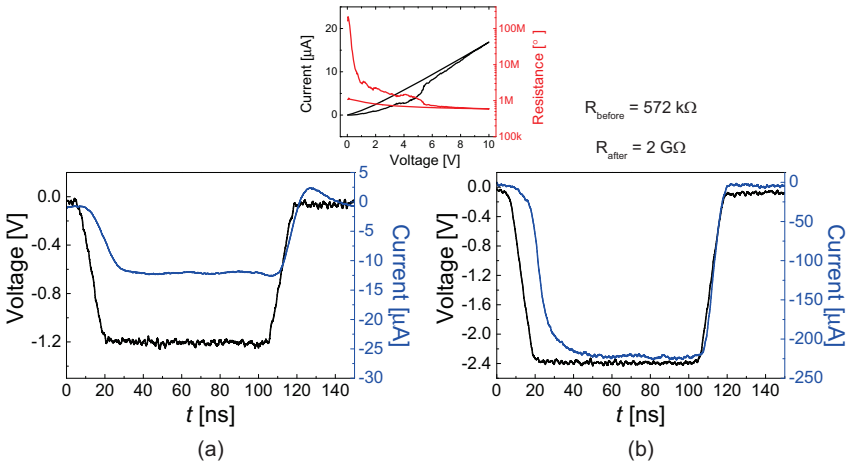


Figure 5.14: AC nonlinearity of a Pt/10-nm-thick TiO_2/Ti/Pt based memory element with 500 kΩ externalseries resistance.

vices were switched into the high resistance OFF state (R_{after}).
The transient currents during the RESET voltage pulses do not scale with the applied series resistance during the electroforming and SET and have approximately the same values of >200 µA. However, the measured $I(V_{\text{RESET}}/2)$ exhibit a clear dependence on the series resistance. The TiO_2based ReRAM device that was electroformed with $R_{\text{tip}} = 100$ kΩ shows the highest current of 50 µA (NL=4). In contrast, only 12.5 µA flow through the ReRAM element that was formed with the highest $R_{\text{tip}} = 500$ kΩ. This results in the NL=18. The summery of the AC NL parameters of the 10-nm-thick TiO_2 based devices is shown in Table 5.1.

R_{tip}	100 kΩ	220 kΩ	500 kΩ
I_{SET} (DC)	40 µA	30 µA	17 µA
$I(V_{\text{RESET}})$	210 µA	205 µA	225 µA
$I(V_{\text{RESET}}/2)$	50 µA	20 µA	12.5 µA
NL	4	10	18

Table 5.1: Nonlinearity parameter of the Pt/10-nm-thick TiO_2/Ti/Pt based ReRAM for the different series resistances R_{tip}.

In conclusion, the series resistance can be utilized to tune the AC nonlinearity parameter of the ReRAM devices. This can be explained by the scaling of the conducting filament by limiting the current during the SET process.

5.2 WO_3 Based Nano-Crossbar ReRAM

The ReRAM based on WO_3 are especially interesting because of its application in current CMOS circuits [3, 26, 130, 131]. The WO_3 based ReRAM devices were fabricated with the developed passive nano-crossbar technology platform to demonstrate its suitability for the integration of different resistive switching materials besides the TiO_2. The electroforming behavior of the VCM type WO_3 based ReRAM devices will be analyzed in this section.

5.2.1 Electroforming Characteristics

The WO_3 based nano-crossbar devices have the layer stack of Pt/25-nm-thick WO_3/Ti/Pt. The quasi-static electroforming process of the device by with the external series resistance of 100 kΩ is shown in the Figure 5.15. The devices exhibit initial resistances in the range of 1 TΩ at 2 V. When the applied voltage is raised to 6.2 V, the electroforming event is observed by the sudden increase in the measured current. The *R-V* graph shows a drop in the resistance of the device from 1 MΩ to 100 kΩ which is dominated by the series resistance. When the applied voltage is reduced, the measured resistance increases. Therefore, the *I-V* characteristics of the WO_3 based ReRAM devices exhibit the nonlinearity similar to the TiO_2 based devices. This can be attributed to the active Schottky-type Pt/WO_3 interface.

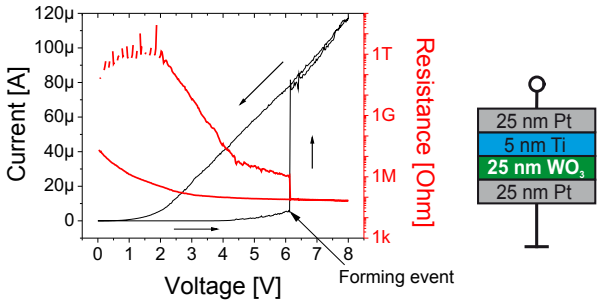


Figure 5.15: Electroforming *I-V* and *R-V* graph of a WO_3 based nano-crossbar device. The device layer sequence Pt/WO_3/Ti/Pt is also shown.

The statistical analysis of the electroforming behavior of the 25-nm-thick WO_3 based nano-crossbar devices is shown in Figure 5.16. The total of 180 devices

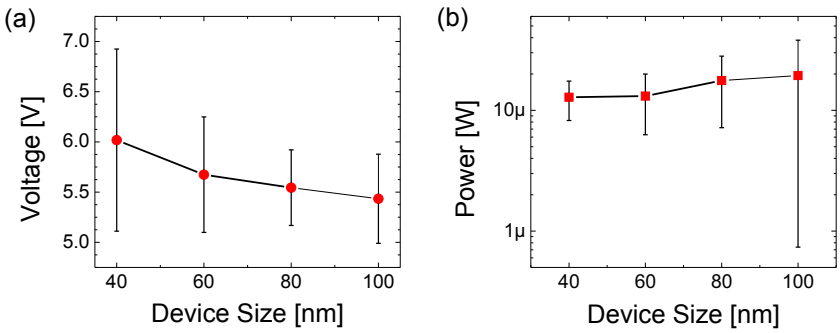


Figure 5.16: Electroforming voltage (a) and required power (b) of the 25-nm-thick WO_3 based ReRAM. The forming voltage increases with decreasing cell sizes while the power shows a slight decrease with the cell size.

were electroformed with series resistances of 47 kΩ, 100 kΩ and 500 kΩ. The mean values of the required forming voltages are shown in Figure 5.16 (a). The forming voltages increase for the decreasing ReRAM device sizes and additionally the deviation in the forming voltages becomes larger. The opposite trend is observed for the required power for the electroforming (Fig. 5.16 (b)). On average, the forming voltages of the WO_3 based devices are slightly higher than for the 25-nm-thick TiO_2 based devices. The ReRAM devices based on the two materials require equivalent power for the electroforming.

The effect of the different R_{tip} on the resistance states and thereby the currents during the first RESET process of the WO_3 based nano-crossbar devices is shown in Figure 5.17. The presented resistance values were read out at a voltage of 100 mV. They show a clear trend towards higher resistance states for higher applied series resistances. The devices formed with $R_{tip} = 100$ kΩ show the smallest deviation of the ON state of approximately 10 MΩ. The size dependence of the ON state is not observed. This leads to the assumption, that the resistive switching in the WO_3 based ReRAM devices can also be explained by the filamentary model [15]. Generally, the higher series resistances enable smaller RESET currents. However, the increased RESET currents (>100 µA) of the devices formed with $R_{tip} = 500$ kΩ can be explained by a breakdown of the devices into a permanent low resistance state during the first RESET process.

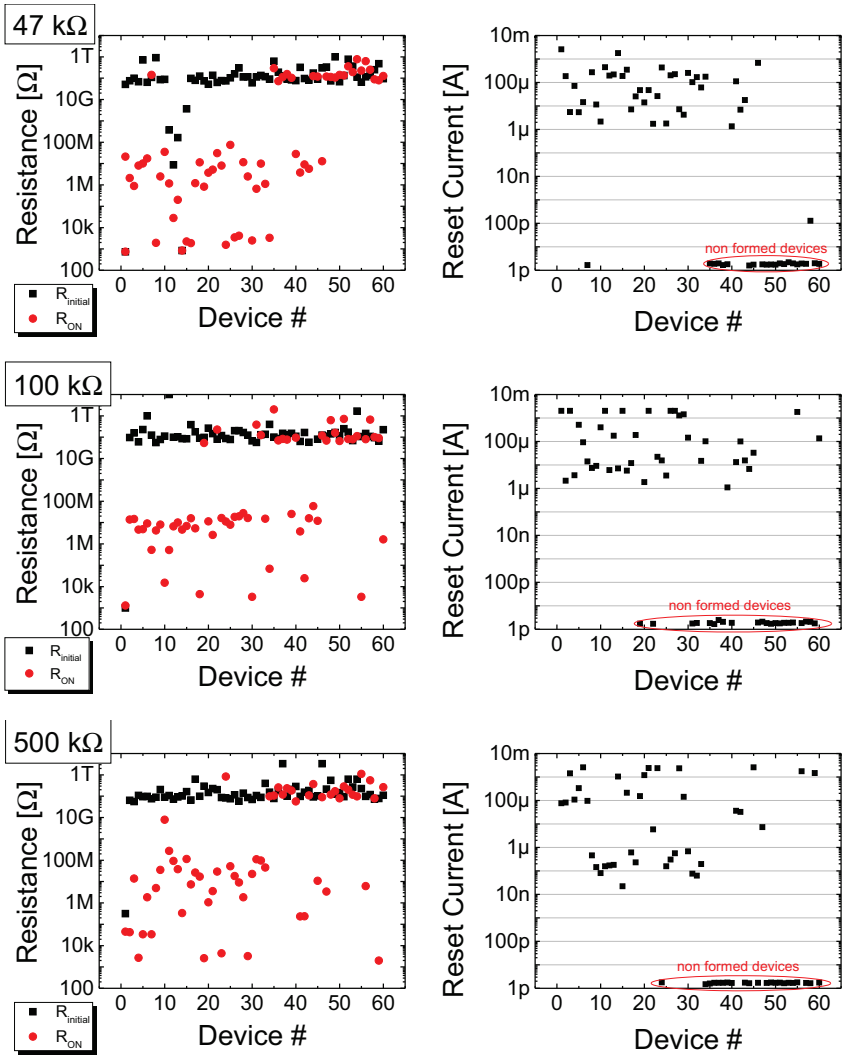


Figure 5.17: Resistances and maximum RESET current of 25-nm-thick WO_3 nanocrossbar devices for different series resistances.

Chapter 6

Electrical Characterization of Integrated ReRAM Devices

The preferred integration platform of ReRAM devices is the passive crossbar array. This is due to its simple device structure which enables a high memory density and makes this technology very cost efficient. However, the addressing of the memory elements in this configuration is challenging because of the sneak-path issue [129]. Three possible solutions to overcome this issue have been discussed in chapter 2. In this chapter, the transistor selected memory elements will be analyzed because they exhibit electrical characteristics that surpass the performance of conventional passive ReRAM elements with respect to low power operation and endurance [107,120,132,133]. This is attributed to the scaling of the conductive filament in the ReRAM element by the prevention of current overshoot phenomena [106]. The impact of the transistor on the resistive switching behavior of the integrated TiO_2 and WO_3 based 1T-1R memory devices, introduced in chapter 3.3, will be analyzed.

6.1 MOSFET Characterization

In order to confirm the functionality of the MOSFET devices, a quasi-static characterization was carried out on the B1500 parameter analyzer. The staring point of the electrical characterization of the 1T-1R devices is the determination of the output and input characteristics of the integrated n-channel MOSFETs. In this research work, the channel dimension of the transistor was fixed

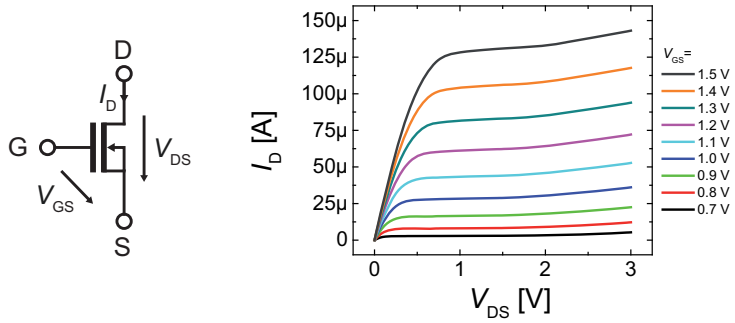


Figure 6.1: Output characteristics of the integrated n-channel MOSFET (W/L = 1/1 µm) with the connection scheme shown on the left side.

to 1 x 1 µm^2. In integrated ReRAM, the drain contact is established through a direct access (monitor pad) without the ReRAM element. The drain current I_D as a function of the applied drain-source voltage V_{DS} for different gate voltages V_{GS} is known as the output characteristics of the transistor, shown in Figure 6.1. Therefore, the current compliance during the ReRAM characterization can easily be controlled by the applied gate voltage. The achievable currents range from 1 µA to 150 µA which is suitable for the resistive switching applications.

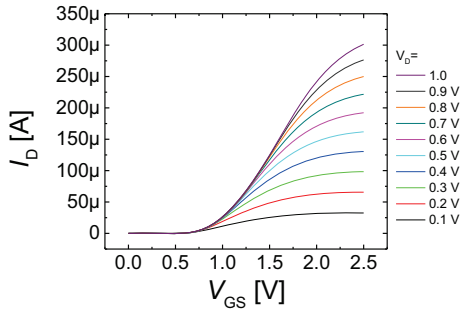


Figure 6.2: Transfer characteristics of the integrated n-channel MOSFET (W/L = 1/1 µm).

The corresponding transfer characteristics of the MOSFET are shown in Figure 6.2. Here, the triangular voltage sweep is applied to the gate of the transistor

for different fixed drain-source voltages. The resulting I_{D} is then measured and plotted over the V_{GS}.

6.2 TiO_2 based ReRAM in 1T-1R configuration

The electrical characterization of the TiO_2 based ReRAM in 1T-1R configuration is first carried out with quasi-static voltage sweeps. Therefore, the applied measurement scheme is introduced. Afterwards, the electroforming behavior as well as the SET and RESET characteristics of the memory elements with the transistor as the current limiter will be analyzed. Also, the impact of the oxide film thickness and the cell size will be discussed. The Nonlinearity in the I-V characteristics is especially important for the integration into future NVM and will be explored before the section is closed with the analysis of the achieved ultra low switching currents.

6.2.1 Quasi-static Electrical Characterization of Integrated ReRAM

The general circuit diagram applied for the quasi-static Forming, SET and RESET process is shown in Figure 6.3 (a). During the quasi-static Forming and also the SET, a stepwise increasing voltage ramp was applied to the top electrode of the memory element (bitline contact) while the source contact of the transistor was grounded. The maximum current through the memory element was controlled by applying the appropriate voltage to the gate contact pad of the transistor.
For the RESET, a current compliance is not required since it is a self-limiting process. Therefore, a voltage ramp of positive polarity was applied to the gate as well as the source contact while the bitline was grounded. The corresponding circuit diagram is shown in Figure 6.3 (b). This scheme prevented an excessive gate-source voltage drop that could damage the transistor. In this configuration, the transistor showed a diode like behavior.

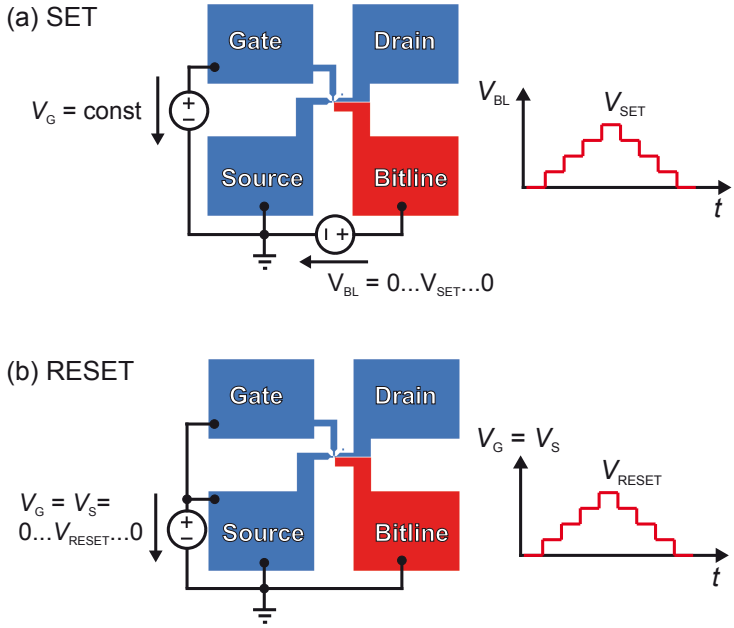


Figure 6.3: Circuit diagram for Forming/SET and RESET of the 1T-1R structure. (a) The SET is performed by applying a constant voltage to the gate contact and a positive voltage sweep to the bit line. (b) For the RESET the positive voltage sweep is applied to the gate and source while the bit line is grounded

6.2.2 Electroforming Characteristics of TiO_2 based ReRAM in 1T-1R Configuration

TiO_2 and WO_3 based ReRAM devices usually require an electroforming (in short: Forming), as mentioned in section 2.1. The negative current driven Forming routine for the TiO_2, as proposed by Nauenheim *et al.* [117], was not applicable for the 1T-1R devices since MOSFET is a voltage-driven device. Here, a positive voltage-driven routine was applied and the transistor served as the current limiter.

6.2.2.1 Impact of the Current Compliance

In order to enable the comparison of measurement results to previous works on reactive sputtered TiO_2 [39, 42, 118], the ReRAM cell with the 25-nm-thick

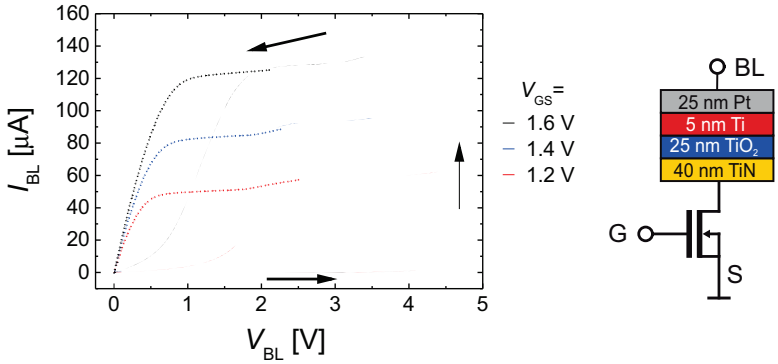


Figure 6.4: Electroforming of 25-nm-thick TiO_2 based 1T-1R devices. The dashed lines represent the transistor output characteristics for the given gate voltage. The circuit diagram with the complete layer stack is shown on the right side. [134]

TiO_2 layer was fabricated on the transistor platform. The $I-V-$ plots in Figure 6.4 represent the typical Forming behavior of the TiO_2 based 1T-1R memory elements. Their layer stack is shown in the right side of the figure. During the measurement, a positive voltage sweep was applied to the bitline contact. The initial resistance of the ReRAM cells read out at $V_{BL} = 0.5$ V was in the 10 GΩ range. The current through the memory element increases gradually with increasing voltage up to a voltage $V_{BL} \geq 4$ V. At this point the currents for all devices was between 500 nA and 5 µA. Then, the soft breakdown occurred and the bitline current increased drastically until it was limited by the transistor. The memory element was formed into the ON state. When the V_{BL} was decreased, the I-V trace was first dominated by the transistor behavior which is plotted with the dashed lines for the denoted gate voltages of 1.2 V to 1.6 V. For $V_{BL} < 1.5$ V the nonlinear ON state resistance of the memory elements limited the current and the I-V traces differed from the output characteristics of the MOSFET.

The ON state resistances of the ReRAM cell after the Forming were measured over the monitor pad with the SRS SR830 lock-in amplifier with a sinusoidal signal generating a voltage drop of 26.5 mV over the cell. They are shown in Figure 6.5.

A clear dependency of the ON state resistance on the maximum current, controlled by the gate voltage of the transistor during the electroforming step,

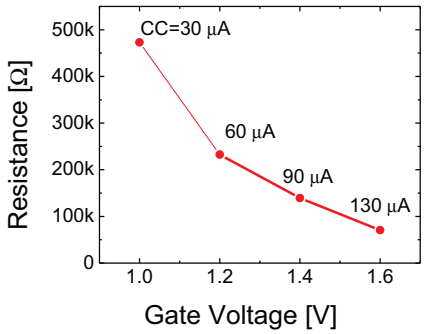


Figure 6.5: Impact of the compliance current on the resistance state after the electroforming for the TiN/25 nm TiO_2/Ti/Pt devices. Smaller gate voltages and lower current compliances result in higher resistances. [134]

was measured. The resistance value after the forming is inversely proportional to the I_C. Similar phenomena have been observed for other oxide materials like NiO_x, ZrO_x and HfO_x in the 1T-1R configuration [107, 120, 133]. The higher resistances are explained by scaling of the conductive filament diameter in the oxide material. This scaling is achieved by reducing the available current during the formation process. The two factors, the response time of the compliance and the discharge of the parasitic capacitance determine the actual current during the forming process [135]. Both factors are summarized as overshoot current which is minimized by the integrated transistor [106]. Therefore, it can be concluded that the current compliance from the integrated MOS transistor is crucial to have a proper control over the electroforming.
However, the minimum possible current compliance value for the 25-nm-thick TiO_2 memory elements was determined to be 30 µA. The further reduction of the I_C during the forming resulted in large cycle-to-cycle variability. This phenomenon has also been reported for the HfO_2 and is attributed to a smaller number of oxygen vacancies inside the filament [136]. Small fluctuations in the amount of vacancies inside the filament can therefore lead to large changes in the electrical behavior [137].

6.2.2.2 Impact of the Cell Size and the Oxide Layer Thickness

As explained in section 3.3.1, the 1T-1R platform offers the possibility for the integration of different memory element sizes. In addition to this, the planarized second generation samples enable the thickness scaling of the sputtered resistive switching layer since no step coverage issues occur. Therefore, samples with TiO_2 film thicknesses of 5 nm, 10 nm and 25 nm were fabricated and electrically analyzed.

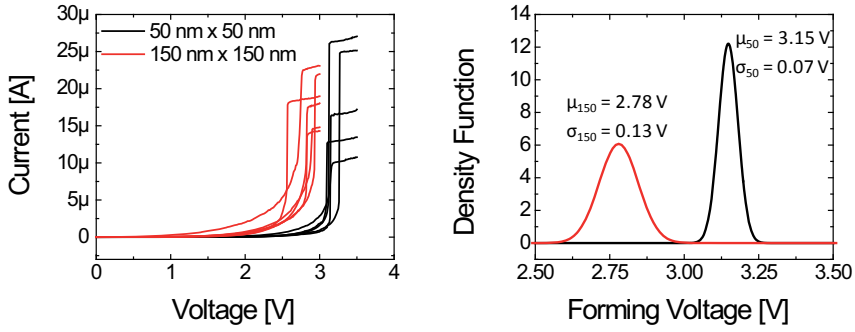


Figure 6.6: Forming voltages of the TiN/10-nm-thick TiO_2/Ti/Pt devices exhibit area scaling. The larger devices have the lower forming voltage as compared to the smaller devices.

The forming *I-V* graphs of the *10-nm-thick TiO_2* based 1T-1R devices are shown in Figure 6.6. Here, two different device sizes of 50 x 50 nm^2 (black) and 150 x 150 nm^2 (red) were measured with identical voltage sweep rates and comparable current compliance values. This is important because it was shown that the forming voltage ($V_{forming}$) depends on the sweeps rate [138]. Also, significantly different series resistances from the transistor change the voltage drop over the memory element and would lead to misinterpretation of the measurement results.

Similar to the 25-nm-thick TiO_2 devices, the 10-nm-thick TiO_2 exhibit a high initial resistance which shows in the low current for small voltages in the *I-V* plot. The devices of the two different sizes electroform at two clearly discriminable voltages. The smaller cells form at the larger mean voltage of 3.15 V as compared to the larger memory elements that have the forming voltage of

2.78 V. However, the deviation in the voltages $\sigma_{50} = 0.07V$ of the 50 x 50 nm^2 cells is slightly lower than the $\sigma_{150} = 0.13V$ of the larger memory elements. A possible explanation for this dependency is based on the stochastic nature of the forming process similar to dielectric breakdown [139, 140]. Peer groups proposed that weak spots at the grain boundaries in the crystalline material determine the forming voltage by supplying preferential paths for the oxygen vacancy movement [141, 142]. Since larger cells contain more grain boundaries in the oxide, there is a higher probability for the presence of such weak spots and thus the forming voltage is lowered [107].
The formation of the conducting filament inside the TiO_2 is known to be affected by electric field and the current induced temperature increase inside the ReRAM element [1, 119]. It is expected that the forming voltage depends on the thickness of the oxide layer since the electric field in a parallel plate MIM device is approximated by:

$$E = -\frac{\Delta\phi}{d} \tag{6.1}$$

with the distance d between the electrodes and $\Delta\phi$ being the potential difference between the electrodes which is equal to the applied voltage. Therefore, the same applied voltage results in a larger field if the oxide thickness is reduced. When comparing the forming voltage of the 10-nm-thick and the 25-nm-thick (Fig. 6.4) TiO_2 samples of $V_{\mathrm{BL}} = 3.15$ V and $V_{\mathrm{BL}} \geq 4$ V respectively, the expected reduction in the forming voltage is observed. However, the forming voltage does not scale linear with the film thickness. Therefore, it can be concluded that the forming process is not driven only by the electric field.

In order to further explore the scaling potential of the reactive sputtered TiO_2 layer thickness, the 1T-1R sample with the *5-nm-thick TiO_2* was fabricated. The electroforming behavior of the memory elements with the scaled down oxide thickness is shown in Figure 6.7. The devices exhibit a dependence of the forming voltage on the memory element size which is shown in Figure 6.8. The largest cells of 135 x 135 nm^2 have the lowest mean forming voltage of $V_{\mathrm{BL}} = 2.7$ V with a narrow distribution. The smaller cells exhibit larger forming voltages of $V_{\mathrm{BL}} \geq 3.1$ V.
The comparison of the forming voltages of the 10-nm-thick and the 5-nm-thick TiO_2 of equal cell sizes reveals that the reduction in V_{f} with decreasing

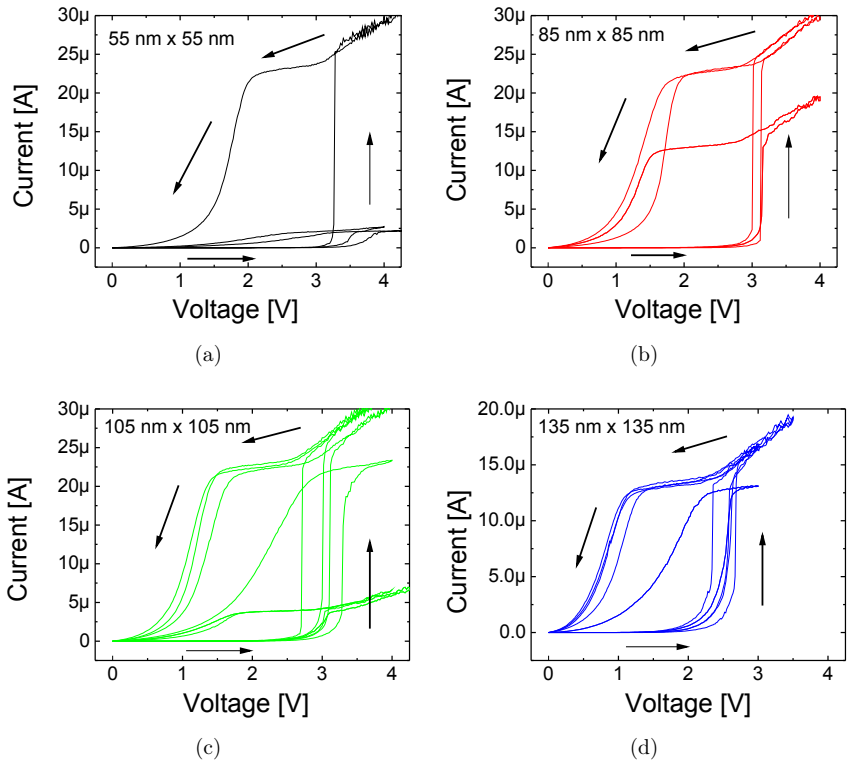


Figure 6.7: Electroforming characteristics of the TiN/5-nm-thick TiO_2/Ti/Pt based 1T-1R devices.

oxide layer thickness saturates. Both samples exhibit approximately the same forming voltages for the given memory element sizes.

The reported barrier for the reduction of the forming current compliance in the 25-nm-thick TiO_2 is overcome by scaling the oxide thickness to 10-nm-thick and 5-nm-thick TiO_2. In this case, the forming current compliance can be reduced to 1 µA. The reduction of the switching currents might be explained by the lower ratio of TiO_2 to Ti (1:1) as compared to the 25-nm-thick TiO_2 (5:1). This ratio results a higher density of oxygen vacancies since the Ti layer acts as an oxygen getter layer that provides oxygen vacancies through local oxidation during processing and under electrical stress [125, 126]. Therefore, a smaller energy is required to form a stable conducting filament. From this discussion,

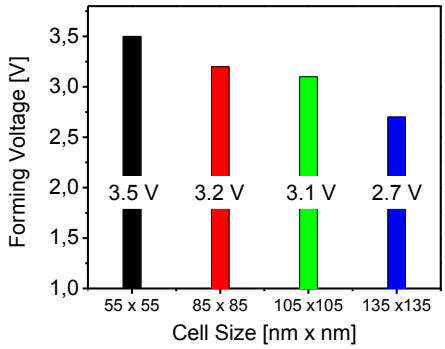


Figure 6.8: Device size dependence of the forming voltage of 5-nm-thick TiO_2 in 1T-1R configuration. The larger devices have a lower forming voltage than the smaller devices.

it can be concluded that a precise control of the I_C during the electroforming and active device thickness is indispensable to improve the ReRAM devices performance and lower down the power consumption [143].

6.2.3 SET and RESET Characteristics

The SET and the RESET characteristics of the ReRAM memory elements provide the figures of merit for the circuit designers like the switching or read voltages and currents, retention time, endurance and switching speed. In this subsection, the electrical characterization of the integrated 1T-1R devices after the electroforming will be shown. Further, the impact of the transistor compliance, the cycle to cycle variability and the oxide material comparison will be discussed.

The quasi-static I-V traces for the first RESET and SET after electroforming of the 1T-1R devices based on 25-nm-thick TiO_2 are shown in Figure 6.9. They correspond to the Forming graphs depicted in Figure 6.4. There, the forming current was precisely controlled by applying the respective V_{GS} to the integrated MOSFET.

The characterized memory elements were in the low resistive ON state after the electroforming. Therefore, the RESET had to be performed first, which

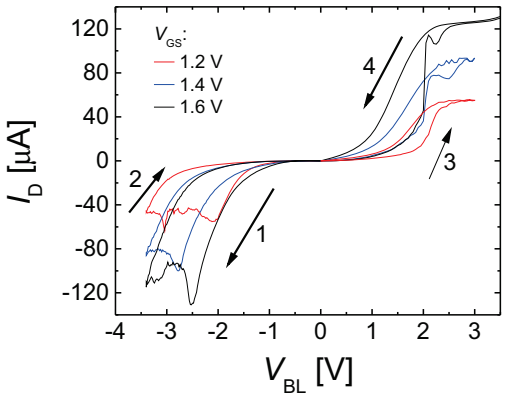


Figure 6.9: I-V characteristics of 25 nm TiO_2 based 1T-1R devices. The maximum RESET current scales depending on the SET compliance. [134]

is marked with the arrows 1 and 2. During the RESET process, no current compliance was used. The RESET in the TiO_2 is not an abrupt process with a sudden decrease of the cell current. In fact, the RESET behavior in Figure 6.9 shows a gradual decrease which can be attributed to the displacement of the oxygen vacancies away from the active TiN/TiO_2 interface.

It is also found, that the maximum RESET currents (I_{RESET}) for the 25-nm-thick TiO_2 based 1T-1R devices are reduced in comparison to 1R devices [1]. In addition, the I_{RESET} scales with the utilized transistor current compliance values during the electroforming. It can be reduced to 60 µA. This scaling of the I_{RESET} can be explained by the fact that the MOSFET effectively controls the filament formation inside the ReRAM device and prevents any excessive overshoot current [106].

Next, the SET was performed with the MOSFET current compliance (Fig. 6.9 arrow 3 and 4). The same V_{GS} values as during the electroforming were applied to the gate contact. The TiO_2 1R memory elements generally exhibit an abrupt SET process [1]. This holds true for the 1T-1R device that was SET with the compliance current of 120 µA at the $V_{\mathrm{GS}} = 1.6$ V. Here, a sudden increase in the drain current at $V_{\mathrm{BL}} = 2.1$ V is observed. However, for the lower compliance currents the jump in the I-V trace vanishes and the current rises gradually. This indicates the controlled formation of the conducting filament.

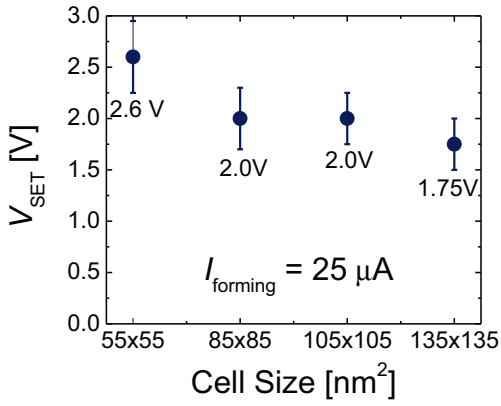


Figure 6.10: Dependence of the SET voltage on the device size for 5-nm-thick TiO_2.

The negative differential resistance is observed during the SET process for voltages lager than 2 V. This might be explained by the voltage divider consisting of the two non-linear resistors (MOSFET and ReRAM) [134]. When the memory element switches into the LRS, the voltage drop and also the electrical field over the memory elements is suddenly reduced. Therefore, the memory element is less conducting which shows in the negative resistance behavior. The further voltage increase switches the device into the stable ON state.

The cell size dependence of the SET voltage for the *5-nm-thick TiO_2* based 1T-1R devices was analyzed in this research work. The results are shown in Figure 6.10. For the same forming condition of I_C = 25 μA, the SET voltages increase for smaller device sizes. This is comparable with the cell size dependence of the electroforming.

6.2.3.1 Variability in the Resistive Switching Characteristics

Small cycle-to-cycle scattering in the switching parameters is crucial for the implementation of the redox-based resistive switching devices into future non-volatile memory. The variability in the switching characteristics is especially interesting for the 1T-1R devices operated at low currents. Since the smaller amount of oxygen vacancies is expected to be involved in the switching, the large cycle-to-cycle variability could be assumed.

The electroforming and the first 10 resistive switching cycles of the *10-nm-thick* TiO_2 memory element in 1T-1R configuration are shown in Figure 6.11. Since

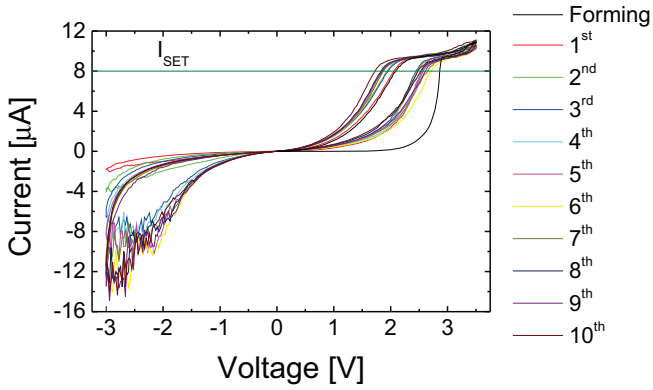
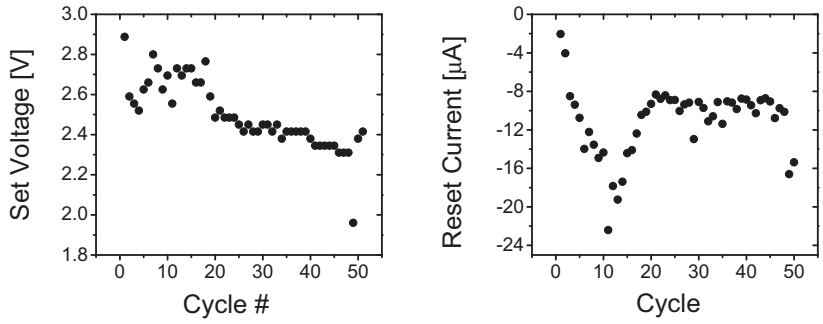


Figure 6.11: I-V characteristics of 10-nm-thick TiO_2in 1T-1R configuration.

the memory element exhibits the gradual SET characteristics, the set voltage cannot be defined as the voltage where the jump in the current occurs. Here, a current level that is usually between 10-20% below the current compliance value is defined as the SET current (I_{SET}). The voltage corresponding to the point where this current level is reached is the SET voltage (V_{SET}). In Figure 6.11, the $I_{\mathrm{SET}} = 8$ μA for the current compliance of 9-10 μA is defined and marked with the green line. The I_{RESET} is defined as the maximum current during the RESET process.

The extracted data for the SET voltage over the cycle number is shown in Figure 6.12 (a). During the first 20 cycles after the electroforming, the SET voltage scatters between 2.5 V and and 2.8 V. Afterwards, the SET voltage reaches a steady state with smaller variability. However, a slight decrease in the V_{SET} is still observed.

The high initial variability is also present in the I_{RESET} data (Fig. 6.12 (b)). While the first RESET requires a very low current of only -2 μA, a steady increase until to the 11^{th} cycle with the $I_{\mathrm{RESET}} = -22$ μA is measured. Then, the maximum RESET current decreases and reaches a mean value of $I_{\mathrm{RESET}} = -9$ μA at the 20^{th} cycle. This matches the applied current compliance value. The subsequent variability in the maximum current is small. The



(a) (b)

Figure 6.12: Extracted values for (a) the SET voltage and (b) the maximum RESET current of the 10-nm-thick TiO_2.

possible explanation for this phenomenon could be the redistribution of oxygen vacancies, that constitute the conducting path, during the high variability part of the experiment.

In order to analyze the impact of the change in current compliance on the switching variability, a total of 100 switching cycles with two different current compliances were performed. First, the 1T-1R device with the 10-nm-thick TiO_2 was electroformed and SET with the I_C of 13 µA for 50 cycles (Fig. 6.13 (a)). Afterwards, the applied gate voltage was raised to the $I_C = 23$ µA (Fig. 6.13 (b)). The I_{SET} (green) were defined to be 11.5 µA for the first half and 21.5 µA for the second half of the switching cycles.

Figure 6.13 (c) and (d) illustrate the impact of the compliance level on the V_{SET} and I_{RESET} respectively. As expected, the $V_{forming} = 2.62$ V is higher than the SET voltages of the subsequent cycles. The scattering of the V_{SET} in this ReRAM element is rather small. However, some cycles have to be performed before the SET voltage levels off at 2.45 V. When the current compliance is changed, an increase of the SET voltage is observed. Again, this increase is not abrupt but the voltages gradually settle down at 2.6 V.

The maximum RESET currents exhibit two levels in dependence of the SET compliance. They first settle at -7 µA before the current compliance is increased and the new I_{RESET} level of -10 µA is reached after some cycles. It seems like the electroforming and first few switching cycles define the state of

the memory element because the I_{RESET} increases only slightly even though the compliance during the SET process is almost doubled. It should be pointed out, that the scatter in the maximum RESET current is small.

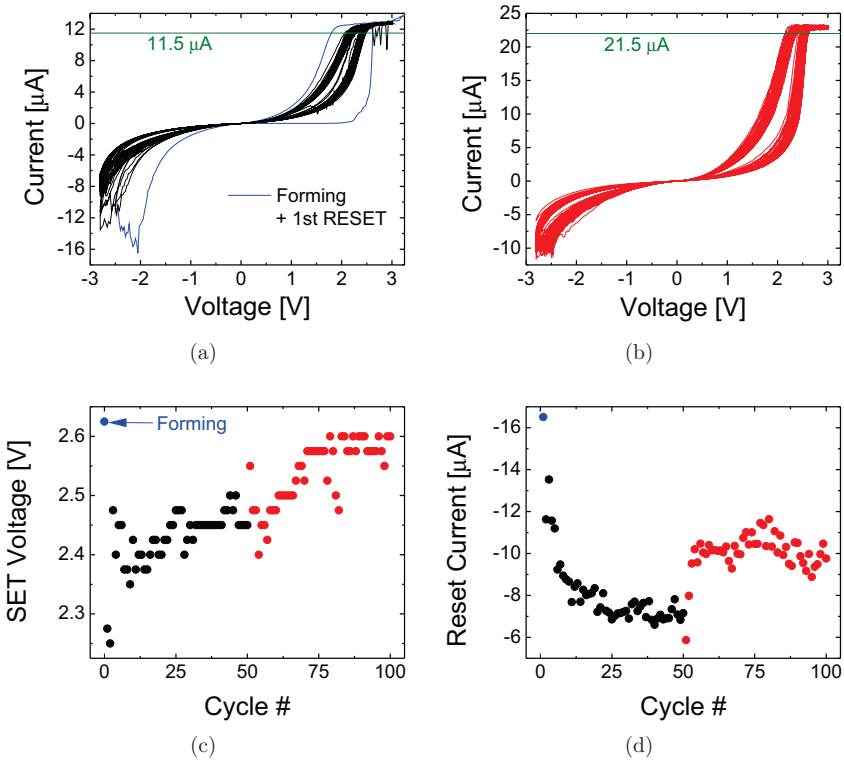


Figure 6.13: Impact of the current compliance on the observed variability in the switching parameters. (a) The memory element is formed and switched 50 times with the lower current compliance. (b) 50 I-V cycles with the higher compliance were performed afterwards. (c) Extracted data for the V_{SET} and (d) I_{RESET}.

6.2.4 AC Nonlinearity of the Integrated 1T-1R Devices

In order to integrate the TiO_2 ReRAM devices into the passive nano-crossbar architecture, a high degree of nonlinearity in the I-V characteristics is required [129], since this property is important to prevent the parasitic current flowing through sneak paths [33, 144]. Especially the nonlinearity of the ON state is highly important for this purpose. The nonlinearity in HfO_2 and other metal-oxide ReRAM has been investigated by peer groups [136] and has generally been controlled by material engineering [144, 145]. In this research work, the nonlinearity in the TiO_2 ReRAM devices was modulated by using the MOS-FET current compliance during the electroforming and SET process.
The circuit diagram for the nonlinearity measurement is shown in Figure 6.14. The 25-nm-thick TiO_2 based 1T-1R devices where first electroformed and SET by quasi-static I-V sweeps (DC) with the transistor compliance in order to determine the impact of the properly controlled currents. The corresponding Forming and SET graphs are shown in Figure 6.4 and 6.9 respectively.

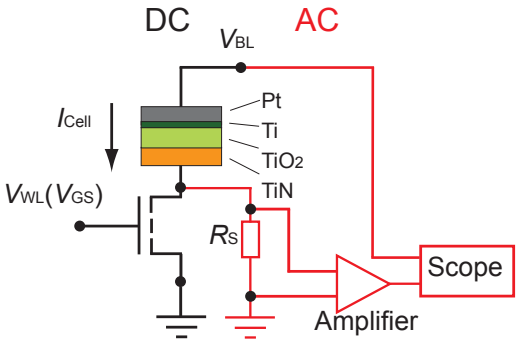


Figure 6.14: Circuit diagram of the AC nonlinearity measurement. First the cell is formed and SET with the transistor as current compliance (DC). Afterwards, the RESET experiment is performed without the transistor (AC). [134]

After the memory elements were switched into the ON state, the nonlinearity measurements were performed. The voltage pulses with a width of 100 ns were applied to the ReRAM cell while monitoring the transient current response through the monitor pad (AC). This enables the analysis of the resistance states without the influence of the transistor.
First, the nonlinearity measurement of *passive crossbar elements (1R)* with

the TiN/10-nm-thick TiO_2/Ti/Pt layer stack was performed and is shown in Figure 6.15. This is an example of the memory element that was formed and switched to the ON state by quasi-static sweeps with the current compliance of 50 µA from the semiconductor parameter analyzer. It is meant to point out the differences between the transistor and the instrument current compliance with respect to the NL. The resistances before and after the pulse application where determined to be $R_{\text{before}} = 12.7$ kΩ and $R_{\text{after}} = 2$ MΩ respectively.

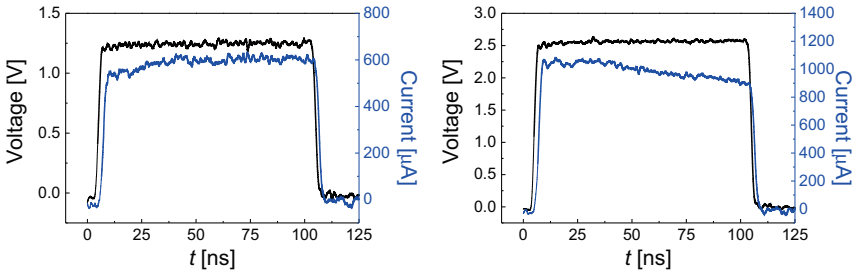


Figure 6.15: Nonlinearity pulse measurement on the 10-nm-thick TiO_2 1R ReRAM element. The nonlinearity value is calculated from the transient current response for the $V_{\text{RESET}}/2$ (a) and $V_{\text{RESET}}/$ (b) pulses.

The transient currents reach peak values of 600 µA for the $V_{\text{RESET}}/2$ and 1100 µA for the V_{RESET} pulse. This results the nonlinearity NL≈2 which is a linear state. This ohmic behavior is explained by the overshoot phenomenon that causes an uncontrolled formation of the conducting filament.
The nonlinearity measurements on the 1T-1R device with the TiO_2 layer thickness of 25 nm are shown in Figure 6.16.
The cells were switched with voltage pulses of $V_{\text{RESET}} = 3$ V (Fig. 6.16 (b),(d),(f)). Therefore, the $V_{\text{RESET}}/2$ had the amplitude of 1.5 V (Fig. 6.16 (a),(c),(e)). The current compliance values for the quasi-static switching to the ON state are marked in the box above each sub-figure. It must be pointed out that the transient currents during the RESET pulses exhibit a decrease depending on the applied I_{C} from 300 µA to 200 µA. The observed decrease in the transient currents for the $V_{\text{RESET}}/2$ pulses from 125 µA to 27 µA is considerably larger. Therefore, the calculated NL in Figure 6.17 shows the increase from 2.5 to 7.4 for decreasing transistor current compliances.

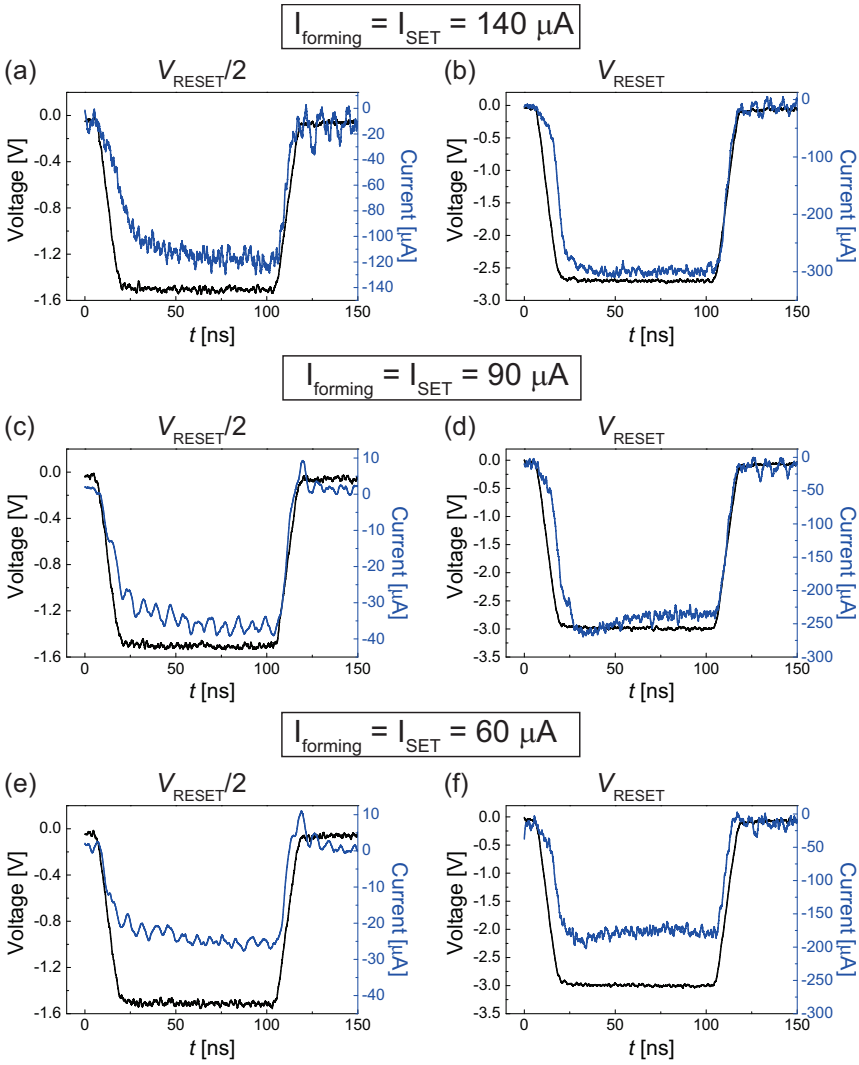


Figure 6.16: Voltage pulse measurement for the analysis of the nonlinearity of 25-nm-thick TiO_2 1T-1R devices.

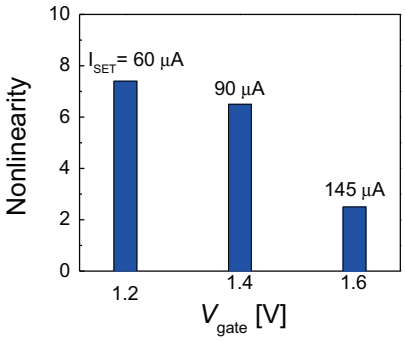


Figure 6.17: Calculated nonlinearity parameters of the TiO_2 based 1T-1R devices. [134]

The highest nonlinearity of 7.4 is achieved for the lowest I_C (60 µA). These results could be interpreted with the filamentary model [15] in the following way: a higher I_C generates a stronger filament in the ReRAM device and leads to enhanced ohmic behavior of the LRS state. To toggle this device back into the HRS or dissolve the filament, the higher current/energy is required. Therefore, the reset current and the nonlinearity is a function of the I_C.

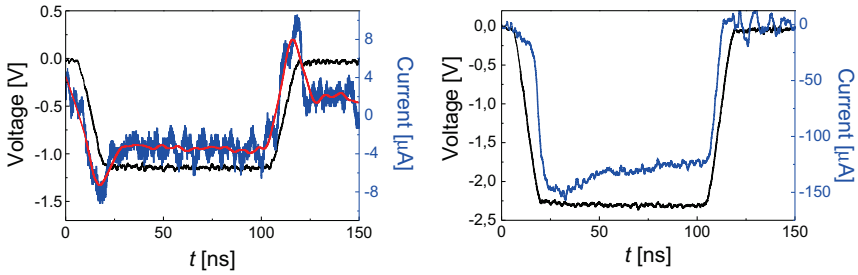


Figure 6.18: Nonlinearity measurement on the 10-nm-thick TiO_2 based 1T-1R device.

A further reduction of the forming and SET currents was achieved for the 10-nm-thick TiO_2 based 1T-1R devices. Since the NL depends on the current compliance, it is expected that these devices can be tuned to higher nonlinearity. The transient current responses of the nonlinearity measurement on the thinner 1T-1R device, switched with the $I_C = 25$ µA, are shown in Figure

6.18. From the peak currents of 150 µA and 5 µA for the V_{RESET} and $V_{\mathrm{RESET}}/2$ respectively, the nonlinearity of 30 is calculated. This is another evidence for the aforementioned dependence of the nonlinearity on the current compliance. In addition, it can be concluded that the reduction of the oxide layer thickness is beneficial for the nonlinearity and thereby the integration of TiO_2 in non-volatile memory.

6.2.5 Ultra Low Current Switching in TiO_2 Based ReRAM

The main advantage of ReRAM in 1T-1R configuration is the superior control of the switching current by the transistor. In this section, the ultra low switching current of the 5-nm-thick TiO_2 based integrated ReRAM will be demonstrated. First, the electrical characterization by quasi-static voltage sweeps will be shown. This will be followed by the fast voltage pulse measurements.

6.2.5.1 Quasi-static Electrical Characterization

In order to enable the ultra low current switching, the 5-nm-thick TiO_2 ReRAM element was electroformed with the transistor as the current limiter. The gate voltage of $V_{\mathrm{GS}} = 0.6$ V was applied to the transistor which results in a maximum current during the electroforming of $I_{\mathrm{BL}} = 2.5$ µA, shown in Figure 6.19. This is important because it was demonstrated in this research work, that the

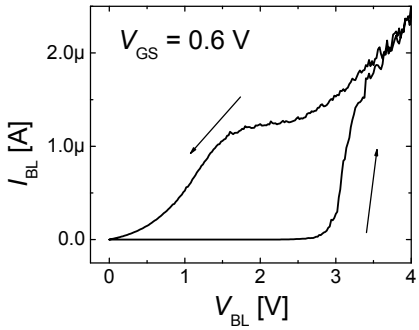
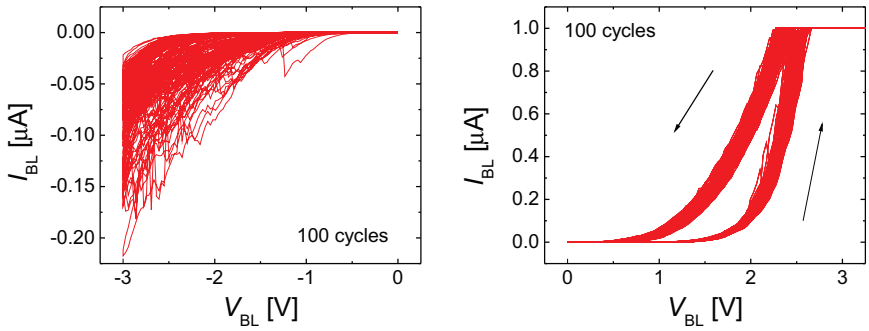


Figure 6.19: Forming characteristic of the 5 nm-thick ultra low current TiO_2 1T-1R device. The current during forming and SET is controlled by the gate voltage $V_{\mathrm{GS}} = 0.6$ V.



(a) (b)

Figure 6.20: I-V characteristics of the ultra low current TiO_2 1T-1R devices. The memory element exhibits unsymmetric currents for (a) RESET and (b) SET.

electroforming process defines the electrical characteristics of the ReRAM device after the forming. Initially the TiO_2 device is in the very high resistance virgin state. At the voltage of approximately $V_{BL} = 3$ V the current increases fast but still gradually until it is limited by the transistor. After the electroforming, the device is in the switchable ON state.

The DC switching behavior of the 5-nm-thick TiO_2 based 1T-1R device is shown in Figure 6.20. The measurement conditions comparable with the electroforming were applied to the memory element ($V_{GS} = 0.6$ V). The current is limited to 1 µA for the 100 DC SET cycles in Figure 6.20 (b). The ReRAM device exhibits remarkable small variability in the set voltage ($V_{BL} = 2.5$ V) and clear distinguishable ON and OFF states.

The RESET of the ultra low current TiO_2 based integrated device is shown in Figure 6.20 (a). The RESET voltage of -3 V was applied to the bitline of the 1T1R device. The RESET behavior shows high variability, which is in contrast to the SET. The maximum measured reset current is 218 nA and for most of the 100 cycles the current is below 100 nA. The I-V graph in the ultra low current regime is unsymmetrical with the considerably smaller RESET current compared to the applied SET current limit. This could be explained by the rectifying behavior of the Schottky barrier at the TiN/TiO_2 interface. Because of the low currents during the SET, the oxygen vacancies concentration in the interface region is lower and the barrier height is less reduced in comparison to

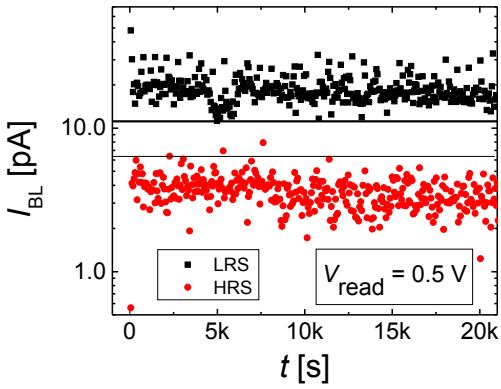


Figure 6.21: Room temperature retention measurement of the ultra low current ReRAM device

the higher current SET. Therefore, the rectifying behavior in reverse direction is more pronounced.

Peer groups have reported that the retention of the resistive switching memory elements depends on the diameter of the conduction filament [137, 146]. It was also proposed that this dimensions of the CF scale with the applied current compliance [147]. Therefore, it had to be explored if the 5-nm-thick TiO_2 devices in 1T-1R configuration, switched at ultra low currents, are non-volatile. Retention measurements of the ON and OFF state were performed and are shown in Figure 6.21. The retention measurements were carried out at room temperature. The device was first switched to the SET and afterwards to the RESET state. For each state, voltage read pulses of 0.5 V and a width of 1 s with the period of 1 min were applied for more than $2 \cdot 10^5$ s. The $R_{OFF}/R_{ON} \approx 4$ was measured and no degradation of either of the resistance states is observed. Although, measurements at elevated temperatures are generally required to determine the retention time, it can still be concluded from the performed measurements that the resistance states have at least several hours of retention time.

6.2.5.2 AC Characterization

To demonstrate the application feasibility of the TiO_2 based 1T-1R devices for the, the electrical characterization with short voltage pulses was carried out in cooperation with A. Fantini from IMEC Belgium. The measurement scheme that was applied for the AC endurance test as well as the switching kinetics experiment are shown in Figure 6.22.

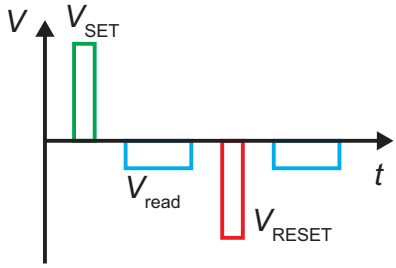


Figure 6.22: Voltage pulse scheme applied for the endurance measurement. SET and RESET pulses of varying pulse width are applied. The cell resistance is determined by read pulses of constant amplitude and duration.

The voltage pulses of different pulse width were applied to test the required voltage stress time to SET and RESET the devices. For voltage pulse width smaller that 100 µs, a precise detection of the ultra low switching currents (<1 µA) with the utilized Keithley Model4200-SCS semiconductor parameter analyzer is not possible. Therefore, the device resistances after each write pulse were determined by read pulses of constant width and amplitude.
Figure 6.23 shows the endurance measurement of the ultra low current TiO_2 device. With the applied $V_{GS} = 0.6$ V, the transistor limited the current to less than 10 µA during the SET. Voltage pulses of 3 V amplitude were applied for the SET while the RESET was performed by voltage pulses with the amplitude of -3 V. The pulse width was fixed to 100 µs during this measurement. The measured currents during the read pulses of $V_{BL} = -1$ V have a value of approximately 40 nA for the ON state with excellent switching variability. The large scatter in the OFF state is explained by the limitation of the measurement resolution. However, the memory window of 100 was measured. In addition, the device did not show any degradation in the switching characteristics during

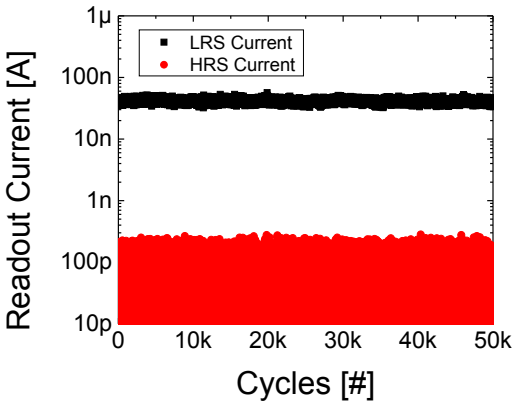
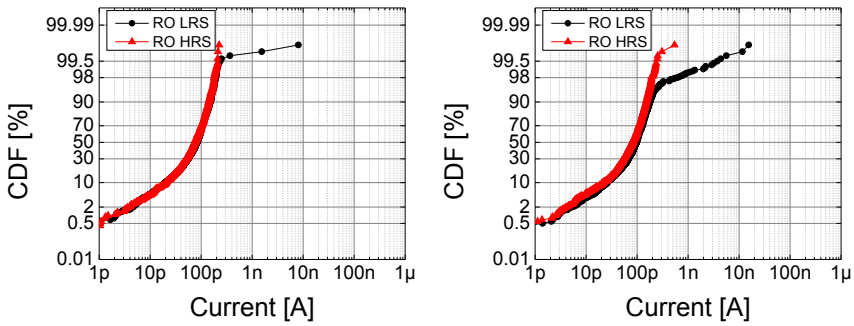


Figure 6.23: Endurance of the ultra low current ReRAM device

the measurement up to 50k cycles.

Furthermore, the endurance test for different pulse width has been performed. The amplitude of the SET and RESET pulses was fixed and the same readout scheme was applied. The the cumulative distribution functions (CDF) of the measured read currents are shown in Figure 6.24. For the given voltage pulse amplitude, the 100 ns pulses were not sufficient to change the resistance state of the TiO_2 based 1T-1R device and less then 1% of the cycles showed a difference between the two states (Fig. 6.24 (a)). When the pulse width is increased (Fig. 6.24 (b),(c)), the memory window begins to open. However, the variability in the currents for the LRS are still high. A steady state with low variability is achieved for voltage pulses with a width of 100 µs, as state before. It was shown by Hermes, that the pulse width for successful writing of the memory elements can be reduced by orders of magnitude when the pulse amplitude is raised [42]. This provides the prospect of reducing the writing time for the ultra low current 1T-1R devices while maintaining the good variability in the future.

The direct comparison of the measurements with different pulse width is given in Figure 6.25. It is interesting, that the measurement results for the 100 µs voltage pulses are identical to the currents of the 1 ms voltage pulses and are hidden behind the 1 ms graph. This is related to the limitation of the current through the device by the transistor that determines the ON state resistance.



(a) 100 ns

(b) 1 µs

(c) 10 µs

(d) 100 µs

Figure 6.24: Switching kinetics of the 5-nm-thick TiO_2 based 1T-1R device.

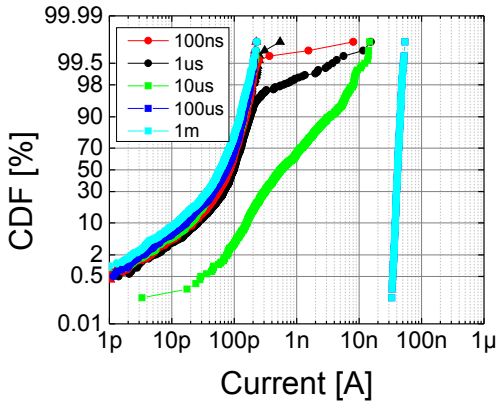


Figure 6.25: Summery of the switching kinetics of the 5-nm-thick TiO_2 based 1T-1R device.

Therefore, the longer switching time does not result in different resistance states.

In summery, the fabricated 5-nm-thick TiO_2 based ReRAM elements with the transistor as selector device exhibited superior performance in terms of endurance, variability and low power consumption during switching.

6.3 WO_3 based ReRAM in 1T-1R configuration

Besides the TiO_2 based devices, memory elements based on WO_3 were integrated into the 1T-1R platform. This enables the comparison of the ReRAM performance of the two material systems.

6.3.1 Electroforming Behavior

The analyzed devices had a layer sequence of TiN/30-nm-thick WO_3/W/Pt (Fig. 6.26). The WO_3 layer thickness was selected because thinner films did exhibit high leakage currents in the pristine state. Therefore, the WO_3 based ReRAM devices are expected to require large forming voltages owing to the higher film thickness. However, as described in section 6.1, the applied bitline voltage must not exceed 4.5 V.

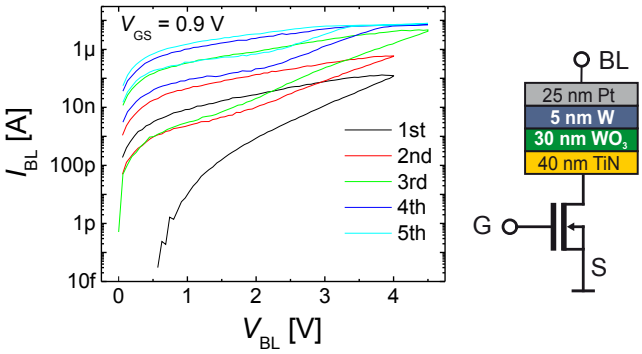


Figure 6.26: WO_3 based 1T-1R device are formed by the gradual process. The memristive behavior of the memory element enables the electroforming by consecutive I-V cycles.

The electroforming of the WO_3 based 1T-1R device by I-V sweeps with the transistor acting as current compliance is shown in Figure 6.26. The gate voltage was kept constant at 0.9 V during the measurement. The first two sweeps were carried out with the maximum $V_{BL} = 4$ V. Here, the forming event in the form of a sudden jump in the I-V trace was not observed. However, a hysteretic behavior was measured with an increasing current for consecutive sweeps. In the fifth sweep, the bitline current reaches the compliance current level at the reduced voltage of 3.4 V. The cell is now in a switchable low

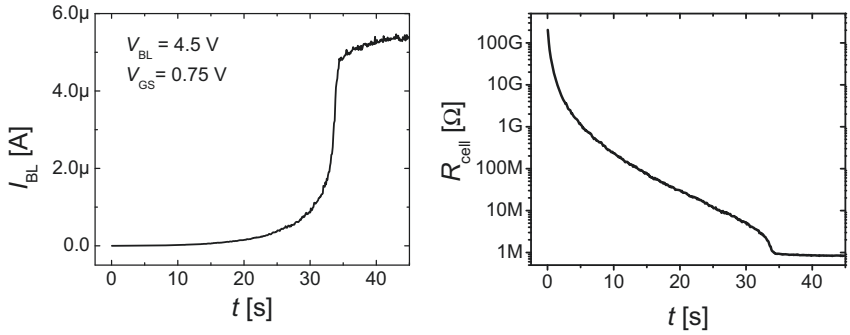


Figure 6.27: Electroforming of the WO_3 cell by constant voltage stress. (a) $I(t)$ graph and (b) corresponding resistance of the 1T-1R device

resistance state which will be shown in section 6.3.2. This gradual forming process is linked to the memristive nature of the ReRAM elements [116, 148]. An alternative forming routine is shown in Figure 6.27. Here, a constant voltage stress of 4.5 V on the bitline is applied to the memory element with the transistor gate voltage of 0.75 V. The evolution of the current over time is monitored and the measurement is stopped when the current reaches the steady state that is limited by the current compliance. Because of the high forming voltage, the smaller devices of this sample could not be formed into the switchable state and therefore no cell size dependent measurements were possible for the WO_3 based 1T-1R elements.

6.3.2 Variability in the SET and RESET Characteristics

The variability in the switching parameters was analyzed for the *30-nm-thick WO_3* based 1T-1R elements. Again, a low current regime (13 µA) was applied. The I-V graphs of 50 consecutive switching cycles are shown in Figure 6.28. The SET process of the 30-nm-thick WO_3 based 1T-1R element is very similar to the gradual transition to the ON state of the TiO_2. The I_{SET} was defined to 11.5 µA. Because of the larger film thickness, higher voltages as compared to the TiO_2 are required to toggle the WO_3 cell to the SET state. During the course of the 50 resistive switching cycles, the V_{SET} exhibits a linear increase as shown in Figure 6.29 (a). The scatter of the maximum RESET current of the

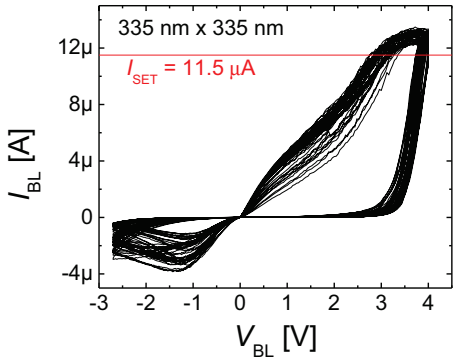
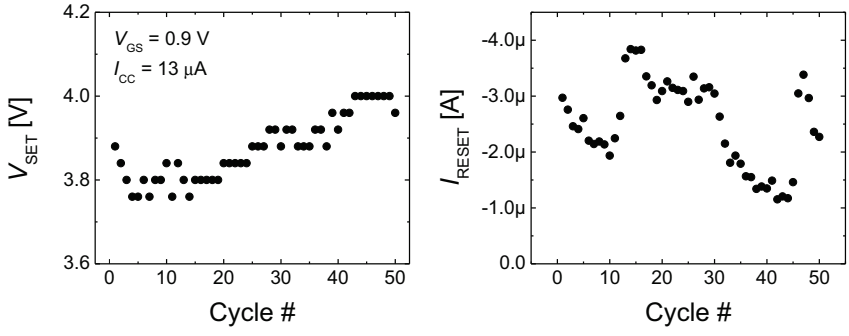
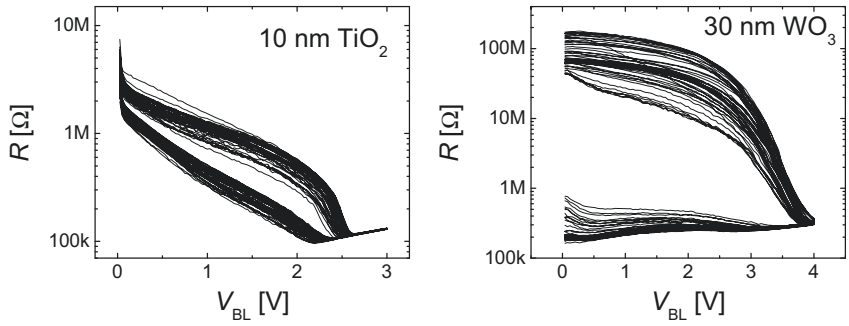


Figure 6.28: Electrical characteristics of 30-nm-thick WO_3 in 1T-1R configuration. The graph shows 50 consecutive switching cycles with the current compliance of 13 µA.



(a) (b)

Figure 6.29: Variability of the V_{SET} (a) and I_{RESET} (b) of the 30-nm-thick WO_3.



(a) (b)

Figure 6.30: Comparison of the resistance states of TiO_2 and WO_3. (a) The TiO_2 based memory element exhibits nonlinear resistance states. (b) Constant resistance states are observed for the WO_3 based memory element.

measured device is larger than the variability of the TiO_2 ReRAM elements. A clear trend towards a certain current level is not observed. However, the RESET currents of the WO_3 based 1T-1R device are below 4 μA which is considered to be very small for a VCM type memory element [149].

The comparison of the resistance states of the two integrated resistive switching oxide materials in the 1T-1R configuration are shown in Figure 6.30. Although the TiO_2 (a) and WO_3 (b) ReRAM cells were electroformed and switched with very similar parameters, they differ strongly in their resistance states. The TiO_2 memory elements feature the nonlinear I-V behavior that shows in the increasing resistances for lower voltages of the ON and OFF state. This is attributed to the Schottky barrier at the TiN/TiO_2 interface [150]. In contrast to this, the WO_3 device exhibits constant ON and OFF resistance states and the switching current is linearly dependent on the applied voltage. However, the OFF/ON ratio read out at 1 V is considerably larger for the WO_3 (≈ 240) than that of the TiO_2 (≈ 4).

6.4 Issues Regarding 1T-1R Characterization

As discussed, the 1T-1R configuration offers several advantages in ReRAM technology. However, some issues occur during the electrical characterization for the given device dimensions of W/L=1 µm/1 µm of the transistor in 65 nm CMOS technology. Two of these issues, that make the thorough investigation challenging, will be discussed in this subsection.

The first issue is the limited drain source voltage V_{DS} that the transistor can tolerate. As stated before, V_{DS} values larger that 4.5 V did frequently destroy the transistor. This is especially disadvantageous for the electroforming since it generally requires larger voltages than the subsequent switching cycle. The typical output characteristics of the MOS transistor before and after the electroforming of a 25-nm-thick TiO_2 memory element is shown in Figure 6.31. The degradation is clearly visible. Therefore, the selection of the applied oxide materials and film thicknesses is restricted to those that exhibit the low forming and switching voltages.

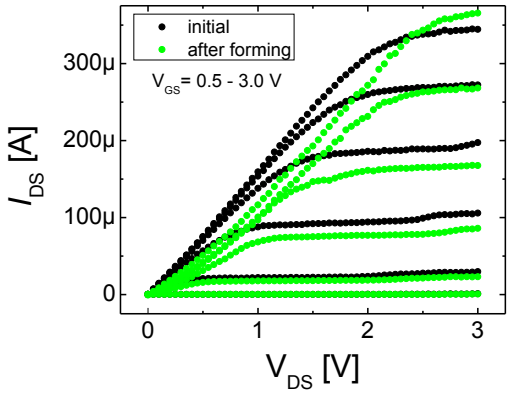


Figure 6.31: The voltages required for the electroforming result in a degradation of the MOSFET output characteristics after electroforming.

Another issue was found during the first RESET switching cycle of the TiO_2 based 1T-1R devices after the electroforming. The typical switching behavior for the successful RESET is shown in Figure 6.32 (a). The memory element starts in the LRS, then the gradual RESET occurs for the applied voltage

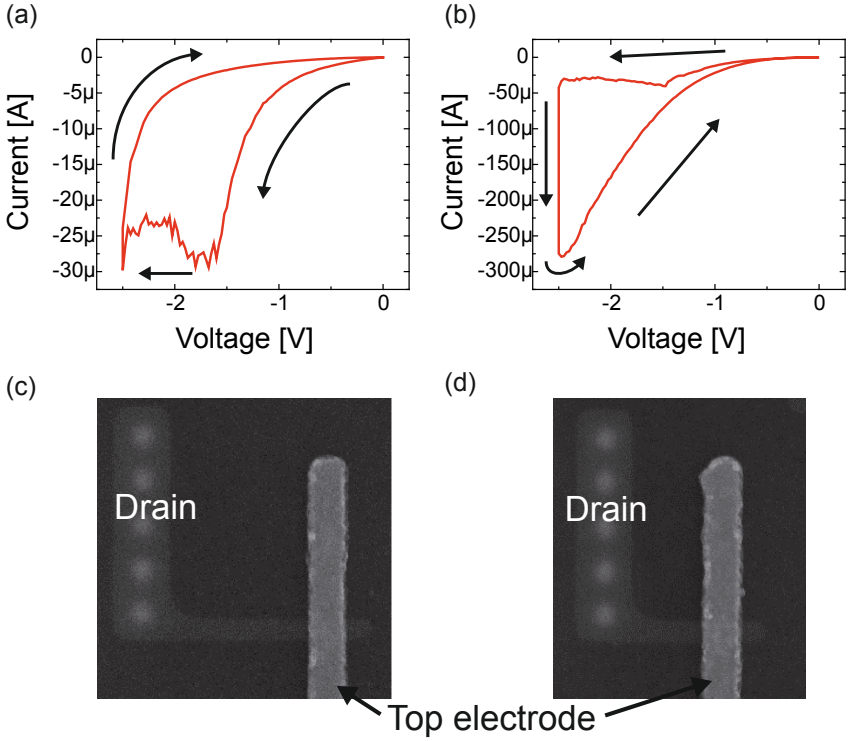


Figure 6.32: Failure of the memory element during first RESET. (a) I-V graph of a successful RESET. (b) I-V trace of the memory element resulting in the irreversible LRS. The SEM image of both devices in (c) and (d) show no structural damage.

amplitude larger than -1.5 V and the cell switches to the HRS. However, when the same RESET routine is applied to the similar memory element, a sudden increase in the current is observed at the $V_{\mathrm{BL}} = -2.5$ V (Fig. 6.32 (b)). In this case, the device ends up in the irreversible low resistance state. Approximately 35% of the ReRAM elements exhibit this RESET failure.

To explore the reason for this failure phenomenon, SEM images of the structures with the successful RESET (Fig. 6.32 (c)) and the RESET failure were taken (Fig. 6.32 (d)). Surprisingly, both memory elements show no structural peculiarities. The physical explanation for this phenomenon is yet unknown.

Chapter 7

Conclusion and Outlook

The scope of this research work is the investigation of the redox-based resistive switching in nanoscale devices for future non-volatile memory applications. In order to realize this, existing patterning technologies were considerably improved. Furthermore, the VCM type TiO_2 and WO_3 based ReRAM devices were integrated in the backend process of the MOS transistors. The fabricated passive and active nano-crossbar devices with the two different oxides were electrically characterized with respect to the electroforming and the switching behavior. The electrical characterization of the ReRAM devices was primarily focused on the impact of different current limitations and the nonlinearity parameter. In addition, the open clamp voltages of the ECM type memory elements were analyzed and explained by the presence of the electromotive force inside the ReRAM devices.

7.1 Technology Improvements

The scalability of the ReRAM devices into the low nanometer regime is crucial for the industrial application in future non-volatile memory. For the analysis of the scaling potential of the ReRAM devices, a technology platform that ensures a cost-effective fabrication of the nano-crossbar devices (F = 40 nm) is essential. In this thesis, the reduction of the feature sizes of the structures on the imprint stamp was achieved through the layer stack engineering. The proposed layer stack for the imprint mold is patterned by e-beam lithography and dry etching processes. The integrated nanostructures have lateral sizes

ranging from 25 nm to 100 nm. In addition, the yield improvement of single structures per wafer was achieved by the redesigning of the mask. To complement the passive ReRAM devices, fabrication processes for the integration of TiO_2 and WO_3 based ReRAM devices on prestructured MOS transistors resulting in the 1T-1R configuration were developed.

7.2 Electromotive Force in ReRAM

The redox processes in the ReRAM devices are mainly responsible for the switching effect. These processes at the nano-scale induce the nanobattery effect in the ReRAM devices. The presence of open clamp voltages in the memory elements was analyzed in this work. The observed voltages were explained by the emf. There are three possible origins of this effect, i.e. the Nernst potential, the diffusion potential and the Gibbs-Thomson potential, of the emf were discussed. The emf affects the ReRAM characteristics, especially the retention failure in ECM type $Cu/WO_3/Pt$ based ReRAM devices.

7.3 TiO_2 and WO_3 based Nano-Crossbar Structures

The electroforming and the RESET processes of passive nano-crossbar devices based on TiO_2 or WO_3 with cell sizes down to 40 x 40 nm^2 were analyzed in this work. During the measurements, the alternative current compliance by external series resistances was observed to influence the formation of the conducting filament inside the ReRAM devices. The elements, that were electroformed with higher external series resistances, exhibit lower currents and higher ON state resistances. This is explained conducting filament property such as size. In addition, the forming voltage was reduced by the scaling down of the resistive switching oxide thickness and increasing the device temperature with the help of an external heater. It was observed, that the applied power for the occurrence of the electroforming event is approximately constant and seems to be an inherent property of the different oxides. To reduce the sneak path current and enable the integration of ReRAM devices into passive crossbar array high degree of nonlinearity in the I-V characteristics of the ReRAM

devices is required. The investigation of the nonlinearity was carried out with transient (AC) voltage pulses (100 ns). The AC nonlinearity was observed to be a function of the applied series resistances. The lower forming and SET currents result in the higher nonlinearity in the I-V characteristics of the TiO_2 based ReRAM devices.

7.4 ReRAM Elements in 1T-1R Configuration

The ReRAM devices are highly prone to the current overshoot phenomena during the electroforming and the SET process. The overshoot was minimized by the integration of the ReRAM devices in the 1T-1R configuration. These devices were electrically characterized by means of quasi-static voltage sweeps as well as transient pulses. The integrated ReRAM devices exhibit the higher forming voltage for smaller device sizes. This drawback was overcome by the reduction of the oxide layer thickness to 5 nm on the planarized 1T-1R devices. These devices exhibit superior performance with regards to low power operation with switching currents below 1 μA. This could be explained by the suppression of the overshoot phenomena. The endurance of the ultra low current devices was proven to be lager than 10^4. In addition, the current limitation by the MOS transistor improves the nonlinearity of the ReRAM device in the short voltage pulse (100 ns) experiment.

7.5 Outlook

The TiO_2 based ReRAM devices in the 1T-1R configuration exhibit excellent properties with regards to low power data operation. However, the physical reason for the resistive switching in the ultra low current regime (< 1 μA) is not fully understood yet. Therefore, further studies on a larger number of devices in combination with modeling and simulation efforts are highly important for the future development of ReRAM devices.
The integration of different metal-oxides as well as bi-layer stacks in ReRAM devices in the developed technology platform could be a potential candidate for further improvement of the device characteristics such as nonlinearity, endurance and retention. Especially the nonlinearity and self-compliance prop-

erty of thin tunnel barriers in combination with the switching oxides in the ReRAM devices are highly interesting. In summery the following tasks can be defined to further improve the ReRAM device performance and get a better understanding of the physical mechanisms for the resistive switching effect:

- Develop a model for the low current switching.
- Material engineering in the ReRAM devices.
- Layer stack engineering in the ReRAM devices.
- Investigate the switching behavior for different metal oxides such as HfO_2, Ta_2O_5 and propose a generic design rule for the ReRAM technology.

Acknowledgement

This thesis would not have been possible without the support of many people. First of all, I would like to thank Prof. Dr. Reiner Waser for giving me the opportunity to work within his institute in the highly interesting field of non-volatile memory research.
Furthermore, I want to express my gratitude to Prof. Dr. Michael Heuken for agreeing to be my co-examiner.
I would like to thank my supervisors Dr. Reiner Bruchhaus, Dr. Ulrich Böttger and especially Dr. Vikas Rana for their great scientific support. Their inspiring ideas and fruitful discussions helped to guide this work into the right direction.
To Dr. Christoph Hermes and Bernd Rösgen I want to express my gratitude for the excellent collaboration within the Intel project. I am grateful to Dr. Roland Rosezin and Dr. Matthias Meier for the introduction to the nanoimprint technique and their advice during the process development. To Dr. Stefan Menzel and Dr. Ilia Valov I express my gratitude for the discussions regarding the interpretation of the experimental results.
Special thanks goes to René Borowski for his support in the clean room work including the dry etching, thin film deposition and many other processing step. I thank Dr. Stefan Trellenkamp for the e-beam writing and the countless discussions on this interesting topic. For the photolithographic processing I would like to thank Mirka Grates. I am thankful for the excellent metal deposition performed by Alfred Steffen and Hans Wingens. The FIB preparation and recording of SEM images were performed by Hans-Peter Bochem, for which I am very thankful. I express my gratitude to Marcel Gerst for the support in the measurement technology. For the help with all other technical questions I thank Manfred Gebauer and Jochen Friedrich.
Furthermore, I thank my office mates, Rohit Soni and Michael Paßens as well as Felix Gunkel, Katharina Skaja, Anja Herpers, Marcel Reiners and Nabeel Aslam and all other colleagues for providing an entertaining working atmosphere.
I thank my family for supporting and encouraging me during my studies. A big thank you goes to my partner, Iris, for her patience and her support. I

want to thank my sons, Kilian and Emil, for bringing so much joy into my life.

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