A novel interconnection scheme for thin-film silicon solar modules with highly conductive intermediate reflector layer

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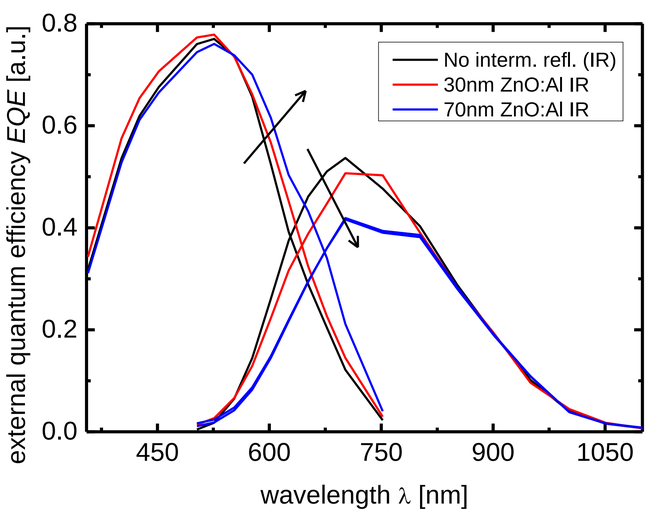
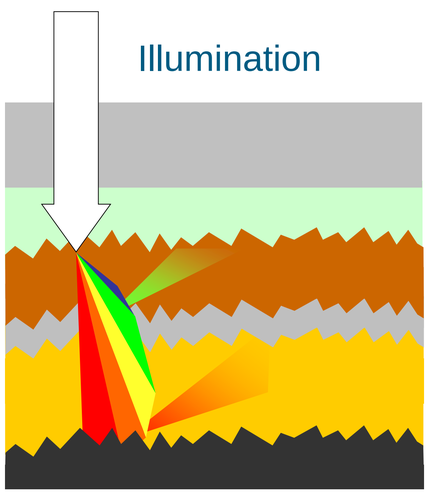
Motivation

Tandem thin-film solar cells with intermediate reflector (IR) layer



- Shift sub-cell current generation from bottom- to top-cell
- Thinner top-cell → increased stability against light-induced degradation
- Aim: higher stabilized overall cell efficiency

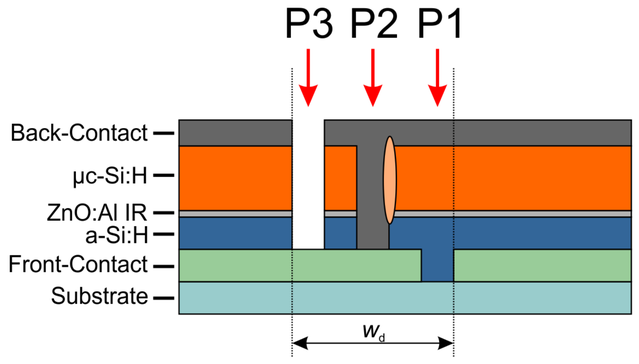
Realization for thin-film silicon solar technology



- Introduction of thin 50nm-100nm layer with suitable refractive index
- Used materials are usually ZnO:Al TCO and/or µc-SiO_x:H
- Demands: Highly conductive, and spectral selective reflectivity

Problems and limitations

- Demand of high electrical conductivity on solar cell level is at the same time problematic on solar module level!



- After interconnection process P2, back-contact deposition will short-circuit the bottom-cell between intermediate reflector and back-contact

Conclusion

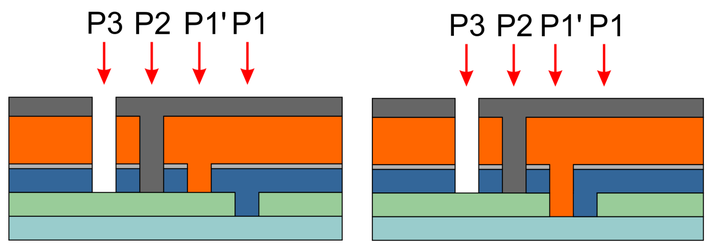
- A novel interconnection scheme for thin-film silicon solar modules with highly conductive ZnO:Al intermediate reflector layer (ZIR) was introduced
- In contrast to designs from literature neither extra scribing steps are needed nor extra active area is lost compared to the standard interconnection scheme
- Implementation into tandem modules with 70nm ZIR layer has proven applicability
- New problems which arise from debris redeposition on the surface were discussed

Results

Possible solutions to the shunting problem

- Known designs from literature to cut current path between P2 interconnect and IR

a) Four scribes [1] b) Four scribes/shift [2]

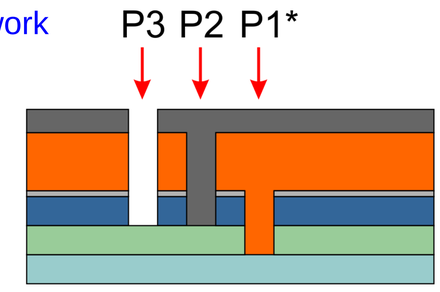


- Four scribes: Introduce a fourth scribe P1‘ before bottom-cell deposition
  - Drawbacks: **additional scribing step** and **additional active area lost!**
- Four scribes/shifted: Move P1‘ closer to P1
  - Active area loss reduced, but **additional scribing step**

[1] Bugnon, G. et al. SOLMAT , 95 (8), pp. 2161-2166
[2] Meier, J. et al. 29th IEEE PVSC., pp. 1118-1121.

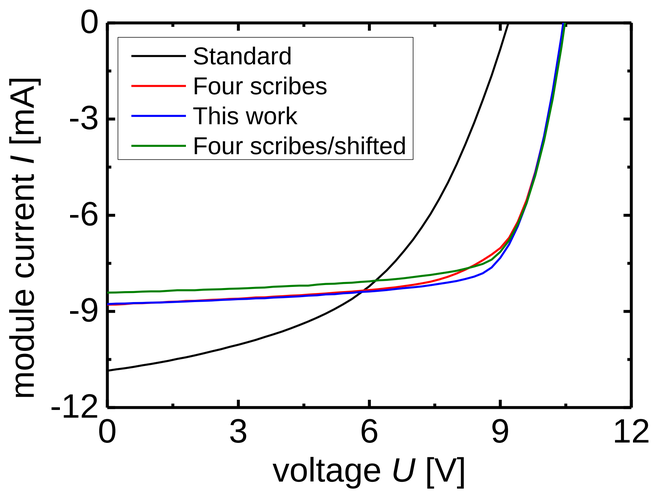
- A new interconnection scheme is proposed

c) This work



- This work: P1* scribe is “delayed” after top-cell + intermediate reflector deposition
  - Bottom-cell is used to cut short-circuit between P2 scribe and intermediate reflector
  - Advantages: NO additional scribing steps and NO additional area losses

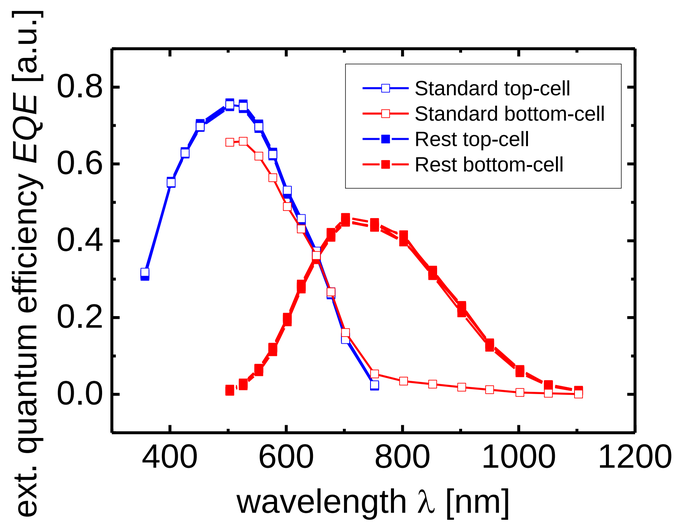
Module characteristics



- *J-V* plot of a tandem module on SnO_2:F with 70nm sputtered ZnO:Al intermediate reflector
  - 8 sub-cells series connected with 1cm cell stripe width and 1cm cell length → Total area A=8cm²
  - 4 Modules processed on one 10x10cm² glass substrate

Interconnetion scheme	Standard scribes	Four scribes	Four scribes/ shifted	This work
Efficiency η [%]	6.21	7.96	8.18	8.4
Fill-Factor *FF* [%]	49.8	69.2	73.16	73.4
Short-circuit curr. dens. J_{sc} [mA/cm²]	10.86	8.8	8.58	8.77
Open-circuit voltage V_{oc} [V]	9.18	10.46	10.42	10.44

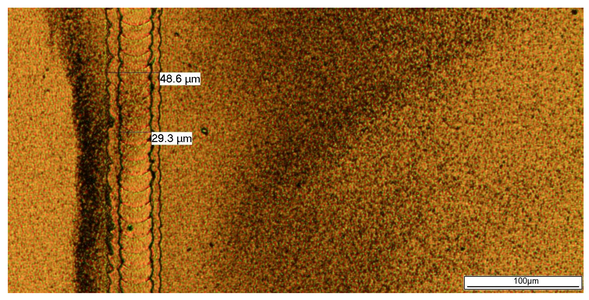
- Shunting with standard interconnection
- High Fill-Factors for the other design schemes → **Proposed design applicable**



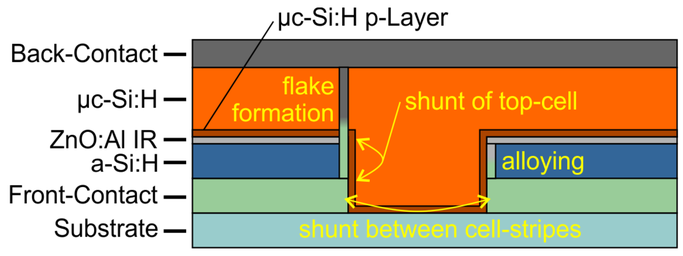
- No shunting with other designs, but strong mismatch

New problems

- Effects on cell properties caused by scribing processes before bottom-cell deposition



- Dark spots due to redeposition on surface, effect amplified when TCO is ablated
- Possible shunting paths created by delayed P1* need to be characterized



- Preliminary experiments with highly conductive µc-Si:H p-Layer showed decrease of fill-factor
- Electrical measurements indicate that shunting between cell-stripes and alloying is unlikely

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