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We developed a T-gate technology based on selective wet etching yielding 200 nm wide T-gate structures used for fabrication of High Electron Mobility Transistors (HEMT). Major advantages of our process are the use of only standard photolithographic process and the ability to generate T-gate stacks. A HEMT fabricated on AlGaN/GaN/sapphire with gate length $L_g = 200$ nm and double-stacked T-gates exhibits 60 GHz cutoff frequency showing ten-fold improvement compared to 6 GHz for the same device with 2 μm gate length. HEMTs with a double-level-T-gate (DLTG) structure exhibit up to 35% improvement of f_{max} value compared to a single T-gate device. This indicates a significant reduction of skin effect losses in DLTG structure compared to its standard T-gate counterpart. These results agree with the theoretical predictions. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4903468]

During the last three decades, the fabrication and performance of transistors operating in the GHz frequency range have been showing a rapid progress by introducing new material systems (e.g., GaAs/InGaAs[1–4] or AlGaN/GaN heterostructures[5–7]), novel technological processes,[6–9] or new device geometries with decreasing gate dimensions.[10–12] The transistor scaling process has the drawback that the parasitic gate resistance increases linearly with decreasing gate length L_g. A small gate length is crucial for the transistor speed; however, the increase of the gate resistance degrades the external device properties, especially the power gain. Therefore, the parasitic gate resistance must be kept as low as possible with decreasing L_g. One solution for the contradictory requirements is to use T-shaped gates allowing fabricating gates with small L_g (corresponding to the base of T) with a low value of R_g, due to the large top of the T. The larger the head, the lower the resistance. The major research effort to provide these T-shaped gates concentrates on structures fabricated by electron beam lithography, deep UV lithography, or nano-imprint techniques.[13] Especially, the fabrication of T-shaped gates by e-beam lithography is commonly used in high frequency device technology. Nevertheless, yield and uniformity of T-gate fabrication are often affected by the extreme lithography and other technological steps required for their realization. At very high frequencies, the skin effect and the roughness of the gate metallization can further increase the gate resistance.

In this work, we present an alternative T-gate structure fabrication with the advantages of using only photolithography and with significantly increased electrode surface. The total cross-section of our developed double-level-T-gate (DLTG) contributing to the current transport is about 2-times higher than for a standard T-gate design (Fig. 1), resulting in halving the gate resistance.

Our DLTG layout is expected to provide significant improvement in high-frequency performance of HEMT (high electron mobility transistor) devices in comparison with conventional T-gate electrodes. Fig. 2 shows the

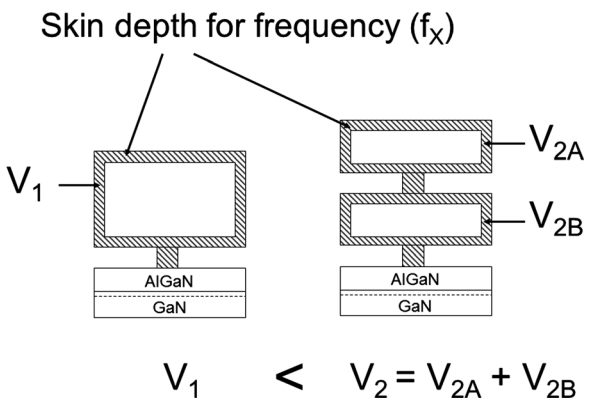

FIG. 1. Principle of double-level T-gate compared to conventional T-gate, showing double cross-section for current transport.

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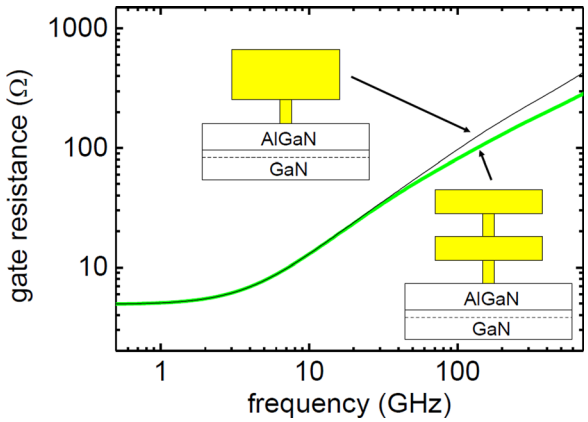

FIG. 2. Calculated gate resistance as function of frequency for T-gate vs. DLTG structure.

calculated frequency dependence of the resistance for both T-gate layouts. The calculations were performed with the COMSOL 4.2 Multiphysics (AC/DC module) software. The gate width was 100 μm, with a gate length of 200 nm. The head of the conventional T-gate had a cross section of 2000 nm $\times$ 400 nm, while each level of the DLTG was 2000 nm $\times$ 200 nm. The results show a pronounced frequency dependence already below 10 GHz. From 50 GHz, the DLTG shows a decrease of the gate resistance compared to the conventional T-gate. At 200 GHz, the decrease is already 25%. The effect of surface roughness should even increase the influence of the DLTG. Figure 3 shows the current distribution of both layouts at 300 GHz. The current density in the Ni layers with high permeability is very strongly suppressed.

The exact influence of the gate resistance (and therefore of our T-gate layout) on transistor performance depends on the other intrinsic and extrinsic transistor parameters (transconductance, capacitances, etc.). In any case, our layout will reduce the skin effect related deteriorations of the transistor properties.

Our DLTG technology was applied on AlGaN/GaN based HEMTs. The HEMT-layer system consisted of a 3-μm-thick undoped GaN layer followed by a 30-nm-thick AlGaN barrier layer with an aluminum mole fraction of

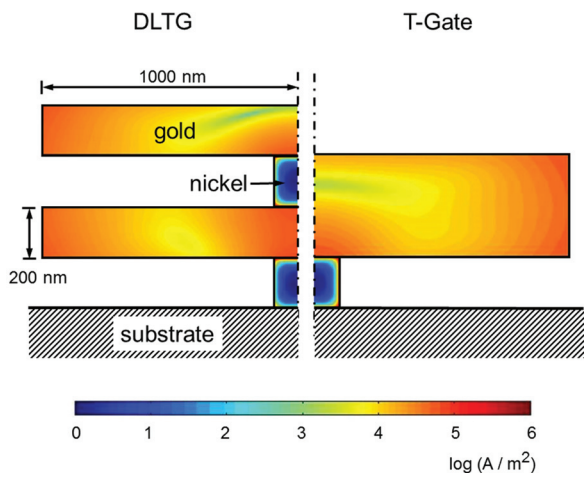

FIG. 3. Current distribution at 300 GHz. Below 1 GHz, the current density in the gold regions is uniform, with log(current density/A m^{-2}) $\approx$ 6.

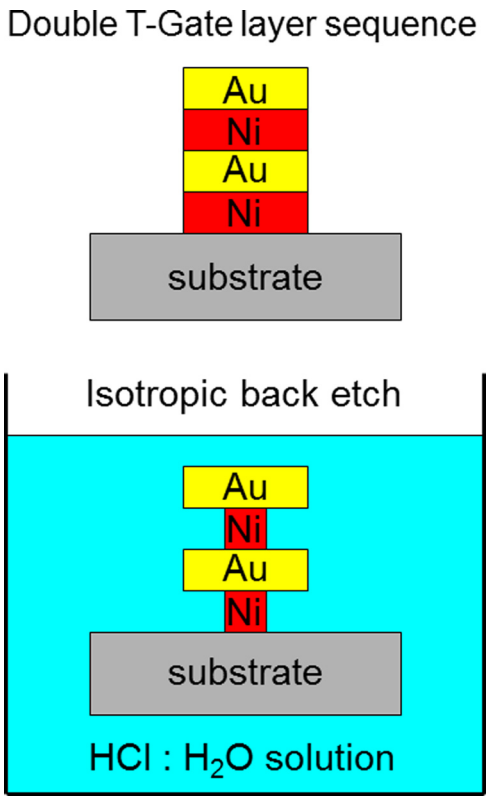

FIG. 4. Schematics of wet etching process for double-level-T-gate fabrication.

26%, grown on sapphire substrate. The transistor devices were fabricated in the conventional way. Mesa insulation was performed using Ar ion milling. Ohmic contact metallization based on Ti/Al/Ni/Au multilayer was annealed at 850 °C for 30 s in N_2 ambient. The source-drain spacing was

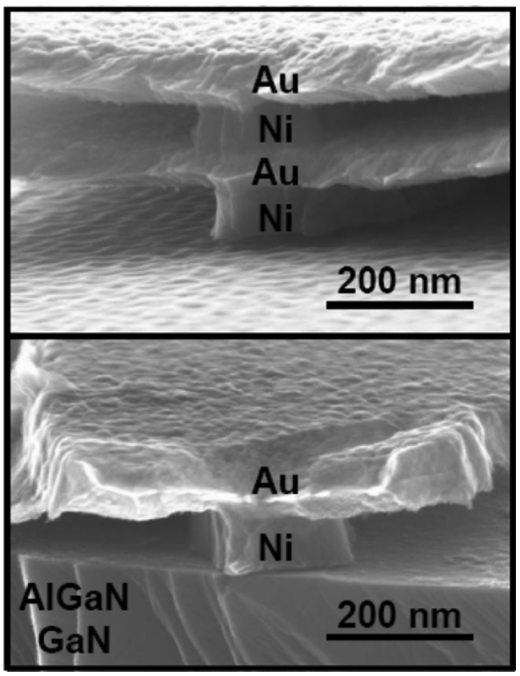

FIG. 5. Scanning electron microscope micrograph of double-level-T-gate contact (top) and T-gate (down) fabricated on AlGaN/GaN/sapphire material. Layer spacing and layer thicknesses are 100 nm, respectively. Hut length is 2 μm.

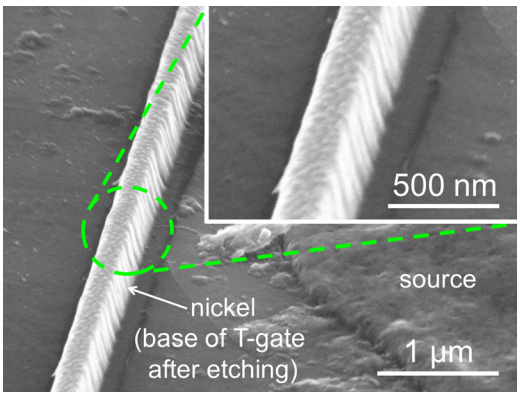

FIG. 6. Etched Ni T-gate foot after removal of the gold metallization, showing a uniform gate length.

3 μm. The gate contacts consisted of a Ni/Au/Ni/Au stack with thicknesses of 200 nm for each layer. The designed gate length was 2 μm. All metallizations were performed by standard photolithographic steps and liftoff processes. Our simple technological process for the fabrication of submicrometer sized T-gate structures is shown in Fig. 4.

The HEMT structures with the 2 μm gate length electrodes were etched in HCl:H_2O (1:100) solution for selective etching of the Ni films while keeping the Au layers intact (Fig. 4). Atomic force microscopy measurements reveal that the roughness of the AlGaN surface has not increased by the exposure to HCl. After etching, the samples were rinsed for 10 min in deionized water to stop the metal-interlayer recess process. The recess etching time was adjusted to fabricate gate electrodes with foot lengths down to 200 nm. Fig. 5 shows electron microscope pictures of a T-gate and a double-level-T-gate (both fabricated by recess etching).

The yield of our process was about 90%. The gold metallization was etched away on fabricated T-gates to investigate the roughness of the Ni etching (Fig. 6). The remaining Ni shows a very good uniformity and only small roughness of the sidewalls. The minimum gate length can be reduced to 100 nm and beyond, if the gate is stabilized mechanically.

The fabricated HEMT devices were first tested by DC measurements, showing nearly 2 times higher maximum drain current (0.7 A/mm) of the double-level-T-gate structures compared to the unetched counterpart with $L_g = 2\,\mu$m (0.4 A/mm). Similarly, the extrinsic transconductance

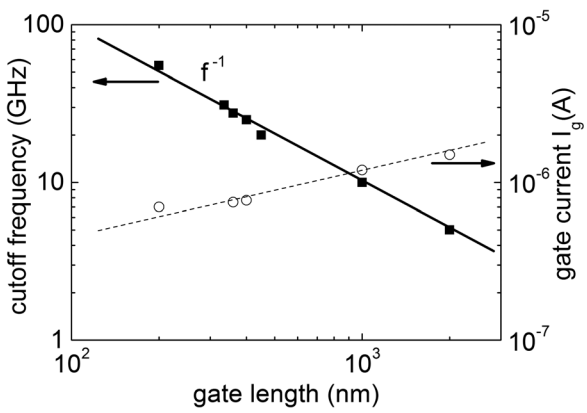

FIG. 7. Cutoff frequency and DC gate current vs. gate length of DLTG devices.

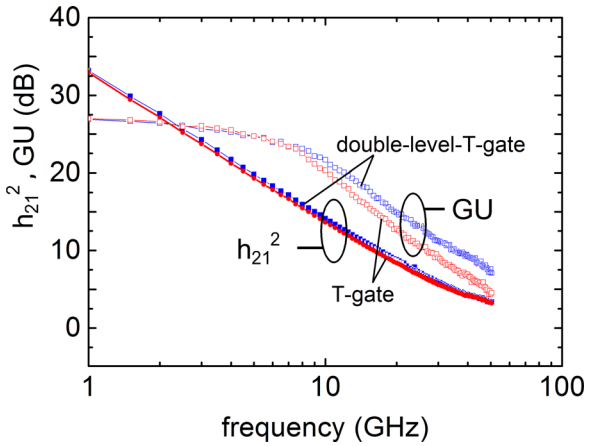

FIG. 8. Comparison of the current gain and unilateral power gain on HEMTs with T-gate structure and double-level-T-gate structure, both with 200 nm gate length. Thickness of T-gate hut is 400 nm, and thickness of DLTG hut is 2 × 200 nm.

exhibits a value of 175 mS/mm for the 200 nm gate length device compared to 125 mS/mm for the 2 μm gate length transistor. The reduction of the gate electrode length due to the recess etching is also demonstrated by the decrease of the threshold voltage from −3 V to −4.6 V for the 200 nm gate HEMT.

High frequency S-parameter measurements show an increase of the cutoff frequency from 6 GHz for the 2 μm device to 60 GHz for the same device after etching the 200 nm double-level-T-gate structure. The cutoff frequency shows a $1/L_g$ dependence without indication of saturation for short gate lengths (Fig. 7). The same figure shows that the DC gate current I_g decreases with decreasing L_g contributing to the improvement of device performance. The behavior is similar for DLTG and T-gate devices.

Figure 8 presents a comparison of current gain and unilateral power gain (GU) of HEMTs with T-gate and double-level-T-gate structure (both with 200 nm gate width). While the performance of both transistors is identical for the current gain (the current gain is nearly independent on gate resistance), the HEMT device with DLTG electrode structure shows improved power gain at high frequencies compared to the T-gate counterpart. The f_{max} value of the DLTG device is 115 GHz compared to 85 GHz for the T-gate transistor that is a 35% increase.

In conclusion, we have developed a multi-level-T-gate technique for fabrication of submicron gate lengths based on wet chemical etching that uses only standard photolithographical processes (no e-beam lithography). HEMT devices with 200 nm gate length showed a cutoff frequency of 60 GHz. HEMTs with a DLTG structure exhibit a 35% improvement of the f_{max} value, compared to their conventional T-gate counterparts. Our technology demonstrates that application of T-gate stacks has a strong potential to decrease skin effect losses in gate structures, leading to substantial improvement of high-frequency performance of HEMTs.

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