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Single trap in liquid gated nanowire FETs: Capture time behavior as a function of current

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The basic reason for enhanced electron capture time, τ_c , of the oxide single trap dependence on drain current in the linear operation regime of p^+-p-p^+ silicon field effect transistors (FETs) was established, using a quantum-mechanical approach. A strong increase of τ_c slope dependence on channel current is explained using quantization and tunneling concepts in terms of strong field dependence of the oxide layer single trap effective cross-section, which can be described by an amplification factor. Physical interpretation of this parameter deals with the amplification of the electron cross-section determined by both decreasing the critical field influence as a result of the minority carrier depletion and the potential barrier growth for electron capture. For the NW channel of n^+-p-n^+ FETs, the experimentally observed slope of τ_c equals (-1) . On the contrary, for the case of p^+-p-p^+ Si FETs in the accumulation regime, the experimentally observed slope of τ_c equals (-2.8) . It can be achieved when the amplification factor is about 12. Extraordinary high capture time slope values versus current are explained by the effective capture cross-section growth with decreasing electron concentration close to the nanowire-oxide interface. © 2015 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4919816>]

I. INTRODUCTION

It is well-known that random telegraph signal (RTS) can be utilized as an extremely sensitive, local, atomic-size probe in nanoscale field-effect transistors (FETs).^{1–6} RTS is caused by the exchange of a single electron between an oxide trap and either a local energetic level or energy band in the semiconductor, while drain current is flowing. A beneficial characteristic of a single trap in the dielectric of liquid-gated FETs is that the RTS behavior can be used as a basic principle for novel, highly sensitive biosensors.⁷ As far as nanoelectronic device dimensions strive to shrink down, RTS becomes more and more important in determining the performance and reliability. Individual charge traps can significantly alter the channel current of nm-sized FETs. At the same time, it has been observed that the capture kinetics of RTS in submicron FETs cannot be described by the well-known Shockley-Read-Hall model,^{1–3,8,9} in particular, at low currents and voltages.

During the last decade, strong electron capture time, τ_c , dependence on drain current was often experimentally observed.^{9–12} Now, it is commonly considered that the decisive factors determining the strong current dependence of τ_c are electron distribution (perpendicular to the Si/SiO₂ interface) dependent on the high electric field near the interface⁹ and Coulomb blockade effect.^{10–12} On the other hand, it is shown by Mueller *et al.*³ that Coulomb energy is not significantly changed in neither accumulation nor inversion regimes versus applied gate voltage. The fact reflects that it will not have a significant or essential influence on the capture time behavior.

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Recently, we showed that taking into account the quantization effect and mobile carrier's tunneling across the triangular energetic barrier near the oxide-nanowire (NW) channel interface in n^+-p-n^+ FET allows a new method of describing, which physical processes take place in the NW FET channel more accurately.¹³ In the present paper, the main concept of carriers' quantization and tunneling¹³ was used in order to investigate and describe the basic reasons for the enhanced dependence of electron capture time on drain current in the linear operation regime of accumulation p^+-p-p^+ Si liquid-gated NW FETs in contrast to n^+-p-n^+ structures.

II. EXPERIMENTAL DETAILS

For investigation of RTS, carrier capture times and drain current behavior of two types of NW FETs were used. Fig. 1

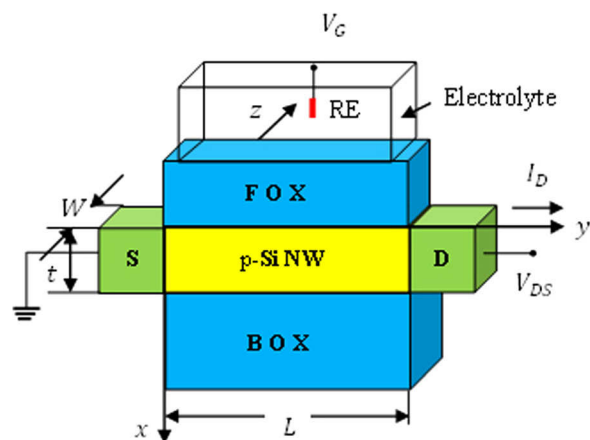


FIG. 1. Schematic presentation of Si NW FET with liquid and back gates. S and D indicate source and drain. RE—reference electrode and V_G —liquid gate voltage.

shows the sensor structure represented by following layers: liquid gate, oxide, p-doped Si NW, buried oxide, and p-doped Si substrate. The first device group included n^+ -p- n^+ Si NW FETs; the second— p^+ -p- p^+ structures. The only difference between the groups was the doping impurity introduced by ion implantation in both source and drain regions. The technology of the NW FET fabrication is described in Ref. 13.

Structures have the following sizes: $d_{FOX} = 9$ nm, $d_{BOX} = 145$ nm, $t = 50$ nm, $L = 200$ nm, and $W = 100$ nm, where d_{FOX} and d_{BOX} are the thicknesses of front (FOX) and buried oxide (BOX) layers. t , L , and W are the nanowire thickness, length, and width, respectively. The concentration of acceptors in both the substrate and NW was 10^{15} cm^{-3} .

III. RESULTS AND DISCUSSION

Measurements were performed in an aqueous solution with $\text{pH} = 7.4$. Devices of the first group were investigated in the inversion regime, while devices of the second group were investigated in the accumulation regime. Typical transfer characteristic and drain current time trace measured for p^+ -p- p^+ Si NW FET structure are shown in Fig. 2.

Distribution of the carrier profiles, calculated using a quantum approach,¹³ is plotted in Fig. 3. Typical electron capture time dependencies on drain current were measured for both n^+ -p- n^+ and p^+ -p- p^+ types of NW FETs. They are presented on a double logarithmic scale in Fig. 4. For the first group of FETs measured, the value of the slope is (-1) , and for the second group, it is (-2.8) .

Theoretical studies and calculations were performed with respect to the quantization and tunneling effects of the mobile carriers in the inversion regime of a nanoscale n-channel n^+ -p- n^+ FET. They demonstrate that the slope of the electron capture time dependence on gate voltage is equal to (-1) , which fully corresponds to the measured data.¹³ Theoretical curves (Fig. 4) were calculated using a quantum approach for capture time.¹³ To explain the enhanced change in τ_c slope for p^+ -p- p^+ FETs, we considered that in the accumulation regime the concentration of holes is considerably higher at the FOX-NW interface

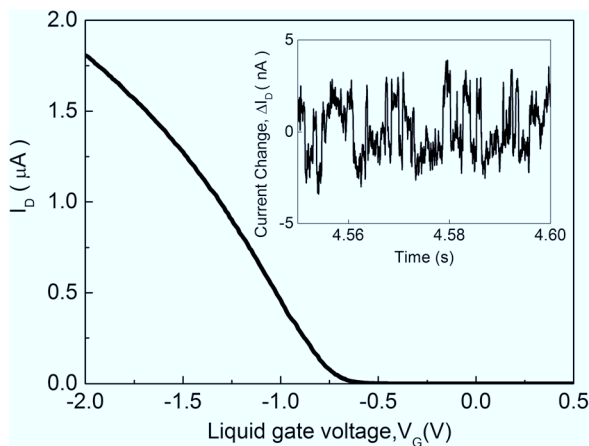


FIG. 2. Typical transfer curve of p^+ -p- p^+ Si NW FET with liquid front gate at $\text{pH} = 7.4$. Inset: typical random telegraph signal (RTS) time trace of drain current change.

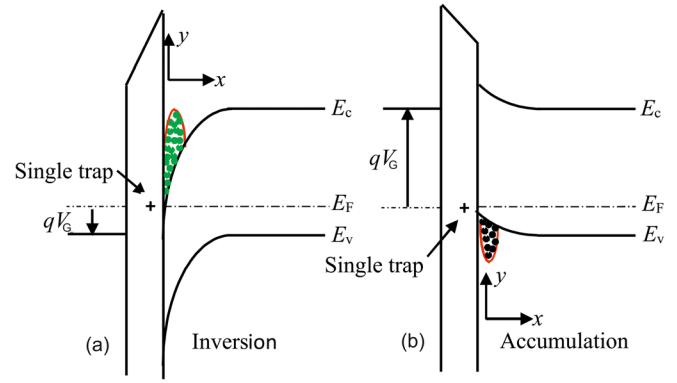


FIG. 3. Energy-band diagrams: (a) for an n^+ -p- n^+ FET in the inversion and (b) a p^+ -p- p^+ FET in the accumulation regime. Carrier distribution profiles in the channel are marked in red. Electrons are plotted as green points and holes as black ones. The single trap in the oxide layer is also shown as “plus.”

(Fig. 3(b)). It should be noted that the change in sign of the applied voltage cannot influence the physical concept, since the sign of the majority carriers also changes.

During the analysis of charge carriers' concentration distribution, we noticed the following features:

- There is a high concentration of free electrons near the interface of n^+ -p- n^+ NW FETs in the inversion regime. One of the carriers can be captured into the oxide trap by tunneling.
- There is a very narrow (about 1 nm) region with a low concentration of holes between the interface oxide and a region of high electron concentration in the case of the inversion regime of the n^+ -p- n^+ NW FETs (Fig. 5).
- Hole distribution has a pronounced maximum in the accumulation regime of the p^+ -p- p^+ FET (see Fig. 6).

The electric field in the nanoscale channel is very high (10^5 – 10^6 V/cm). It should be noted that a strong exponential cross-section, σ , dependence on the field in the oxide was reported.¹⁴ It can be represented as the following equation:^{4,14}

$$\sigma \propto \exp(E_{ox}), \quad (1)$$

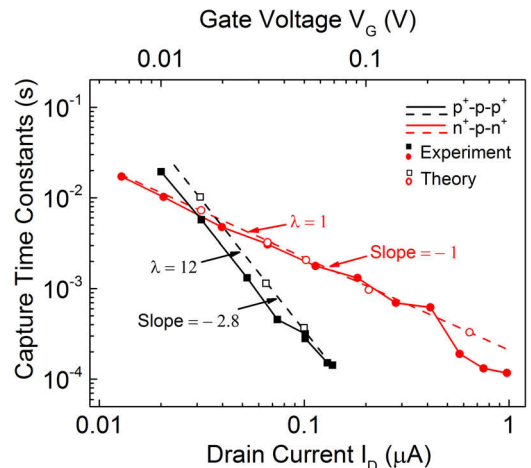


FIG. 4. Measured (filled symbols) and calculated (empty symbols) oxide trap electron capture time dependencies on drain current, according to Eq. (5). The curve for the n^+ -p- n^+ FETs (inversion regime) is plotted in red and the p^+ -p- p^+ (accumulation regime) in black.

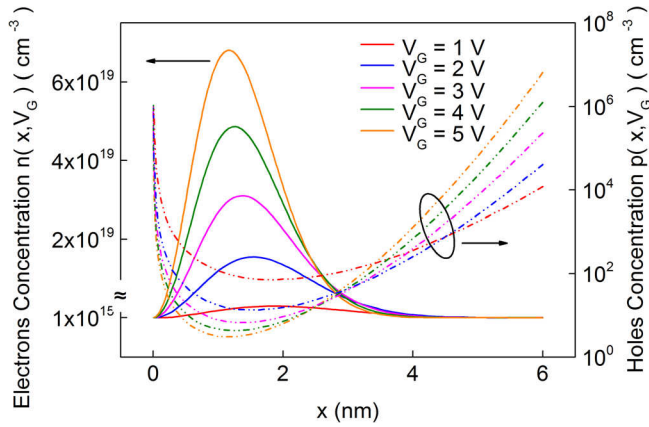


FIG. 5. Electron concentration $n(x, V_G)$ (solid lines) and hole concentration $p(x, V_G)$ (dashed lines) in the nanowire of n^+-p-n^+ FETs are plotted versus the depth of the channel x from the FOX-NW interface. Curves with different colors represent distributions for specific gate voltages.

where

$$E_{ox} = \frac{|V_G - V_{th}|}{d_{FOX}}. \quad (2)$$

For the electron effective capture cross-section, we can rewrite relation (1) in the following form:

$$\sigma_n = \sigma_{n0} \exp\left(\frac{V_G - V_{th}}{\varepsilon_{cr} d_{FOX}}\right). \quad (3)$$

Here V_G and V_{th} are the gate and threshold voltages, respectively; ε_{cr} is the critical field (for $E_{ox} = \varepsilon_{cr}$ the cross-section, σ , is changed by e times). For p^+-p-p^+ NW FETs, the effective capture cross-section grows with the strong decrease in carrier number (electrons) near the FOX-NW interface. We can describe this behavior by means of the amplification factor λ ($\lambda \geq 1$)

$$\sigma'_n = \sigma_{n0} \exp\left[\frac{\lambda(V_G - V_{th})}{d_{FOX}\varepsilon_{cr}}\right]. \quad (4)$$

On the contrary to the n^+-p-n^+ structures, p^+-p-p^+ FETs work in the accumulation mode. The surface region of the Si NW is depleted of the minor carriers—electrons (Fig. 5).

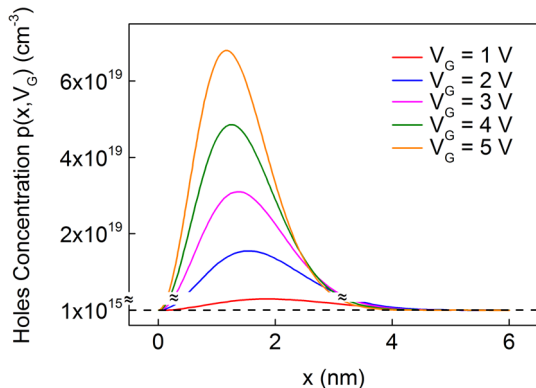


FIG. 6. Hole concentration $p(x, V_G)$ versus depth of the channel x from the FOX-NW interface in the nanowire of p^+-p-p^+ FETs. Different colors represent curves for different specific gate voltages.

The distance between the repulsive trap in the oxide layer and the mobile electrons of the Si conductive band increases. The potential barrier, which an electron must surmount to be accepted in the trap increases simultaneously. Thereby, the action of the critical field ε_{cr} becomes weaker.

The physical interpretation of the amplification parameter, λ , is related to the amplification of the electron cross-section determined by both decreasing the critical field's influence as a result of the removal of the captured electron and by the growth of the potential barrier for their capture. In the case of n^+-p-n^+ structures, the electrons in the conductive band of Si NWs do not move from the Si NW interface, the potential barrier does not grow, ε_{cr} does not change considerably, and therefore $\lambda = 1$. It is clear that the parameter λ has to be dependent on the gate voltage. Determination of this dependence is a separate challenge that needs further investigation.

We found that in the p^+-p-p^+ FETs, the cross section capture increases by hundreds of times for the critical field, $\varepsilon_{cr} \propto (10^5 - 10^6)$ V/cm when compared to the low-field value, σ_{n0} , during variation of applied gate voltages on the order of 1 V.

Applying the electron capture time calculation method used in Ref. 13, and taking into account the quantization and tunneling effects of the mobile carriers from Eq. (4), we can obtain a new expression for τ_c

$$\tau_c = \frac{\exp\left[\gamma z_t + \beta z_{QM} - \frac{\lambda(V_G - V_{th})}{\varepsilon_{cr} d_{FOX}}\right]}{\ln\left[1 + \frac{1}{2} \exp\left(\frac{V_G - V_{th}}{\eta \varphi_T}\right)\right]} \times \tau_{c0}, \quad (5)$$

where

$$\tau_{c0} = \frac{t}{2T_0 \sigma_{n0} v_{th} n_{st}}.$$

For the case of n^+-p-n^+ FETs, we have to take $\lambda = 1$; and for the case of the p^+-p-p^+ FETs $\lambda > 1$. It should be noted that $\beta = 0.1\gamma$ and other denotations in Eq. (5) are the same as they were introduced in Refs. 12 and 13.

The terms of Eq. (5) considering quantum approach are the following:

- $\exp(\gamma z_t)$ —the trap location in the oxide [dependence $\tau_c \propto \exp(\gamma z_t)$]. γ is the attenuation coefficient of the electron wave function in the oxide layer and z_t is the trap distance from oxide-channel interface.
- $\exp(\beta z_{QM})$ —the tunneling of electrons. It depends on the depth of the maximal value of the carrier density at the channel-oxide interface.
- $\exp\left[-\frac{\lambda(V_G - V_{th})}{\varepsilon_{cr} d_{FOX}}\right]$ —the field dependence of the cross-section in the oxide layer (Eq. (4)).
- $\ln\left[1 + \frac{1}{2} \exp\left(\frac{V_G - V_{th}}{\eta \varphi_T}\right)\right]$ —the quantization and specific distribution of the mobile carriers in the channel.

Assuming that the FETs are working in the linear regime at low changes of applied gate voltage, $(|V_G - V_{th}|) \propto (0.1 \div 0.5)$ V, we calculated the slope of τ_c vs drain current using following parameters: $\sigma_{n0} \approx 10^{-20}$ cm², $T_0 = 1$,

$z_t = 2$ nm, $t = 50$ nm, $v_{th} = 2.3 \times 10^7$ cm/s, $\epsilon_{cr} \approx 4.5 \times 10^5$ V/cm, $d_{FOX} \approx 9$ nm, $z_{QM} = 1.21 + 1.64 \times \exp(-0.88V_G)$, and remaining values from Ref. 13. For the n^+ -p- n^+ FET, the capture time slope equals (-1) at $\lambda = 1$ and for the p^+ -p- p^+ FET, the slope equals (-2.8) at $\lambda = 12$.

Thus, the enhanced values of the τ_c slope can be described using Eq. (4) when considering the λ amplification factor, determined by accumulated carriers. Obviously, we can obtain higher slope values of capture time dependence with values of $\lambda > 12$ (Fig. 7).

Fig. 7 shows the electron capture time slope's dependence on the amplification factor λ ($d_{FOX} = 9$ nm). For $\lambda = 1$, the slope equals (-1) , while at $\lambda = 12$ the slope equals (-2.8) .

The capture time dependence on the oxide layer thickness is shown in Fig. 8. τ_c changes very slowly for the n^+ -p- n^+ FETs. Moreover, $\tau_c = \text{const}$ at the $d_{FOX} \geq (5 - 8)$ nm. For the p^+ -p- p^+ FETs, the exponential decrease is obtained with higher values of capture time slope beginning from $d_{FOX} \approx (20 - 40)$ nm and reaching $\tau_c = \text{const}$ for $d_{FOX} \geq 50$ nm. The decrease of τ_c strongly depends on the gate voltage determining the working point. Such behavior of τ_c can be explained by the rapid growth of the electron concentration in the inversion regime at the FOX-NW interface. In case when the n^+ -p- n^+ FET, the layer with high electron concentration blocks the influence of increasing E_{ox} on the capture time, which changes very slow. On the contrary, for the p^+ -p- p^+ FET in the accumulation regime at very low electron concentrations increased E_{ox} influence results in a rapid decrease of τ_c .

Figure 9 shows the electron capture time slope dependence on the front oxide thickness for the p^+ -p- p^+ FET. The characteristic slope value is calculated using Eq. (5) according to the following expression:

$$\text{Slope} = \frac{\log(\tau_c)|_{V_{G,min}} - \log(\tau_c)|_{V_{G,max}}}{\log(V_{G,min}) - \log(V_{G,max})}. \quad (6)$$

The decrease of electron capture time slope strongly depends on the gate voltage determining working point and amplification factor. Thus, the key role of the quantization effect on the capture kinetics of the random telegraph signal is demonstrated. Considering the theoretical argumentation

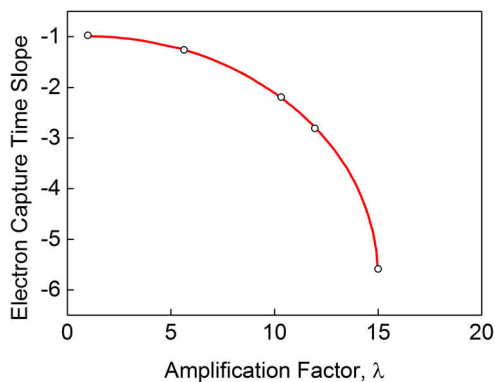


FIG. 7. The electron capture time slope as a function of the amplification factor λ .

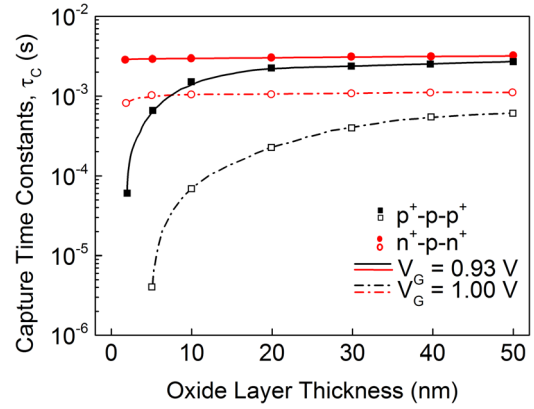


FIG. 8. The electron captures time dependence on oxide thickness when using the quantum-mechanical approach.

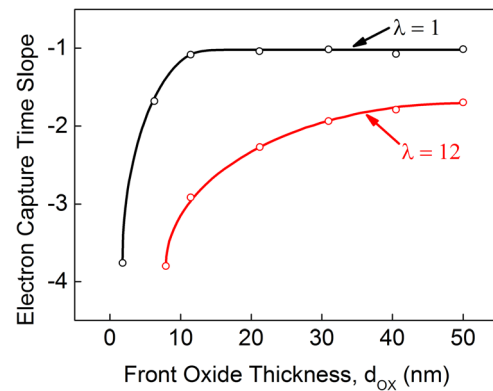


FIG. 9. The electron capture time slope dependence on the front oxide thickness.

for the experimental results, this explanation represents a new way to analyze the increasing τ_c slope versus drain current for the case of a repulsive single trap for tunneling of the mobile carriers in the silicon oxide layer in the accumulation mode of a NW channel in a p^+ -p- p^+ FET.

IV. CONCLUSION

For a more accurate explanation of the strong capture time slope dependence on drain current in nanowire FETs, in addition to already known factors, the following elements have to be taken into account:

- quantization of the mobile carriers in the channel;
- specific distribution of free carriers in the channel and tunneling of the electrons into the oxide single trap;
- sharp growth of the electron cross-section with the decrease of electron concentration at the oxide-NW interface.

It should be noted that the first two factors are determined by the electron concentration distribution in the plane perpendicular to the NW-FOX interface, which is in agreement with the data of Schulz and Mueller.⁸ The last factor plays a significant role in the formation of the capture time slope vs drain current in the strong accumulation regime.

The value of the capture time slope as a function of drain current strongly increases with a decrease of the oxide thickness. Moreover, it plays a dominant role for the

formation of the slope magnitude for $d_{FOX} < 5$ nm (n^+ -p- n^+ FETs) and for $d_{FOX} < 50$ nm in p^+ -p- p^+ FETs.

It is shown that increased values of the slope can be explained by the strong increase of the effective capture cross-section, σ , with a decrease of the concentration of minor carriers in the channel. From our calculations, it follows that the high surface electric field plays an insignificant role in the accumulation regime.

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