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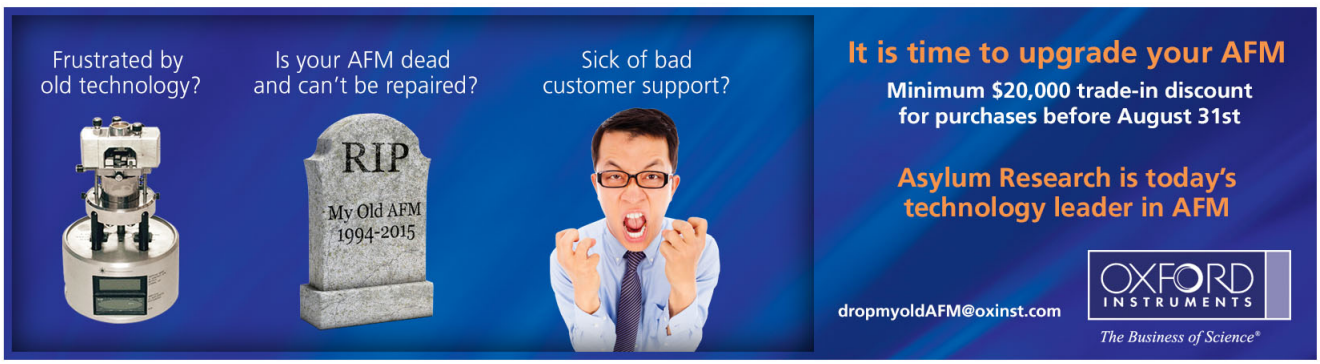

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Controlling the interface charge density in GaN-based metal-oxide-semiconductor heterostructures by plasma oxidation of metal layers

Herwig Hahn,[1,2,a)] Béla Pécz,[3] András Kovács,[2,4] Michael Heuken,[1,5] Holger Kalisch,[1,2] and Andrei Vescan[1,2]
[1]*GaN Device Technology, RWTH Aachen University, 52074 Aachen, Germany*
[2]*JARA-Fundamentals of Future Information Technologies, 52425 Jülich, Germany*
[3]*MTA EK MFA, Konkoly Thege Street 29-33, 1121 Budapest, Hungary*
[4]*Ernst Ruska-Centre for Microscopy and Spectroscopy with Electrons (ER-C) and Forschungszentrum Jülich, Peter Grünberg Institut (PGI-5), 52425 Jülich, Germany*
[5]*AIXTRON SE, 52134 Herzogenrath, Germany*

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In recent years, investigating and engineering the oxide-semiconductor interface in GaN-based devices has come into focus. This has been driven by a large effort to increase the gate robustness and to obtain enhancement mode transistors. Since it has been shown that deep interface states act as fixed interface charge in the typical transistor operating regime, it appears desirable to intentionally incorporate negative interface charge, and thus, to allow for a positive shift in threshold voltage of transistors to realise enhancement mode behaviour. A rather new approach to obtain such negative charge is the plasma-oxidation of thin metal layers. In this study, we present transmission electron microscopy and energy dispersive X-ray spectroscopy analysis as well as electrical data for Al-, Ti-, and Zr-based thin oxide films on a GaN-based heterostructure. It is shown that the plasma-oxidised layers have a polycrystalline morphology. An interfacial amorphous oxide layer is only detectable in the case of Zr. In addition, all films exhibit net negative charge with varying densities. The Zr layer is providing a negative interface charge density of more than $1 \times 10^{13}\,\mathrm{cm}^{-2}$ allowing to considerably shift the threshold voltage to more positive values. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4921867]

I. INTRODUCTION

GaN-based heterostructure field effect transistors (HFETs) have enabled high efficiencies and large power densities in RF power amplification.[1] Such devices have conventionally been fabricated using a Schottky gate for which the metal is in direct contact to the semiconductor.[1] This is a stable and viable option as GaN-based HFETs are traditionally of depletion mode (d-mode)[1] and hence the Schottky diode is not biased above its forward turn-on voltage. However, since GaN is now also seen as a viable option for application in power-switching, enhancement mode (e-mode) behaviour becomes more favourable as it provides fail-safe property together with easier circuit design of inverters, converters, etc.[2] With e-mode devices, the application of a gate dielectric is a must considering that devices need to be turned on without excessive gate current.[3] Furthermore, the application of an insulator provides an additional interface, at which the presence of charge influences the electrostatics of the heterostructure.[4–7] Of particular importance is that deep interface states D_{it} at the oxide/barrier interface do not change their charge state under normal operating conditions of a metal semiconductor heterostructure field effect transistor (MISHFET).[8] Only at high forward biases, at which carriers can be accumulated at the dielectric/barrier interface or at elevated temperatures (emission times become short enough), D_{it} can affect dynamic results via hysteresis or dispersion.[8] Hence, obtaining D_{it} may be seen as a possible means for controlling the threshold voltage V_{th}. Accordingly, with the control of the interface state density which is in the following regarded as a fixed interface charge N_{it}, e-mode behaviour with very large values of V_{th} could be enabled.

Oxide-semiconductor interface charge characterisation has been reported several times in the past.[5,6,8] For the control of N_{it} (and bulk oxide charge N_{ox} which can work in the same way), various methods have been presented, such as gate-recess,[9] plasma oxidation of AlN,[10] or fluorination of a gate oxide.[11] Our group has also shown first results indicating that thermal annealing of a plasma-oxidised Al thin film as gate dielectric leads to V_{th} shifts to more positive values due to the presence of oxide-related charge.[12] However, using the plasma-oxidised Al layer, N_{it} has not shown to be sufficiently high to enable a V_{th}, which is higher than one of the Schottky gated references. In a second approach, we have used plasma-oxidised Al/Ti thin films showing a V_{th} very close to the Schottky reference, suggesting an increased N_{it} in this case.[13] However, exact numbers for N_{it} have not been extracted for this approach so far. Rather, only electrical characteristics limited to gate leakage current and transistor characteristics have been evaluated. In this paper, we present a comprehensive study of Al, Al/Ti, and Zr-based thin oxide films. The possibility of increasing the dielectric thickness is investigated by performing a double deposition-oxidation process. The fabricated structures are analysed in

a)Electronic mail: herwig.hahn@rwth-aachen.de

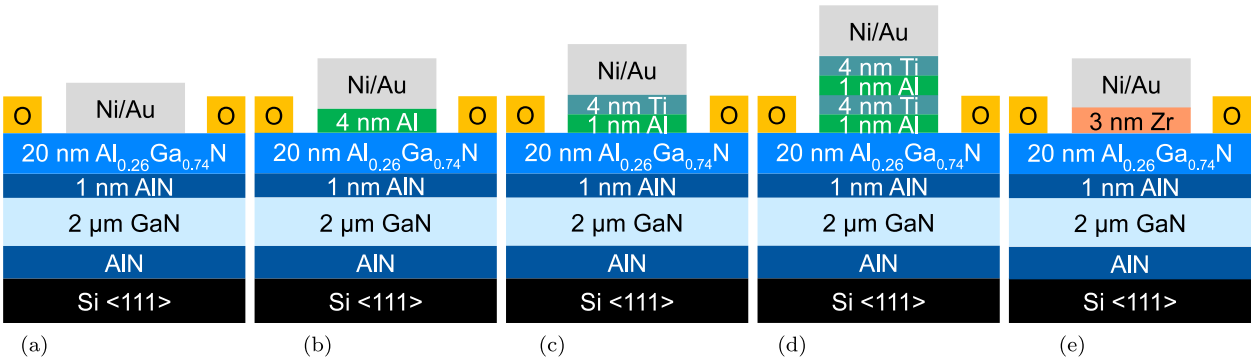


FIG. 1. Cross sections of the processed devices illustrating the various fabricated gate stacks. "O" is for ohmic contacts.

terms of crystallinity, I-V, and C-V characteristics. Values for N_{it} are extracted and a pathway for obtaining e-mode behaviour is sketched.

II. EXPERIMENTAL

The epitaxial layer stack used for device processing was grown on a 6-in. Si substrate in an AIXTRON SE planetary reactor. The growth was initiated with a low-temperature AlN nucleation layer. On top, a high temperature AlN layer and a GaN buffer were deposited. The epitaxial process was finalised with the growth of a thin AlN spacer layer and a 23 nm $Al_{0.26}Ga_{0.74}N$ barrier layer. A two-dimensional electron gas (2DEG) is formed below the AlN spacer. Before device processing, the wafer was diced into square samples.

Five samples for which the large-area diode cross sections are illustrated in Fig. 1 were prepared for device fabrication. The samples were subjected to a chlorine-based dry etch for mesa isolation and to the deposition of a Ti/Al/Ni/Au stack for ohmic contact formation. After the deposition, the samples were annealed at 825 °C for 30 s in nitrogen atmosphere. The gate patterning step differed for the five samples. For the Schottky-gated reference, a conventional Ni/Au stack was evaporated in an electron beam (e-beam) chamber. Samples Al, Al/Ti, and Zr were processed following the process flow described in Ref. 12. After patterning the resist for gate lithography, thin metal layers (either Al, Al and Ti, or Zr) were deposited on the samples by means of e-beam evaporation. Subsequently, the samples were subjected to an oxygen plasma in an inductively coupled plasma reactive ion etch (ICP-RIE) chamber. To obtain optimal results for each sample, the DC bias during oxidation was slightly different for the samples (details in Table I). Other process parameters were kept constant, such as the chamber pressure of 13.3 Pa, the oxidation time of 10 min, the ICP power of 50 W, and the oxygen flow rate of 30 sccm. For sample 2xAl/Ti, the last two steps were repeated to double the gate dielectric thickness. Following the oxidation step, the samples (together with the reference) were reinserted in the e-beam chamber and the final Ni/Au (50 nm/200 nm) gate electrode was deposited. To activate interface and/or oxide charges,[12] the samples with the oxidised metal layers were finally subjected to an annealing step under nitrogen atmosphere for 10 min. The actual layer thicknesses of the thin films, the parameters during the oxidation step, and the annealing temperature are given in Table I.

TABLE I. Process parameters which were different for the five samples.

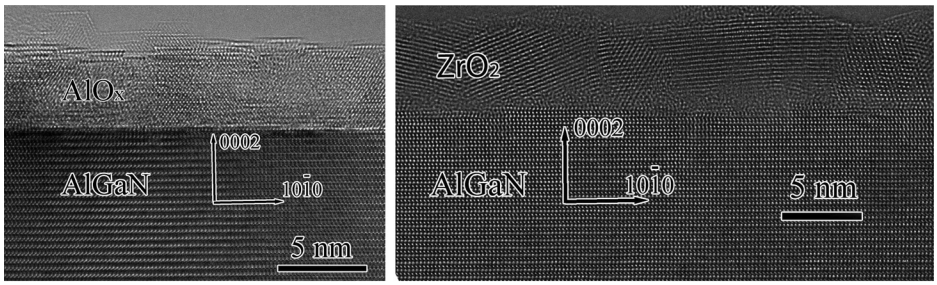
Sample	LayerThickness (nm)	DC bias in ICP (V)	Annealing temperature (°C)
Schottky	…	…	…
Al	4	−55	600
Al/Ti	1/4	−55	400
2xAl/Ti	1/4/1/4	−55	400
Zr	3	−90	600

For the characterisation of the plasma-oxidised metal layers, transmission electron microscopy (TEM) and energy dispersive X-ray spectroscopy (EDX) were performed on large-area control samples featuring only the gate stack on top of the heterostructure. These samples were also annealed in the same run as their respective fully processed sister samples. Cross-sectional TEM specimens were prepared using mechanical polishing and Ar ion milling. The specimens were studied in high-resolution using spherical aberration-corrected TEM that allowed to observe the interface structure between the AlGaN layer and gate contacts without delocalisation. Additionally, I-V and C-V characterisation was performed on large-area diodes with a diameter of 100 μm.

III. RESULTS AND DISCUSSION

First, sample Al and sample Zr were investigated by means of TEM and EDX (no such analyses were performed on the other samples). The oxide of sample Al for which the TEM micrograph is shown in Fig. 2(a) appears to be polycrystalline throughout the layer. Between the AlGaN barrier and the AlO_x layer, no amorphous interface layer is detectable. Additionally, the interface between oxide and barrier seems to be sharp with only single atomic steps. On the upper interface, the oxide layer appears slightly less well defined with an increased roughness of about two atomic layers. The total thickness of the layer is about 5.5 nm. By EDX analysis, the presence of oxygen in the Al layer is clearly identified.

For the Zr sample (Fig. 2(b)), the appearance of the oxide is slightly different. Although the oxide layer is also polycrystalline, a poorly ordered and a possibly amorphous layer at the oxide-barrier interface is visible. This layer, however, seems to be not continuously present. It rather consists of islands between which also crystalline parts of ZrO_2 in contact to AlGaN are seen. Consequently, the interface is not as sharp as



(a) (b)

FIG. 2. Aberration-corrected high-resolution TEM image of (a) sample Al and (b) sample Zr.

in the case of AlO_x. It varies over two atomic layers. The surface roughness appears to be very similar to the one of AlO_x. The thickness of the layer is extracted to be 6.0 nm.

The insulating properties provided by the plasma-oxidised layers were investigated by I-V measurements of large-area diodes. The resulting I-V characteristics are shown in Fig. 3. The measurement was performed from negative to positive bias. For each sample (except 2xAl/Ti), several devices are shown. The Schottky sample exhibits already quite a low reverse leakage current of about 3×10^{-5} A/cm^2. Under forward bias, the diode turns on with a steep slope reaching 1 A/cm^2 at about 1.4 V. Sample Al shows a reduction of reverse leakage current by about one order of magnitude. In addition, thermionic emission responsible for the sharp turn-on of the Schottky diode is suppressed at positive gate bias. However, it is not possible to maintain a very low current level above +1 V. At +4 V gate bias, the current reaches a value of about 0.1 A/cm^2. Compared to a 6 nm thick atomic layer deposited AlO_x layer, the insulation is less effective.[7] Compared to sample Al, a very similar picture is observed for the Al/Ti sample. Leakage in reverse direction is reduced by two orders of magnitude. Under positive gate bias, however, the suppression is less pronounced than in the case of AlO_x. The sample reaches 1 A/cm^2 at 3.3 V. The double oxidised sample 2xAl/Ti shows no suppression of leakage current in reverse direction. However, the current in forward direction is apparently much comparable to one of the single oxidised samples Al/Ti. It appears that, despite the twofold physical thickness, no extra insulation is provided. Finally, the Zr sample features the lowest reverse leakage current of all samples with a value of about 1×10^{-8} A/cm^2. Also under forward bias, the sample shows significant reduction in current

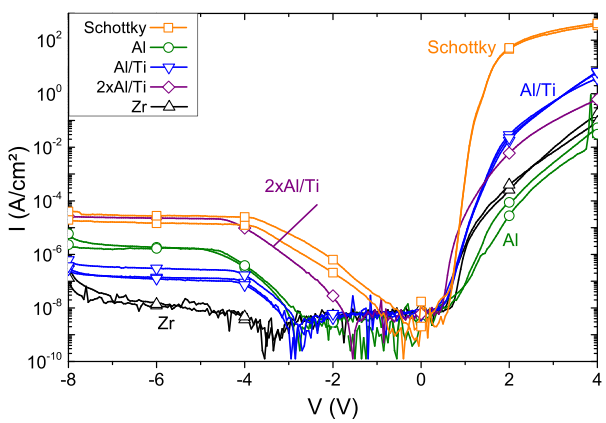


FIG. 3. I-V characteristics of large-area diodes.

reaching a level similar to one of the AlO_x samples. In addition to the different levels of leakage current, the zero crossing of the currents apparently deviates from 0 V for each plasma-oxidised sample. The value of the zero current point appears to correlate with the reverse leakage current level. This effect is strongest for the ZrO_x sample and gives already a first sign towards the existence of charge in the oxide or at the oxide-barrier interface.

To allow for the extraction of the oxide capacitance C_{ox}, C-V measurements were analysed on large-area diodes (diameter 100 μm) at a frequency of 1 MHz. The results of the C-V characterisation are shown in Fig. 4. Values for C_{ox} were extracted by taking into account that the total capacitance is determined by the series connection of oxide and barrier capacitance. The latter was determined via the Schottky-gated reference. To ensure comparable boundary conditions for all samples, the capacitance values were taken at biases at which the same sheet carrier concentrations of $n_s = 5 \times 10^{12}$ cm^{-2} were obtained. As expected, all samples with plasma-oxidised dielectric films yield significantly lower capacitance values than the Schottky reference. This confirms the presence of oxide layers. Sample Al features the lowest capacitance, most likely due to the rather low relative permittivity ϵ_r for Al_2O_3 of about 9.[7,14] The oxide capacitance of the AlO_x layer in this study is 181 nF/cm^2. With the oxide thickness of 5.5 nm extracted from the TEM image, the resulting ϵ_r would be extremely low with a value of about 1.1. Since these values seem to be unreasonably low, it must be assumed that the Ni gate electrode is also oxidised. As has been shown in Ref. 12, the value for C_{ox} is decreasing with increasing annealing temperature. Furthermore, it has been shown that by providing oxygen via the ambient, thin Ni films oxidise already at lower temperature of about 500 °C.[15] In our case, the oxygen is most likely provided by the plasma-oxidised metal layer. By assuming a relative permittivity of 9 for AlO_x, an AlO_x thickness of 5.5 nm and a relative permittivity of 17 for NiO,[16] the NiO thickness would be 73 nm, a value which may seem reasonable for 50 nm Ni. However, it is highly likely that no stoichiometry is given for the NiO and that the permittivity is well below the value of 17, such that the 73 nm can be considered as an upper limit.

This assumption is confirmed by EDX analyses which were performed on the prepared cross-sections. The cross-section for sample Zr is exemplarily shown in Fig. 5(a) (holds as well for sample Al). It is noted that during sample preparation, the upper metal stack peeled off, turned upside down, and hence, Ni is seen on top of Au (Fig. 5(a)). Based

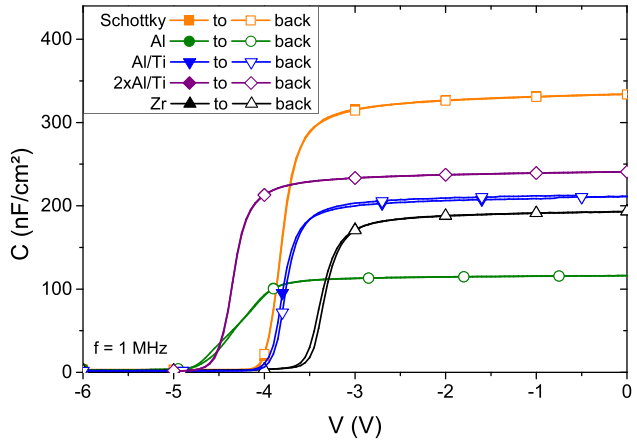


FIG. 4. C-V characteristics of large-area diodes.

on the C-V and I-V characteristics, we can exclude this for the patterned samples. The resulting EDX spectra for Au, Ni, and O are depicted in Figs. 5(b), 5(c), and 5(d), respectively. Apparently, the oxygen concentration is very large in the Ni-rich volume. Increased amount of oxygen is also seen in the plasma-oxidised layer. The presence of oxygen in the Au layer is correlated with background noise. In higher resolution images (not shown), a very sharp interface is visible for the oxygen plot at the plasma-oxidised layer/AlGaN barrier interface. This indicates that, indeed, only the metal layer was oxidised and not the barrier material.

The C-V curve for sample Al shows quite a large stretch-out in the threshold region. This may well be correlated to either slight thickness inhomogeneities as observed in Fig. 2(a) or to local variations in the density of fixed charges (interface and/or oxide). Both effects would in turn result in an inhomogeneous V_{th} and hence, a non-uniformity in capacitance onset.

For sample Al/Ti, C_{ox} is considerably increased to a value of 575 nF/cm^2. This increase is likely to have two origins. First, for TiO_x layers, values for ϵ_r have been reported to reach almost 100 (Refs. 17 and 18) (which in those cases is most probably related to the rutile phase[19]), well above one of the AlO_x. In our case, at annealing temperatures of 400 °C, the anatase phase may be more likely. Still, for this phase, ϵ_r is typically about 40.[19] Due to the missing TEM analysis for the Al/Ti sample, no exact value of ϵ_r can be extracted here. As second origin of the increased value of C_{ox}, the annealing temperature for this sample was well below one of the AlO_x samples giving rise to the assumption that less Ni is oxidised. For sample 2xAl/Ti, an increase in capacitance is observed. This behaviour can only be explained if incomplete oxidation of the double Al/Ti stack is assumed and it clearly shows the limitation of this method.

The Zr sample shows a moderate capacitance value. C_{ox} is in between those of AlO_x and AlO_x /TiO_x. This is within expectation as ϵ_r values for ZrO_x have been reported to be in the range of 20 to 30.[20,21] With a C_{ox} of 467 nF/cm^2 and a layer thickness of 6 nm, ϵ_r for this oxide layer is calculated to be 3.2, indicating again the formation of NiO. Depending on the permittivity of ZrO_x, the NiO thickness is calculated

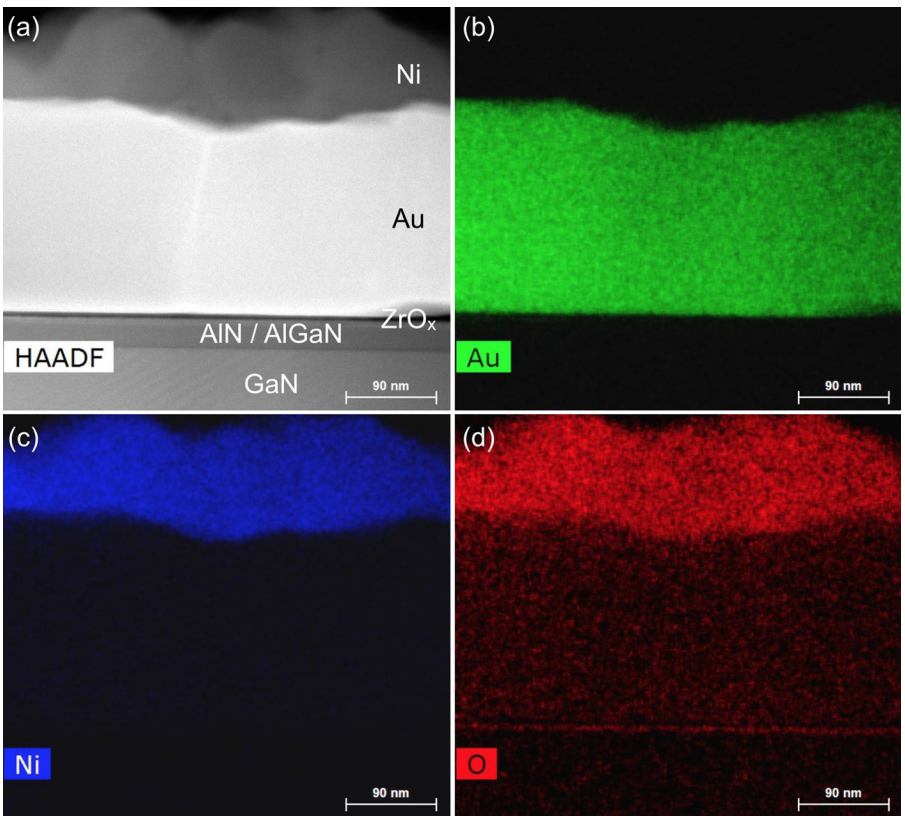


FIG. 5. (a) High-angle annular dark field (HAADF) scanning TEM (STEM) micrograph of sample Zr and elemental maps for (b) Au, (c) Ni, and (d) O extracted from EDX analysis.

to be 27 to 29 nm. With the same annealing temperature as for sample AlO_x, the same NiO thickness would be expected. Hence, this gives rise to believe that the amorphous layer seen in the TEM images is of low permittivity and further that the relative permittivity of ZrO_x may be well below 20. Although oxide formation is reported successfully here, it is concluded that the capacitance values are much lower than expected.

To extract values for V_{th}, the C-V curves were integrated over the voltage and a linear fit was applied at 0 V gate bias providing the value of V_{th} at the x-axis intercept. The Schottky sample exhibits a V_{th} of −3.8 V. With the low capacitance for the plasma-oxidised samples, very negative values for V_{th} would have been expected. However, as apparent from Fig. 4, this is not the case. The most negative V_{th} is extracted for sample 2xAl/Ti with a value of −4.3 V, followed by sample Al with −4.2 V. In contrast, also positive V_{th} shifts (ΔV_{th}) with reference to the Schottky sample have been realised for sample Al/Ti with $V_{th} = -3.7$ V and for sample Zr with $V_{th} = -3.3$ V. These positive ΔV_{th} are very favourable for the realisation of e-mode devices.

With these low negative or even positive ΔV_{th} values, the presence of negative charges in the oxide or at the oxide-semiconductor interface has to be assumed. For simplicity, all relevant charge contributions may be expressed as a single quantity, which is N_{it} (at the expense of losing information like location or density distribution). For a quantitative estimate of the fixed charge density, a simplified equation based on Ref. 6 lumping all charges into the single quantity N_{it} is used

$$N_{it} = -\frac{C_{ox}}{e}\left[V_{th} - \left(\frac{\Phi_B}{e} - \frac{\Delta E_C}{e}\right) + \frac{\sigma_{int}}{C}\right]. \quad (1)$$

Φ_B corresponds to the Schottky barrier height, ΔE_C to the conduction band offset between barrier and channel, σ_{int} to the difference in polarisation charge between barrier and channel, and e to the elementary charge. As boundary condition, it is assumed that the increase in barrier height for a MOS structure compared to a Schottky-gated structure is fully compensated by the additional conduction band offset between oxide and barrier. This assumption appears arbitrary, however, even assuming reasonable variations in the order of 0.3 eV,[22] the resulting change in N_{it} would only be about 10%. On the basis of the Schottky sample, parameters for Φ_B and σ_{int} have been extracted to be 1.36 eV and 1.53 μC/cm^2, respectively. ΔE_C was calculated to be 0.46 eV. As a result of the negative ΔV_{th} for sample 2xAl/Ti and Al, N_{it} is lower than σ_{int}/e with values of -6.9 and -9.1×10^{12} cm^{-2}, respectively. For the samples showing the positive ΔV_{th}, N_{it} is necessarily higher than σ_{int}/e. While for sample Al/Ti, N_{it} equals to -9.9×10^{12} cm^{-2}, it is -1.1×10^{13} cm^{-2} for sample Zr. With these extracted values, it appears that there is a direct relation between the value of the zero-current offset and the amount of fixed charge as discussed for Fig. 3.

Despite having AlO_x in contact with the semiconductor in three samples, there is apparently a difference in extracted values of N_{it}. While for sample 2xAl/Ti, this may well be correlated to its incomplete oxidation (oxygen is not completely moving to the interface), for samples Al/Ti and Al, there is still a slight difference of about 10%. The difference can either be referred to the limited accuracy of the extraction or to the presence of fixed charges in the oxide, which are likely to be differing for AlO_x and TiO_x.

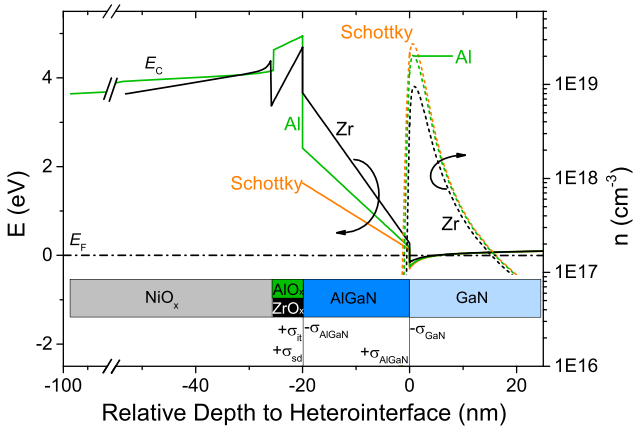


FIG. 6. Band diagrams and 2DEG electron density of samples Schottky, Al and Zr. The corresponding interface charges are also illustrated.

To illustrate the effect of the interface charge and the oxides on the conduction band E_C alignment, band diagrams were simulated by solving self-consistently the Poisson equation for the Schottky-gated sample and for samples Al and Zr. For the latter two, it is assumed that all oxide-related charges reside at the oxide-semiconductor interface. Band parameters for the nitrides were taken from Ref. 23, for AlO_x and ZrO_x from Ref. 24, and for NiO from Refs. 25 and 26. It is noted that, in particular for NiO_x, band parameters can vary by large in dependence on the composition.[25] The thicknesses were used as extracted from TEM and C-V analysis. The resulting conduction bands are shown in Fig. 6 together with the various interface charge densities. σ_{sd} denotes the surface donor charge which is compensating the polarisation charge of the barrier σ_{AlGaN}. σ_{it} is the resulting charge of the fixed interface charges ($\sigma_{it} = e \cdot N_{it}$) and σ_{GaN} the polarisation charge of the buffer.

It is seen that with both oxides, E_C in barrier and channel is lifted. This is originated in the presence of the negative

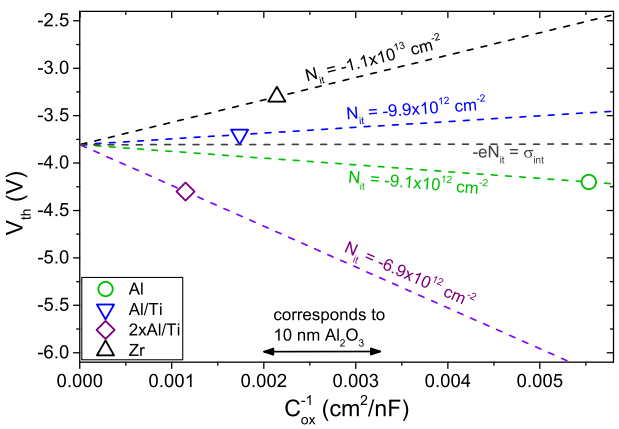


FIG. 7. Behaviour of threshold voltage vs. the inverse oxide capacitance for four different interface charge densities, which were extracted for the four samples. The stars depict the actual values extracted for the samples. The dashed line which is aligned horizontally indicates the case of the interface charge matching the polarisation difference between barrier and channel.

N_{it}. The E_C lift leads to a reduction in 2DEG density. In the case of Al, this conduction band lift is considerably weaker than for Zr. Owing to the reduced capacitance, however, V_{th} is still more negative in the case of Al (not shown for the simulation), whereas it is more positive in the case of Zr.

As illustrated in Fig. 7, for sample Zr, the low overall capacitance is beneficial in moving V_{th} to more positive values. If one would deposit a charge-free dielectric on top of the plasma-oxidised layer, an additional positive ΔV_{th} of +0.5 V could be realised, e.g., by the deposition of 22.5 nm charge-free Al_2O_3. Hence, this method is shown to be very beneficial to control N_{it} and thus also for the realisation of e-mode behaviour. The latter can easily be realised by applying, e.g., a barrier with low polarisation, a backbarrier, and a gate recess (all effects discussed in Ref. 9) in combination with the plasma-oxidised metal layer. As we have shown negative N_{it} of $-2.3 \times 10^{13}\,cm^{-2}$ for gate-recessed devices with ALD-oxide in the past,[9] it would be very promising to investigate N_{it} using the plasma-oxidised metal layers in combination with a gate recess.

IV. CONCLUSION

In summary, we have analysed MOS heterostructures fabricated with plasma-oxidised metal layers as gate dielectric. By TEM analysis of selected oxidised layers, the morphology of these has been identified to be polycrystalline. While for Al as thin film, no amorphous interfacial layer has been observed, for Zr as thin film, amorphous parts appeared at the oxide-semiconductor interface. I-V characteristics have revealed considerable leakage current reduction, which is, however, not sufficient for the application in e-mode devices. By analysis of C-V measurements, the relative permittivity of the AlO_x and ZrO_x thin films have been extracted. With the very low values derived, it has appeared that not only the thin metal film was oxidised but that during annealing also the Ni gate electrode has been oxidised at least partly. Additionally, V_{th} has been analysed to gain insight into the interface charge density. In particular, the sample featuring ZrO_x has shown a very high number of negative N_{it}, allowing for positive ΔV_{th}. In the future, the plasma-oxidised Zr layer should be combined with a highly insulating gate dielectric such as atomic layer deposited Al_2O_3 to both benefit from better insulation as well as further positive ΔV_{th}.

ACKNOWLEDGMENTS

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