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Tools and methods for measuring and tuning the energy efficiency of HPC systems

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Abstract. Energy costs nowadays represent a significant share of the total costs of ownership of High Performance Computing (HPC) systems. In this paper we provide an overview on different aspects of energy efficiency measurement and optimization. This includes metrics that define energy efficiency and a description of common power and energy measurement tools. We discuss performance measurement and analysis suites that use these tools and provide users the possibility to analyze energy efficiency weaknesses in their code. We also demonstrate how the obtained power and performance data can be used to locate inefficient resource usage or to create a model to predict optimal operation points. We further present interfaces in these suites that allow an automated tuning for energy efficiency and how these interfaces are used. We finally discuss how a hard power limit will change our view on energy efficient HPC in the future.

Keywords: Energy efficiency, energy and performance measurement, HPC, high performance computing, energy optimization tools, energy models, energy-efficiency tuning

1. Introduction to energy efficiency considerations in HPC

Within the last decade, energy costs of High Performance Computing (HPC) systems have significantly increased and now represent a significant share of the total cost of ownership (TCO) of such a system. Thus, servers and HPC systems are now not only evaluated in terms of throughput, but also in terms of energy efficiency as a second major requirement. In order to improve energy efficiency, research and developments targeting a lower power consumption have intensified with the ultimate goal to reach a maximum throughput within a given energy budget. The developments include the addition of hardware and operating system support for energy efficient operation in processors, node devices and memory. Current HPC systems are built from components with this kind of energy efficiency support and provide interfaces to control them. However, tuning energy efficiency is still a matter of research. HPC poses additional challenges regarding energy efficiency, as the impact on performance has to be very low in order to be acceptable. Higher performance and low power consumption are contradictory when a decrease in power consumption results in a

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longer execution time. Still, more and more HPC centers use the facilities to manipulate the energy consumption of applications e.g., by reducing the processor voltage and frequency. To find an optimal balance between energy efficiency and high performance of computations, hardware and software characteristics have to be taken into account.

The field of power and energy consumption analysis of HPC systems and applications is currently dominated by administrators and researchers, with very few application developers caring about these topics. However, with more and more HPC systems providing power measurement capabilities, HPC centers are able to switch from a CPU hour based allocation of resources to an allocation and accounting scheme that also reflects power bounds and electricity costs. Energy-aware scheduling has been detailed in [24,49,50] and is already supported by LoadLeveler [5]. Thus, in the near future all users of HPC systems might have to deal with energy efficiency, for which we provide an overview on several key areas.

The rest of the paper is organized as follows. We discuss several energy-efficiency metrics for both HPC systems and applications in Section 2. To complement the discussion on the basic steps prior to tuning, we provide guidelines for the choice of power measurement tools and interfaces in Section 3 and Section 4. The inclusion of performance and energy data into existing performance measurement infrastructures is described in Section 5. The paper is enriched with the illustration of an energy model that describes how the usage of power saving mechanisms influences performance and energy-efficiency in Section 6. We present tuning approaches and the integration of tuning cycles in performance analysis tools in Section 7. We close this paper with an outlook to the upcoming challenge of optimizing performance under a constant power consumption in Section 8 and provide a summary and outlook in Section 9.

2. Energy efficiency metrics

As in every optimization process, energy efficiency optimizations are highly influenced by the applied performance metric. While traditional performance metrics focus solely on throughput (e.g., FLOPS, IPC, MB/s), energy efficiency metrics focus on a trade-off between throughput (i.e., runtime) and energy costs (i.e., consumed energy). In this section, we discuss the most prominent metrics, the reader needs to know when interpreting energy-efficiency-performance data.

In HPC, the most common and known metric is FLOPS/W and depicts how efficient a system can execute the LINPACK benchmark, which is known to be very energy intensive. This metric is associated with the Green500 list [14] that was announced to accompany the established TOP500 list [13]. A major drawback of using LINPACK as the only benchmark case is that it does not reflect the typical workload of production HPC systems. The SPEC OMP2012 [33] benchmarks allow to accompany performance results with power and energy information. SPEC provides an infrastructure to measure the power consumption and defines measurement rules and certified watt-meters to avoid the submission of inaccurate results.

Energy-to-solution is an established metric to quantify the energy efficiency on a system for a specific code solving a specific problem. However, this metric only reflects the energy budget of running the application. The aim to either increase throughput within a given energy budget or reduce energy for a given throughput is not reflected. Thus, other metrics emphasize both runtime and energy consumption of an application. One metric in this context is the energy-delay product (EDP) introduced in 1994 [21]. It presents a compromise between low power and high performance and is well suited to guide research efforts. For scenarios where performance is even more important, the delay part may be emphasized by using an $\mathrm{ED}^n\mathrm{P}$ metric [10], often $\mathrm{ED}^2\mathrm{P}$ is used, or the generalized FTTSE metric [9], where an arbitrary function defines the ratio of performance and energy consumption.

In a computing center context though, energy efficiency is only one of the requirements. Additional constraints may be maximum power capping or constant power consumption with only small perturbation. If those constraints are met, a power supplier can often provide a significantly lower price, thus increasing the efficiency in terms of TCO. In Section 8 we discuss the challenges that arise with such a hard power bound.

3. Measuring power and energy

Prior to tuning energy consumption, researchers have to select an appropriate measuring tool with the required spatial and temporal granularity. In this section we discuss different solutions for measuring power and energy, accompanied by an overview of advantages and shortcomings for possible use cases. The following devices present an overview from finer to coarser spatial granularities of common power measurement alternatives.

RAPL [37], APM [26], and various performance counter based approaches (e.g. [11,18,25,43]) implement power consumption or energy consumption models based on processor events in hardware or software. One advantages of using such a model is the high update frequency (e.g., 1 kHz for RAPL), which is suitable for understanding the behavior of short code paths. However, there are several disadvantages when using processor event counters. These include for example measurement overhead due to the in-band measurement and model inaccuracies.

Power meter toolkits also allow measurements of fine granular devices such as CPU, disk, or different voltage lanes with dedicated current or power sensors. Examples of tools interfacing such sensors are PowerPack [15], PowerMon [8] and Amester [27]. High measurement frequencies of up to 1 kHz make them appropriate for code paths instrumentation and longer running applications. One disadvantage reported by Diouri et al. [12] are the differences in the accuracy of the measurements (more than 50% variation). The paper concludes that these tools require careful calibration.

At node level, common interfaces include paddle cards and power supply units (PSU) that provide Intelligent Platform Management Interface (IPMI) sensors. The temporal granularity is mostly within the range of 1–10 Hz [19,22]. Thus, they can only be used to create statistical profiles for long running applications, but will fail to examine short code paths. Hackenberg et al. [19] report accurate results from IPMI PSU measurements for constant power consumption scenarios. However, they also show that such sensors can be inaccurate if the running workflow provides a high power fluctuation.

There are "smart" Power Distribution Units (PDUs) which also feature a built-in powermeter circuitry capable of reporting out-bound measurements of instantaneous power via IPMI. These PDUs usually allow power readings on node level, rack level, or for the networking equipment. Typically, the queries can be done at the scale of seconds [19] or minutes [35]. Due to the low temporal resolution, they are only useful for obtaining statistical information.

Due to the diversity of tools, we only provide an overview. If one targets to lower the energy consumption of a specific component (e.g., main memory, CPU, or accelerator card) or a certain code-path, a fine grained instrumentation should be chosen. To verify optimizations at application level, the power should be measured at least at node level. The most important considerations when choosing a power measurement infrastructure include accuracy, and requirements on time and spatial resolutions.

4. Energy-efficiency related performance data

Measuring the power consumption is not necessarily sufficient to analyze applications and systems. To explain why and where a certain amount of energy has been spent when running an application, additional data is necessary. A low power consumption, for example, can be achieved by using a low frequency, but it could also be caused by the use of idle states, thermal throttling, or instructions that use less power. A high power consumption of a computing node can result from an intense use of an accelerator or the processor. Thus, the first step is to obtain additional data to understand the reasons for a certain power level and in the next step to lower the energy consumption.

Different aspects influence the power consumption of processors. These include the ACPI standardized P-, C-, and T-states [2], utilization of execution units and data transfers [32], and the clock gating of different parts of processors and processor cores [26]. While some of them are transparent (small scale clock gating), others can be observed via software and hardware counters. P-States that refer to voltage and frequency changes can be observed via instrumentation on methods that issue a change [39], via hardware performance monitoring units (PMUs) or special model specific registers (MSRs) like `APERF` and `MPERF` on newer x86 processors. C-States that implement idle-states can also be measured via instrumentation [39] and specialized MSRs [7] (residency counters). On recent Intel and AMD processors, T-States that refer to a processor throttling due to thermal constraints can be measured via MSRs as well as the temperature of computing cores. The Linux operating system allows to access most of this information in terms of special virtual file systems as `sysfs` and `procfs`.

C-States for example are measured on a per CPU base where each C-state issue is counted. Statistics about the C-state usage are reported in the `sysfs` on a per-CPU base. Due to C-state undemotion these numbers are, however, not entirely correct but represent only the issued C-states, not the ones that were actually initiated by hardware. Access to the hardware information is provided by residency counters [23] that can be accessed via the `msr` kernel module. A higher level of abstraction provides the powertop tool that provides statistics based on MSR readings.

Data transfers and computations in processor cores influence the power consumption to a high degree [32]. Many relevant performance events about processor core and cache activities and can be extracted from the hardware PMUs available on all modern processors. PMU counters that define activities within a processor core are often available per core or per thread (if simultaneous multi threading is active). Counters related to shared parts of the chip (often referred to as uncore by Intel or northbridge by AMD) require to program special PMUs which are valid on a per chip scope. To access the PMU data hardware performance monitoring tools like perf (included in the Linux kernel) or LIKWID [46] may be used.

5. Performance analysis tools and energy efficiency metrics integration

In the previous section we described how one can measure energy and performance related metrics. In this section, we present current state-of-the-art HPC performance analysis tools that integrate such information. These tools allow the measurement and comparison of the energy efficiency of parallel applications and relate energy information with performance data. Thus, they allow performance analysts to understand the reasons for an inefficient or efficiency energy consumption and what bottlenecks different application regions (e.g., subroutine calls) face.

A common way to observe the resource usage of an application is using hardware performance counters like floating-point instructions or cache misses via an interface like PAPI [44]. Most common HPC performance measurement tools (e.g., [1,16,17,29,30,36,40, 42,46]) allow performance counter measurements at a region level or a sampling of performance counters. As discussed in Section 2, several researchers build power and energy models based on hardware counters which would allow to estimate the energy consumption of such software regions. However, performance counter based models have to be determined for every new hardware generation and even for each processor or processor core due to process variation which can be unfeasible. Thus, to support power and energy measurements the performance tools need to include support for power meters and relevant data.

Instrumentation-based tracing tools record all events in an application (e.g. function enter/exit, MPI communication, etc.) and stores that in a trace file which can be analyzed post mortem, either manually with tools like Vampir or Paraver or automatically with Scalasca. Tracing provides a very high overhead and generates enormous amounts of data, especially when hardware counters are recorded. Instrumentation-based profilers obtain usually the same events as the tracing tools, but aggregate them instead of storing each event.

In summary, with profiling it is possible to see how much time was spent in a function and how often it was called, but only with tracing is it possible to examine each execution of the function.

5.1. Profiling-based tools

Power consumption data is often provided asynchronously to the application instrumentation, thus it can not necessarily be related to a certain code region. Additionally the power measurement is often implemented out-of-band to avoid interfering with the performance measurement. In such a case, power data is collected after the instrumented application finishes its execution. While this post-mortem integration is not necessarily a problem for tracing, it is for profiling.

Ideally, profiling tools access energy counters. These counters integrate the power data transparently to the measurement system and return the energy consumption between two measurement points. However, only few systems provide such an interface. Intel's RAPL interface that we discussed in Section 3 can be a solution for systems with Intel processors even though it is limited [19]. The alternative would be a power measurement sampling between the two measurement points by the tools and an integration in software, but this again implies an inherent overhead.

The profiling tool Periscope implements an interface to measure energy in Sandy Bridge-EP microarchitectures via the enopt library [34]. The current version of this library allows to measure the energy consumed at the instrumented regions of the user application.

5.2. Tracing-based tools

Tracing-based tools do not need the energy information at runtime but can merge this information into the trace in a post-mortem step. They also do not rely on energy data that is provided at the same time scale as the instrumentation points. Thus, there is a variety of tools supporting power and energy information. Schöne et al. [39] describe an plugin counter interface for VampirTrace [29] that can be used to include external information in application traces. They also present the inclusion of power relevant data, like frequency changes, the use of idle states and power consumption.

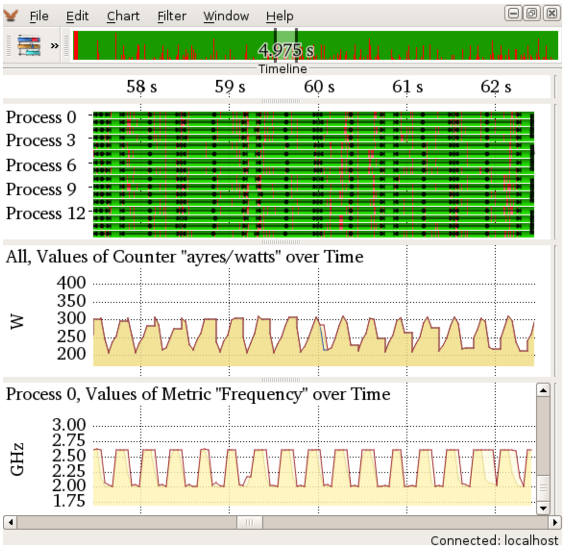
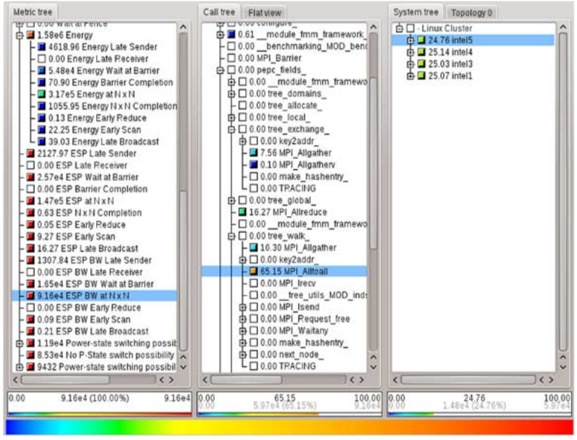


Fig. 1. Vampir: Displaying power and frequency information for an DVFS optimized execution of the MPI parallel NPB benchmark SP on a dual-socket Sandy Bridge system. (Colors are visible in the online version of the article; http://dx.doi.org/10.3233/SPR-140393.)

Figure 1 shows an example where power consumption and processor frequency is plotted with application runtime characteristics. Hackenberg et al. [19] and Knobloch et al. [27] implement counter plug-ins include other power sources allowing for fine-grained power measurements on IBM POWER7 hardware.

The interface for including external data into application traces has been ported to the Score-P measurement system and is included in the current release. The Technische Universität Dresden is implementing plug-ins for several power measurement devices so that experiments can be performed on power-aware HPC-systems.

Knobloch et al. [28] have analyzed the external power information in Vampir to see that a parallel application has shown high power consumption in MPI routines due to active waiting, i.e. polling with highest frequency whether the communication partner is ready. Using this information, Scalasca has been extended to determine the energy-saving potential in wait-states of parallel applications. An example of such an analysis is shown in Fig. 2. However, due to the aggregation of the data, Scalasca requires energy consumption data (similar to the profiling tools requirements) to perform a meaningful analysis. With such an energy data source available, it would be possible to determine whether it is better to do a race-for-idle or slow down computation to reduce wait times.



```
1.58e6 Energy
  4618.96 Energy Late Sender
  0.00 Energy Late Receiver
  5.48e4 Energy Wait at Barrier
  70.90 Energy Barrier Completion
  3.17e5 Energy at N x N
  1055.95 Energy N x N Completion
  0.13 Energy Early Reduce
  22.25 Energy Early Scan
  39.03 Energy Late Broadcast
2127.97 ESP Late Sender
0.00 ESP Late Receiver
2.57e4 ESP Wait at Barrier
0.00 ESP Barrier Completion
1.47e5 ESP at N x N
0.63 ESP N x N Completion
0.05 ESP Early Reduce
9.27 ESP Early Scan
16.27 ESP Late Broadcast
1307.84 ESP BW Late Sender
0.00 ESP BW Late Receiver
1.65e4 ESP BW Wait at Barrier
9.16e4 ESP BW at N x N
0.00 ESP BW Early Reduce
0.09 ESP BW Early Scan
0.21 ESP BW Late Broadcast
1.19e4 Power-state switching possit
8.53e4 No P-State switch possibility
9432 Power-state switching possibil

0.00    9.16e4 (100.00%)    9.16e4
```

```
0.61 __module_fmm_framework_
0.00 __benchmarking_MOD_benc
0.00 MPI_Barrier
0.00 pepc_fields_
  0.00 __module_fmm_framewo
  0.00 tree_domains_
  0.00 tree_allocate_
  0.00 tree_local_
  0.00 tree_exchange_
    0.00 key2addr_
    7.56 MPI_Allgather
    0.10 MPI_Allgatherv
    0.00 make_hashentry_
    0.00 TRACING
  0.00 tree_global_
  16.27 MPI_Allreduce
  0.00 __module_fmm_framewo
  0.00 tree_walk_
    10.30 MPI_Allgather
    0.00 key2addr_
    65.15 MPI_Alltoall
    0.00 MPI_Irecv
    0.00 __tree_utils_MOD_ind:
    0.00 MPI_Isend
    0.00 MPI_Request_free
    0.00 MPI_Waitany
    0.00 make_hashentry_
    0.00 next_node_
    0.00 TRACING

0.00    65.15    100.00
0.00    5.97e4 (65.15%)    9.16e4
```

```
- Linux Cluster
  24.76 intel5
  25.14 intel4
  25.03 intel3
  25.07 intel1

0.00    24.76    100.00
0.00    1.48e4 (24.76%)    5.97e4
```

Fig. 2. Scalasca: Displaying energy-saving potential (ESP) of PEPC, a plasma physics application from JSC, on an Intel Nehalem based cluster. The left pane shows the metric tree, here the ESP in collective MPI communication. The middle pane shows the distribution of these properties on the call tree, we see that 65.1% of the ESP is in a call to MPI_Alltoall in the tree_walk subroutine, and on the right pane the distribution among the system tree is shown, which indicates an equal distribution of the ESP across the nodes of the cluster. (Colors are visible in the online version of the article; http://dx.doi.org/10.3233/SPR-140393.)

Alonso et al. [4] present a framework which leverages Extrae and Paraver to analyze the power consumption and the energy consumption of parallel MPI and/or multithreaded scientific applications. The framework includes the `pmlib` library [6], which offers a simple interface to interact with a variety of wattmeters. Servat et al. [41] extend Extrae and Paraver to include power consumption information into traces from the RAPL energy model provided by current Intel processors.

5.3. *Use case*: *Detection of inefficient wait methods*

In [7] Barreda et al. define power sinks as a disagreements between the application activity and the system power consumption during the execution. They also present an inspection tool, based on Extrae + Paraver, that automatically detects power sinks by conducting a direct comparison between the application performance trace and the C-state traces per core.

In order to illustrate the possibilities of the inspection tool, Barreda et al. use an example corresponding to the concurrent solution a sparse linear system using ILUPACK,[1] a package that implements multilevel preconditioners for general and Hermitian posi-

[1] http://ilupack.tu-bs.de.

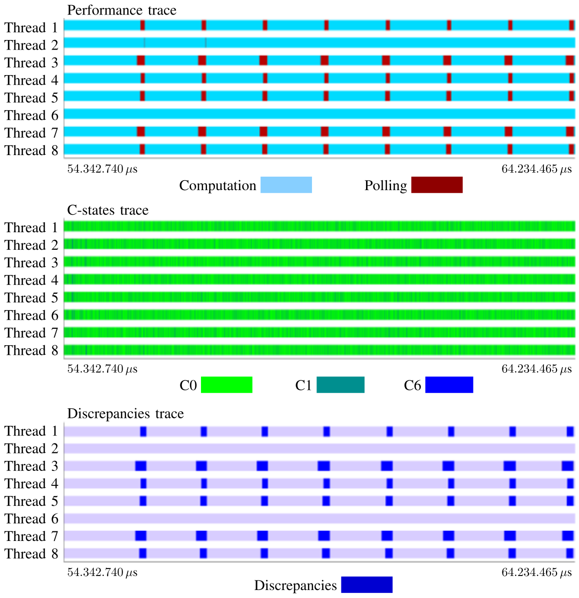


Fig. 3. Performance (*top*), C-states (*middle*) and discrepancies (*bottom*) trace, visualized with Paraver, for the concurrent execution of ILUPACK. (Colors are visible in the online version of the article; http://dx.doi.org/10.3233/SPR-140393.)

tive definite problems. The parallelization of this solver for multicore platforms in [3] relies on a task partitioning of the sparsity graph associated to the coefficient matrix of the system that yields a task acyclic graph. At runtime, tasks that are ready for execution (i.e, all dependencies are fulfilled) are added to a centralized queue. When a thread finishes its work, it polls to check if there is a new task in this queue.

Figure 3 shows fragments of the obtained performance and C-states traces for the parallel iterative solution stage of ILUPACK on a dual socket Nehalem system. The performance trace of the figure (top plot) shows that initially all threads perform computations. At regular intervals, threads wait for new tasks. The C-state trace (middle plot) does not show any significant variation. Thus, we can conclude that the threads perform a busy-wait. This is captured by the power-sink inspector, in the *power-sink* trace (bottom plot), which indicates a period where the application has performed no useful computation, but the cores remained active.

6. Using power models to predict energy efficient operation points

The ability to measure power enables the connection of the energy consumption to other parameters as code characteristics, runtime settings and frequency. In this section we describe how we can use the input from Section 5 for a simple qualitative power model that couples performance and energy to solution. We apply this model to the scalable `dgemm` benchmark. We use the ECM-model introduced in [45] and further refined and accompanied with a qualitative power model in [20]. In addition to previous publications we present the results by plotting energy to solution versus performance. This novel visualization technique has been introduced in [48].

The following basic assumptions go into the power and performance model:

(1) The whole N_c-core chip dissipates a certain baseline power W_0 when powered on, which is independent of the number of active cores and of the clock speed.[2]
(2) An active core consumes a dynamic power of $W_1 f + W_2 f^2$. We consider deviations from the baseline clock frequency f_0 such that $f = (1 + \Delta\nu) f_0$, with $\Delta\nu = \Delta f / f_0$.
(3) At the baseline clock frequency, the serial code under consideration runs at performance P_0. As long as there is no bottleneck, the performance is linear in the number of cores used, t, and the normalized clock speed, $1 + \Delta\nu$. The latter dependence will not be exactly linear if some part of the hardware (e.g., the off-core cache) runs in its own frequency domain. In presence of a bottleneck (like, e.g., memory bandwidth), the overall performance with respect to t is capped by a maximum value P_{roof}:

$$\begin{aligned} P(t) &= \min\bigl((1 + \Delta\nu) t P_0, P_{\mathrm{roof}}\bigr) \\ &= \min(t P_0 f / f_0, P_{\mathrm{roof}}). \end{aligned} \tag{1}$$

Since time to solution is inverse performance, the energy to solution becomes

$$E = \frac{W_0 + (W_1 f + W_2 f^2) t}{\min(t P_0 f / f_0, P_{\mathrm{roof}})}. \tag{2}$$

This model shows that any increase in performance (P_0 or P_{roof}) leads to proportional savings in energy to solution. Performance is thus the first-order tuning parameter for minimum energy. For the measurements in

[2] As can be seen in Fig. 4 W_0 is actually a function of the number of active cores. However, the qualitative insights from the model remain unchanged.

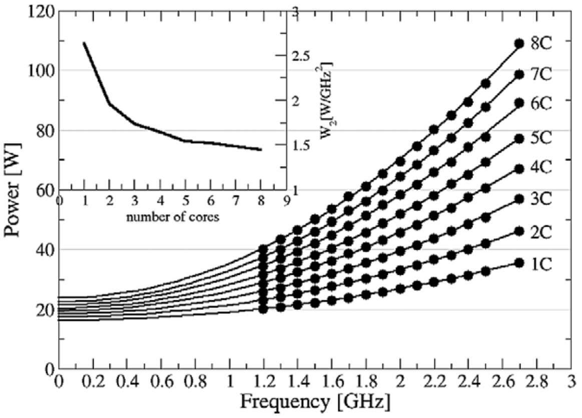


Fig. 4. Power for dgemm using different frequencies and core counts for single chip measurements. The filled circles are measured, the corresponding lines are fit functions determining the model parameters W_0, W_1 and W_2. The W_0 value varies from 16–23 W depending on the number of cores. This is due to the fragile fit on the left tail as there are no measurements below 1.2 GHz and also due to different states of all cores for different core counts. W_1 had no significant contribution and was therefore neglected on this test system. The resulting values for W_2 are shown in the inlet as function of number of cores. The TDP for this chip is 130 W.

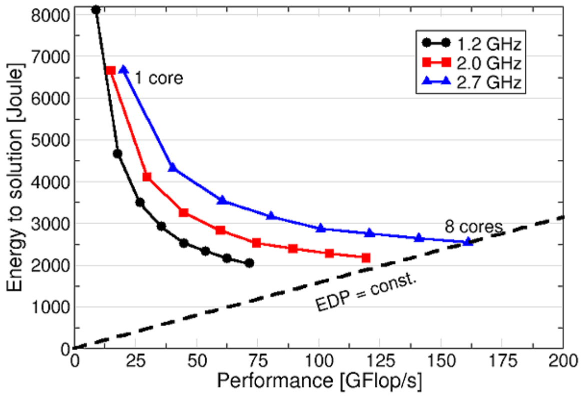


Fig. 5. Modelled power and performance. The modelled results predict correctly the optimal frequency for minimum EDP for dgemm. (Colors are visible in the online version of the article; http://dx.doi.org/10.3233/SPR-140393.)

this paper only the chip baseline power is taken into account neglecting any other power contribution on the node level. For more realistic estimates it is crucial to take into account the complete node baseline power. As demonstrated in [20] it is possible to analytically derive the frequency f_{opt} from Eq. (2) for minimal energy to solution:

$$f_{\text{opt}} = \sqrt{\frac{W_0}{W_2 t}}. \tag{3}$$

A large baseline power W_0 forces a large clock frequency to "get it over with" ("clock race to idle"). If considering the overall baseline power on current compute nodes (100 W on our test system) this case applies in many cases.

For qualitative results it is sufficient to assume approximate values that reflect general region properties known from code analysis and performance modeling (memory-boundedness, SIMD vectorization, pipeline utilization). For the test case covered in this paper the parameters were measured using RAPL on a 2.7 GHz Sandy Bridge processor. The chip power is measured for different core counts and frequencies and W_0, W_1, and W_2 are determined by fitting function to the measured points. Figure 4 shows the results for dgemm, for which on this particular chip there was a diminishing linear factor, thus W_1 was neglected. The inlet of Fig. 4 illustrates that the model parameter W_2 is a function of cores used per chip. Due to limited accuracy of the function fit and influence of C states on different cores also W_0 varies with core count.

With the model parameters determined energy to solution can be computed with core count and frequency as inputs. A useful way to visualize the relation between energy to solution and performance is to plot energy to solution versus performance with the number of cores used as a parameter within a data set for a specific frequency. One advantage of this plot variant is that points of constant EDP are straight lines. The targeted operation area is in the lower right quadrant defining the optimization space for a given code. For dgemm Fig. 6 shows that the lowest EDP is achieved if running at the highest nominal frequency. Still the turbo mode frequency is nearly as good in terms of EDP and better than lower frequencies. The model provided results shown in Fig. 5 correctly predict the optimal frequency setting. It enables qualitative insights in the energy to solution behavior of application codes. This model may be used in tuning tools Section 7 to determine the optimal operating point in terms of frequency and number of cores used surpassing solutions setting the frequency based on simple heuristics or generic settings.

7. Using performance analysis tools for auto-tuning energy efficiency

In this section we present how performance measurement infrastructures can be used to tune for energy efficiency. The advantage of combining analysis

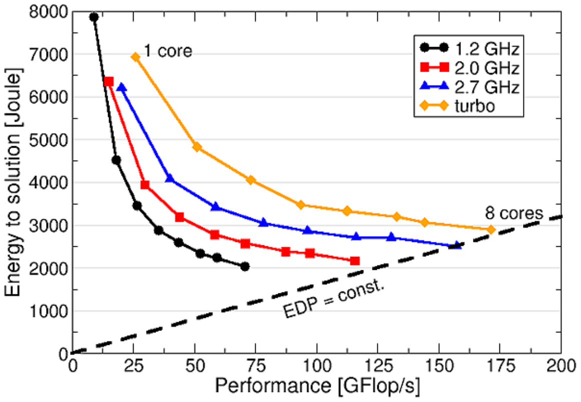


Fig. 6. Measured power and performance. The dashed line shows points of constant EDP fitted to the 2.7 GHz result with 8 cores, which represents the optimal operating point and is predicted by the model. (Colors are visible in the online version of the article; http://dx.doi.org/10.3233/SPR-140393.)

and optimization are the reuse of the instrumentation framework, and the traceability of the outcome of an optimization.

One example for such an integration is Score-P. It provides an Online Access mechanism which is enabled by an additional user instrumentation to the application that should be analyzed or optimized [30]. Periscope [17] and the Periscope Tuning Framework PTF [31] implement an online analysis for automatically tuning the energy consumption. The tool is currently developed in the AutoTune [31] project that aims for performance and energy optimizations. In their current approach Navarrete et al. [34] use an instrumented code to find an optimal processor frequency setting for the energy-to-solution of applications.

Schöne and Molka also increase the energy efficiency of applications using performance measurement tools. In [38] they use the VampirTrace framework and follow a 2-step approach. First, they instrument the application and measure hardware performance counters at a per region scale. Second, they use this information and the existing instrumentation to adjust hardware and software settings at runtime per region. With the inclusion of wattmeters in VampirTrace, Schöne and Molka validate their setup choices with another measurement run, as shown in Fig. 7. They propose multiple optimizations like frequency scaling, concurrency throttling and prefetcher settings.

8. Constant-power tuning considerations

The forgoing sections have demonstrated how algorithmic approaches to saving energy (and to a lesser extent, saving power) have developed into a mature field of study with significant impact on hardware design. However, as supercomputers continue to move to exascale, the primary constraint on performance becomes the bound on electrical power available to the system. Diverging from this bound, either above or below, will incur significant cost. The question turns from one of energy efficiency to one of optimizing performance under a power bound. Changing the focus from energy to performance has several profound effects on the design of extreme-scale systems.

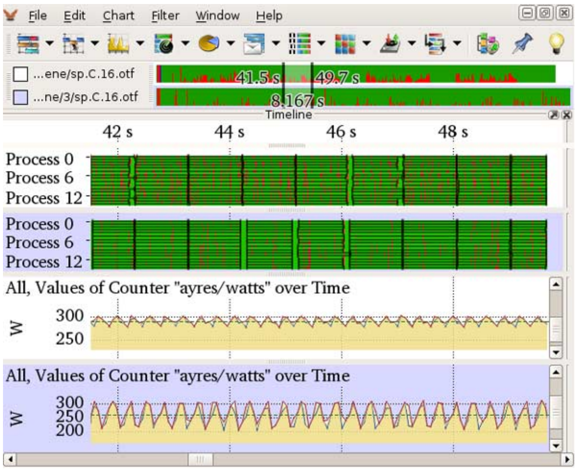


Fig. 7. Vampir Comparison View: Normal vs. energy efficient execution of the MPI parallel NPB benchmark SP on a dual-socket Sandy Bridge system. Energy efficiency is provided by the usage of DVFS via `libadapt` and VampirTrace. (Colors are visible in the online version of the article; http://dx.doi.org/10.3233/SPR-140393.)

Hardware overprovisioning. Given that utilization should be measured from the scarce resource, the utilization of existing machines is (correctly) measured in terms of node-hours. For these designs, machines were provisioned to have power sufficient to run all nodes at peak performance (*worst-case provisioning*). If this provisioning model was to carry over to extreme-scale designs, the node count would be limited by the assumption that nodes would always draw peak power. Such a system would never exceed its power limit, but as most scientific codes do not consistently require peak node power, a portion of the allocated power would be consistently unused. From a node-hours point of view the machine may be fully utilized, but measuring percent power consumption tells a different story. To guarantee full power utilization, designs should instead be *hardware-overprovisioned*. The system would have more nodes than can be run at full power until the power bound, and a combination of the job scheduler and runtime system will limit per-node power consumption so that the full allocation of power is used at all times. This may require that a subset of nodes be idled from time to time, but as power (not nodes) is the bottleneck resource, this outcome should maximize performance.

Scheduling. Job scheduling over time and node counts is already a known NP-hard problem [47]. Adding a user-requested power allocation adds another level of complexity. Users need to understand how power, node counts and performance interact with their code in order to request an appropriate amount of power for a given job. The scheduler must release the job when both a sufficient number of nodes and power is forecast to be available for the expected duration of the job. When a job completes, the scheduler will be required to decide whether the newly-freed nodes and power should be used to start another job in the queue, or whether some or all of the newly-freed nodes should be put into a low-power sleep state and the power distributed to already-running jobs. The scheduler may also be required to handle a fluctuating system-wide power bound, either due to dependence on variable sources of energy (such as wind or solar) or hour-to-hour fluctuations in the pricing of electricity.

Node configuration. With the introduction of Turbo frequencies on newer x86 processors, performance modeling became significantly more difficult. Existing models, such as those described earlier in this paper, rely on a simplification that performance (in the absence of other bottlenecks) increases linearly with core count if no bottleneck is present. Turbo mode turns this on its head: higher frequencies are available, but only if few cores are used. Memory bus bottlenecks are common for scientific codes, and adding either more cores or higher frequencies once the bus is saturated burns power without any increase in performance. Adding a power bound to this mix complicates performance modeling still further: should per-node power be reduced in order to bring up additional nodes, or should fewer, hotter nodes be scheduled? The decision whether to use multi-threading, GPU accelerators, or vector units takes this problem well beyond what existing models can handle.

Load imbalance. Despite years of research, real-world applications continue to suffer from load imbalance. Rebalancing power within a running job rather than rebalancing work distributions may be more efficient in terms of both performance and energy. Taken in combination, we expect data balancing only needs to get within 10% of the ideal for power balancing to approach optimal execution.

Getting to an exaflop within 20 MW is largely a hardware problem. Making the best use of such a system in a production environment however is a system software problem, and one that will need to be solved not only for exascale, but for all systems going forward into the future.

9. Conclusion and outlook

In this paper we have described some aspects of state-of-the-art energy efficiency tuning. We have presented common energy efficiency metrics and provided an overview of energy efficiency analysis tools. We have discussed what problems arise from including such information and how different tools make use of the metrics to provide users with hints how energy is wasted in parallel applications. The integration of energy and power metrics into performance measuring infrastructures however is only a first step to tuning. The next step will be the integration of tuning cycles and performance measurement. The reusage of sampling and instrumentation infrastructures provides a convenient front end for such an integration. We have discussed first attempts for such an integration in previous papers.

The Online Access feature of Score-P provides a promising interface for auto-tuning performance and energy. The future plans of the energy aware AutoTune plug-ins are related to the optimization of the search algorithm by reducing the search space, which should lead to a better performance. Currently, the search algorithm consists of an independent and exhaustive search which tests all available frequencies and governors. The next versions of the plugin will integrate a heuristic search to focus the search just on a minimized set of frequencies and governors. The heuristic will be based on a energy model which is ongoing development.

The measurement of power consumption however is still an open field for engineering and research. Most power measurement devices and infrastructures provide a limited temporal, spatial, or reading resolution. Also external influences like OS noise and temperature issues influence the quality and reproducibility of power measurements.

Another part of our future work is the development of performance counter based energy models. As was said before, measuring the power consumption of tasks at a fine granular level is currently hard to achieve. Thus, a model that does not rely on asynchronous data with low resolution is inevitable to understand the energy efficiency at fine grained region level. Creating such a model however provides certain pitfalls.

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