

Improved designs of tunable ferroelectric capacities for microwave applications

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(Received 10 September 2001; accepted for publication 14 January 2002)

Epitaxial SrTiO₃ films are deposited by on-axis magnetron sputtering on CeO₂-buffered *r*-cut sapphire. The ferroelectric films possess low losses (e.g., $\tan \delta \approx 0.001$ – 0.004 at 300 K) and a large tunability at small electric fields. Different complex designs for ferroelectric capacities are prepared via dry etching ranging from standard designs to those in which the ferroelectric material is restricted to the gap of the capacity. The resulting capacity data can be explained in terms of an analytic model for parallel capacities. Due to modifications and optimization of the design, the quality factors for an improved capacity design exceeds the requirement for most applications $K > 45$ already for extremely small voltages $U \approx 18$ V, which demonstrates the good properties of the design in combination with the quality of our ferroelectric films. © 2002 American Institute of Physics. [DOI: 10.1063/1.1459486]

The rapid development of microwave applications in, among others, communication technology has triggered a strong demand for frequency tunable resonators and filters operating in the GHz regime. Thin films of ferroelectrics such as BaTiO₃, SrTiO₃ (STO) and several others provide high dielectric constants ϵ and the possibility of tuning since their ϵ depends on the electric field strength, $\epsilon = \epsilon(E)$. For tunable electronic devices and circuits, such films are, therefore, used as dielectric material in capacitors (see Fig. 1). Especially, the combination with conductors of extremely low rf losses like high- T_C superconductors (HTS) seems to be promising. However, up to the present, the disadvantage of ferroelectric films is given by (i) the relatively high dielectric loss, for instance represented by typical values of the loss tangent of $\tan \delta > 0.01$ for STO films, (ii) the large voltages $U \geq 100$ V necessary for the frequency tuning, and (iii) the degradation of either the ferroelectric or HTS film in hybrid structures. This calls for a careful production control and an intelligent design of the capacitors. In this work, we demonstrate that low losses can be obtained in STO films, that small bias voltages of $U < 20$ V can lead to a considerable tuning of $n \approx 1.6$, and that degradation problems in the ceramic components might be avoided by a special design of the capacity.

250 to 500 nm thick STO films are grown on CeO₂-buffered *r*-cut sapphire (Al₂O₃). Sapphire possesses extremely low microwave losses ($\tan \delta \approx 10^{-7}$ – 10^{-8}), whereas the CeO₂-buffer layer (30 nm thickness) reduces the lattice mismatch between STO and substrate. Furthermore, this substrate system has proven to be ideal for the deposition of high-temperature superconducting films,¹ i.e., the combination of STO with YBa₂Cu₃O₇ for the tunable high- Q resonators is feasible for this system. The layers are deposited via on-axis magnetron rf sputtering technique. CeO₂ growths (200) oriented with a full width at half maximum of $\Delta\omega \approx 0.8^\circ$ – 1.3° . The structural orientation of STO depends strongly on gas pressure and substrate temperature during deposition. At low process pressure and temperature, STO

growths predominantly (110) oriented, whereas at higher temperature $T_H > 840^\circ\text{C}$ the (111)-oriented phase starts to take over. In contrast to STO films on LaAlO₃ or sapphire without buffer, (100)-oriented STO is not detected in our films.

The dielectric properties are determined by capacity measurements at 1 kHz and 1 MHz with a experimental resolution of 10^{-5} pF and 10^{-5} for the capacity and losses, respectively. Reference measurements are executed at 1–4 GHz and confirmed the data obtained at low frequencies. For the measurements of the tunability, additional voltage contacts are attached to the two-sided electrodes. The dielectric constant of ϵ_{STO} (300 K) ≈ 200 – 250 with a maximum of $\epsilon_{\text{STO,max}} \approx 300$ – 450 at 55–65 K of our STO films are comparable to literature data.^{2–4} The dielectric loss of the STO layer are very low, i.e., $\tan \delta_{\text{STO}}$ (300 K) ≈ 0.002 – 0.004 with a maximum of $\tan \delta_{\text{STO}} \approx 0.005$ – 0.01 at 35–55 K. The losses are very small compared to typical literature data for STO films on sapphire⁵ and comparable to the best values obtained via postannealing treatment of STO on LaAlO₃.⁴

The aim of this work was to develop and examine different capacity designs in order to improve the tunability of the capacities especially at low electric voltages. In standard designs (see Fig. 1) coplanar electrodes are either positioned on top of the ferroelectric layer or the electrodes are covered by the ferroelectric layer. In both cases, the electromagnetic rf field is not restricted to the gap between the electrodes. As a consequence, small tuning rates are obtained that lead to unpractical tuning voltages up to 100 V, and unnecessary rf losses occur in the covered ferroelectric material.

In our improved capacity designs (Fig. 1), the ferroelectric material is restricted to the capacity gap. Therefore, the rf field is also concentrated between the electrodes. The rf field in the substrate ($\epsilon \approx 10$ and $\tan \delta < 10^{-7}$) can be neglected. Two different designs are tested and compared to the standard design (Fig. 1). In both cases, 500 nm thick STO layers are patterned via optical lithography and IBE in order to obtain a ferroelectric filling that is restricted to the capacity gap (width of the STO striplines ranging between 2 and 10 μm). Special care is taken to obtain steep edges by etching

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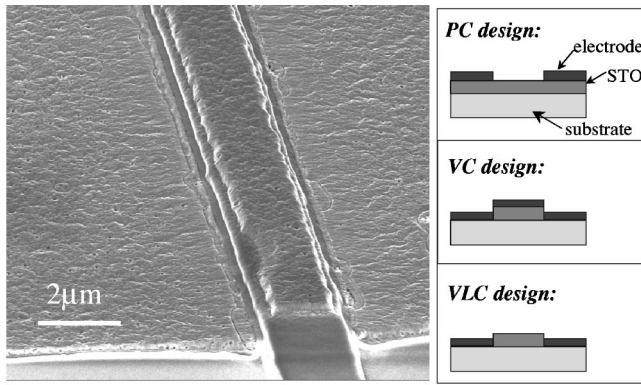


FIG. 1. Scanning electron microscopy images of a “vertical capacity.” The schematic drawings represent the different arrangements of the capacities.

under an angle of 45° along the edge of the STO stripline. The resulting steepness is about 85° . Subsequently, a metallic layer is deposited onto the STO stripline. The metallic layer automatically forms the two electrodes plus a top electrode on top of the STO stripline. In order to remove possible Galvanic contacts between the top electrode and capacity electrode, the capacity is etched (IBE: voltage of 88 V) under a shallow angle of 88° . The resulting conductivity between the electrodes of the capacity was smaller than $2 \times 10^{-8} \Omega^{-1}$. Finally, the additional electrode on top of the STO layer is either removed by lift-off technology [vertical lift-off capacity (VLC) design] or kept [vertical capacity (VC) design] (see Fig. 1). In the latter case, the top electrode creates additional capacities (see discussion below) and can be used as a voltage contact for the electronic tuning of the capacity. Figure 1 shows typical scanning electron microscopy images of a vertical capacity. For convenience, the different capacity designs are named planar capacity (PC), VC and VLC, respectively.

Figures 2(a) and 2(b) represent a comparison of the dielectric properties of the different designs for a gap size of the capacities is $2 \mu\text{m}$. Over the whole temperature regime, the VC design shows better dielectric properties compared to the standard design, i.e., larger capacity and lower effective losses are measured for the VC capacity. In the temperature regime of 50–77 K, which is of interest for application of STO in tunable high- T_C filters, the capacity is improved by about 18% whereas the losses are significantly reduced by about 35% compared to the planar design.

Figure 2(c) represents a comparison of the voltage dependence of the capacity for the different designs. It displays the tunability $n = C(0 \text{ V})/C(U_{dc})$ for the different types and gap sizes of the capacities. Whereas the vertical capacities show a linear voltage dependence at low voltages, PC and VLC capacities show a nonlinear behavior at low voltages ($U_{dc} < 10 \text{ V}$) and a linear behavior at high voltages. The curvature observed for some of the VC capacities at higher voltages indicates a saturation effect, which arises due to small leaking currents, that reduce the electric field at the capacity gap at high voltages. The largest tuning rates are obviously obtained for the smallest gap size, i.e., $2 \mu\text{m}$, since the resulting electric field of the tuning voltage is largest for the smallest gap. However, the difference is smallest for the vertical design. Furthermore, large tuning rates are obtained for extremely small voltages for the vertical design, e.g.,

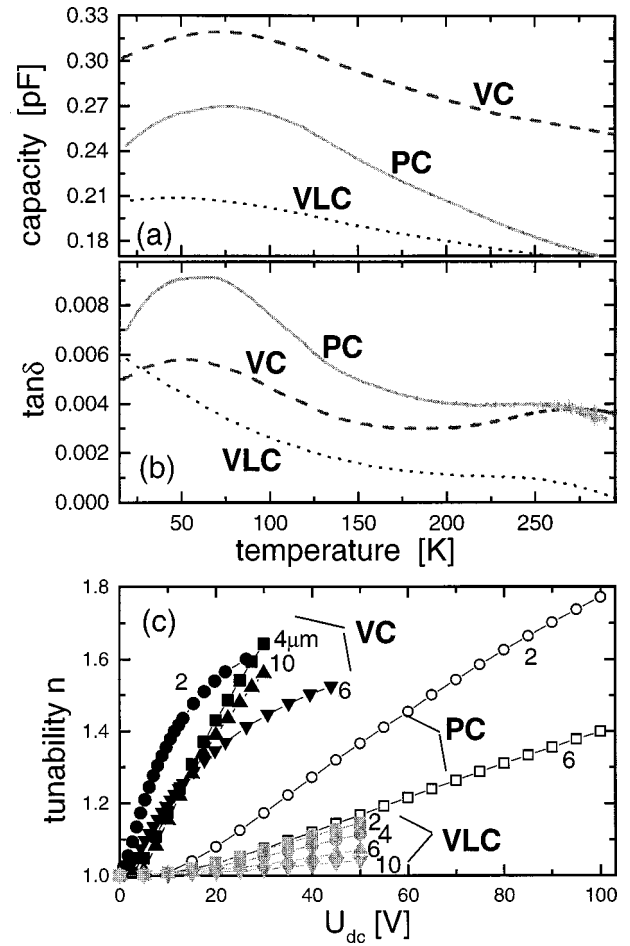


FIG. 2. Temperature dependence of the capacity (a) and effective loss (b) for all three capacitor geometries. The capacity change reflects the change in ϵ , the gap size is $s = 2 \mu\text{m}$, and no bias voltage is applied ($U_{dc} = 0 \text{ V}$). (c) Dependence of the tunability n on the applied bias voltage (U_{dc}). (The definition of n follows that in Ref. 5). The gap sizes are indicated, the measurements are carried out at 70 K.

$n(10 \text{ V}) = 1.36$ and $n(20 \text{ V}) = 1.55$ for the VC with $2 \mu\text{m}$ gap size. The vertical capacities with removed top electrode (VLC) show a similar behavior as observed for the planar design. However, the tunability is slightly smaller. The reduction of the tunability probably has to be ascribed to the additional preparation procedure during remove of the top electrode.

In order to understand the dielectric properties of the different designs, we analyze the data in terms of a model for parallel capacities,⁶ i.e.,

$$C_{\text{total}} = C_{\text{STO}} + C_{\text{sapphire}} + C_{\text{air}}, \quad (1)$$

neglecting the contribution of the thin CeO_2 -buffer layer. The different contributions are

$$C_{\text{sapphire}} = \epsilon_0 \times \epsilon_{\text{sapphire}} \times \frac{1}{\pi} \times \ln \frac{16 \times h_{\text{sapphire}}}{\pi \times s} \times d, \quad (2)$$

$$C_{\text{air}} = \epsilon_0 \times \epsilon_{\text{air}} \times \frac{2}{\pi} \times \ln \frac{4 \times l}{s} \times d, \quad (3)$$

$$C_{\text{STO,PC}} = \epsilon_0 \epsilon_{\text{STO}} \times \frac{\pi}{4 \times [\ln 2 + (\pi s / 4 h_{\text{STO}})]} \times d. \quad (4)$$

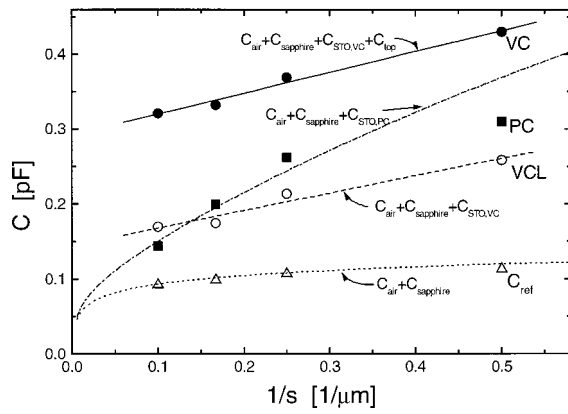


FIG. 3. Experimental data (data points) and theoretical predictions (lines) of the capacity as function of inverted gap size s for PC, VC, and VLC at 70 K. For the predictions in terms of a parallel capacities model according to Eqs. (1)–(4) and parallel plate model Eq. (5) dielectric constants of $\epsilon_{\text{air}}=1$, $\epsilon_{\text{sapphire}}=9.6$, and $\epsilon_{\text{STO}}=300$ are used. The additional contribution of the top electrode is given by $C_{\text{top}} \approx 0.15$ pF.

In the case of the VC and VLC, the contribution of the STO is described in terms of a parallel plate capacity:

$$C_{\text{STO,VC}} = \epsilon_0 \times \epsilon_{\text{STO}} \times \frac{h_{\text{electrode}} \times d}{s}. \quad (5)$$

C_i characterizes the capacity, ϵ_i is the dielectric constant and h_i is the thickness of the different components, s represents the width of the capacity gap, and d is the width of the electrodes. The model has been checked via simulation using the software SONNET and test measurements on planar capacities on CeO_2 -buffered Al_2O_3 .

Figure 3 shows a comparison of the experimental and theoretical capacities of PC, VC, and VLC with different gap sizes from 2 to 10 μm . The theoretical predictions are derived from Eqs. (1)–(5) using literature and experimental values, respectively, for the dielectric constants of $\epsilon_{\text{air}}=1$, $\epsilon_{\text{sapphire}}=9.6$, and $\epsilon_{\text{STO}}=300$. The top electrode leads to an additional contribution C_{top} to the total capacity of the VC design. This contribution arises from the two capacities between each side and top electrode. The experimental data yield a value of $C_{\text{top}} \approx 0.15$ pF that is in agreement with estimations obtained for a parallel plate model with the experimental geometry and Eq. (5). The theoretical predictions show an excellent agreement with the experimental data, which indicated, (i) that dielectric constant, which is the experimentally determined prior to the preparation of the devices, is not degraded during the different steps of the preparation, and (ii) that complex arrangements of electrodes with ferroelectric filling can be described and predicted by the analytic model of parallel capacities.

Finally, the quality of the tunable capacities has been checked. For this purpose, a standard quality criterion that considers tunability, loss and applied voltage can be defined:⁵

$$K(U) = \sqrt{\frac{(n-1)^2}{n \times \tan \delta(0 \text{ V}) \times \tan \delta(U_{\text{dc}})}}, \quad (6)$$

that provides a figure of merit. Simple considerations demonstrate, that values $K(U_{\text{max}}) > 45$ are required for most microwave applications of tunable capacities.⁵ In Fig. 4, the

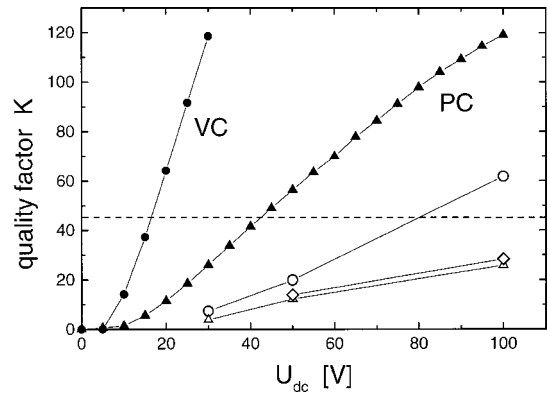


FIG. 4. Quality factor as function of applied voltage of our PC and VC on sapphire (solid symbols) and literature data for standard capacities (PC) on sapphire and STO substrates (Refs. 5 and 7). Values $K(U_{\text{max}}) > 45$ (dashed line) are required for most microwave application.

quality factor is shown as function of the applied bias voltage for our VC and PC type capacities. For comparison, K values of representative planar STO capacitors obtained from literature^{5,7} are added. The plot demonstrates, that (i) our STO films on CeO_2 -buffered sapphire possess a good quality (i.e., $K > 45$ is obtained for both designs at relatively low voltages) and (ii) that the design shows extremely high quality at very low voltages (i.e., $K > 45$ for $U_{\text{dc}} > 18$ V).

In conclusion, STO films were produced by on-axis magnetron sputtering on CeO_2 -buffered sapphire. The STO films show very low losses (e.g., $\tan \delta_{\text{STO}} \approx 0.001$ – 0.004 at 300 K) and a large tunability at low electric fields. Different designs of ferroelectric capacities have been tested ranging from standard designs to vertical designs. The experimental data can consistently be explained for all designs using an analytic model for parallel capacities. Sufficiently large quality factors $K > 45$ are obtained already for voltages $U \approx 18$ V for the vertical capacity, which demonstrates the good properties of the design in combination with the quality of our STO films. Finally, due to the fact, that the ferroelectric material is restricted to the gap of the capacity, the vertical design might be more suitable for the combination of STO with HTS material since due to the separation of both materials the degradation problem should be avoided.

Valuable support from S. Bunte, P. Dymachevski, W. Hofer, E. Hollmann, N. Klein, A. Kozyrev, U. Krüger, R. Kutzner, P. Lahl, I. Vendik, and O. Vendik is greatly acknowledged.

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