Si/SiGe n-MODFETs on Thin SiGe Virtual Substrates Prepared by Means of He Implantation

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***Abstract*—Si/SiGe n-type modulation-doped field-effect transistors grown on a very thin strain-relieved $Si_{0.69}Ge_{0.31}$ buffer on top of a Si(100) substrate were fabricated and characterized. This novel type of virtual substrate has been created by means of a high dose He ion implantation localized beneath a 95-nm-thick pseudomorphic SiGe layer on Si followed by a strain relaxing annealing step at 850 °C. The layers were grown by molecular beam epitaxy. Electron mobilities of 1415 cm^2/Vs and 5270 cm^2/Vs were measured at room temperature and 77 K, respectively, at a sheet carrier density of about $3 \times 10^{12}/cm^2$. The fabricated transistors with Pt-Schottky gates showed good dc characteristics with a drain current of 330 mA/mm and a transconductance of 200 mS/mm. Cutoff frequencies of $f_t = 49$ GHz and $f_{max} = 95$ GHz at 100 nm gate length were obtained which are quite close to the figures of merit of a control sample grown on a conventional, thick $Si_{0.7}Ge_{0.3}$ buffer.**

***Index Terms*—He implantation, n-MODFET, SiGe heterostructure, SiGe virtual substrate, strained Si.**

I. Introduction

In THE Si microelectronics, Si-Ge-based strained layer heterostructures are presently of enormous interest for the fabrication of high-performance devices due to their improved carrier transport properties and the possibility of band gap engineering [1]. The exceptional potential of this material system has already been demonstrated by publications e.g., on Si/SiGe based hetero-FETs (HFETs) with promising cutoff frequencies [2]–[6] and low noise figures [7], [8]. A key element for these heterodevices is a substrate with a lattice parameter tunable in between that of Si and Ge. Such a virtual substrate (VS) can be created by a strain-relieved SiGe alloy layer on Si standard wafer whereby the alloy composition and the degree of relaxation determine the in-plane lattice parameter of the VS. To date, the most successful approach to achieve a high quality VS is the growth of a compositionally graded SiGe buffer layer on a Si(100) substrate [9], [10], with the rule that the shallower the ramp the better is the structural quality. However, the relatively large thickness of this buffer version involves some decisive disadvantages. Thick SiGe buffers reduce the wafer throughput, cause nonacceptable surface topology if implemented in combined technologies like CMOS, suffer from the lower thermal conductivity of SiGe alloys compared to Si, and may degrade the RF performance by a parasitic conductivity.

Recently, a highly interesting technique has been reported as effective in achieving a very thin strain relaxed SiGe buffer with a low threading dislocation density [11]–[13]. The basic feature of this method is to create a narrow defect band by a high dose He^+ implantation slightly underneath the interface of a pseudomorphic SiGe alloy layer grown on a Si(100) substrate. By proper choice of energy and dose, a high density of platelet-like or sphere-like bubbles filled with over-pressurized He develop during a subsequent annealing step. It is assumed that these stressed cavities release dislocation loops which then form strain-relieving misfit branches at the Si/SiGe interface while the threading arms are annihilated quite effectively. Up to now, SiGe buffers with 30% Ge content and about 70% relaxation have been realized with an excellent surface quality and a threading defect density of approximately $10^7/cm^2$.

In this letter, we report on the preparation and device results of an n-MODFET structure grown on this novel VS type. Both the SiGe buffer layer on Si(100) substrate and the Si/SiGe n-MODFET layer stack were deposited by MBE. Mesa-type HFETs were prepared with Pt-Schottky gates. From the fabricated devices dc characteristics were recorded, and finally RF measurements were performed.

II. Wafer and Device Preparation

A metastable, strained layer $Si_{0.69}Ge_{0.31}$ alloy film with a thickness of 95 nm was grown on a 1000 Ωcm 4-in p-Si(100) standard wafer. A 4-nm Si cap layer guards the SiGe and is also used as a sacrificial layer for subsequent wet-chemical cleaning steps. Then a He^+ implantation followed with an energy of 18 keV and a dose of $2 \times 10^{16}/cm^2$. Due to the implantation, a defect band about 100 nm beneath the SiGe/Si interface was produced while the $Si_{0.69}Ge_{0.31}$ layer remained still fully pseudomorphic. A post-implantation anneal of the sample was then carried out in a rapid thermal annealing furnace at 850 °C for 600 s resulting in a relaxation of the SiGe layer of about 65%.

Finally, the VS was reinserted into the MBE for deposition of a standard Si/SiGe n-MODFET structure. In this first attempt, a 100-nm $Si_{0.7}Ge_{0.3}$ alloy starting layer was grown to separate the active device structure from the interface of the growth break. Then the transistor layer stack followed consisting of a 12-nm-thick strained Si film sandwiched between

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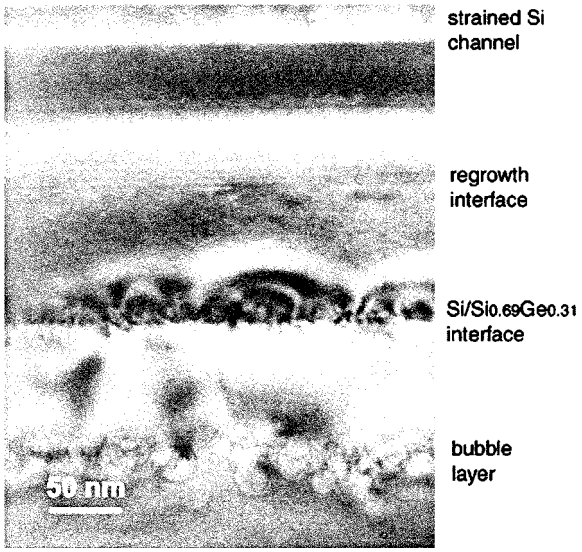

Fig. 1. Cross section TEM picture of the complete layer set-up on the Si substrate after pseudomorphic SiGe growth, He^+ implantation, anneal, and regrowth. Important details are marked.

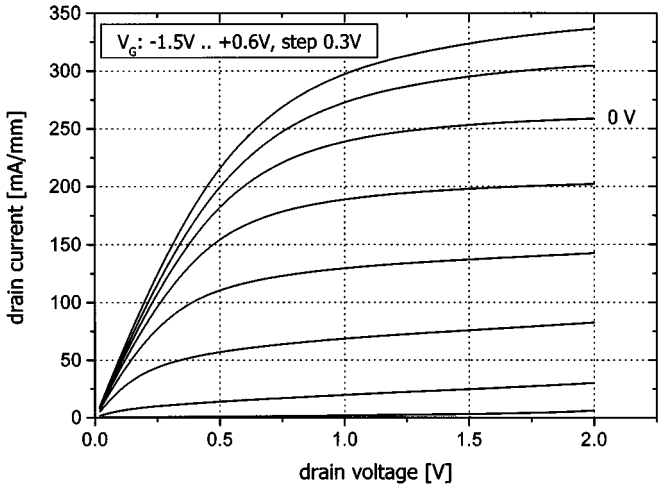

Fig. 2. Typical dc output characteristic of an n-MODFET on thin $Si_{0.7}Ge_{0.3}$ virtual substrate demonstrating a high saturation current and good pinch-off behavior.

5-nm-thick Sb-doped supply layers (backside $1–2 \times 10^{18}/cm^3$, front-side $1–2 \times 10^{19}/cm^3$) which are set-back from the Si quantum channel by a 3 nm backside and a 4-nm front-side spacer. An 8-nm undoped $Si_{0.7}Ge_{0.3}$ and a 4-nm undoped Si cap layer complete the epitaxy structure. After the second epitaxy process, it has been found that the additional 100 nm SiGe alloy and the temperature cycle of the regrowth process enhanced the degree of relaxation of the VS up to 70–75% resulting in a conduction band discontinuity between the strained Si channel and the adjacent $Si_{0.7}Ge_{0.3}$ of about 120 meV [14]. The transistor stack and the relaxed SiGe are free of structural defects as confirmed by the cross-section transmission electron micrograph in Fig. 1. Smooth interfaces define the strained Si channel and there are no faults at the regrowth interface. The bubble layer formed due to the He^+ implantation is located about 80 nm below the Si/relaxed $Si_{0.69}Ge_{0.31}$ buffer interface which is identified by the strain contrast of the misfit dislocations. Small composition fluctuations are responsible for the faint contrast variations in the upper SiGe buffer part.

To have a reference to this novel concept, a control sample with the same transistor layer set-up but grown on a 2.6-μm-thick, compositionally graded $Si_{0.7}Ge_{0.3}$ buffer was prepared and processed. For the device fabrication, common technological processes and tools were applied, with the only constraint that, as usual for SiGe MODFETs, the maximum temperature was kept below 600 °C to avoid thermally induced disturbance of the doping profile. Mesa structures were defined by dry etching using a CF_4 plasma. After deposition of a 200 nm field oxide by low pressure CVD at 350 °C for passivation and planarization, the active transistor area on the mesa was opened by wet chemical etching with HF. Source and drain contacts were formed by a shallow P implantation with an energy of 20 keV and a dose of $2 \times 10^{15}/cm^2$ followed by a rapid thermal annealing at 575 °C for recrystallization and dopant activation. The Ti/Pt/Au contact metallization was structured by lift-off. Mushroom-like Schottky gates consisting of 30 nm Pt reinforced by 300 nm Au were patterned by means of e-beam lithography. The minimum source-drain distance was 1 μm and gate lengths around 100 nm were achieved.

III. Device Results

After wafer processing van der Pauw measurements were carried out. At room temperature, an electron mobility of $\mu = 1415$ cm^2/Vs at a sheet carrier density of $n_s = 3.2 \times 10^{12}/cm^2$ was obtained. The corresponding 77 K numbers are $\mu = 5270$ cm^2/Vs and $n_s = 3 \times 10^{12}/cm^2$ indicating that the majority of electrons are in the Si quantum channel. The dc properties of the fabricated transistors were measured on-wafer at 300 K by recording Schottky diode, output, and transfer characteristics. Fig. 2 shows the output characteristics of a transistor with 100 nm gate length and 2×25 μm gate width. The curves indicate a good pinch-off behavior and a high maximum drain current of 330 mA/mm at a gate voltage of 0.6 V. The transfer characteristics (not shown) reveal a fairly broad transconductance plateau in the gate voltage range from -0.2 V to -0.9 V, with a maximum of 200 mS/mm at about -0.6 V. Typical gate current values are in the range of 10-μA/mm at -0.5 V. S parameters have been recorded at RT with a HP 8510B network analyzer in the frequency range from 200 MHz to 50 GHz. The transistor S parameters were corrected for the parasitic pad contributions by means of short and open structures which results in approximately 15% higher values compared to the raw data. The de-embedded spectra for the current gain $|h_{21}|^2$, the maximum stable gain (MSG) (range $k \leq 1$), the maximum available gain (MAG) (range $k > 1$), and the stability factor k are plotted in Fig. 3. The extrapolation of the current gain and the MAG by 20 db/decade lines leads to cutoff frequencies values of $f_t = 49$ GHz and $f_{\max} = 95$ GHz, respectively. The control sample with the 2.6-μm-thick, compositionally graded $Si_{0.7}Ge_{0.3}$ VS shows with $f_t = 54$ GHz and $f_{\max} = 100$ GHz about the same RF performance.

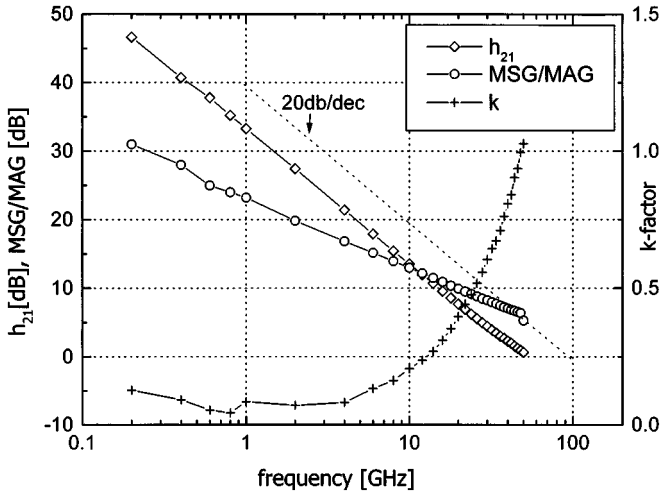

Fig. 3. RF characteristic of an n-MODFET showing the current gain $|h_{21}|^2$, the maximum stable gain (MSG), maximum available gain (MAG), and the stability factor k. Cutoff frequencies of $f_t = 49$ GHz and $f_{\max} = 95$ GHz can be deduced.

IV. Conclusion

We reported for the first time on structure and device results of Si/SiGe n-type MODFETs grown by MBE on very thin SiGe VS created by means of high dose He^+ implantation. The required relaxation of the SiGe buffer was effectuated by a He implantation at an energy of 18 keV and a dose of $2 \times 10^{16}/\text{cm}^2$ followed by an 850 °C annealing step for 10 min. The fabricated transistors exhibited an $f_t = 49$ GHz and an $f_{\max} = 95$ GHz. This is an excellent RF performance which demonstrates impressively the potential of this thin SiGe virtual substrate. In particular, the significance of this approach is made clear by the fact that the figures of merit are about equal to that of a reference sample grown on a thick, "state-of-the-art" $Si_{0.7}Ge_{0.3}$ VS. This novel kind of VS is a highly interesting tool for both n-and p-type strained layer FET structures in Si-based microelectronics which are presently gaining enormous attention. The small thickness makes it compatible with CMOS technologies and minimizes the influence of low thermal conductivity of SiGe alloys.

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