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Strained Si and SiGe Nanowire Tunnel FETs for Logic and Analog Applications

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ABSTRACT Guided by the Wentzel–Kramers–Brillouin approximation for band-to-band tunneling (BTBT), various performance boosters for Si TFETs are presented and experimentally verified. Along this line, improvements achieved by the implementation of uniaxial strain in nanowires (NW), the benefits of high-k/metal gates, and newly engineered tunneling junctions as well as the effect of scaling the NW to diameters of 10 nm are demonstrated. Specifically, self-aligned ion implantation into the source/drain silicide and dopant segregation has been exploited to achieve steep tunneling junctions with less defects. The obtained devices deliver high on-currents, e.g., gate-all-around (GAA) NW p-TFETs with 10 nm diameter show $I_D = 64\ \mu A/\mu m$ at $V_{DS} = V_{GS} - V_{off} = -1.0$ V, and good inverse subthreshold slopes (SS). Tri-gate TFETs reach minimum SS of 30 mV/dec. Dopant segregation helps to minimize the defect density in the junction and thus trap assisted tunneling (TAT) is reduced. Pulsed current-voltage (I-V) measurements have been used to investigate TAT. We could show that scaled NW devices with multigates are less vulnerable to TAT compared to planar devices due to a shorter tunneling path enabled by the inherently good electrostatics. Furthermore, SiGe NW homo- and heterojunction TFETs have been investigated. The advantages of a SiGe/Si heterostructure as compared to a homojunction device are revealed and the effect of line tunneling which results in an increased BTBT generation is demonstrated. It is also shown that complementary strained Si TFET inverters and p-TFET NAND gates can be operated at V_{DD} as low as 0.2 V. This suggests a great potential of TFETs for ultralow power applications. The analysis of GAA NW TFETs for analog applications provided a high transconductance efficiency and large intrinsic gain, even higher than for state-of-the-art 20 nm FinFETs at low voltages.

INDEX TERMS Strained Si nanowire, SiGe, tunnel-FET, subthreshold slope (SS), inverter, NAND, analog.

I. INTRODUCTION

Band-to-band tunneling (BTBT) probability and currents in a TFET device depend on both the materials and the device structures as predicted by the Wentzel-Kramers-Brillouin (WKB) approximation [1]:

$$I \propto T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}E_g^{3/2}}{3q\hbar\left(\Delta\Phi+E_g\right)}\right) \quad (1)$$

where the effective mass, m^*, and the energy bandgap, E_g, are the main semiconductor material parameters. λ is the screening length of the electrical potential, consisting of two contributions: $\lambda = \lambda_{dop} + \lambda_{ch}$ [2]. λ_{dop} reflects the steepness of the doping profile of the tunneling junction and λ_{ch} the device architecture. Both, λ_{ch} and λ_{dop} should be minimized by good electrostatic control and steep doping profiles to achieve high tunneling currents. $\Delta\Phi$ denotes the energy

overlap of valence and conduction bands, q the elementary charge and $\hbar$ the reduced Planck's constant.

For achieving high tunneling currents, semiconductors with lower bandgap E_g are required [3], [4]. III-V materials with low and direct bandgap offer distinct advantages in achieving high tunneling currents [5], [6]. However, the incompatibility with Si processing and the poor high-k interface are still the main limitations for III-V TFETs. Typically a high density of interface states (D_{it}) and defects in the high-k layers lead to strong trap assisted tunneling (TAT) resulting in a high inverse subthreshold slope (SS). In addition, most of the reported III-V TFETs are n-type, while p-type devices for complementary logic application are missing. The most recently developed low band gap GeSn alloys on Si(100) with direct band gaps may exhibit also great potential [7]–[9].

The advantages of Si TFETs encompass easy processing, better high-k interfaces and highly doped source/drain for both, n- and p-type, as required for complementary TFETs. However, the large indirect band gap E_g of Si limits the tunneling current. The implementation of strain reduces the bandgap while processing remains fully Si compatible. It has been shown that tensile strained Si (sSi) significantly improves tunneling currents [10], [11]. This advancement stems also from the effect, that uniaxial strain in Si nanowires along the <110> direction lifts the sub-band degeneracy of the valence and conduction bands, leading to a carrier repopulation in the subbands and hence to a reduction of the effective mass m^* of electrons and holes [12].

Furthermore, SiGe is an attractive material for TFETs due to its lower E_g and Si compatible process [13]–[16]. Moreover, the compressively strained SiGe pseudomorphically grown on Si substrates further reduces E_g, and hence increases BTBT currents [17], [18]. Increasing the Ge content to >80% in the SiGe layer could result in the direct tunneling, enhancing the BTBT currents [19].

In order to optimize the design of TFETs considering Eq.(1) is most instructive. Obviously, the tunneling current can be enhanced by optimizing the device geometry by using scaled nanowire (NW) structures with multi-gates, since they provide optimized electrostatics with a low λ_{ch} [20]–[22]. High-k gate oxides are also beneficial to achieve a small λ_{ch}. Another critical technology step is the formation of optimized tunneling junctions to achieve steep dopant profiles and thus a small λ_{dop}. Conventional tunneling junctions in Si-TFETs are normally realized by ion implantation and rapid thermal annealing. However, pronounced diffusion of dopants during annealing broadens the junctions and yields to small tunneling currents, as typical for $p^+ - i$ junctions formed by B^+ ion implantation. Hence, better SS characteristics are obtained for p-TFETs, since the As^+ implanted $n^+ - i$ junctions are much steeper than the B doped junctions due to less diffusion of As [21]–[23].

In this paper we provide an overview of the recent progress of Si and SiGe TFETs. First, improvements due to strain, high-k/metal gates, dopant segregated tunneling junctions and NW scaling are discussed. We demonstrate a novel and simple method to fabricate tunneling junctions by dopant segregation (DS) in sSi nanowire TFETs. By exploitation of this technique we have fabricated complementary TFETs (C-TFETs) with much higher on-currents and better SS than by the use of directly implanted tunneling junctions. This concept also prepared the experimental demonstration of C-TFET inverters and first TFET NAND logic circuits.

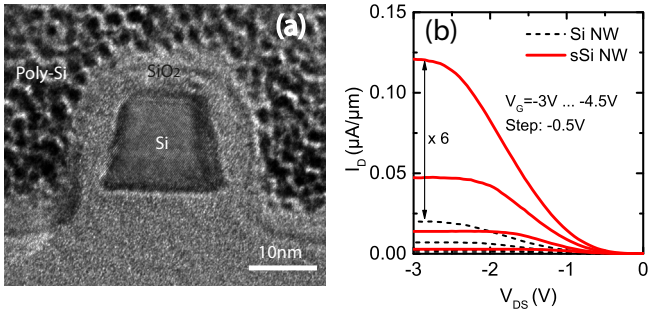

FIGURE 1. (a) Cross section TEM (XTEM) image of Si NW TFET structure, showing a Si NW with a cross section of 20 × 20 nm^2 and a SiO_2/poly-Si gate stack. (b) Comparison of output characteristics of p-channel TFETs with strained and unstrained Si NWs, showing large improvement of currents by the strain.

II. Si AND STRAINED Si NW TFETs

Slightly p-doped (1×10^{15} cm^{-3}) silicon on insulator (SOI) and strained silicon on insulator (sSOI) substrates with a biaxial tensile strain of $\varepsilon = 0.8$ % were used as the starting materials for the NW TFETs. In the first process step an array of 100-1000 parallel nanowires was patterned by e-beam lithography and reactive ion etching. In case of the sSOI substrate the strain across the patterned wires is relaxed, while the strain along the wires is maintained. Therefore, the nanowires are uniaxially strained along the wire direction, which was demonstrated theoretically by 2D finite element simulations [24] and experimentally by Raman measurements performed on similar processed nanowires [25]. It was also shown that uniaxial strain along ion implanted nanowires recovers after spike annealing of the partially amorphized sSOI [25].

A. ENHANCED TUNNELING CURRENTS DUE TO UNIAXIAL STRAIN

In this section we show the impact of the uniaxial strain on BTBT currents. For comparison, both Si and sSi NW array TFETs were fabricated with a nanowire cross section of 20×20 nm^2 and a gate length of 450 nm. The gate stack consists of 4.2 nm thermally grown SiO_2 and 200 nm n^+-doped poly-Si, as shown in the cross sectional TEM image of Fig. 1(a). In this case the source/drain (S/D) junctions were formed by direct As^+ and B^+ implantations into the Si/sSi and spike annealing at 1000°C.

Fig. 1(b) shows a comparison of p-channel output characteristics of strained and unstrained Si nanowire TFETs with

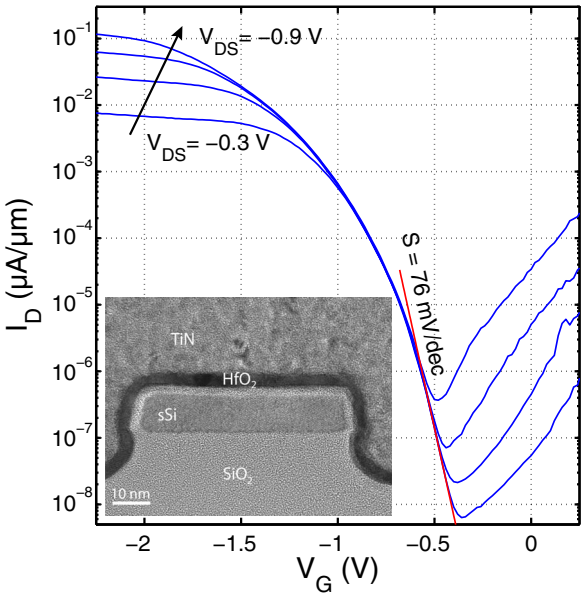

FIGURE 2. **Transfer characteristic of a nanowire array TFET with a HfO_2/TiN gate stack for different V_{DS}. The minimum slope is 76 mV/dec and the average slope over four orders of magnitude amounts 97 mV/dec at $V_{DS} = -0.3$ V. The inset shows a cross sectional TEM image of a single nanowire (10 × 50 nm^2) underneath the gate. The wire is covered with 3.5 nm HfO_2 as gate dielectric on top of an SiO_x interlayer of about 2 nm. The TiN gate covers the nanowire in an Ω-shape.**

SiO_2 and poly-Si gate. The 6-fold increase in tunnelling current for the sSOI devices can be attributed to the reduction of E_g and m^* in the strained Si since the tunneling current exponentially increases with decreased E_g and m^*, as predicted by Eq.(1). The inverse subthreshold slope *SS* in the p-channel transfer characteristics is also improved (not shown). However, due to the non-optimized tunneling junctions with strong trap assisted tunneling (TAT), *SS* is still poor, above 400 mV/dec [10]. In the following we will focus mainly on the strained Si NW TFETs due to the inherent advantage of sSi.

B. HIGH–K GATE DIELECTRICS AND JUNCTION ENGINEERING

The performance can be further improved by combining strained silicon nanowires with a high-k/metal gate stack. In the following example the gate stack consists of 3.5 nm HfO_2 deposited by ALD and 60 nm TiN deposited by atomic vapor deposition (AVD). The tunneling junctions were formed by direct implantations with BF_2^+ and As^+ ions into the strained Si and a 1000 °C spike annealing. After structure passivation with an SiO_2 layer metallization of source, drain and gate was performed. Finally, the devices with high-k/metal gate stack were annealed in forming gas at 450 °C for 10 minutes. A TEM image shows the device structure in the inset of Fig. 2 for a single sSi NW with a cross section of 10 × 50 nm^2.

The corresponding transfer characteristics of a p-channel nanowire array TFET with HfO_2/TiN gate with 100 nm gate length are shown in Fig. 2. The device exhibits a minimum *SS* of 76 mV/dec and an average slope of 97 mV/dec over four orders of magnitude of I_D at $V_{DS} = -0.3$ V. The I_{on}/I_{off} ratio reaches 10^6 at $V_{DS} = -0.3$ V, where I_{off} is defined as the minimum off-current in the curves. Due to the high-k dielectric and hence improved electrostatics these slopes are much better, and the on-current is about 20x higher than for the nanowire TFETs with SiO_2 oxide and poly-Si gate, shown in Fig. 1(b). However, *SS* is still above 60 mV/dec in these devices, which is mainly caused by the non-optimized tunneling junction. The symmetric design of the device results in a strong ambipolar behavior of the transfer characteristics. The increase of I_D with increasing V_{DS} at $V_G = 0$ V can be explained by BTBT at the drain-channel junction.

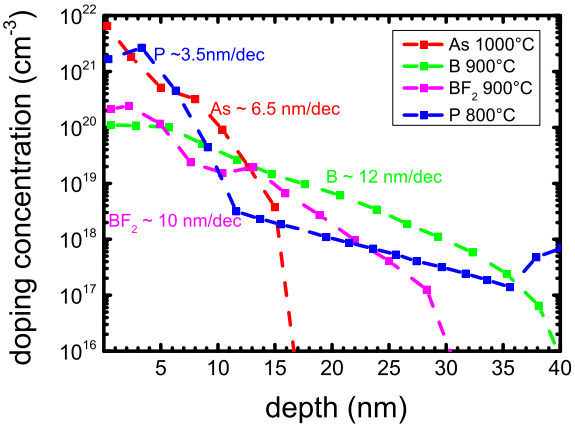

FIGURE 3. **ECV profiles of junctions formed by ion implantation and spike annealing. The slopes of these dopant profiles are not favorable for TFETs.**

Tunneling junctions formed by direct ion implantation into Si/sSi and spike annealing are not sufficiently steep due to extended dopant diffusion and possess remaining implantation defects. Fig. 3 shows electrochemical C-V (ECV) profiles of junctions formed by As^+, P^+, B^+ and BF_2^+ ion implantations with a constant dose of 1×10^{15} cm^{-2} after spike annealing at different temperatures. The results of Fig. 3 indicate that it is difficult to achieve junctions with dopant gradients below 5 nm/dec at temperatures above 900° C. Spike annealing of phosphorous implanted junctions at 800° C provides steep profiles, reaching 3.5 nm/dec, however, the thermal budget is not sufficient to heal the defects which may cause severe TAT. Moreover, dopant diffusion in Si nanowires is even faster compared to diffusion in bulk Si [26]. In our work, n-channel TFETs showed poorer performance, larger *SS* and smaller on-currents than p-TFETs due to the broader tunneling junction caused by stronger diffusion of boron. Nonconventional annealing techniques, like laser annealing, can improve the tunneling junction and thus the device performance [27].

C. DOPANT SEGREGATION BOOSTS TUNNELING CURRENTS

Remarkable progress was achieved by adapting a dopant segregation (DS) process to produce highly doped steep

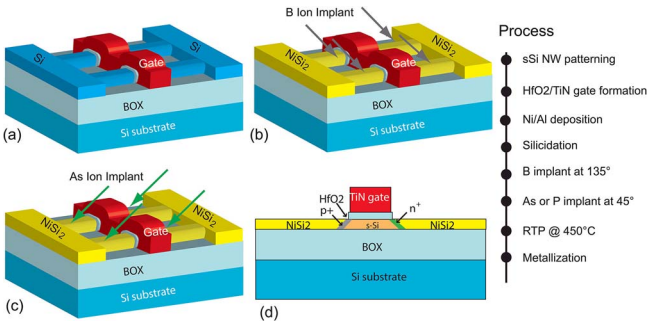

FIGURE 4. **(a)–(c) TFET fabrication process using tilted B^+ and As^+ ion implants into epitaxial $NiSi_2$ S/D contacts. (d) Highly doped n+ and p+ pockets at the silicide edges are formed after a low temperature anneal due to DS.**

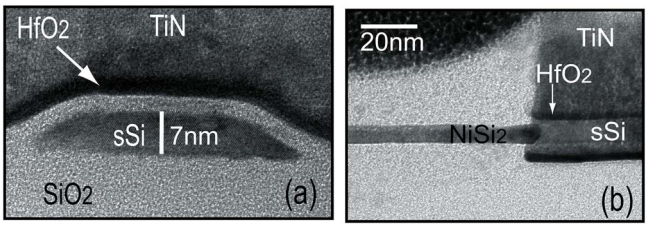

FIGURE 5. **(a) XTEM image of single sSi nanowire tri-gate TFET. (b) XTEM cross section along the NW, indicating a perfectly aligned $NiSi_2$ contact to the channel.**

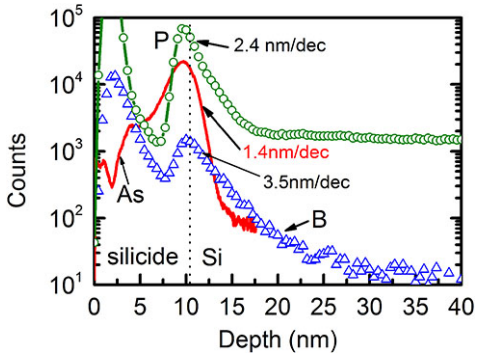

FIGURE 6. **SIMS measurements of B, P, and As doping profiles of $NiSi_2$/Si junctions with very steep dopant gradients achieved by ion implantation into silicide and dopant segregation.**

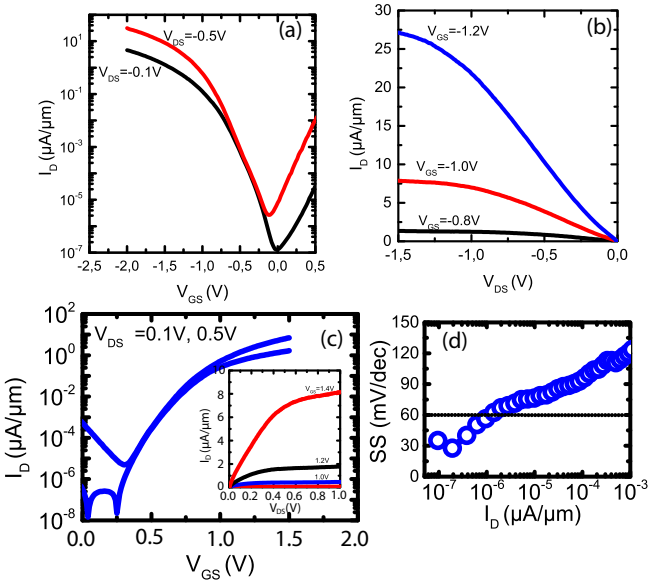

FIGURE 7. **(a) I_D-V_{GS} and (b) I_D-V_{DS} of a trigate sSi NW p-TFET (L_g = 200 nm). (c) I_D-V_{GS} and I_D-V_{DS} (inset) of trigate sSi NW n-TFET showing high I_{on}. (d) SS-I_D showing a minimum of 30 mV/dec at 300 K.**

tunneling junctions. Low energy ion implantation into the silicide (IIS) in combination with ultra-thin Ni source/drain contacts and a low temperature annealing turned out to be most efficient [28]–[30]. Fig. 4 illustrates the sequence of the device fabrication process. After patterning the sSOI layer into uniaxial strained NW arrays, the gate stack consisting of 3 nm HfO_2 dielectric and 60 nm thick TiN gate metal was deposited. Each TFET consists of an array of 100 parallel NWs with a gate length of 200 nm. Epitaxial $NiSi_2$ contacts at S/D were formed by depositing Ni films thin enough, with respect to the Si layer thickness, to be consumed completely during silicidation. Thus, the formation of the ultrathin, epitaxial $NiSi_2$ layer allowed perfect alignment of the S/D contacts to the gate, avoiding any encroachment as observed for thicker silicide layers. Fig. 5 shows cross-sectional TEM (XTEM) images across (Fig. 5(a)) and along (Fig. 5(b)) a single NW. As a novelty, the S/D doped junctions were formed without additional implantation masks. The gate stack was used as a shadow mask for the tilted (45°/135°) As^+ and B^+ ion implants into the silicide (IIS), as illustrated in Fig. 4(b) and (c). This allows the formation of perfectly self-aligned, highly doped n^+ and p^+ pockets right at the edges of the $NiSi_2$ S/D after low temperature annealing (450°C) by DS (Fig. 4(d)). Very steep, vertical doping profiles with gradients of 1.4 nm/dec for As, 2.4 nm/dec for P and 3.5 nm/dec for B, respectively, were measured by SIMS on $NiSi_2$ formed on bulk Si(100) substrates as indicated in Fig. 6. Apart from the steepness of the junctions, the essential advantage of this method is that no intentional ion implantation into the channel material is employed, such that less defects are generated in the tunneling junction. This is a key aspect to minimize TAT as one of the major issues of TFETs.

Obvious progress is reflected in the following transistor characteristics. Fig. 7(a) shows the transfer curves for a p-TFET with a tri-gate structure as shown in Fig. 5. As expected for symmetric homojunction TFETs, ambipolar characteristics are observed. A minimum *SS* of 90 mV/dec with a slight kink in the $I_D - V_{GS}$ curves, indicating TAT, is observed. The corresponding output characteristics of the p-TFET, displayed in Fig. 7(b), show a relatively high I_{ON} of 7 μA/μm (at $V_{DS} = V_{GS} = -1$ V). I_{ON} is more than two orders of magnitude higher compared to the device shown in Fig. 2 with direct implantation into sSi and thus less steep source doping profile. The larger I_{ON} can be attributed predominantly to the improved

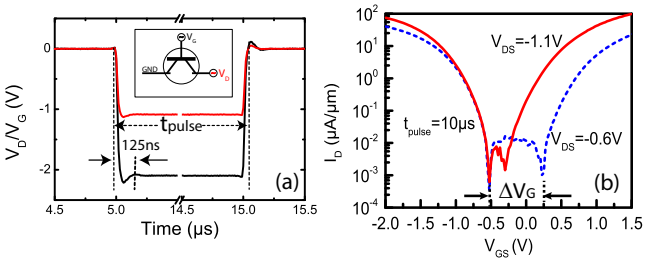

FIGURE 8. **(a) Pulse measurement setup (inset) and pulse waveform applied for I-V measurements. (b) Pulsed I_D-V_{GS} of p-TFET at $V_{DS} = -0.6$ V and -1.1 V with a pulse length of 10 μs.**

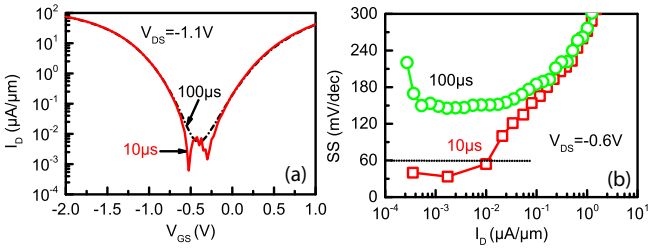

FIGURE 9. **(a) Comparison of pulsed I_D-V_{GS} for TFETs ($L_g = 200$ nm) with two different pulse lengths. (b) SS versus I_D measured on p-TFETs with two different pulse lengths proving less TAT at shorter pulses.**

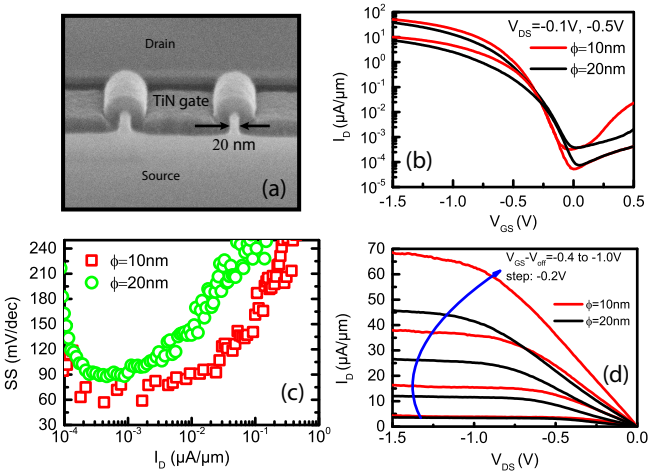

FIGURE 10. **(a) SEM image of GAA TFET structure with a NW diameter of 20 nm. (b) Comparison of static I_D-V_{GS} characteristics and (c) SS-I_D for 20 nm and 10 nm NW GAA TFETs, indicating smaller SS in scaled NW TFETs due to better electrostatics. (d) Comparison of static I_D-V_{DS} characteristics indicates high I_{ON} for TFETs with smaller NW diameter.**

tunneling junctions with steeper doping profiles achieved by DS.

The benefit of this approach is further substantiated by the results obtained for n-TFETs. Fig. 7(c) shows the I_D-V_{GS} characteristics and the inset presents the I_D-V_{DS} curves of the n-TFET. The n-TFET shows a much steeper *SS* than the p-TFET, reaching a minimum *SS* $\sim$ 30 mV/dec with *SS* $<$ 60 mV/dec over a range of more than one order of magnitude of I_D, as displayed in Fig. 7(d). For the n-TFET the tunneling junction is doped with B. Normally, fast diffusion of B prevents the formation of steep junction, however, IIS and DS overcome this problem. In addition, as mentioned above, direct ion implantation into the channel is avoided to a large extent, and thus defects and degrading TAT effects are reduced. DS requires only a low temperature annealing (around 500°C) which reduces the B diffusion and enables very steep junctions with very high doping concentration. The latter is essential to overcome the problem of S-shaped I_D-V_{DS} onsets, typical for TFETs with non-optimized junctions [31], [32]. The inset of Fig. 7(c) shows perfectly linear $I_D - V_{DS}$ characteristics, proving high dopant concentrations in the DS junctions and relatively large tunneling currents. References [31], [32] indicate that a high doping concentration in the junctions is a prerequisite to match the density of states in the source, channel and drain to obtain linear $I_D - V_{DS}$ response and to improve drain conductance.

However, As and B doped junctions differ also after DS due to different diffusion behavior, solubility limit and dopant activation energy. The heavy mass of As^+ ions produces more defects in the Si due to the non-optimized tilted implant angle. These defects are not removed after low temperature annealing leading to a significant TAT contribution to the tunneling current and poorer *SS* of the p-TFET (Fig. 7).

D. SHORT PULSES ELIMINATE TAT

The results shown above indicate that TAT degrades *SS* in TFETs. We investigated TAT using pulsed *I-V* measurements by pulsing both, gate and drain voltages while keeping the source grounded. Different pulse lengths (t_{pulse}) were applied while the TFET currents were reliably sampled starting from 125 ns after the pulses were applied, as illustrated in Fig. 8(a). I_D was averaged over 25 pulses. The measurement range for I_D is limited to a minimum value of $\sim 1 \times 10^{-4}$ μA/μm by the resolution of the measurement setup. Fig. 8(b) shows the pulsed I_D-V_{GS} characteristics of a p-TFET with $t_{pulse} = 10\mu s$ at $V_{DS} = -0.6$ V and -1.1 V. Due to TAT and ambipolarity, the onsets of p- and n-branches cannot be separated in DC measurements as shown in Fig. 7(a). Under short pulses TAT is suppressed, leading to steeper *SS*, and as a consequence to a separation of the onsets of n- and p-TFET branches with a $\triangle V_G$ proportional to E_g-$|V_{DS}|$ (Fig. 8(b)).

TAT depends strongly on the pulse length since charge trapping and detrapping occurs on a certain time scale. Fig. 9(a) compares the $I_D - V_{GS}$ curves measured with $t_{pulse} = 10\mu s$ and $t_{pulse} = 100$ μs, respectively. At a long pulse of t_{pulse}=100 μs, there is no clear separation between the onsets of p- and n-branch in the $I_D - V_{GS}$ characteristics. The presence of TAT results in larger *SS* (Fig. 9(b)). At shorter pulses TAT diminishes and a minimum *SS* of 30 mV/dec at $t_{pulse} = 10\mu s$ is reached, as shown in Fig. 9(b).

E. TOWARDS 1-D: NANOWIRES ENHANCE BTB TUNNELING

NW TFETs with gate all around (GAA) structures were fabricated. The SEM image of Fig. 10(a) exhibits a 3 nm HfO_2 /50 nm TiN gate stack wrapped around the sSi NWs with a diameter of 20 nm. Fig. 10(b) shows the I_D-V_{GS} characteristics of GAA sSi NW p-TFETs with NW diameters of 10 nm and 20 nm, respectively. In contrast to the tri-gate devices discussed above, the silicided source is implanted with P^+ ions, instead of heavy As^+ ions, to minimize the defect generation. In addition, a Schottky silicide drain (without implantation at the drain side) was used to suppress the ambipolarity. The I_D-V_{GS} curves reveal that the ambipolar behavior is indeed suppressed. A comparison of $I_D$vs V_{GS} and *SS* vs I_D (Fig. 10(b) and (c)) clearly indicates that the 10 nm NW GAA TFETs, reaching ~60 mV/dec, outperform the 20 nm NW GAA TFETs in terms of minimum *SS*, and output currents. Fig. 10(d) shows the output characteristics of 10 nm and 20 nm GAA NW p-TFETs, respectively. A high I_{ON} of 64 μA/μm at $V_{DS} = V_{GS} - V_{off} = -1.0$ V is obtained for the 10 nm NW TFET, much higher than the 20 nm one, further demonstrating the improved device performance by scaling the NW diameter.

In summary, the strongly improved electrostatics shortens the effective tunneling length and thus enhances BTBT. As a result TAT becomes less apparent in highly scaled, nearly 1-dimensional nanowires.

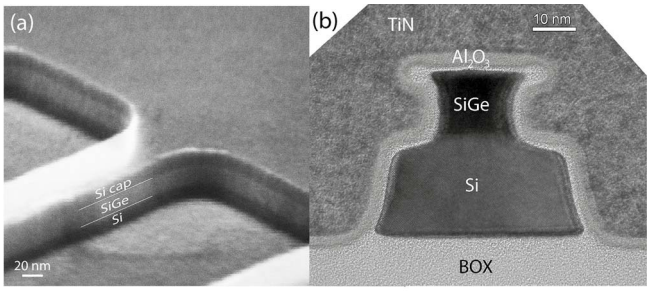

FIGURE 11. **(a) Tilted angle SEM image of a NW array etched into a $Si/Si_{0.5}Ge_{0.5}$/SOI substrate. (b) XTEM image of a single SiGe on SOI NW with Al_2O_3/TiN gate stack.**

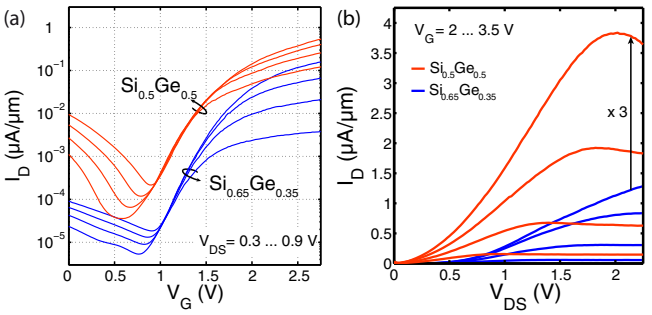

FIGURE 12. **(a) Transfer and (b) output characteristics of n-channel homostructure $Si_{1-x}Ge_x$ on SOI NW array TFETs with x = 35% and 50% Ge content.**

III. SiGe NANOWIRE TFETs

A. SiGe HOMOJUNCTION NW TFETs

As discussed above SiGe is attractive for TFETs due to the smaller bandgap as compared to Si. Homojunction SiGe NW TFETs were fabricated on wafers with 15 nm $Si_{1-x}Ge_x$ grown pseudomorphically on 15 nm SOI substrates with a Si cap layer of 5 nm. Due to the pseudomorphic growth of SiGe the in-plane lattice constant adapts to the smaller lattice constant of Si and the SiGe layer becomes compressively strained. Substrates with Ge contents x = 35% and x = 50% were used. Assuming pseudomorphic growth yields to strain levels of $\varepsilon = -0.98$ % and $\varepsilon = -1.41$ %, respectively. The compressive strain lifts the degeneracies of valence and conduction band causing a further decrease of E_g compared to unstrained SiGe [33]. Furthermore, m^* is reduced due to a reduction of the hole mass in the highest valence band. This reduction of m^* further enhances BTBT according to eq. (1).

An array of NWs with 40 nm width was patterned and covered with a high-k/metal gate consisting of 3.5 nm Al_2O_3 and TiN. SEM images from the NW array and a cross-sectional TEM of a single NW are shown in Fig. 11. The width of the SiGe layer in the NW was reduced by the cleaning process with hydrofluoric acid (HF) etching and ozone oxidation to clean the sample surface and provide a thin oxide layer as passivation prior to high-k deposition. Source and drain regions were formed by ion implantation with As^+ and $BF_2{}^+$ and activation at 650 °C for 1 min.

The n-channel transfer characteristics of a $Si_{0.65}Ge_{0.35}$ and $Si_{0.5}Ge_{0.5}$ nanowire array TFET are shown in Fig. 12(a). The drain current I_D obtained for the device with higher Ge content is significantly larger. I_{ON} for the $Si_{0.5}Ge_{0.5}$ device is about three times higher than for the $Si_{0.65}Ge_{0.35}$ device as shown in the output characteristics in Fig. 12(b). This can be attributed to the smaller bandgap E_g of higher Ge content alloys and hence increased tunnelling current. However, also the off-current increases by about one order of magnitude for 50% Ge compared to 35% Ge as shown in Fig. 12(a). The increase in I_{OFF} with decreasing E_g has two main contributions which are given by a Shockley-Read-Hall (SRH) generation-recombination current and tunneling at the channel-drain junction. The SRH contribution is proportional to the number of intrinsic carriers $n_i = exp(-E_g/2k_BT)$, where k_B is the Boltzmann constant and T the temperature. Due to the smaller E_g of $Si_{0.5}Ge_{0.5}$ compared to $Si_{0.65}Ge_{0.35}$ SRH generation increases I_{OFF} for the larger Ge content. Also the off-current contribution due to channel-drain tunneling increases for smaller E_g.

TAT has a large influence on the SiGe devices, which was observed in temperature dependent measurements of the transfer characteristics [18]. Traps are introduced in the SiGe devices at the channel gate dielectric interface as well as at the source-channel and channel-drain junctions by the ion implantations used to form the tunnel junctions.

The cleaning process for the binary compound semiconductor SiGe prior to the gate stack deposition is much more challenging than for Si. The wafer cleaning used for these devices, removes the native oxide in a HF bath and builds up a thin oxide layer in a subsequent ozone oxidation as passivation layer. Charge pumping measurements on the SiGe nanowire devices reveal an interface state density D_{it} of 3×10^{12} cm^{-2}. Compared to RCA cleaned strained Si NWs shown in [10] this D_{it} value is one order of magnitude higher. A larger number of interfacial traps at the oxide can give rise to TAT and also degrades the gate control since the gate electric field is screened by the trap charges. Thus higher values for *SS* are observed in the SiGe devices compared to the presented Si NW TFETs.

The SiGe NW TFETs demonstrate the potential for increasing BTBT by small band gap materials. However, higher D_{it} levels causing reduced gate control and increased I_{off} degrade the performance. Since larger on-currents are crucial in order to increase the switching speed of TFETs the problem of increasing off-currents for small band gap materials needs to be solved by asymmetric structures or the introduction of heterostructures as discussed in the following section.

High on-currents in TFETs based on SiGe NWs directly on insulator are demonstrated by Villalon *et al.* [16]. Further improvement of I_{on} in SiGe TFETs could also be achieved by combining small band gap materials with the dopant segregation technique for achieving steep source doping profiles introduced in section II.C.

B. SiGe/Si HETEROJUNCTION NW TFETs

A promising concept to avoid the off-current increase in TFETs based on small band gap materials is the use of heterostructure tunnel junctions. A heterostructure n-type TFET with a SiGe source and Si channel/drain offers the same effective E_g at the tunnel junction as an all SiGe TFET due to the valence band offset from SiGe to Si. On the other hand, SRH generation and channel drain tunnelling in the off-state of the TFET are reduced by the larger Si band gap in channel and drain regions.

Such a SiGe/Si heterostructure TFET was fabricated using a NW array design on substrates with 12.4 nm in situ doped $Si_{0.5}Ge_{0.5}$ grown pseudomorphically on 21 nm SOI substrate capped with 9.4 nm Si. The boron dopant concentration in the in situ doped $Si_{0.5}Ge_{0.5}$ layer is 2×10^{20} cm^{-3}. NWs with a width of 40 nm were patterned on the substrate with a step down to the bottom Si layer at the drain side as illustrated in the Fig. 13(a). The step was covered with a tri-gate consisting of 4 nm HfO_2 and 40 nm TiN deposited by ALD and AVD, respectively. Fig. 13(b) and (c) show SEM images of the nanowire array with etched drain step before and after formation of the gate with gate length of 2 μm. The drain was formed by self-aligned ion implantation with As^+ ions.

Compared to the homojunction NW devices from the previous sections, where BTBT occurs only in a confined region at the source-channel junction close to the gate, the NW

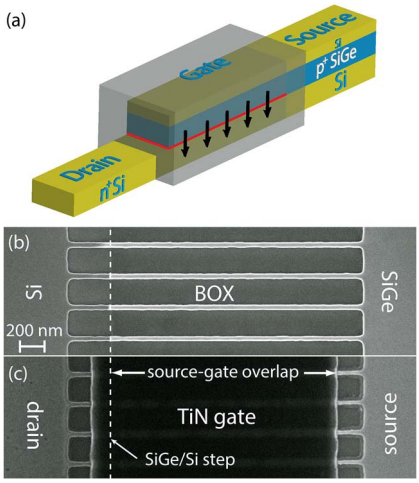

FIGURE 13. (a) Schematic of a single NW in the SiGe/Si heterostructure TFET with tri-gate. (b) Top view SEM image of the heterostructure NW array before gate stack deposition and (c) after gate stack deposition and patterning.

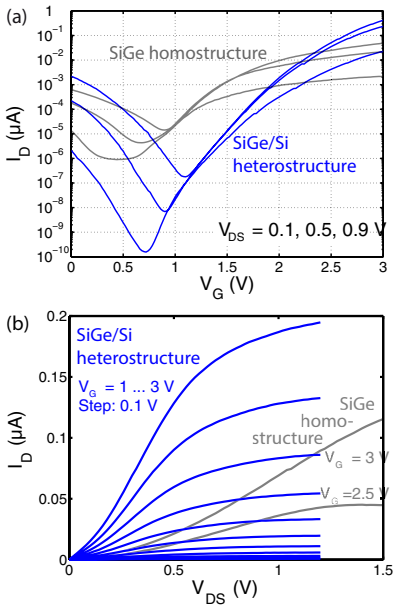

FIGURE 14. Comparison of (a) transfer and (b) output characteristics of a $Si_{0.5}Ge_{0.5}$/Si heterostructure NW TFET (blue) and a $Si_{0.5}Ge_{0.5}$ homostructure NW TFET (gray). Currents are normalized per nanowire.

heterostructure design offers an enlarged tunneling junction area. BTBT from source to drain is enabled along the line between SiGe source and bottom Si channel marked in red in Fig. 13(a). Additionally, due to the overlap of source and gate a thin layer of the p-doped source region can be inverted for sufficiently large gate potential and BTBT occurs perpendicular to the gate along the electric field lines increasing the tunneling area further. This process is also referred to as line tunneling [34].

Fig. 14(a) shows the n-channel transfer characteristics of a SiGe/Si heterostructure NW TFET with a gate length of 2 μm. The transfer characteristics of a $Si_{0.5}Ge_{0.5}$ homostructure NW TFET from the previous section is

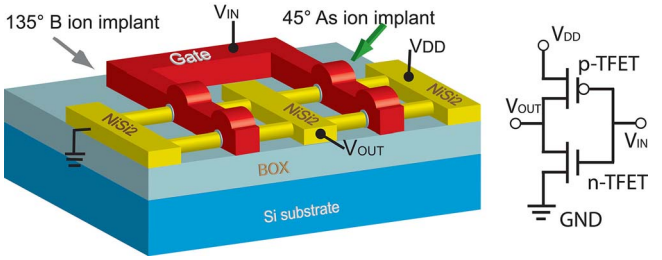

FIGURE 15. Schematic of sSi NW TFET inverter fabricated using tilted B^+ and As^+ ion implantations into epitaxial $NiSi_2$ S/D contacts.

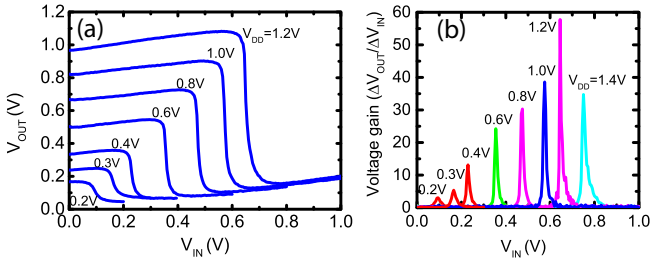

FIGURE 16. (a) VTC and (b) voltage gain for trigate sSi NW TFET inverters, showing a sharp transition even at V_{DD} = 0.2 V.

shown as a comparison. The drain current I_D is normalized per nanowire for both devices since the dimensions of the homostructure and heterostructure nanowires are comparable. However, the tunnel junction width in the heterostructure scales with the gate source overlap making normalization per gate width not suitable for the heterostructure device. The heterostructure device exhibits a minimum *SS* of 90 mV/dec and I_{ON}/I_{OFF} ratio of 6 orders of magnitude at V_{DS} = 0.9 V. The homostructure TFET in comparison shows a maximum I_{ON}/I_{OFF} ratio of 3.5 orders of magnitude. The heterostructure design with Si channel and drain decreases SRH generation and tunneling at the channel-drain junction compared to the homojunction due to the larger Si bandgap in channel and drain. Thus a lower I_{OFF} and a large I_{ON}/I_{OFF} ratio can be achieved. Fig. 14(b) exhibits output characteristics of the heterostructure for V_G from 1 V to 3 V in steps of 0.1 V. For comparison output curves of the homostructure at V_G = 2.5 V and 3 V are shown. The *S*-shape of $I_D - V_{DS}$ curves is far less pronounced in the heterostructure, which shows a current saturation at V_{DS} well below 1 V. This can be attributed to a steeper doping profile in the in situ doped source, decreasing the tunnel distance compared to the implanted source region of the homojunction NW device. The current per wire in the heterostructure exceeds that of the homostructure, which is not only related to the higher junction quality, but also to the difference in device geometry and the increased tunnel junction area. I_D in the heterostructure TFET scales with the gate length due to the enlarged tunnel junction area along the overlap of source and gate as shown in [15]. Temperature dependent measurements of the transfer characteristics in [15] exhibit a much smaller variation with *T* compared to the ion implanted homostructure SiGe devices. This can be attributed to a smaller number of trap states in the in situ doped tunnel junction and thus suppressed TAT. In conclusion, the SiGe/Si heterostructure TFET enables low I_{OFF} in combination with increased I_{ON} due to low effective band gap and steep doping profile in the in situ doped source. Corresponding p-channel heterostructure TFETs required for complementary TFET logic inverter have already been realized based on InAs as source material and Si channel in [35]. Also an integration scheme for n- and p-channel heterostructure TFETs has been demonstrated [36].

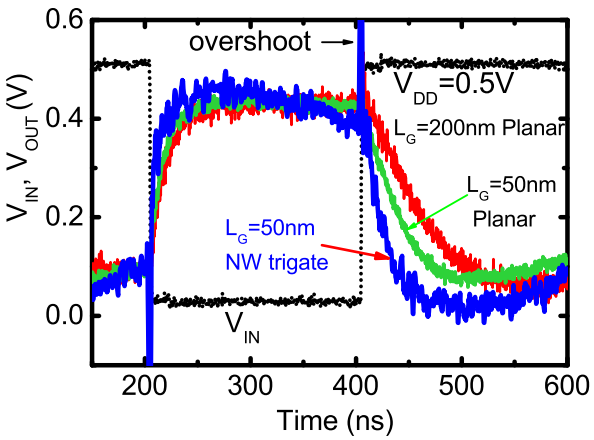

FIGURE 17. Transient time response measurements for different TFET inverters indicate that scaling the gate length and/or the NW improves the response speed.

IV. TFETs FOR LOGIC APPLICATION

The almost symmetric performance of n- and p- sSi NW TFETs with IIS and DS allowed to investigate first TFET logical circuits. In the following we will present experimental results of complementary TFET inverters and p-logic TFET NAND gates.

A. Si C-TFET INVERTERS

With the tilted implantation and DS silicided S/D it is fairly easy to fabricate c-TFET inverters with 2 gate fingers, as schematically shown in Fig. 15. Fig. 16(a) shows the voltage transfer characteristics (VTC) at different V_{DD} for an inverter consisting of tri-gate NW c-TFETs. A sharp transition with wide noise margin was observed even at a V_{DD} as low as 0.2 V. The gain $\Delta V_{OUT}/\Delta V_{IN}$ at various V_{DD} is displayed in Fig. 16(b). A high gain of 57 was obtained at V_{DD} = 1.2 V. Even at a very low V_{DD} = 0.2 V still a gain of ≈3 is achieved. The VTC curves show a degradation of output voltage V_{OUT}, which means $V_{OUT} < V_{DD}$ at small input voltage V_{IN} and $V_{OUT} > 0$ V at high V_{IN}. Simulations indicate that the degradation of V_{OUT} is mainly due to the ambipolar behavior [11].

The transient time response of different TFET inverters is compared in Fig. 17 at V_{DD} = 0.5 V. All devices show overshoots related to an enhanced Miller capacitance. The comparison of the planar TFET inverters indicates a shorter

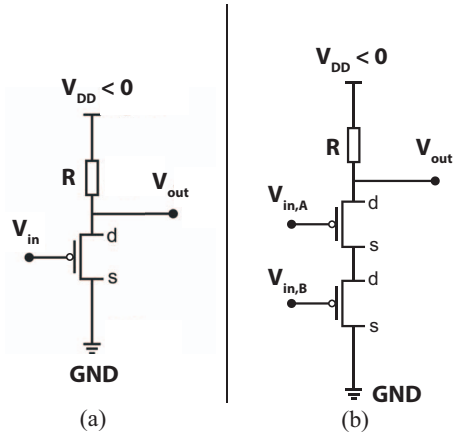

FIGURE 18. **(a) Schematic of a p-logic inverter and (b) p-logic NAND gate.**

time response for shorter gate length due to the reduced gate capacitance, even though the tunneling currents are less dependent on the gate length in DC measurements. Fig. 17 further reveals that superior performance can be achieved using scaled NW TFETs due to better electrostatics, smaller parasitic capacitance and reduced sensitivity for TAT.

B. p-LOGIC TFET NAND

Fig. 18 depicts the schematics of a p-logic inverter and NAND gate consisting of a resistor and one or two p-TFETs, respectively. For the NAND gate GAA sSi NW TFETs with a NW diameter of 20 nm, as shown in Fig. 10, were used. Fig. 19(a) shows the measured VTC of the p-TFET inverter at V_{DD} from −0.5 V down to −0.15 V. The resistor R is adjusted for different V_{DD}, in order to achieve switching voltages close to $V_{DD}/2$, which corresponds to the maximum noise margins. Fig. 19(b) exhibits the corresponding time response measurements of the inverter output V_{out} for different V_{DD}. The rise time t_{rise} decreases for the smaller pull-up resistor due to decreased load times at higher current levels. The fall time t_{fall} of V_{out} is determined by the current flow through the p-TFET and thus decreases with higher V_{DD}. Since the resistance of the p-TFET in the on-state has to be smaller compared to R in order to pull the output to ground t_{rise} is always larger compared to t_{fall} and thus limits the switching speed of the device. Switching is also slower than of the tri-gate NW C-TFET inverters shown in Fig. 16.

Fig. 20 exhibits the time response measurement of a p-TFET NAND gate as depicted in Fig. 18(b). The input pattern for $V_{in,A}$ and $V_{in,B}$ is shown as an example for $V_{DD} = -0.5$ V and V_{out} of the NAND gate is displayed for $V_{DD} = -0.2, -0.3$ and -0.5 V. The truth table of a NAND gate is clearly observed.

V. TFET FOR ANALOG APPLICATION

TFETs are also interesting for low power analog, RF- and sensor applications due to their ability of reaching steep slopes and excellent output saturation. However, there are only a few theoretical [37]–[39] and even less

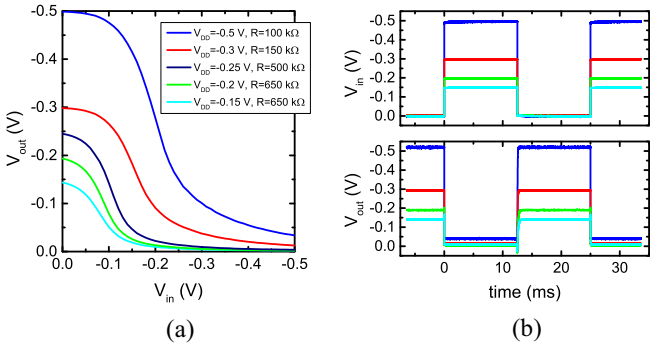

FIGURE 19. **(a) Voltage transfer characteristics (VTC) of a p-TFET inverter with resistors adjusted for each V_{DD}. (b) Corresponding time response measurement of p-logic inverter.**

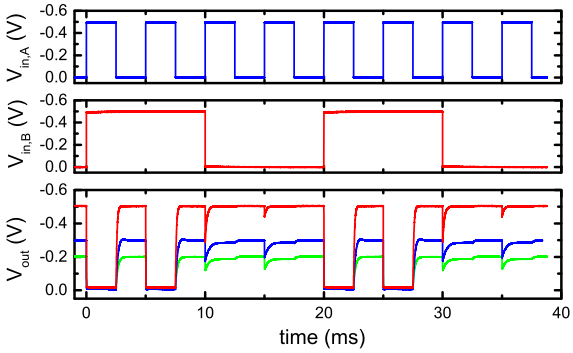

FIGURE 20. **Time response measurement of a p-logic TFET NAND gate for different supply voltages. Input voltages $V_{in,A/B}$ are shown only at supply voltage 0.5 V for simplicity.**

experimental [40] studies on analog and RF applications of TFETs. The simulations show that TFETs have the ability to outperform MOSFETs in terms of transconductance $g_m = \partial I_d/\partial V_g$, transconductance efficiency g_m/I_d and intrinsic voltage gain $A_i = g_m/g_d$ especially due to good output saturation (small $g_d = \partial I_d/\partial V_d$) and when sub 60 mV/dec slopes (high g_m/I_d) come into play. For analog devices especially the intrinsic gain $A_i = g_m/g_d$ is crucial as it defines the DC voltage gain. Reaching high A_i is a particular challenge for highly integrated MOSFETs due to degraded output characteristics. However, due to large Miller capacities TFETs tend to have reduced bandwidth in comparison to MOSFET making TFETs especially interesting for low power application in a moderate frequency range [39].

As TFET device physics differs from MOSFETs due to their fundamentally different charge injection mechanisms, MOSFET device models and analog characterization methods cannot be directly transferred to TFETs. Thus, we focus on device physics independent key parameters such as g_m, g_d, g_m/I_d and A_i.

Planar and GAA NW p-TFETs with NW diameters of 20 nm and 10 nm described above were utilized for analog characterization. By scaling from planar devices to 20 nm to 10 nm NW GAA p-TFETs an improvement in the maximum g_m by a factor of 12 was realized as can be seen in Fig. 21(a),

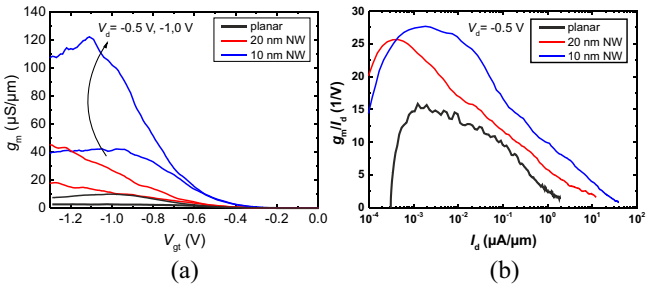

FIGURE 21. Comparison of (a) g_m and (b) g_m/I_D for planar and GAA NW p-TFETs, showing improved performance for scaled NW TFETs.

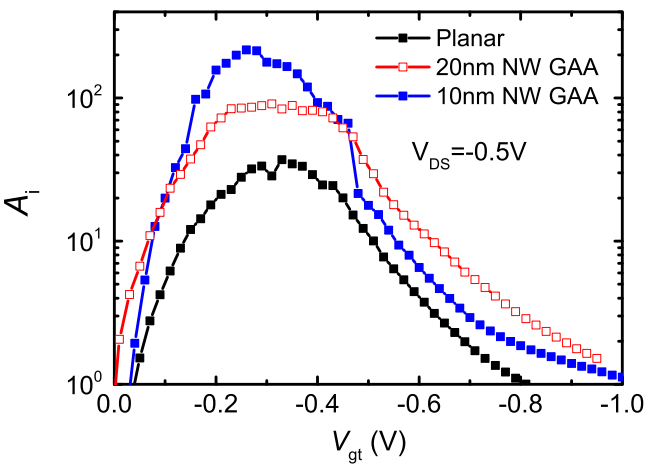

FIGURE 22. Comparison of A_i for planar and GAA NW p-TFETs, showing outperformance of NW TFETs over planar TFETs.

where $V_{gt} = V_{GS} - V_{min}$ is the gate overdrive voltage and V_{min} corresponds to the gate voltage where I_{DS} reaches the minimum. The 10 nm NW-TFETs reach a maximum g_m of 122 µS/µm, which is the highest reported value for Si TFETs. The improvement is also visible in g_m/I_d where the NW TFETs feature higher values over the whole current range making them more power efficient than the planar devices as depicted in Fig. 21(b).

Fig. 22 shows the intrinsic voltage gain for p-TFETs operated at $V_{DS} = -0.5$ V. The GAA NW p-TFETs outperform the planar p-TFET. The highest intrinsic gain of $A_{imax} = 217$ was reached with the 20 nm NWs and surprisingly not with the 10 nm NW TFETs. However, this could be attributed to slightly degraded output saturation (higher g_d) for higher values of V_g of all devices which could be explained by a drain induced barrier lowering of the Schottky drain junction. As the 10 nm NW TFETs feature a lower source tunnel resistance this effect is more pronounced for the 10 nm NW-devices (see Fig. 10) and thus leads to a degraded intrinsic gain. However, the intrinsic gain at $V_d = V_{gt} = -0.5$V for the 10 nm GAA NW p-TFET is even higher than the state of the art 20 nm n-FinFET [41].

VI. CONCLUSION

We have presented an overview of our most recent Si and SiGe NW TFETs. Evidently, strained Si NW TFETs outperform conventional Si NW TFETs due to the smaller band gap and effective mass. We have shown that tuning of the electrostatics by using high-k/metal gates leads to increased tunneling currents. Particular emphasis has been placed on the improvement of tunneling junctions. For this purpose, tilted ion implantation into the silicide followed by a low temperature annealing to induce segregation of dopants to the source/channel interface has been demonstrated. Very steep junctions have been achieved which is key for achieving high on-currents and *SS*<60mV/dec. Trap assisted tunneling was investigated using pulsed I-V measurements. The results indicate that scaled NWs with GAA geometry significantly increase the tunneling currents, lower *SS* and lessen TAT.

SiGe NW homostructure and SiGe-source-Si-channel heterostructures implemented in a tri-gate nanowire array TFETs have been investigated. Line tunneling at the side walls of the nanowires has been demonstrated. Utilizing line tunneling by properly designing the TFET structure provides further options for improving the tunneling currents.

Finally, first logic applications of TFETs have been experimentally demonstrated and analog parameters of the devices have been extracted. Complementary TFET inverters as well as GAA NW p-TFET NAND gates were operated at very low V_{DD}, explicitly at 0.2V, demonstrating a great potential of ultra-low power applications of TFETs. The analysis of transconductance g_m, transconductance efficiency g_m/I_D and intrinsic gain $A_i = g_m/g_d$ of p-TFETs has proven that GAA NW devices outperform planar TEFTs. Surprisingly high transconductance efficiency and intrinsic gain have been achieved for TFETs.

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