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Suppression of the surface-inversion layer of *p*-type InAs

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The resistivity of spatially selectable regions on *p*-type InAs is increased by epitaxial growth of a larger band-gap material, i.e., InAlAs, on top of InAs. Due to this InAlAs layer, the formation of a two-dimensional electron gas in the InAs layer is suppressed. This is demonstrated experimentally and supported by calculations of the conductance and valence band profile. At low temperature (4.2 K), the resistance of *p*-InAs coated with InAlAs and InGaAs is increased by a factor of 180 compared with bare *p*-InAs. © *1999 American Institute of Physics.* [S0021-8979(99)06612-8]

I. INTRODUCTION

p-type InAs has several properties, which makes it attractive for superconductor/semiconductor hybrid structures, e.g., Josephson weak links and three-terminal devices.[1–4] The most remarkable property is the native inversion layer on the surface, which has the characteristics of a two-dimensional electron gas (2DEG). This is because the Fermi level at metal/*p*-type InAs or vacuum/*p*-type InAs interfaces is pinned inside the InAs conduction band.[5,6] The Fermi level pinning leads to the absence of a Schottky barrier at the metal/InAs interface, thus allowing us to prepare low resistive metal/2DEG contacts. If the 2DEG is connected to closely spaced (a few 100 nm) superconducting electrodes, a supercurrent can flow. By placing a gate between the superconducting electrodes, the supercurrent can be controlled by applying an appropriate gate voltage. A Josephson field effect transistor (JOFET) based on the surface-inversion layer on *p*-InAs has been demonstrated[1] and a hybrid three-terminal step junction has been proposed[3] and realized.[4] However, the surface-inversion layer based devices and junctions have the disadvantage of the lack of device isolation. The use of *p*-InAs allows only vertical isolation, since the surface inversion layer is separated from the conductive region by a depletion region (see Sec. II). The presence of a conducting layer over the entire surface of both *n*- and *p*-type InAs crystals, even after etching of a mesa, results in a reduction of the product of critical current–normal state resistance I_cR_N and makes it difficult to isolate devices laterally. Kleinsasser *et al.*[7] have shown that an increase of the I_cR_N product of InAs-coupled Josephson weak links can be achieved by using an InAs mesa, which is grown on semi-insulating GaAs.

In this article, we report on a method to increase the resistivity on arbitrary regions of the *p*-type InAs wafer by using epitaxially grown *p*-InAlAs layers and *p*-InGaAs layers on top of *p*-InAs. The carrier concentration at the InAs/InAlAs interface can be adjusted by changing the Al content in the thin InAlAs layer. If the group-III component (In,Al) contains 60% aluminum ($In_{0.4}Al_{0.6}As$), our simulations show that the 2DEG at the interface between InAs and InAlAs is removed. The InGaAs cap layer is necessary to protect the InAlAs layer against oxidation of Al.

Our experiments show that the resistivity of InAs coated with InAlAs and InGaAs is increased up to a factor of 180 compared with bare *p*-InAs. By selective removal of the InAlAs and InGaAs layers only in the area of the semiconductor/superconductor weak link junction an ''insulation'' of the semiconducting material around the junctions can be provided. This method promises therefore an increase of the I_cR_N product of the *p*-InAs Josephson weak links. Furthermore, the device isolation is important for the performance of the gate control with hybrid three-terminal step junctions presented in Refs. 3 and 4. In these devices, a gate embedded in *p*-InAs needs to be electrically isolated from the superconducting electrodes.

In Sec. II, the investigated layer systems are described. The valence and conduction band profile as well as the carrier concentration profile of bare *p*-InAs and *p*-InAs covered with InGaAs and InAlAs are calculated. In Sec. III the sample preparation is described. In Sec. IV A, results on bare *p*-type InAs while Sec. IV B results on *p*-InAs coated with InAlAs/InGaAs are discussed.

II. THE SEMICONDUCTOR STRUCTURES

Figure 1 shows the two layer systems considered here: The first structure (type A) consists of a 300-nm-thick low *p*-doped (p^-)-InAs layer, which is grown by molecular beam epitaxy (MBE) on a 500-μm-thick InAs p^+ substrate. The doping level of the epitaxial layer is $p=5\times10^{16}$ cm^{-3}, and the doping level of the InAs substrate is $p=10^{17}$ cm^{-3}. For the second layer system (type B), a 300-nm-thick p^--InAs layer, a 30-nm-thick p^--$In_{0.4}Al_{0.6}As$ layer, followed by a 10-nm-thick p^--$In_{0.53}Ga_{0.47}As$ layer are grown on the p^+-InAs substrate.

At the surface of *p*-InAs, with acceptor concentrations below 2×10^{17} cm^{-3},[8] a native inversion layer (*n*-type) is

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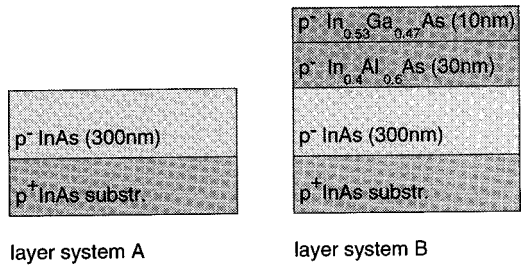

FIG. 1. Layer structure (A): 300 nm p^--InAs are grown by molecular beam epitaxy on a p^+-InAs substrate. Layer structure (B): 10 nm p^--InGaAs and 30 nm p^--InAlAs are grown epitaxially on top of structure A.

formed, which has the properties of a 2DEG. Figure 2 shows a self-consistent calculation[9] of the conductance and valence band profile (a) together with the carrier concentration (b) for low *p*-doped (p^-)-InAs (layer system A in Fig. 1). The simulation is based on the density functional method.[10] The energy gap of InAs is $\epsilon_g = 0.418$ eV at a temperature $T = 4.2$ K and the Fermi level is pinned above the conduction band edge. The spatial extension of the surface inversion layer is approximately 20 nm. The *n* layer is separated by an approximately 100-nm-thick depletion layer from the bulk *p* layer. A typical sheet carrier density at the surface of InAs is $\approx 10^{12}$ cm^{-2}.[11] In order to obtain a carrier concentration of the 2DEG at the surface of, e.g., $n_{2D} = 0.7 \times 10^{12}$ cm^{-2} [Fig. 2(b)] a Fermi energy of 0.25 eV above the conduction band edge at the surface was assumed.

At $T = 300$ K, the conductivity of *p*-InAs is *p*-type. With decreasing temperature, the hole density freezes out. For $T < 250$ K, the conductivity of our structures is *n*-type as confirmed by Hall effect measurements.[12] This is because at low temperatures the two-dimensional surface channel conductance is larger than the bulk conductance. Due to the carrier freeze out at low temperature, the current carried by the holes in the InAs is smaller that the current carried by the 2DEG.

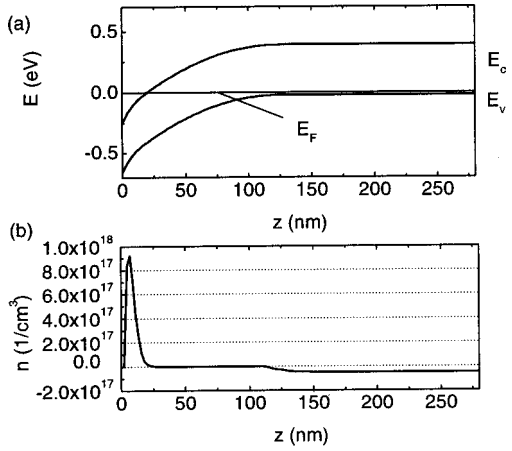

FIG. 2. (a) Calculation of the band scheme (band energy vs *z* coordinate normal to the surface $z=0$) for p^--doped InAs at $T = 4.2$ K. E_F is the Fermi energy, E_c indicates the lower conduction band edge, and E_v the upper valence-band edge. (b) Carrier concentration vs *z* coordinate. Parameters of the calculation: doping level $p = 5 \times 10^{16}$ cm^{-3}, $E_c(z=0) = -0.25$ eV, with respect to the Fermi energy, $\epsilon_g = 0.418$ eV.

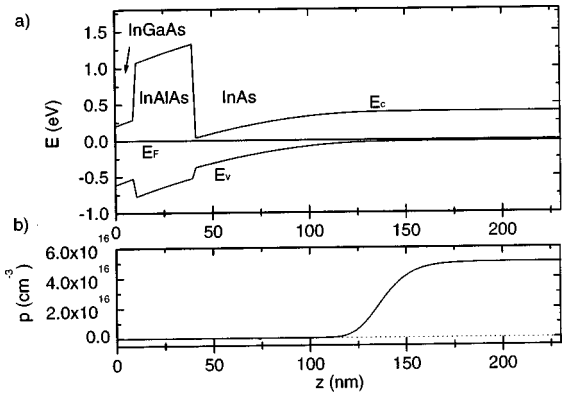

FIG. 3. Calculation of the band-structure (a) and the carrier concentration (b)of a *p*-type InAs/InAlAs/InGaAs structure. E_F is the Fermi energy, E_c indicates the lower conduction band edge, and E_v the upper valence-band edge. $0 < z < 10$ nm: InGaAs, 10 nm$< z <$40 nm: InAlAs, 40 nm$< z <$340 nm: InAs.

The conduction and valence band profile as well as the carrier concentration profile of InAs can be modified by an *in situ* grown material with a different energy gap ϵ_g. In Fig. 3, the band structure (a) and the carrier concentration profile (b) of the InAs/InAlAs/InGaAs layer system (sample B, see Fig. 1) is shown.

For the simulation, the doping level of $p = 5 \times 10^{16}$ cm^{-3} for all three layers is used, which approximately corresponds to the background doping level. The two top layers are 30-nm-thick $In_{0.4}Al_{0.6}As$ and 10-nm-thick $In_{0.53}Ga_{0.47}As$. The values of the conduction and valence band offsets (ΔE_c and ΔE_v) as well as the values for the band gap are taken from Fig. 1 in Ref. 13. Since in Ref. 13 the parameters of the compounds are given for $T = 300$ K only, we use as reference points the energy gap values of InAs (0.418 eV), InAlAs (1.84 eV), and InGaAs (0.813 eV) given in Ref. 8 for $T = 4.2$ K. The band offsets between the different materials at 4.2 K are subsequently obtained by a linear approximation of the data given in Ref. 13. For the conduction band offsets ΔE_c ($In_{0.4}Al_{0.6}As$/InAs) = 1.3 eV and ΔE_c($In_{0.4}Al_{0.6}As$/$In_{0.53}Ga_{0.47}As$) = 0.9 eV area obtained. The conduction band edge of InGaAs at the surface is assumed to lie 0.2 eV above the Fermi level.[14]

As can be seen in Fig. 3, the *n*-conducting layer at the interface between InAs and InAlAs is suppressed. If the Al content in the InAlAs layer is reduced to, e.g., 20%, a small *n*-conducting region at the interface with a carrier concentration $n_{2D} \approx 2 \times 10^{19}$ cm^{-2} is still present.

III. SAMPLE PREPARATION

In order to investigate the specific resistance and the magnetotransport properties a Corbino geometry[15] was used (see Fig. 4). The influence of the contact resistance between Au and InAs is avoided by using four concentric ring-shaped Au electrodes for current supply and voltage measurements. The inner d_i and outer diameter d_o of the rings are: d_o(D1) = 60 μm, d_i(D2) = 100 μm, d_o(D2) = 180 μm, d_i(D3) = 300 μm, d_o(D3) = 380 μm, d_i(D4) = 420 μm, d_o(D4) = 500 μm. For the investigation of layer system (A), the Au ring electrodes are evaporated directly on InAs. For

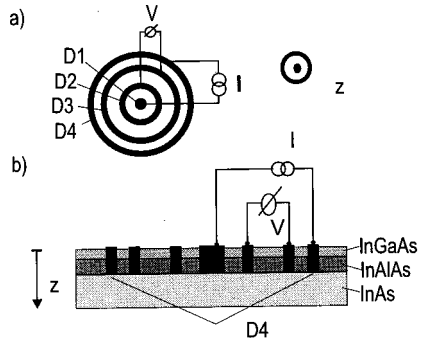

FIG. 4. Sketch of the four-point Corbino geometry. Four concentric Au ring electrodes are evaporated on top of InAs. The current is applied between the inner (D1) and the outer ring (D4). The voltage is measured between ring electrodes D2 and D3. (a) View from top. (b) Cut through the Corbino disk for layer system B.

the investigations of layer system (B), the InAlAs and InGaAs layers are removed in the area of the Corbino rings. This is indicated in a cut through the Corbino disk shown in Fig. 4(b). The following wet-chemical etching solutions are used to remove the InGaAs and InAlAs layer. First, native oxides are removed from the InGaAs surface by dipping into $2H_2O$:1HCl for 30 s. Then, the 10-nm-thick InGaAs layer is removed by etching with citric acid: H_2O_2 for 35 s. Finally the 30-nm-thick InAlAs layer is removed by a solution of $1H_2O$:3HCl for 5 s. The citric acid: H_2O_2 solution stops at AlInAs, and the HCl etch stops at InAs. After etching, the Au electrodes are deposited on the InAs surface.

To avoid destruction of the semiconductor due to the bonding procedure, all rings are covered with SiO_2, leaving just small windows open for contact bridges. The bonding pads are outside the Corbino disks.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A. Results with *p*-type InAs

Figure 5 shows a set of current–voltage ($I-V$) characteristics of the Corbino disk on bare *p*-InAs for different

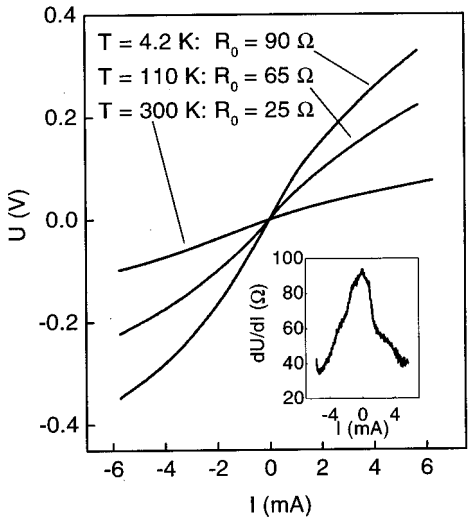

FIG. 5. $I-V$ curves of the Corbino disk on bare *p*-InAs for different T. The inset shows the differential resistance as a function of the bias current I for $T=4.2$ K.

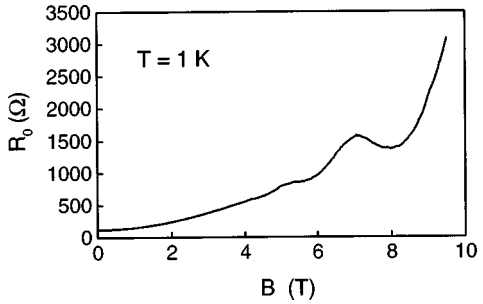

FIG. 6. R_0 of the Corbino disk as a function of a magnetic field B in z direction at $T=1$ K.

temperatures. From the resistance value at zero bias current R_0, the sheet resistance can be estimated using the equation

$$R_{\square}=2\pi R_0\left[\ln\left(\frac{d_i(\mathrm{D3})}{d_o(\mathrm{D2})}\right)\right]^{-1}, \tag{1}$$

where $d_i(\mathrm{D3})=300$ μm is the inner diameter of ring D3, and $d_o(\mathrm{D2})=180$ μm is the outer diameter of ring-electrode D2 [see Fig. 4(a)]. The zero-bias resistance R_0 increases from $R_0\approx 25$ Ω at $T=300$ K to $R_0\approx 90$ Ω at $T=4.2$ K. The sheet resistance is calculated to $R_{\square}\approx 300$ Ω at $T=300$ K and 1.1 kΩ at $T=4.2$ K.

If the differential resistance dV/dI at zero current bias R_0 is measured as a function of a magnetic field B, which is applied in the z direction, Shubnikov–de Haas oscillations are observed. Thus, the main contribution to the total conductivity is provided by the 2DEG. The Shubnikov–de Haas oscillations (for $B>4$ T) are depicted in Fig. 6, which shows R_0 of the Corbino disk as a function of B.

The period of the oscillations in ($1/B$) yields a carrier concentration in the 2DEG of $n_{2\mathrm{D}}\approx 10^{12}$ cm^{-2}. From the increase of $R_0(B)$ for small B ($B<1$ T), the mobility μ is estimated to be $\mu\approx 5000$ cm^2/V s using the approximation $[R_0(B)-R_0(0)]/R_0(0)\approx\mu^2B^2$.[16] From n and μ, the sheet resistance is calculated to be $R_{\square}=(en_{2\mathrm{D}}\mu)^{-1}\approx 1.25$ kΩ. This value is in reasonable agreement with $R_{\square}$ obtained from the zero-bias resistance of the Corbino disk (see above) so that it can be concluded that no significant bypass channel is present.

We also performed measurements with Corbino disks having an additional gate ring–electrode between ring D2 and D3 (not shown here, see Ref. 12). The thickness of the gate oxide (SiO_2) is 250 nm. Measuring the zero-bias resistance R_0 as a function of the gate voltage for different magnetic fields between 0 and 10 T, we obtain the result that the carrier concentration $n_{2\mathrm{D}}$ varies linearly with the gate voltage V_g. For $V_g=-6$ V: $n_{2\mathrm{D}}\approx 2\times 10^{11}$ cm^{-2}, $V_g=0$ V: $n_{2\mathrm{D}}\approx 1.2\times 10^{12}$ cm^{-2}, and $V_g=2$ V: $n_{2\mathrm{D}}\approx 1.6\times 10^{12}$ cm^{-2}. For $V_g=0$ V only the first subband is occupied.[12]

B. Results with InAlAs/InAGaAs coverage *p*-type InAs

In this section, the experimental results obtained with layer system B (InGaAs/InAlAs on top of InAs, Fig. 1) are presented. Figure 7(a) shows a set of $I-V$ curves of the Corbino disk [sample configuration is shown in Fig. 4(b)] for

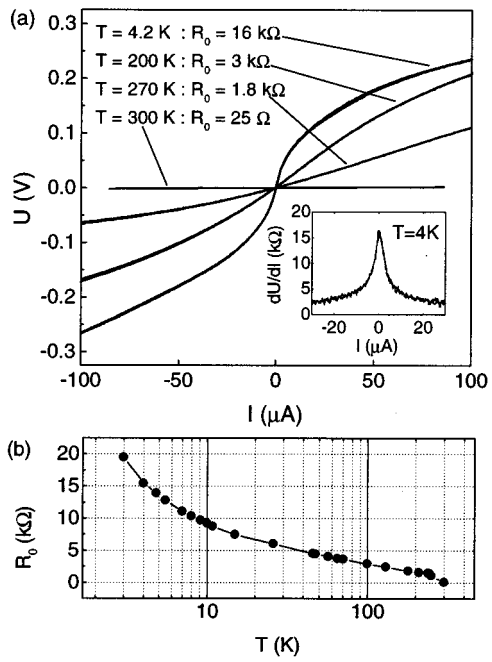

FIG. 7. (a) $I-V$ curves of the Corbino disk using p-type InAs coated with InAlAs/InGaAs (layer system B) for different temperatures. The InAlAs and InGaAs cap layers are removed in the contact area of the ring electrodes. The inset shows the differential resistance dV/dI as a function of I for $T=4.2$ K. (b) Temperature dependence of the zero-bias resistance R_0.

different temperatures. Figure 7(b) depicts the zero-bias resistance $R_0=dV/dI(I=0)$ vs T. The inset shows the differential resistance dV/dI as a function of the bias current I.

The resistance of the Corbino disk increases from $R_0=25\ \Omega$ at $T=300$ K to $R_0=19$ kΩ at $T=2$ K. At 4.2 K R_0 has a value of 16 kΩ, which results in a sheet resistance $R_\square$ of 195 kΩ. This is an increment of a factor of 180 compared with $R_\square$ of bare p-InAs at 4.2 K. The resistance increase at low temperatures shows that the presence of the InAlAs layer on top of InAs changes the low-temperature electronic properties of the InAs surface layer. At higher temperature this difference is not that large as can be seen in Fig. 7(b) due to the increasing contribution of the p-type conductance of the InAs layer.

At $T=300$ K, $R_\square$ of covered InAs is equal to $R_\square$ of bare InAs ($\approx 300\ \Omega$). This indicates that the properties of the holes, which are not frozen-out at room temperature, are not significantly affected by the presence of the InAlAs/InGaAs cap layer.

The magnetic field dependence of the zero-bias resistance R_0 at low temperatures ($T=0.3$ K) differs from the behavior observed for bare p-InAs (for the latter see Fig. 6). R_0 of the covered InAs depends only weakly on the magnetic field and decreases with B. Between $B=0$ T and $B=9$ T, R_0 is decreased by approximately 5%. No Shubnikov–de Haas oscillations are observed, therefore no 2DEG is present in the structure.

Since the Au rings on InAs are not insulated from the InGaAs and InAlAs layers, the measured resistance of the covered p-InAs is limited by the conductivity of the two cap layers. As determined from measurements in Corbino geometry, where the Au rings are evaporated directly on top of InGaAs, the sheet resistance of InGaAs at 4.2 K is determined to be $R_\square\approx 200$ kΩ, which is approximately the value obtained above. Thus $R_\square=195$ kΩ is just a lower limit of the sheet resistance of the covered p-InAs layer system at 4.2 K. The InGaAs cap layer is necessary to protect the InAlAs layer against oxidation. Attempts to replace the InGaAs layer by a layer which is insulating and provides sufficient protection of the InAlAs have not been successful, yet.

To exclude that the increase in resistivity of the covered InAs is due to an artifact during sample preparation, i.e., incomplete removal of the InAlAs/InGaAs cap layers or contact resistance, the following test has been performed. First, Corbino disks on covered InAs were measured (structure B), giving the results discussed above. Then the cap layers have been removed completely. These modified samples have shown the properties of bare p-InAs. For this test, the Au rings served directly as contact pads.

The amount of increase in resistivity depends on the Al content and on the doping level of the InAlAs cap layer. With InAs coated with $In_{0.52}Al_{0.48}As$, the increase in resistivity is only a factor of 2 compared with bare p-InAs. This confirms the expected result (see also calculation shown in Sec. III) that the carrier density in the surface layer depends on the concentration of Al in the InAlAs layer.

V. CONCLUSIONS

A method to reduce the carrier density of the surface inversion layer of p-InAs is presented. Experimental results and band structure calculations are discussed for bare p-type InAs and for p-type InAs coated with InAlAs and InGaAs. The surface inversion layer of p-InAs has an electron concentration $n_{2D}\approx 10^{12}$ cm^{-2}, a mobility $\mu\approx 5000$ cm^2/V s, and a sheet resistance $R_\square\approx 1.1$ kΩ at $T=4.2$ K. If the p-InAs is coated with $In_{0.4}Al_{0.6}As$, no 2DEG exists at the interface between InAs and InAlAs. The sheet resistance of the interface layer is increased up to $R_\square\approx 230$ kΩ at $T=2$ K, which shows that our method of device isolation is well suited for low temperature applications.

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[1] H. Takayanagi and T. Kawakami, Phys. Rev. Lett. **54**, 2449 (1985).
[2] A. W. Kleinsasser and W. J. Gallagher, *Three-Terminal Devices*, in Superconducting Devices, edited by S. T. Ruggiero and D. A. Rudman (Academic, Boston, 1990), p. 325; A. W. Kleinsasser, *Field Effect Devices*, in The New Superconducting Electronics, edited by H. Weinstock and R. W. Ralston (Kluwer Academic, Dordrecht, 1993), p. 249.
[3] A. Kastalsky, ''Hybrid Devices, Particularly Josephson Transistors,'' patent, U.S. No. 5793055 (August 1998); German Patent offices, No. 19649500.8 (submitted, November 1996).
[4] S. G. Lachenmann, A. Kastalsky, A. Förster, D. Uhlisch, K. Neurohr, and Th. Schäpers, J. Appl. Phys. **83**, 8077 (1998).
[5] C. A. Mead and W. G. Sitzer, Phys. Rev. **134**, 713 (1964).
[6] J. N. Walpole and K. W. Nill, J. Appl. Phys. **42**, 5609 (1971).
[7] A. W. Kleinsasser, T. N. Jackson, G. D. Pettit, H. Schmid, J. M. Woodall, and D. P. Kern, Appl. Phys. Lett. **49**, 1741 (1986).
[8] Landolt-Bernstein, *New Series*, edited by O. Madelung, Group III: Crystal

and Solid State Physics, Vol. 22, Semiconductors (Springer, Berlin, 1987).
[9] A. Leuther, Ph.D. thesis. Ber. d. Forschungszentrums, Jülich **Jül-3229**, Germany, 1996.
[10] W. Kohn and L. J. Sham, Phys. Rev. A **140**, 1133 (1965).
[11] W. Mönch, Surf. Sci. **132**, 92 (1983).
[12] I. Friedrich, Diploma thesis, Rheinisch-Westfälische Technische Hochschule, Aachen, Germany, 1997.
[13] S. Tiwari and D. J. Frank, Appl. Phys. Lett. **60**, 630 (1992).
[14] K. Kajiyama, Y. Mizushita, and S. Sakata, Appl. Phys. Lett. **23**, 458 (1973).
[15] O. M. Corbino, Phys. Z. **14**, 561 (1911).
[16] M. Shur, *Physics of Semiconductor Devices* (Prentice Hall, Englewood Cliffs, NJ, 1990).