# Full silicidation process for making $CoSi_2$ on $SiO_2$

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A silicidation process was developed to produce high-quality $CoSi_2$ directly on $SiO_2$, which can be used for metal gates of metal–oxide-semiconductor field-effect transistors (MOSFETs). Normally, the formation of a $CoSi_2$ layer on $SiO_2$ is very difficult because of the requirement for an exact Co/Si thickness ratio. In our process, an additional Si layer was deposited after the first rapid thermal processing (RTP) at 500 °C and selective etching of the unreacted Co. The additional Si layer provided a Si supply for the second RTP at a higher temperature. This method allows the Co layer thickness to be varied over a fairly large range, and in addition, the microstructure of the silicide layer and the $CoSi_2/SiO_2$ interface were substantially improved. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1728299]

As silicon metal–oxide-semiconductor field-effect transistor (MOSFET) devices are scaled below the 100 nm gate-length node, the conventional polysilicon gate faces problems such as high gate resistance, poly-depletion, or boron penetration into the channel. All these limitations can be overcome by using a metal gate. Metal gates can be manufactured by utilizing the damascene/replacement technique, which avoids problems related to high-temperature budget, contamination, and metal etching. However, this increases the complexity of the process. Recently, silicided gates manufactured by full silicidation of polysilicon have been applied to fabricate MOSFETs.[1–4] The fully silicided gate reduces the complexity of the process. Of the silicides, $CoSi_2$ is one of the important materials that has been used as the metal gate for MOSFETs on silicon-on-nothing (SON).[1,2] It has a low resistivity, high thermal stability, and allows scaling to less than 100 nm.

Nevertheless, it is very difficult to achieve high-quality $CoSi_2$ on oxide by using the conventional full silicidation process. The Co/Si ratio is the most important parameter that could affect the $CoSi_2/SiO_2$ quality. The Co thickness, which should be determined from the Co/Si ratio in the targeted silicide phase, must be strictly controlled in proportion to the silicon thickness. A larger amount of Co deposition leads to the formation of a Co-rich silicide layer which has a higher resistivity. On the other hand, the silicon layer cannot be fully silicided if a smaller amount of Co is deposited. The variations of both the silicon and Co thicknesses would cause problems for the $CoSi_2/SiO_2$ structure.

In this letter we present a new full silicidation process to solve the above-mentioned problems, and to improve the $CoSi_2/SiO_2$ interface quality as compared to the conventional silicidation process.

In our first experiments, a standard silicidation process on n-type Si(100) wafers with two-step rapid thermal processing (RTP) was used. After standard silicon cleaning, a 7 nm $SiO_2$ layer was grown by dry oxidation in $O_2$. An amorphous Si ($\alpha$-Si) layer and a Co layer were deposited using a molecular beam epitaxy (MBE) system at room temperature (RT). A 5 nm Si layer was also deposited as a cap on the Co film to protect the Co layer from oxidation. The thickness of the Co was strictly controlled to achieve a Si/Co ratio of 3.64, which is the value required to consume all the $\alpha$-Si layer (including the cap layer) to form $CoSi_2$. The thicknesses of $\alpha$-Si and Co are 122 and 35 nm, respectively. After a first RTP (RTP1) at 540 °C for 45 s in forming gas ($90\%N_2+10\%H_2$) and a selective etching to remove the unreacted Co, a second RTP (RTP2) was performed at 800 °C for 45 s in $N_2$ to form $CoSi_2$. The resulting $CoSi_2$ layer has a thickness of ~147 nm. The sheet resistance is 1.8 Ω/square, corresponding to a resistivity of 26 $\mu\Omega$-cm, which is higher than the normal value for $CoSi_2$ (15–20 $\mu\Omega$-cm).[5] Figure 1 shows a cross-sectional transmission microscope (XTEM) image of the $CoSi_2$ layer on $SiO_2$ of poor quality. Residual Si and voids are observed at the interface, and have also been reported in a full silicidation process with a Ti cap.[2] The x-ray diffraction measurement shows that a small amount of CoSi phase still exists in the silicide layer, which results in a high resistivity of the silicide layer. The silicide layer introduces very large nonuniform stress onto the substrate because of the poor, irregular interface. A high-temperature anneal (RTP2) at 1000 °C eliminated the CoSi phase, but generated an even worse $CoSi_2/SiO_2$ interface.

In order to improve the structure and the layer quality,

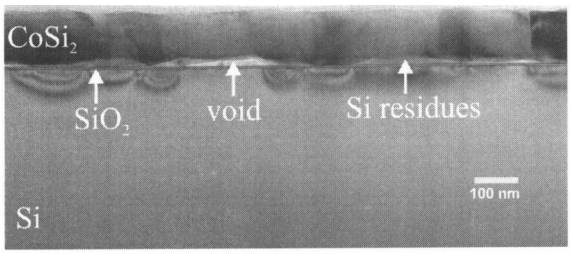


FIG. 1. XTEM image of a $CoSi_2$ layer on $SiO_2$ formed by a conventional full silicidation of a Si layer on $SiO_2$ using two-step RTP. The Co/Si thickness ratio is maintained at 3.64.

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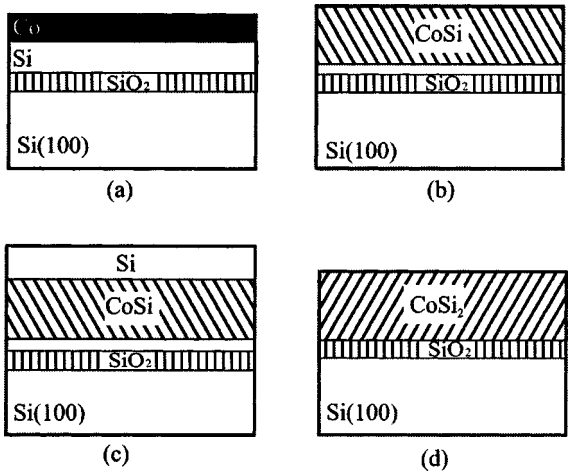


FIG. 2. Schematic drawing of a silicidation process for making $CoSi_2$ on $SiO_2$: (a) deposition of a Si and a Co layer on a $SiO_2$/Si(100) substrate; (b) formation of CoSi by an RTP1 at a lower temperature (500 °C) and a following selective etch to remove the unreacted metal; (c) deposition of an additional Si layer on top of the CoSi layer; (d) formation of $CoSi_2$ by an RTP2 at a higher temperature and a following selective etch to remove the residual Si.

we developed a process as shown in Fig. 2. After growing 10 nm thermal $SiO_2$ on a Si(100) wafer, a 100 nm $\alpha$-Si layer and a 40 or 65 nm Co layer were deposited at RT [Fig. 2(a)]. According to calculations, the Si/Co thickness ratio should be 1.82 to consume all the $\alpha$-Si layer to form CoSi, and 3.64 to form $CoSi_2$.[5,6] In our cases, to form CoSi phase on $SiO_2$, Si is rich for the thinner Co layer (40 nm), while for the thicker one (65 nm) Co is rich. In both cases, the amount of Co is more than the amount required to form $CoSi_2$ phase on $SiO_2$ considering the thickness of Si. In the second step, an RTP1 process was performed at 500 °C for 40 s in a forming gas ambient. After chemical selective etching of the unreacted metal a $CoSi/Co_2Si$ layer was formed with a thin layer of Si between the silicide and $SiO_2$ layers [Fig. 2(b)]. Figure 3 shows the Rutherford backscattering (RBS) spectra of the $CoSi/Co_2Si$ layers formed after RTP1 and selective etching of the unreacted Co for two different Co thicknesses. In the case of the 40 nm Co, only CoSi phase with a thickness of ~70 nm was formed, and the original 100 nm Si layer was not totally consumed with a residual Si thickness of ~32 nm between the CoSi layer and the $SiO_2$ layer. As for the thicker

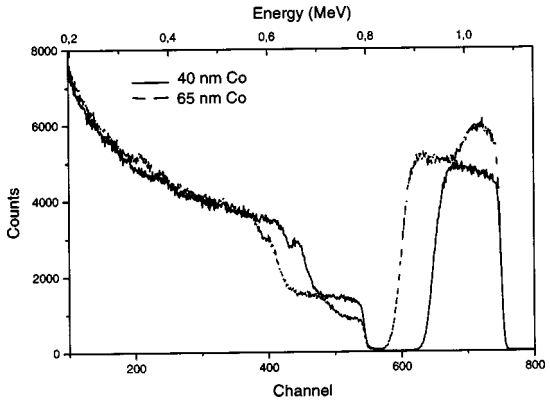


FIG. 3. RBS spectra of silicides formed after RTP1 at 500 °C for 40 s and selective etching with an initial Co layer thickness of 40 and 65 nm on $Si/SiO_2/Si(100)$ structure.

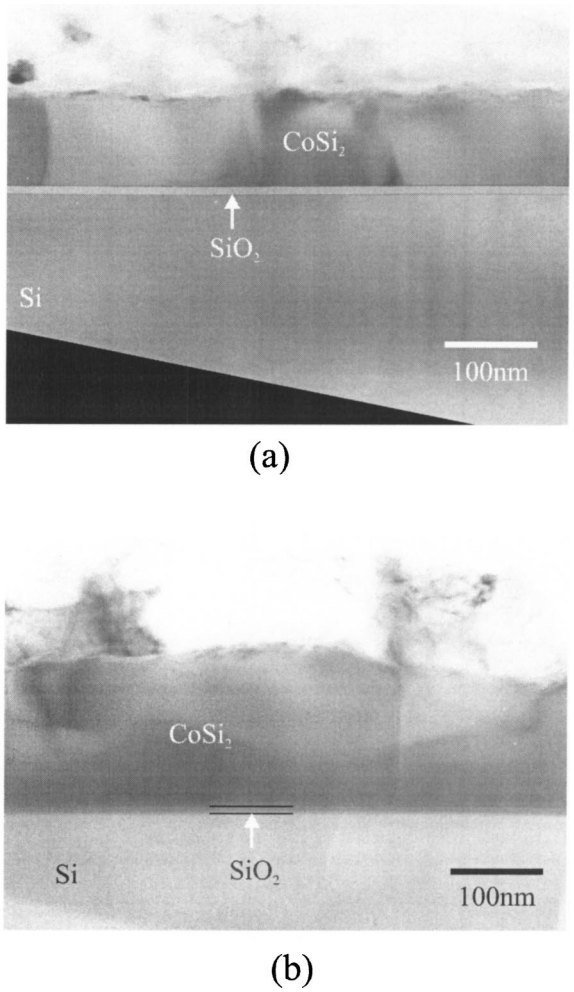


FIG. 4. XTEM images of $CoSi_2/SiO_2/Si(100)$ structure formed using the process shown in Fig. 2 with an initial Co layer thickness of (a) 40 nm; and (b) 65 nm.

Co (65 nm) layer, a silicide layer mainly consisting of $Co_2Si$ phase at the surface and CoSi phase on top of the $SiO_2$ was formed. A residual Si layer with a thickness of ~18 nm still exists between the silicide and $SiO_2$ layers after RTP1. As is already known, the phase transitions during $CoSi_2$ formation are $Co \rightarrow Co_2Si \rightarrow CoSi \rightarrow CoSi_2$.[5] The phase $Co_2Si$ converts to CoSi at lower temperatures, and the last transition from CoSi to $CoSi_2$ occurs at a higher temperature (>550 °C).[5] Therefore, no $CoSi_2$ phase is formed after RTP1. For a thicker (65 nm) Co layer, $Co_2Si$ was formed at a very early stage and then converted to CoSi phase. The dominant diffusion atoms are Si in the phase transition from $Co_2Si$ to CoSi. When the CoSi layer is thick, and Si atoms cannot pass through the CoSi layer to the surface during RTP1, two phases are formed.

In the third step, an additional $\alpha$-Si layer with a thickness of ~250 nm was deposited on top of the silicide layer at RT [Fig. 2(c)]. This provides an additional Si supply for the next reaction to form $CoSi_2$. Finally, an RTP2 at 800 °C was performed for 1 min to form $CoSi_2$ on $SiO_2$. The residual unreacted Si at the surface was selectively etched after RTP2 [Fig. 2(d)].

Figure 4 shows XTEM images after silicidation with an RTP2 at 800 °C for 1 min for samples with an initial Co layer thickness of (a) 40 nm, and (b) 65 nm. With respect to the

conventional silicidation process of Fig. 1, the layer structure was much improved, as is indicated by perfect $CoSi_2/SiO_2$ interfaces without any Si residues and voids in Fig. 4. The roughness of the $CoSi_2$ surface is partly due to the etching of the unreacted silicon after RTP2. The $CoSi_2$ layer thicknesses are 110 and 180 nm for the 40 and 65 nm Co layers, respectively. The sheet resistance was measured as 1.42 $\Omega$/square for the 110 nm $CoSi_2$ layer and 0.85 $\Omega$/square for the 180 nm $CoSi_2$ layer, corresponding to a resistivity of $\sim$15.6 $\mu\Omega$-cm, which is comparable to the value of the single crystalline $CoSi_2$ grown by molecular beam allotaxy.[7] This indicates a high quality of $CoSi_2$ layers without any other phases. The grain size shown in Fig. 4 is as large as 200 nm in the lateral direction. In the following we discuss the various mechanisms.

The transition from CoSi to $CoSi_2$ is a nucleation controlled process.[5] The main moving species in the phase transition from CoSi to $CoSi_2$ are Co atoms. In the conventional silicidation process, Co atoms diffuse only towards the bottom. The high Co diffusion flux leads to the rapid nucleation and growth of large $CoSi_2$ grains near the $SiO_2$ layer. It is well known that layers produced from nucleation reactions are often rough. Due to the rough interface and thickness variations of the silicide layer, in the area where the Si layer is completely consumed, the agglomeration and growth to large $CoSi_2$ grains at the $SiO_2$ surface result in voids formation. On the other hand, in some areas the excess Co atoms near the surface have difficulty in passing the large $CoSi_2$ grains to reach the $SiO_2$ interface during RTP2 at 800 °C for 45 s. As a consequence, residual Si, and Co-rich phases are formed after RTP2 during the conventional silicidation process. Although an enhanced diffusion of Co atoms during a higher temperature RTP2 (e.g., 1000 °C) could eliminate the residual Si and CoSi phase, more voids formed because of the higher agglomeration rate. In the case of our process, during RTP2, Co atoms diffuse both upwards and downwards, and the nucleation of $CoSi_2$ occurs at two interfaces. The Co diffusion flux to the $SiO_2$ is reduced compared to the conventional process, and thus the nucleation and agglomeration rates near the $SiO_2$ layer decrease. The thin Si interlayer between CoSi and $SiO_2$ is consumed very soon before the formation of large $CoSi_2$ grains during RTP2. The excess Co atoms in the middle CoSi layer diffuses towards upwards.

In summary, high-quality $CoSi_2$ layers on $SiO_2$ were formed by a modified silicidation process. After the first RTP process and the selective etching, an additional Si layer was deposited on the surface, and then the second RTP process led to the formation of a $CoSi_2$ layer on $SiO_2$ with a perfect $CoSi_2/SiO_2$ interface. The additional Si layer provided a supply of Si during the second RTP process for the phase transition from CoSi (or other Co-rich phase) to $CoSi_2$. This technique avoids the critical Co/Si thickness ratio requirement in the conventional full silicidation process, and improves the layer and $CoSi_2/SiO_2$ interface quality. It can be used for the formation of full silicided gates for nanometer MOSFETs.

[1] B. Tavel, T. Skotnicki, G. Pares, N. Carriere, M. Rivoire, T. Leverd, C. Julien, J. Torres, and R. Pantel, IEDM Tech. Digest, 825 (2001).
[2] S. Monfray, T. Skotnicki, B. Tavel, Y. Morand, S. Descombes, A. Talbot, D. Dutartre, C. Jenny, P. Mazoyer, R. Palla, F. Leverd, Y. Le Friec, R. Pantel, M. Haond, C. Charbuillet, C. Vizioz, D. Louis, and N. Buffet, IEDM Tech. Digest, 263 (2002).
[3] J. Kedzierski, E. Nowak, T. Kanarsky, Y. Zhang, D. Boyd, R. Carruthers, C. Cabral, R. Amos, C. Lavoie, R. Roy, J. Newbury, E. Sullivan, J. Benedict, P. Saunders, K. Wong, D. Canaperi, M. Krishnan, K.-L. Lee, B. A. Rainey, D. Fried, P. Cottrell, H.-S. Philip Wong, M. Ieong, and W. Haensch, IEDM Tech. Digest, 247 (2002).
[4] Z. Krivokapic, W. Maszara, K. Achutan, P. King, J. Gray, M. Sidorow, E. Zhao, J. Zhang, J. Chan, A. Marathe, and M.-R. Lin, IEDM Tech. Digest, 271 (2002).
[5] K. Maex, Mater. Sci. Eng., R. **11**, 53 (1993).
[6] *Properties of Metal Silicides*, edited by K. Maex and M. van Rossum (INSPEC, The Institution of Electrical Engineers, London, 1995).
[7] S. Mantl, J. Phys. D **31**, 1 (1998).