Fabrication of epitaxial $CoSi_2$ nanowires

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(Received 19 March 2001; accepted for publication 4 June 2001)

We have developed a method for fabricating epitaxial $CoSi_2$ nanowires using only conventional optical lithography and standard silicon processing steps. This method was successfully applied to ultrathin epitaxial $CoSi_2$ layers grown on Si(100) and silicon-on-insulator substrates. A nitride mask induces a stress field near its edges into the $CoSi_2$/Si heterostructure and leads to the separation of the $CoSi_2$ layer in this region during a rapid thermal oxidation step. A subsequent etching step and a second oxidation generate highly homogenous silicide wires with dimensions down to 50 nm. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1390318]

Constantly decreasing feature sizes in silicon nanoelectronics entail advanced requirements for the process technology as well as for the involved materials. As optical lithography reaches its limits at 130 nm, methods to achieve smaller feature sizes receive considerable investigation. Ion-beam projection lithography, *e*-beam projection lithography, x-ray lithography, and deep UV lithography are the most promising candidates to replace the conventional methods although they involve enormous technical difficulties and costs.[1] This encourages the search for alternative and reasonably priced methods for generating nanostructures with the current industrial equipment. The introduction of silicon-on-insulator (SOI) substrates in combination with these methods enables their use for developing modern nanoscale silicon devices. On the metallization side $CoSi_2$ provides excellent properties as a contact and interconnect material due to its low resistivity and high scalability and is well established in silicon technology. With its small lattice mismatch of about -1.2% it can be epitaxially grown on Si(100) substrates, using a number of different techniques.[2–4] The epitaxial silicide provides superior qualities with respect to the polycrystalline material such as the absence of grain boundaries, better film uniformity, higher thermal stability, and improved electrical properties. Nanometric patterning of epitaxial silicides provides a new approach to the future silicon nanoelectronics.[5] However, in addition to the lithography problems, nanopatterning of $CoSi_2$ is difficult because of the lack of appropriate dry etching processes. In this work we report a self-assembly method for fabricating epitaxial $CoSi_2$ nanowires with dimensions down to 50 nm on both Si(100) and SOI substrates using only optical lithography and standard silicon processing steps. This method involves the local oxidation of silicides (LOCOSI).[6,7]

First, we have grown 20–30 nm thick $CoSi_2$ layers on Si(100) by molecular beam allotaxy (MBA).[4] For the SOI material we used bonded wafers separated by the Smartcut® process with an initial silicon top layer thickness of 100 nm. These were thinned down by furnace oxidation and wet etching before introduction into the ultrahigh vacuum (UHV) chamber. MBA produces high quality single-crystalline $CoSi_2$ layers on both substrates. The subsequent patterning process is sketched in Fig. 1. First, we deposited mask layers of 20 nm SiO_2 and about 400 nm Si_3N_4 on top of the $CoSi_2$ by plasma enhanced chemical vapor deposition (PECVD) and patterned these layers along the ⟨110⟩ direction using conventional optical lithography and reactive ion etching (RIE) [Fig. 1(a)]. Due to the intrinsic stress of the nitride, a stress field is induced into the underlying layers which leads to a homogeneous separation of the silicide layer near the edge of the nitride mask during rapid thermal oxidation (RTO) [Fig. 1(b)].[6] This is caused by the stress induced anisotropic diffusion of the Co atoms during the oxidation pro-

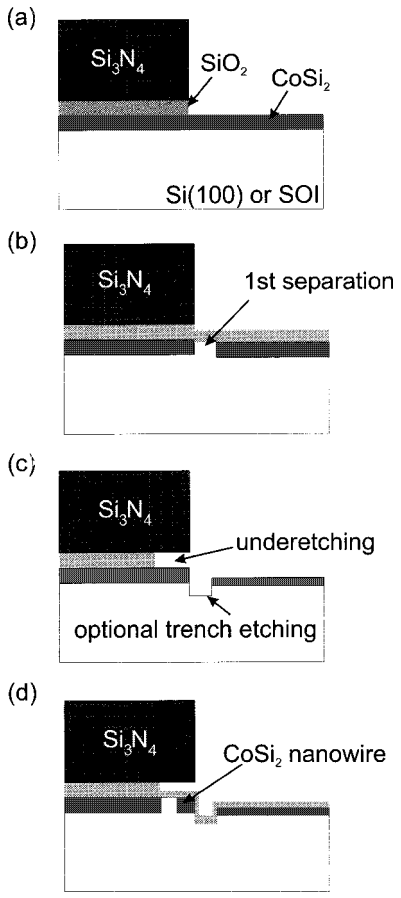

FIG. 1. Process steps of nanowire fabrication: (a) patterning of the LOCOSI mask; (b) separation after first RTO; (c) underetching of the nitride mask with optional trench etching; (d) wire formation during second RTO.

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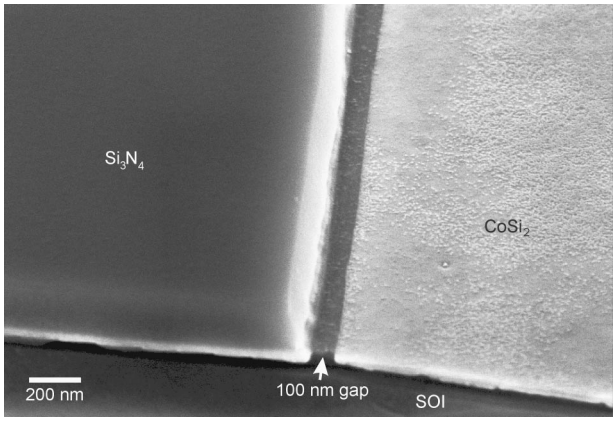

FIG. 2. SEM image of a 100 nm gap in a 24 nm $CoSi_2$ layer on 70 nm SOI after RTO at 950 °C for 1 min in dry O_2.

cess. Additionally, the unprotected part of the silicide is hereby shifted into the substrate, where its thickness and uniformity are maintained. This oxidation step is performed at 950 °C in dry O_2. The gaps created in this manner are of dimensions between 50 and 130 nm depending on the oxidation time, silicide thickness, and substrate type. For a 21 nm $CoSi_2$ layer on Si(100) oxidation for 1 min produces a 50 nm gap. For a 24 nm layer on 70 nm SOI an oxidation time of 1 min yields a 100 nm gap. A scanning electron microscopy (SEM) image in Fig. 2 shows the highly uniform separation of a 24 nm $CoSi_2$ layer on SOI after removing the oxide which was generated on top during the oxidation. The use of SOI substrates in this step offers new processing opportunities due to the modified stress and will be reported elsewhere.

In the next step, wet etching in buffered HF was used to selectively etch the SiO_2 underneath the nitride mask [Fig. 1(c)]. In this way the stress field of the nitride mask is shifted underneath it. The unprotected silicide layer is also etched by this process step and thereby partly or completely removed, depending on its thickness and the underetching time. For 30 nm $CoSi_2$ on a Si(100) substrate etching of a trench in the gap was necessary to modify the stress conditions in the regions near the edge of the mask. This was performed by RIE. A second RTO step produces narrow homogeneous $CoSi_2$ wires resulting from the same effects that lead to the first separation [Fig. 1(d)].

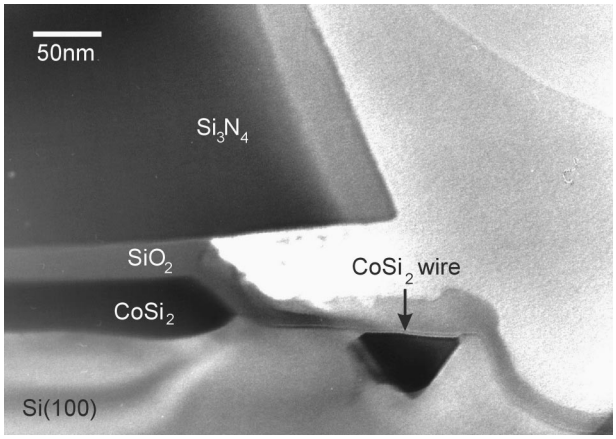

FIG. 3. XTEM micrograph of a 70 nm wide $CoSi_2$ wire on Si(100).

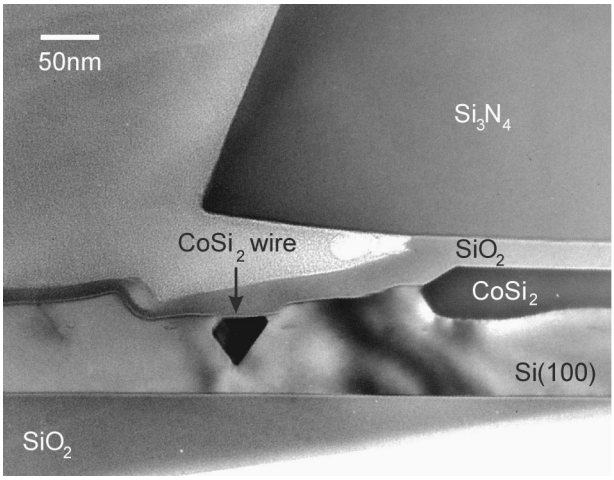

FIG. 4. XTEM micrograph of a 50 nm wide $CoSi_2$ wire on SOI.

Figure 3 shows a TEM image of a nanowire ~70 nm wide from a 30 nm $CoSi_2$ layer. The first oxidation was performed for 3 min and the second oxidation for 5 min at 950 °C in dry O_2. The underetching width was ~200 nm and the trench depth was about 70 nm. Its triangular shape results from the formation of the energetically favorable ⟨111⟩ facets on the edges of the wire.

Figure 4 shows a TEM image of a 50 nm wire on a 70 nm SOI substrate. Here the first and second oxidations were performed at 950 °C in dry O_2 for 1 and 3 min, respectively, and the underetching width was ~200 nm. No trench etching was necessary for this process. The Si hump on the left-hand side of the wire displays the separation area from the first oxidation step.

The successful generation and the width of the resulting wires are determined by an interplay of many parameters such as the thickness of the initial $CoSi_2$ layer, oxidation times, underetching, and trench etching. The difference between SOI compared to conventional substrates arises due to the different stress conditions. The width of the wire is predominantly controlled by the oxidation times, the silicide thickness, and the underetching width. There appears to be a minimum underetching width for a certain silicide thickness to get a full separation, determining also a minimum width of

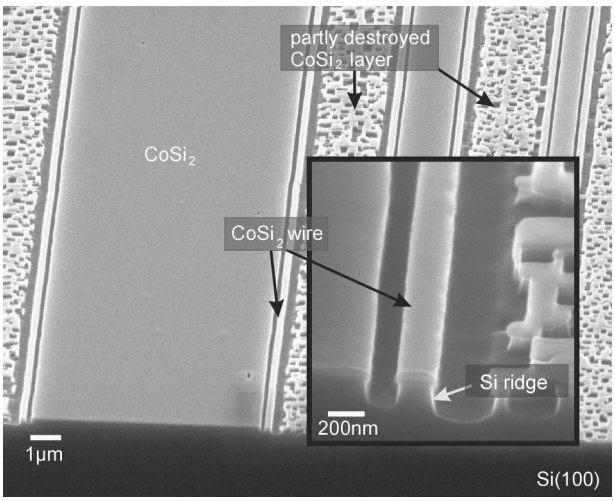

FIG. 5. SEM images of silicon nanoridges fabricated by RIE using the $CoSi_2$ nanowires as an etching mask.

the wire. Thinner silicide results in narrower wires. A slightly greater underetching than the minimum width has no significant influence on the wire thickness. First, the separation gap increases keeping a constant wire thickness. Further etching increases the wire width. For the 30 nm $CoSi_2$ layers a trench with a minimum depth of about 15 nm was also needed for a full separation. Deeper trench etching has no influence on the wire width. This behavior produces an uncritical parameter window for the etching steps involved and leads to the observed high reproducibility of this process.

Using 21 nm $CoSi_2$ on a Si(100) substrate also requires no trench etching as in the SOI case. The silicide thickness seems to have a profound influence on the stress conditions in the second oxidation step. This is not surprising, considering the high lattice mismatch stresses the epitaxial $CoSi_2$ created in the substrate.

For further processing and to investigate the uniformity of the wires, the nitride was selectively removed by wet etching. The SiO_2 was then removed by HF. Presently, these nanowires were used as an etching mask for RIE to etch highly uniform silicon nanoridges. Figure 5 shows SEM images of these ridges produced by using 200 nm wires as an etching mask. These wires were generated using a 30 nm $CoSi_2$ layer performing 3 min for the first and 5 min for the second oxidation at 950 °C in dry O_2 with an underetching width of ~350 nm between and an initial trench of about 20 nm in depths. A further oxidation step followed by wet etching can reduce the width of the wire/ridge-structure significantly, maintaining the wire quality.

In conclusion we have investigated a method for fabrication of epitaxial $CoSi_2$ nanowires on conventional and SOI substrates using a two step local oxidation process. Only conventional optical lithography is involved to achieve highly uniform wires as narrow as 50 nm. These wires were used as an etching mask to etch highly uniform silicon nanoridges. Currently we are investigating their properties concerning resistivity, process stability, and potential use for devices.

The authors would like to thank H.-P. Bochem for the SEM micrographs.

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