High Performance $Si/Si_{1-x}Ge_x$ Resonant Tunneling Diodes

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***Abstract*—Resonant tunneling diodes (RTDs) with strained i–$Si_{0.4}Ge_{0.6}$ potential barriers and a strained i–Si quantum well, all on a relaxed $Si_{0.8}Ge_{0.2}$ virtual substrate were successfully grown by ultra high vacuum compatible chemical vapor deposition and fabricated using standard Si processing methods. A large peak to valley current ratio of 2.9 and a peak current density of 4.3 kA/cm^2 at room temperature were recorded from pulsed and continuous dc current-voltage measurements, the highest reported values to date for $Si/Si_{1-x}Ge_x$ RTDs. These dc figures of merit and material system render such structures suitable and highly compatible with present high speed and low power $Si/Si_{1-x}Ge_x$ heterojunction field effect transistor based integrated circuits.**

***Index Terms*—Germanium, resonant tunneling diodes, silicon, strain.**

I. Introduction

RESONANT tunneling diodes (RTDs) [1] are promising band gap engineered heterostructures that can operate over the wide temperature range of commercial integrated circuits (ICs), with reproducible and reliable characteristics comparable to that of current transistor technologies [2]. These quantum devices possess a distinctive negative differential conductance (NDC) feature in its current–voltage (I–V) trace that can be exploited for various electronic circuit functions [2], [3]. Large scale integration of RTDs with heterojunction field effect transistors (HFETs) have been demonstrated in III–V compound semiconductors [2] [3]. Such a hybrid on-chip system is proven to reduce component count while simultaneously achieving low power dissipation and high speed in memory and logic circuit applications.

Since the microelectronics industry evolves around Si complementary metal-oxide-semiconductor (CMOS) technology, it is of great interest if these RTDs can be realized on a compatible Group IV material system, in particular using $Si/Si_{1-x}Ge_x$. Unfortunately, such attempts have been less than successful due to a lack of high performance Si-based RTDs. At present, the best room temperature dc figures of merit that have been recorded for double barrier single well $Si/Si_{1-x}Ge_x$ electron RTDs are a peak current density (J_P) of 5.0 kA/cm^2 [4] and a peak to valley current ratio (PVCR) of 1.2 [5].

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Even more impressive dc characteristics have been reported for Group IV Esaki diodes, e.g., $J_P = 8.0$ kA/cm^2 with PVCR $= 5.5$ in a $Si/Si_{1-x}Ge_x$ p$^+$-i–n$^+$ interband RTD [6] and $J_P =$ 47 kA/cm^2 with PVCR $= 1.3$ for an all Si-tunnel diode [7]. However, there are potentially some technological difficulties associated with the incorporation of such devices into standard CMOS ICs. For instance, these structures can only be formed by low temperature molecular beam epitaxy and require a very tight control of a precise delta-doped epilayer [7]. Post-growth thermal annealing at a specific temperature is then necessary for dopant activation. The thermal budget for current CMOS ICs will result in problems with dopant segregation and diffusion that will significantly reduce the dc performance [7].

In this letter, a $Si/Si_{1-x}Ge_x$ RTD with strained i– $Si_{1-x}Ge_x$ potential barriers and a strained i–Si quantum well, all grown on a relaxed $Si_{1-y}Ge_y$ virtual substrate where $x > y$, is proposed and demonstrated. Vastly improved dc figures of merit at room temperature can be observed. Details on the wafer structure, growth, sample fabrication, and experimental dc I–V characteristics are presented. Such a band gap engineered device can potentially be tailored for compatibility with commercially available $Si/Si_{1-x}Ge_x$ HFETs (e.g., from DaimlerChrysler and AmberWave Systems Corporation).

II. Device Structure, Growth, and Fabrication

In the $Si/Si_{1-x}Ge_x$ material system, the heterojunction conduction energy band gap height is expected to increase if the i–$Si_{1-x}Ge_x$ epilayer on a relaxed $Si_{1-y}Ge_y$ buffer is compressively strained, i.e., when $x > y$ [8]. Based on this fact, a RTD with improved dc performance should be realized by adopting strained i–$Si_{1-x}Ge_x$ alloy as potential barriers, instead of the conventional unstrained approach i.e., $x = y$ (Fig. 1) [5]. (Although the effective energy gap seen by the incident tunneling electrons is much higher if n–Si replaces the n–$Si_{1-y}Ge_y$ emitter and collector electrodes, this approach cannot be feasible due to the limited critical thickness of strained Si on a relaxed $Si_{1-y}Ge_y$ virtual substrate.)

Material for the devices was obtained commercially (from DERA Malvern, UK). Wafers were grown in a cold wall ultra high vacuum (UHV) compatible chemical vapor deposition (CVD) system. SiH_4 and GeH_4 gases in a H_2 carrier are employed to produce the $Si_{1-x}Ge_x$ alloy whereas AsH_4 is used for the n–doped electrodes. Deposition commenced with the formation of a 3 μm n–$Si_{1-y}Ge_y$ strain relaxation buffer, graded from $y = 0$ to 0.2, on a (100) n-type Si substrate. Next, a 0.9 μm thick n–$Si_{0.8}Ge_{0.2}$ collector electrode heavily doped with As up to 3×10^{18} cm^{-3} was grown. The CVD was then

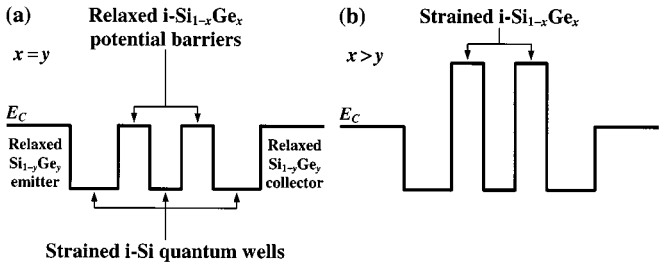

Fig. 1. Schematic conduction band diagram for a Si/Si$_{1-x}$Ge$_x$ RTD with (a) unstrained ($x = y$) and (b) strained ($x > y$) Si$_{1-x}$Ge$_x$ alloy potential barriers on a relaxed Si$_{1-y}$Ge$_y$ virtual substrate (assuming a nonequilibrium flat band approximation i.e., electrostatic effects are neglected).

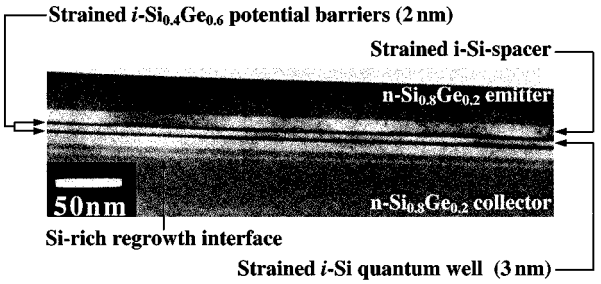

Fig. 2. High resolution cross-sectional TEM micrograph of the strained Si/Si$_{0.4}$Ge$_{0.6}$ RTD wafer grown on a relaxed Si$_{0.8}$Ge$_{0.2}$ virtual substrate.

interrupted in order to remove excess As on the surface by an *ex situ* modified RCA clean [9]. This step was necessary to circumvent the common problem of dopant segregation and subsequent upward carrier diffusion in CVD produced materials [10]. After this process, the wafer was returned to the growth chamber and the remaining layers were deposited: 10 nm i–Si$_{0.8}$Ge$_{0.2}$ buffer, 10 nm strained i–Si spacer, 2 nm i–Si$_{1-x}$Ge$_x$ potential barrier, 3 nm strained i–Si quantum well, 2 nm i–Si$_{1-x}$Ge$_x$ potential barrier, 10 nm strained i–Si spacer, 50 nm n–Si$_{0.8}$Ge$_{0.2}$ emitter electrode and a thin 4 nm n–Si cap (both of these top regions doped with As up to 3×10^{18} cm^{-3}). Two wafers, each with a Ge concentration $x = 0.2$ and 0.6 in the tunnel barriers, unstrained and strained, respectively, were grown.

High resolution cross sectional transmission electron microscope (TEM) images from different parts of the four inch wafer indicate that the strained i–Si$_{0.4}$Ge$_{0.6}$ potential barriers and strained i–Si quantum well appeared to be extremely flat, without any noticeable threading dislocation (Fig. 2). Such micrographs demonstrate that ability of CVD in producing good quality Si/Si$_{1-x}$Ge$_x$ epilayers. Also evident is the Si-rich regrowth interface [9], a faint but visible line between the lower tunnel junction and the bottom n–Si$_{0.8}$Ge$_{0.2}$ collector electrode. Previous research suggests that this region hardly affected the carrier mobility or the quantum mechanical resonant tunneling of electrons [4], [9].

Two-terminal devices were fabricated by standard processing techniques. Various sized square tunnel junction mesas were defined by reactive ion etching (in a CHF_3 and H_2 plasma mixture). Au ohmic contacts with 1% Sb dopants were then deposited and annealed (300 s at 150 °C and 400 °C for the emitter and collector, respectively).

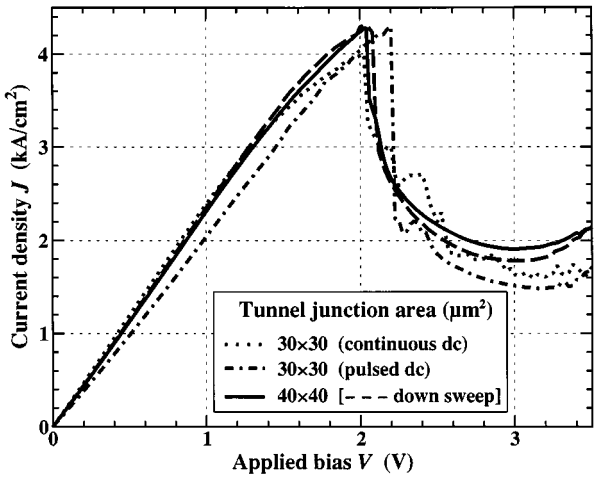

Fig. 3. Typical two-terminal continuous and pulsed dc J–V characteristics for a 30×30 μm^2 and 40×40 μm^2 lateral tunnel junction area strained Si$_{0.4}$Ge$_{0.6}$ potential barrier RTD at room temperature. (Samples biased with respect to the collector while the emitter remained grounded.)

III. Experimental Results

Pulsed two-terminal dc I–V characteristics at 1 : 100 mark space ratio were performed on the RTDs at room temperature ($T = 298$ K). Similar dc behavior can also be obtained by continuous voltage sweeps, as experimentally measured (Fig. 3). However, the former technique was adopted to prevent these devices from shorting out as localized heating effects often caused the lightly annealed shallow emitter metal spiking through the thin 2 nm Si$_{1-x}$Ge$_x$ barriers. Samples were biased with respect to the collector ohmic contact whilst the emitter electrode remained grounded.

Clear NDC on the I–V traces for the RTD with strained i–Si$_{0.4}$Ge$_{0.6}$ potential barriers were observed in numerous samples (Fig. 3). In addition, I was determined to scale consistently with the lateral tunnel junction area and also independent of the bias direction, as indicated by the current density J versus applied voltage V plot. Representative characteristics for different sized devices in the positive regime are depicted, e.g., 30×30 μm^2 and 40×40 μm^2 (Fig. 3). Similar behavior was observed in the negative domain. These direct probed RTDs could not be biased too far beyond the valley point as the emitter ohmic contact alloy tended to diffuse through the tunnel barriers, thus destroying these samples. Devices with smaller dimensions, hence less tunneling current, and a reduced voltage operation range should solve this problem. Lower peak voltages have been successfully demonstrated on a separate wafer designed for low power memory applications, with more As dopants in the emitter and collector electrodes i.e., 1×10^{19} cm^{-3} and graded i–Si$_{1-x}$Ge$_x$ spacers [11]. Near superposition of the two-terminal J–V traces also indicates negligible extrinsic ohmic contact resistance. Moreover, it also implies good material quality, with minimal defect density and threading dislocation in such relatively large samples, as confirmed by the TEM micrographs (Fig. 2).

On the other hand, this NDC feature did not occur in the RTD with unstrained Si$_{0.8}$Ge$_{0.2}$ alloy barriers. Since both wafers were nominally identical apart from the Ge composition

within the tunnel barriers, this result implies that the strain in the i–$Si_{1-x}Ge_x$ layer effectively increases the conduction band gap as predicted theoretically [8], producing a better defined quasibound quantum well state and hence, the enhanced resonant tunneling of electrons [1]. This conclusion can be further supported by the large measured dc figures of merit e.g., $J_P = 4.3$ kA/cm^2 and PVCR $= 2.9$ (Fig. 3), the highest recorded to date for any Si/$Si_{1-x}Ge_x$ RTD. These values are closer to those required for applications such as logic elements than previous reports of $J_P = 0.4$ kA/cm^2 and PVCR $= 1.2$ at room temperature in devices from a different wafer structure and composition, with relaxed but thicker 7.5 nm $Si_{0.7}Ge_{0.3}$ tunnel barriers on matched virtual substrate [5].

An interesting feature in the dc I–V trace is the absence of any threshold voltage before the onset of current flow (Fig. 3). Such a characteristic suggests that the Fermi energy on both outer sides of the $Si_{0.4}Ge_{0.6}$ potential barriers is matched, within kT, with the lowest position in the quasibound quantum well subband (whereby k and T are the Boltzmann constant and temperature, respectively) [4], [5]. Further details on this trait and the resonant electron tunneling process in such a Si/$Si_{1-x}Ge_x$ RTD have been discussed and published elsewhere [4]. In this present work, shallow ohmic contacts were successfully realized compared to the nonannealed Schottky ones employed previously [4]. Consequently, the improvement in the PVCR can be attributed to more efficient injection of tunneling charge carriers and also less nonresonant current components from thermionic emission and hot electron effects.

IV. Conclusion

High dc performance resonant tunneling diodes with strained $Si_{0.4}Ge_{0.6}$ potential barriers and a strained Si quantum well on a relaxed $Si_{0.8}Ge_{0.2}$ virtual substrate were successfully grown by UHV compatible CVD and fabricated using standard Si processing methods. A room temperature PVCR of 2.9 and J_P of 4.3 kA/cm^2 were measured. Both these dc figures of merit are the highest recorded values published to date in such heterostructures and allow large scale on-chip integration with current Si/$Si_{1-x}Ge_x$ HFETs for low power memory and high speed logic circuits.

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