A Vertical Resonant Tunneling Transistor for Application in Digital Logic Circuits

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***Abstract*—A vertical resonant tunneling transistor (VRTT) has been developed, its properties and its application in digital logic circuits based on the monostable-bistable transition logic element (MOBILE) principle are described. The device consists of a small mesa resonant tunneling diode (RTD) in the GaAs/AlAs material system surrounded by a Schottky gate. We obtain low peak voltages using InGaAs in the quantum well and the devices show an excellent peak current control by means of an applied gate voltage. A self latching inverter circuit has been fabricated using two VRTTs and the switching functionality was demonstrated at low frequencies.**

***Index Terms*—Monostable-bistable transition logic element (MOBILE), monostable-to-bistable transition, resonant tunneling diode (RTD), resonant tunneling transistor.**

I. Introduction

In recent years, several new memory and logic circuits based on resonant tunneling diodes (RTDs) have been reported [1]–[3]. Compared to conventional devices, RTDs take advantage of their higher speed of operation, lower power dissipation, and reduced circuit complexity due to higher functionality.

Most of the applications make use of the monostable-bistable transition logic element (MOBILE) operation principle [4] that is described in detail below. This logic gate employs a monostable-to-bistable transition of a circuit which consists of two RTDs connected in series. A small difference between the peak currents of the RTDs determines the state of the circuit after the transition.

There are different approaches to gain control of the RTDs peak current. On the one hand, conventional transistors can be integrated within the circuit [5], [6], and on the other hand, three-terminal resonant tunneling devices manipulating the peak current by means of a Schottky gate [7]–[12] or a pn-junction [4] have been fabricated.

The concept of a three-terminal resonant tunneling device has some serious advantages over the integration of RTDs and conventional transistors like heterostructure field effect transistors (HFETs). The HFET and RTD characteristics have to match, e.g., the transistor current with respect to the RTD peak current. Thus, the transistors have to be designed in a narrow window of device properties. In a three-terminal RTD, the matching between RTD and FET is inherently fulfilled. Furthermore, this concept offers the potential for reaching a reduced complexity.

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In this paper, we report on the fabrication of a vertical resonant tunneling transistor (VRTT) with low peak voltage and good peak current control by means of a Schottky gate. The asymmetric behavior of the current-voltage (I–V) characteristics is analyzed and the transistors are characterized with respect to their peak voltage, peak-to-valley ratio (PVR), peak current density, and gate function. We demonstrate the switching functionality of a self latching inverter circuit consisting of two VRTTs.

II. Device Fabrication

A. Layer Structure

The epitaxial structure used to fabricate the VRTT device was grown by molecular beam epitaxy (MBE) on semi-insulating (100)-orientated GaAs substrate. Fig. 1 shows a cross-sectional view of the layer structure which can be subdivided into the actual RTD layer structure and two adjacent electron reservoirs.

The RTD layer structure is nominally undoped and consists of a 5-nm wide $In_{0.1}Ga_{0.9}As$ quantum well embedded in two AlAs barriers of 1.7 nm width. $In_{0.1}Ga_{0.9}As$ instead of GaAs was used to decrease the peak voltage.

This double barrier quantum well structure (DBQW) is symmetrically surrounded by the following layer sequence: 7 nm GaAs (nominally undoped), 200 nm n^--GaAs ($n^- = 5 \cdot 10^{16}$ cm^{-3}) and finally 500 nm n^+-GaAs ($n^+ = 4 \cdot 10^{18}$ cm^{-3}). The nominally undoped GaAs layers serve as spacer layers between the n-doped electron reservoirs and the nominally undoped DBQW structure in order to reduce dopant diffusion and therefore improve the interface quality. The low-doped n^--GaAs layers are introduced to achieve enhanced control of the device current. According to Poisson's equation the depletion region d of the Schottky gate

$$d = \sqrt{\frac{2\epsilon\epsilon_0(U_D - U_G)}{en^-}} \tag{1}$$

depends on the Schottky barrier height U_D, the gate voltage U_G, and the doping concentration n^- of the adjacent semiconductor layer. As a consequence, the effective area of the mesa and therefore the current can be controlled efficiently by the gate voltage particularly at low doping concentrations n^-. Finally, the high-doped n^+-GaAs layers serve as contact layers for the ohmic contacts that are processed later on.

B. Fabrication Process

The VRTT device consists of a small square mesa diode surrounded by a Schottky type depletion gate which is structured

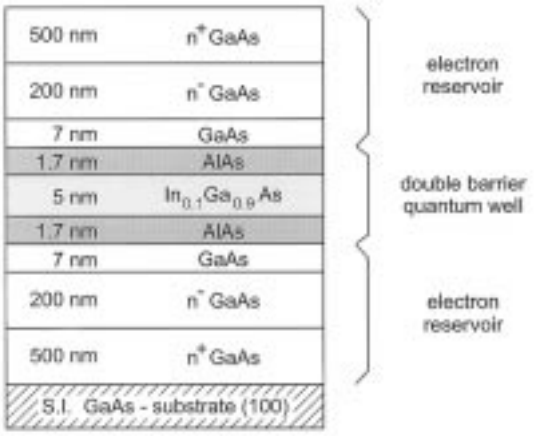

Fig. 1. Layer structure of the vertical resonant tunneling transistor. The doping concentrations are $n^- = 5 \cdot 10^{16}$ cm^{-3} and $n^+ = 4 \cdot 10^{18}$ cm^{-3}.

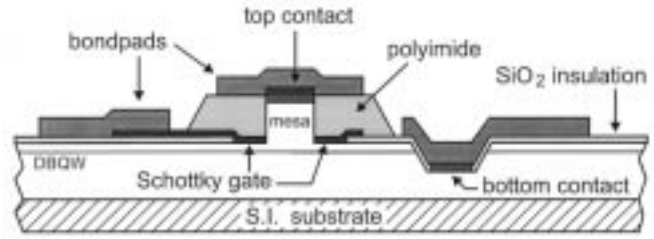

Fig. 2. Schematic view of the completely processed device.

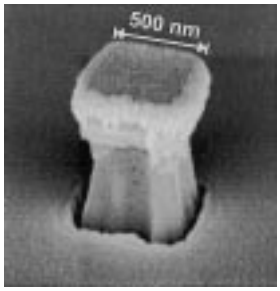

Fig. 3. Scanning electron micrograph of a mesa with 500 nm edge length and surrounding Schottky gate metallization. The reactive ion etching process leads to an undercut of the mesa sidewalls that allows a self-aligned evaporation of the gate metallization.

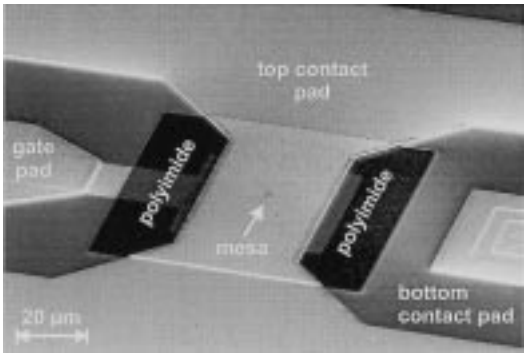

Fig. 4. Scanning electron micrograph of a completely processed resonant tunneling transistor.

in a self-aligned evaporation process. Fig. 2 shows a schematic view of the device.

In the first process step electron beam lithography and lift-off technique were applied to fabricate small ohmic top contacts with an edge length between 0.5 and 2.0 μm using a Ni/AuGe/Ni/Ti metallization. The final Ti layer served as an etch mask for the following mesa preparation in a reactive ion etching (RIE) process with a H_2/CH_4 plasma. After this process step the mesas had an overall heigth of 660 nm. Thus, the double barrier structure lies 50 nm underneath the semiconductor surface.

Fig. 3 shows a scanning electron micrograph of such a mesa with an edge length of 500 nm and the surrounding Schottky gate metallization. One can see that the plasma process results in an undercut of the mesa sidewalls which allows a self-aligned evaporation of the gate metallization. We attribute this behavior to the special geometry during the plasma etching process. The square sample with an edge length of 1 cm was placed on an insulating quartz plate. Hence, the n-doped sample forms an equipotential surface in the plasma and represents the counterelectrode to the reactor electrode. Compared to the size of the plasma reactor electrode the sample size is very small. This leads to a more isotropic distribution of the electric field on the sample surface which results in the observed undercut of the mesa sidewalls.

After the H_2/CH_4 RIE process the sample was exposed to an O_2 plasma to remove polymers that may cover the ohmic top contact. In order to provide a bottom ohmic contact for the RTDs a wet chemical etching process was performed using a H_2SO_4: H_2O_2: H_2O etch to expose the substrate sided n^+-GaAs layer. After that a Ni/AuGe/Ni/Au metallization for the ohmic bottom contact was evaporated. The ohmic contacts were annealed in a RTA (rapid thermal annealing) oven at 530 °C for 2 min.

In the next process step, the sample was covered with a SiO_2 layer of 80 nm thickness. This SiO_2 layer served as an insulation layer for the bondpads that were processed later on. Furthermore, it was used to define the area where the gate metallization has direct contact to the semiconductor surface. Therefore the SiO_2 was removed wet chemically in a 30-μm square window around each mesa using a $(NH_4)HF_2$ buffered hydrofluoric acid solution. This solution etches SiO_2 only but does not attack photoresist, GaAs or any metallization.

After the preparation of the SiO_2 layer a Ti/Pt/Au metallization for the Schottky gate was evaporated in a self-aligned process using conventional optical lithography and lift-off technique. The undercut of the mesa sidewalls successfully prevents a shortcut between the mesa top contact and the gate metallization during the evaporation. The gate provides a controllable lateral confinement of the active region of the device due to its depletion region.

In order to enable an electric contact to the top of the mesa via bondpads the sample was covered with an polyimide layer that was structured by optical lithography forming 90-μm squares around each mesa. The polyimide was partially etched back in a O_2/CF_4 plasma to reexpose the top contacts. Finally, the bondpads for the top, the bottom and the gate contact were evaporated using a Ti/Pt/Au metallization. Fig. 4 shows a scanning electron micrograph of the completely processed device.

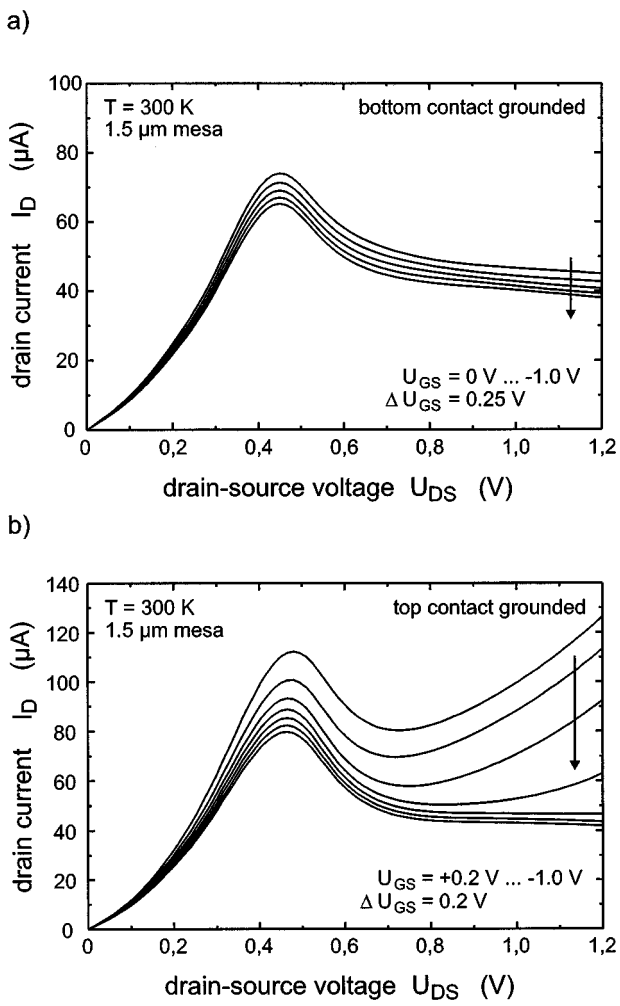

Fig. 5. $I-V$ characteristics of the VRTT device for different bias voltage configurations. (a) Bottom contact is grounded, the gate voltage is varied from 0 V to -1.0 V in steps of 0.25 V. (b) Top contact is grounded, the gate voltage is varied from +0.2 V to -1.0 V in steps of 0.2 V.

III. Device Properties

In the following section, typical properties of the VRTT device are presented with special regard to possible applications in digital logic circuits.

Although the device is based on a completely symmetric layer structure the $I-V$ characteristics exhibits an asymmetric behavior with respect to the bias voltage polarity. In Fig. 5(a), a positive bias voltage is applied to the top contact related to the grounded bottom contact. In Fig. 5(b), the top contact is grounded and a positive bias voltage is applied to the bottom contact. Regardless of the specific configuration the $I-V$ characteristics shows a clear resonance peak followed by a region of negative differential resistance (NDR). The drain current can be controlled efficiently by the gate voltage. In Fig. 5(a) however, the drain current shows a saturation-like behavior at higher bias voltages whereas in Fig. 5(b) no saturation was observed.

We have already shown in the past [12] that these effects are related to the asymmetric geometry of the device itself. Calculations using the classical device simulation software SILVACO [13] prove that the different bias voltage configurations have different potential and electric field distributions which result in different $I-V$ characteristics. In the configuration of Fig. 5(a) in which the bottom contact is grounded the mesa channel is more and more depleted with raising bias voltage and thus, the effective cross section of the mesa decreases. This compensates for the effect of increasing electric field parallel to the current direction leading to the observed saturation in the drain current. In the configuration of Fig. 5(b) the top contact is grounded and the simulation shows that in this situation the mesa channel is less depleted with raising bias voltage. Thus, the effective cross section of the mesa increases and the drain current raises without any saturation. Concerning a possible application in digital switching units the $I-V$ characteristics in Fig. 5(b) deserves special attention as it exhibits the behavior of a RTD with controllable peak current. Gate voltages in the range from U_{GS} = +0.2 V to U_{GS} = -1.0 V have been applied. Thus, also positive gate voltages can be used to control the peak current. The corresponding gate leakage current was less than 3 nA and hence five orders of magnitude lower than the measured drain current. In the specific range of gate voltages the peak current could be reduced from $I_P = 112\mu$A at $U_{GS} = +0.2$ V to $I_P = 80\,\mu$A at U_{GS} = -1.0 V. The peak voltage of $U_P = 0.47$ V scarcely depends on the applied gate voltage. Peak-to-valley ratios between 1.4 and 2 with a peak current density of 6600 A/cm^2 were obtained. In summary, the gate voltage can control the peak current efficiently. Thus, the device is suitable for an application in digital switching units operating at room temperature.

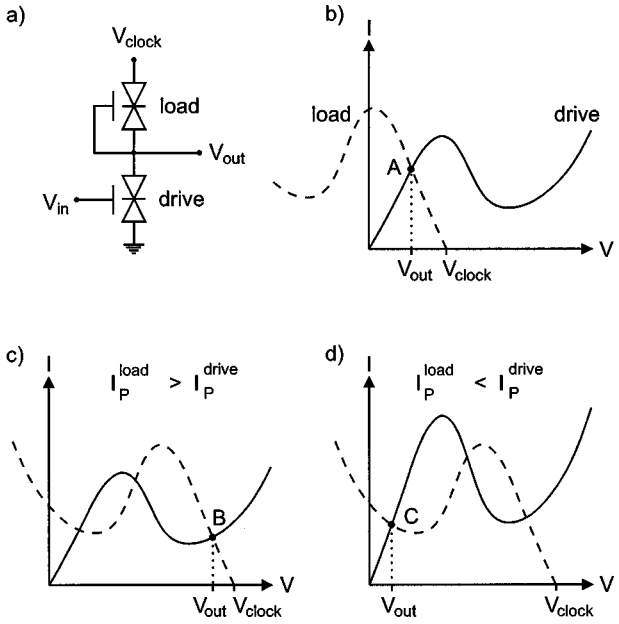

Fig. 6. Loadline analysis of the MOBILE circuit. The solid and the dashed line show the $I-V$ characteristics of the drive and the load VRTT, respectively. The stable points of the circuit (A-C) are marked with a dot. (a) Circuit configuration of the VRTT MOBILE. (b) $V_{\rm clock} < 2V_P$. (c) $V_{\rm clock} > 2V_P$ and $I_P^{load} > I_P^{drive}$. (d) $V_{\rm clock} > 2V_P$ and $I_P^{load} < I_P^{drive}$.

IV. Operation Principle of VRTT Mobile

Two resonant tunneling transistors are connected in series [Fig. 6(a)] and are driven by an oscillating clock voltage ($V_{\rm clock}$). As long as the clock voltage is less than twice the peak voltage ($2V_P$) there is only one stable point [A in Fig. 6(b)].

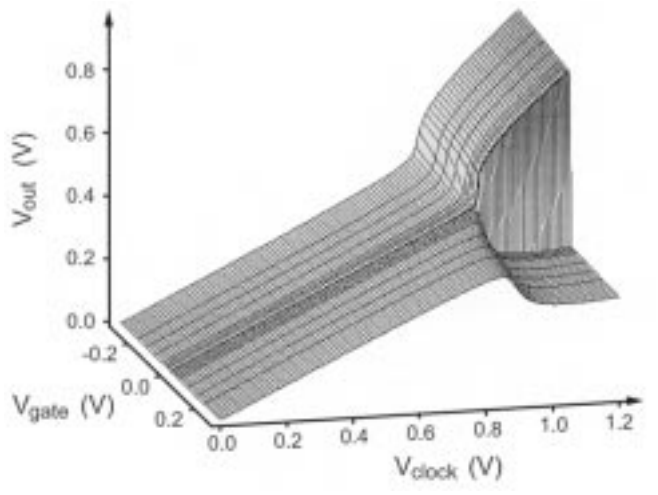

Fig. 7. Measured switching characteristics (output voltage versus clock voltage) of the MOBILE circuit for different gate voltages. There is a very sharp transition between the two output states when the clock voltage reaches $2V_P \approx 0.9$ V.

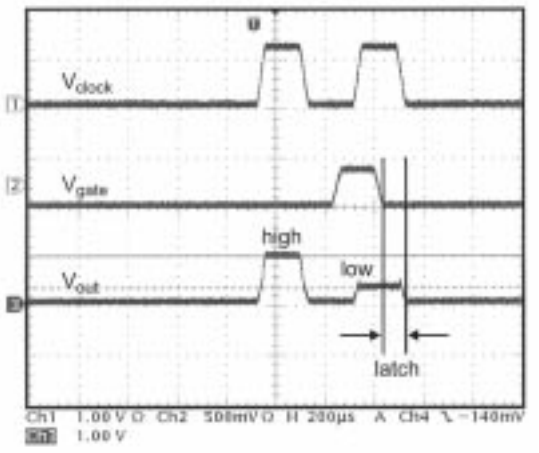

Fig. 8. Oscilloscope picture of clock voltage, gate voltage, and output voltage signals demonstrating the self latching inverter operation of the MOBILE circuit.

If the clock voltage exceeds $2V_P$ this stable point splits into two stable points (B and C in Fig. 6(c) and (d), respectively) representing the two logic states of the MOBILE. After this monostable-to-bistable transition the state of the circuit is determined by a small difference in the peak currents of the load and the drive VRTT. If the peak current of the drive VRTT is smaller than the peak current of the load VRTT the circuit switches to the stable point B corresponding to a high output voltage [Fig. 6(c)]. A greater peak current in the drive VRTT results in the stable point C with low output voltage [Fig. 6(d)]. Thus, the state of the circuit is determined by the magnitude of the peak current of the drive VRTT which can be controlled by the gate voltage.

V. Inverter Operation

The operation of a self latching inverter circuit based on the MOBILE principle was tested. Two VRTTs with square mesas of 2 μm edge length were used and the circuit [Fig. 6(a)] was driven by a clock voltage of $V_{\text{clock}} = 1.2$ V. A gate voltage was applied to the drive VRTT in order to induce the output voltage transition. Fig. 7 shows the measured switching characteristics (output voltage versus clock voltage) of the MOBILE for gate voltages in the range from $V_{\text{gate}} = +0.3$ V to $V_{\text{gate}} = -0.3$ V. When the clock voltage reaches $2V_P \approx 0.9$ V the MOBILE switches either to the high or to the low state depending on the applied gate voltage. The figure exhibits a very sharp transition between the two output states around $V_{\text{gate}} = 0$ V. Only a slight variation in the gate voltage results in a large change of the output voltage. Finally, when the clock voltage has reached its maximum of 1.2 V the output voltage is approximately 0.3 V in the low state and 0.9 V in the high state.

Fig. 8 demonstrates the inverter operation of the MOBILE circuit using pulsed gate and clock voltages. The traces show the clock voltage, the gate voltage, and the output voltage from top to bottom. The output switches to the high level if the input voltage is low and it switches to the low level if the input voltage is high. One should note that the output voltage remains on a constant value until the clock voltage returns to zero although the gate voltage has already changed. This self latching characteristic is an important requirement in digital circuit applications as it makes complex circuits more tolerant to signal delay times and hence it can save the use of additional latching elements.

VI. Conclusion

VRTTs with a Schottky gate have been fabricated and characterized with respect to their performance at room temperature. The devices show a very good peak current control by means of an applied gate voltage. Because of the extremely sensitive switching characteristics of the VRTT MOBILE the device is very suitable for digital applications. In principle it should be possible to decrease the size of the device down to the several hundred nanometer scale.

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