Cascaded integrator comb filters with smoothly varying coefficients for reduced delay in synchrotron feedback loops

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The Rapid Cycling Synchrotron (RCS) of the J-PARC complex in Tokai, Japan, is designed to accelerate a high intensity proton beam from 181 MeV, and later 400 MeV to 3 GeV in 20 ms within the 40 ms machine cycle. The beam power up to 1 MW demands a stable beam control to avoid excessive losses and activation of the accelerator chain. The fully digital control system is based on quadrature modulation and demodulation. In the amplitude control loops standard FIR filters separate the harmonics ($h = 2$) and ($h = 4$) after down conversion. For the phase loops at ($h = 2$) and ($h = 4$), intended to damp synchrotron oscillations, the delay in a FIR filter would limit the loop stability. Cascaded integrator comb filters, also called CIC filters, provide a shorter delay because they filter the longitudinal beam signal only where it is necessary. The notches are located at multiples of the revolution frequency of the proton beam. For fixed frequency accelerator applications, digital comb filters with fixed clock frequency are widely used to improve loop stability. For variable frequency accelerator applications, as in a proton synchrotron, where the frequency swing is larger than the notch width, usually the clock frequency of the comb filter is variable and chosen to be an integer multiple of the particle revolution frequency. At J-PARC RCS, the clock frequency has to be fixed. Tracking the frequency would require a variable noninteger number of filter taps. Here we present a filter, based on the weighted output of 2 CIC filters with variable length, and one tap difference. The filter function looks like a CIC with smoothly varying coefficients, where the notches follow the revolution frequency of the proton beam. The delay of this filter is approximately half of the corresponding FIR filter, so that the phase loops have a higher stability margin.

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I. INTRODUCTION

The Rapid Cycling Synchrotron (RCS) of the J-PARC complex [1] in Tokai, Japan, is designed to accelerate a high intensity proton beam from 181 MeV in a first stage, and 400 MeV in a later stage to 3 GeV in 20 ms at 25 Hz repetition frequency. The beam power will be up to 1 MW; therefore it is mandatory to keep the beam stable to avoid excessive losses and activation of the accelerator chain.

The acceleration cavities for RCS [2] are loaded with magnetic alloy, adjusted so that their quality factor is approximately 2, which allows dual harmonic operation. These cavities require no tuning loop in contrast to ferrite cavities.

Dual harmonic operation [3] uses ($h = 2$) for acceleration and ($h = 4$) for longitudinal beam shaping. For precise control and synchronism of the amplitudes and phases of the 11 cavities, the fully digital control system [4] uses a common reference oscillator to supply a phase reference for both harmonics to the cavity driver modules. The signal processing is based on digital quadrature modulation and demodulation. For the amplitude control loops [5] standard FIR filters [6] are used to separate the harmonics. For the phase loops at ($h = 2$) and ($h = 4$), which damp synchrotron oscillations, the delay in a FIR filter would limit the loop stability.

Digital cascaded-integrator-comb filters, also called CIC filters have a shorter delay, because they filter the signal, just where it is necessary, e.g., the notches of the filter are located at multiples of the revolution frequency of the proton beam. Originally, CIC filters were introduced for audio applications [7]. A reference for the application of digital comb filters in a high-energy proton synchrotron is given in [8]. For variable frequency accelerator applications, as in a proton synchrotron, where the frequency swing is larger than the notch width, the clock frequency of the comb filter is an integer multiple of the particle revolution frequency [9], so that a one-turn delay is achieved. For fixed frequency accelerator applications, as in electron or positron synchrotron storage rings [10], digital comb filters [11,12] with fixed clock frequency are widely used to improve the loop stability.

At J-PARC RCS, the clock frequency is fixed to a common 12 MHz reference. The filter presented here is based on the weighted output of 2 CIC filters with variable length, and one tap difference. The filter function looks like a CIC with smoothly varying coefficients, where the

notches follow the revolution frequency of the proton beam.

II. DERIVING A CIC FILTER WITH VARIABLE LENGTH

A. Digital receiver basics

The basic subsystem for digital down conversion of a revolution harmonic is shown in Fig. 1. The longitudinal beam signal is detected by a fast current transformer (FCT), filtered by an analog low pass, and sampled by an AD converter. A digital local oscillator with sine and cosine of the selected center frequency multiplies the digital data. The digital low-pass filters remove the upper sidebands after mixing. Then a digital coordinate transformer [13] processes the in-phase and quadrature components of the detected signal, so that amplitude and phase appear at the outputs. The components, such a digital receiver is made of, are described in [14].

The digital filter after down conversion of the selected harmonic has a low-pass characteristic, which rejects unwanted signals. In a synchrotron we expect to have longitudinal signals at each revolution frequency harmonic. Therefore the cutoff frequency of the filters has to be smaller than the revolution frequency. At injection time of RCS, at 181 MeV, the revolution frequency is $f_{\mathrm{rev}} = 469\,250$ Hz. At extraction time, at 3 GeV, the revolution frequency is 835 867 Hz.

If we were allowed to use a variable system clock, we could select a fixed number of taps n_{tap} and then apply a variable clock frequency f_{clk}, which tracks the revolution frequency f_{rev} of the synchrotron.

$$f_{\mathrm{clk}} = n_{\mathrm{tap}} \cdot f_{\mathrm{rev}}. \tag{1}$$

This means for a CIC filter, which is a special type of FIR filter where all taps have the same weight, that the notch spacing will follow the acceleration in the synchrotron.

B. Standard CIC filters

An example of such filter, shown in Fig. 2 has 32 taps. The clock frequency for this filter would vary from 15.016 MHz to approximately 26.7477 MHz during the RCS cycle. Such type of filtering is standard for the low-level system of COSY [15], with a revolution frequency between 490 and 1578 kHz. At COSY the number of taps is set to 16, so that the maximum clock frequency is not much higher than 25 MHz. This sample rate limit was defined by the available 12-bit AD-converters and 16-bit multipliers around 1995.

The transfer function for a CIC filter with n_{tap} taps is

$$h(f) = \frac{\sin(n_{\mathrm{tap}}\pi\frac{f}{f_{\mathrm{clk}}})}{n_{\mathrm{tap}} \cdot \sin(\pi\frac{f}{f_{\mathrm{clk}}})} \exp\left(-jn_{\mathrm{tap}}\pi\frac{f}{f_{\mathrm{clk}}}\right). \tag{2}$$

With $\Omega = f/f_{\mathrm{clk}}$, it becomes

$$h(\Omega) = \frac{\sin(n_{\mathrm{tap}}\pi\Omega)}{n_{\mathrm{tap}} \cdot \sin(\pi\Omega)} e^{-jn_{\mathrm{tap}}\pi\Omega}. \tag{3}$$

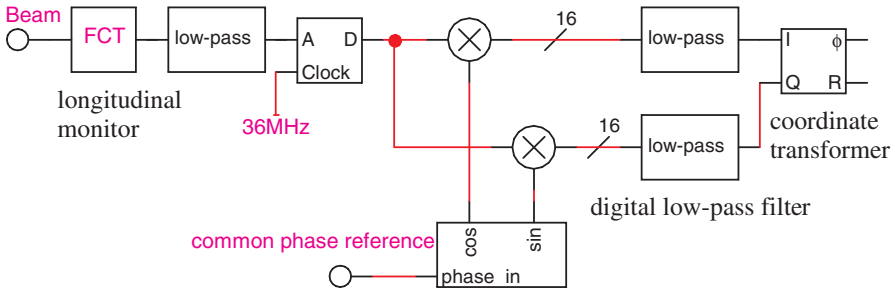

FIG. 1. (Color) Digital receiver for harmonic down conversion with I/Q demodulation.

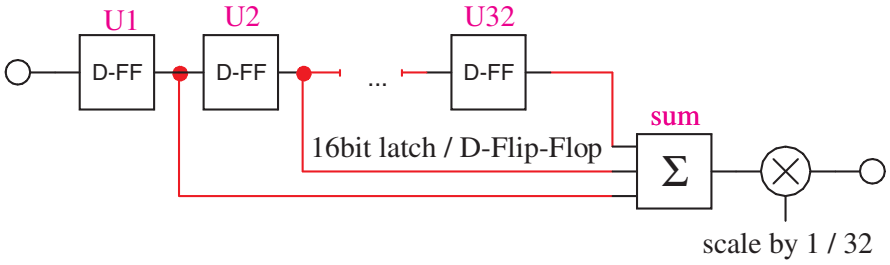

FIG. 2. (Color) CIC filter for a variable clock with fixed number of 32 taps.

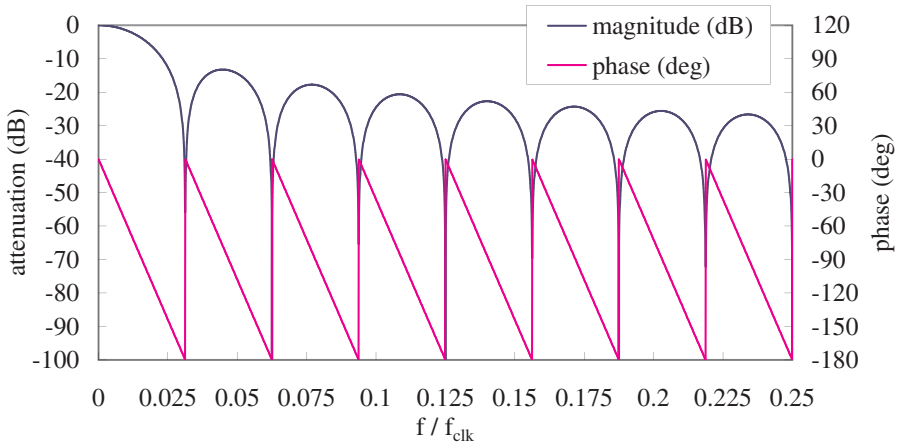

FIG. 3. (Color) Transfer function of a CIC filter with 32 taps for variable clock.

$$|h(\Omega)| = \mathrm{abs}\left(\frac{\sin(n_{\mathrm{tap}}\pi\Omega)}{n_{\mathrm{tap}}\cdot\sin(\pi\Omega)}\right);$$
$$\theta(\Omega) = -n_{\mathrm{tap}}\pi\Omega + \pi\,\mathrm{int}(n_{\mathrm{tap}}\Omega). \tag{4}$$

The transfer function for the filter with 32 taps is plotted in Fig. 3. The first zero of the transfer function is at $f/f_{\mathrm{clk}} = 1/32 = 0.031\,25$. All harmonics of the revolution frequency f_{rev} below f_{clk} are attenuated.

However, this solution is not applicable for J-PARC RCS, because the clock frequency of the digital system for RCS is fixed to 36 MHz. In J-PARC, the injector Linac, the RCS, and the main ring (MR) are synchronized to a common 12 MHz reference oscillator [16]. With fixed clock frequency, there is the other option to change the number of taps as a function of revolution frequency during RCS acceleration. However, this results in another conflict. The frequency pattern of the RCS cycle is a smooth function, and one expects the filter notches to track accordingly. However, the number of taps of a simple CIC filter can only be changed in integer steps, so that the resulting frequency step for the notches is bigger than the notch width. In other words, there is no straightforward version of a digital delay for a fraction of a clock cycle. This restriction is removed by linear interpolation between 2 CIC filters, which have a different number of filter taps, as is shown in Fig. 4, and then explained.

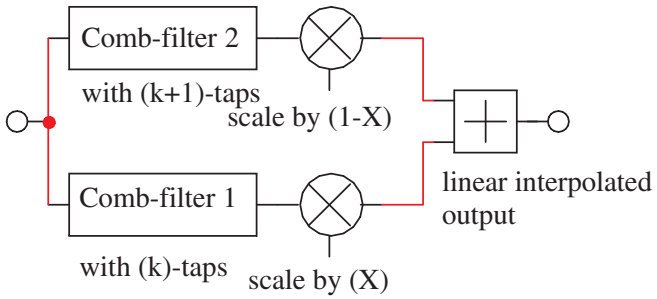

FIG. 4. (Color) Interpolation between 2 comb filters.

At time of injection at RCS, the optimum CIC filters for a variable clock could have 76 taps at a clock frequency of 35.663 MHz [Fig. 5(a)] or 77 taps at a clock frequency of 36.132 25 MHz [Fig. 5(b)]. For a fixed clock of 36 MHz, the number of taps would be the fractional number 76.718 in between. The magnitude of the transfer functions of the filters in Figs. 5(a) and 5(b) that are almost identical, are shown in Fig. 6.

C. Interpolation at fixed clock frequency

In contrast to Figs. 5(a) and 5(b), here we assume, that both filters, the one with 76 taps, and the other with 77 taps are running at a fixed clock of 36 MHz. The transfer functions of both CIC filters have different frequencies where maximum attenuation occurs. These notches are at multiples of $(36\ \mathrm{MHz}/77) = 467.53$ kHz for the filter with 77 taps, and at multiples of $(36\ \mathrm{MHz}/76) = 473.68$ kHz for the filter with 76 taps. This is shown for the first 2 notches in Fig. 7. The frequency to be suppressed, $f_{\mathrm{rev}} = 469.25$ kHz, is located in between the notches of both filters.

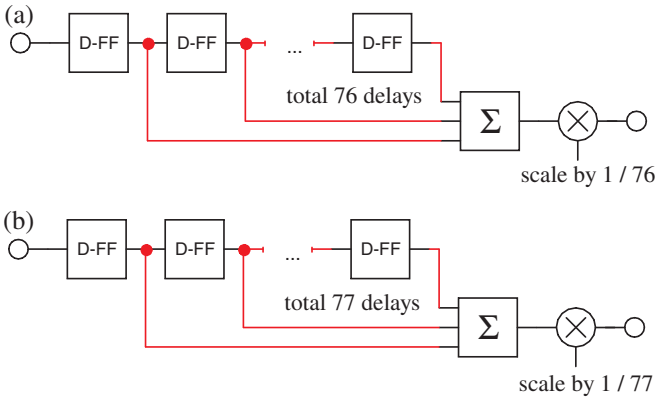

FIG. 5. (Color) (a) CIC filter with 76 taps for RCS injection with 35.663 MHz clock; (b) CIC filter with 77 taps at RCS injection with 36.132 25 MHz clock.

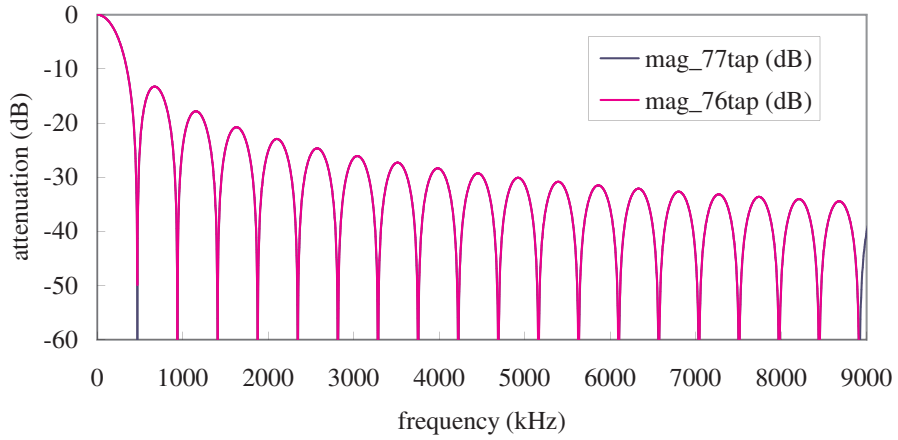

FIG. 6. (Color) Transfer function of CIC filters for variable clock with 76 taps at $76 f_{\mathrm{rev}}$ and 77 taps at $77 f_{\mathrm{rev}}$ at RCS injection with $f_{\mathrm{rev}} = 469.25$ kHz. The harmonics of f_{rev} are attenuated.

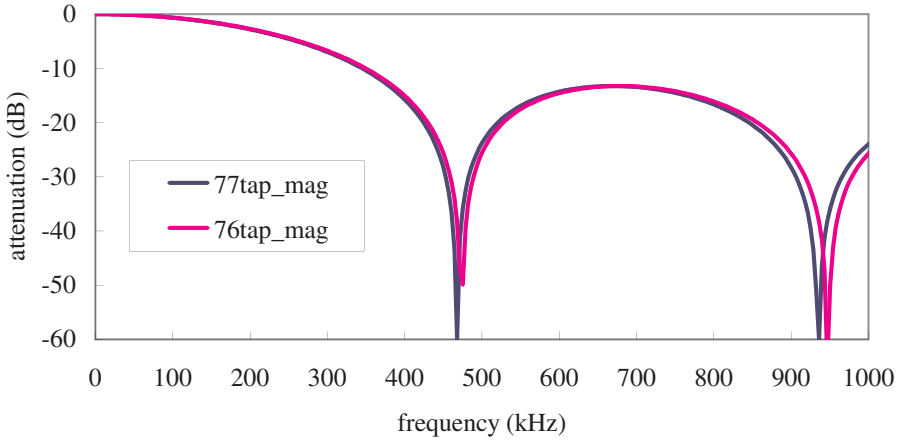

FIG. 7. (Color) CIC filter with 76 and 77 taps: attenuation at 36 MHz fixed clock frequency for $f_{\mathrm{rev}} = 469$ kHz (RCS injection).

The optimum number of taps k_{opt} is noninteger:

$$k_{\mathrm{opt}} = f_{\mathrm{clk}}/f_{\mathrm{rev}};$$
$$\text{here } k_{\mathrm{opt}} = 36\ \mathrm{MHz}/0.469\,25\ \mathrm{MHz} = 76.718. \quad (5)$$

We define the integer number of taps:

$$k_{\mathrm{int}} = \mathrm{int}(k_{\mathrm{opt}}) = \mathrm{int}(f_{\mathrm{clk}}/f_{\mathrm{rev}}); \qquad \text{here } k_{\mathrm{int}} = 76, \quad (6)$$

and the remaining fraction:

$$k_{\mathrm{frac}} = k_{\mathrm{opt}} - k_{\mathrm{int}} = k_{\mathrm{opt}} - \mathrm{int}(k_{\mathrm{opt}}); \quad \text{here } k_{\mathrm{frac}} = 0.718. \quad (7)$$

Then a scaling process, similar to linear interpolation between two points is applied. The output of the filter with 77 taps is scaled by $k_{\mathrm{frac}} = 0.718$, and the output of the filter with 76 taps by $(1–k_{\mathrm{frac}}) = (1–0.718) = 0.282$ and both scaled values are added. The combined filter shown in Fig. 8 has a transfer function, plotted in Fig. 9, which is almost like the transfer function of a single CIC filter with variable clock. The D-flip-flop resources for the delays $1 \ldots 76$ can be used for both filters. Also the generation of the sum can be shared. A filter version with optimized usage of resources, important for implementation in FPGA (field programmable gate array), is shown in Fig. 10. The result for the average of 76 taps is available one clock cycle earlier than the result for the 77 taps—therefore another D-flip-flop is put before scaling with (1/76). The filter in Fig. 10 is equivalent to a nonsymmetric FIR filter, shown in Fig. 11, where the first 76 coefficients are unity, and the coefficient 77 is variable between 0 and 1, and finally a scaling is applied to obtain unity gain at dc. At first glance, it looks obvious, to combine the cascaded multipliers to save resources. However, the final scaling for unity gain at dc requires a signal-processing environment that supports floating-point numbers.

D. Interpolated CIC filters with a variable number of taps

Between injection and extraction of RCS, the revolution ($h = 1$) frequency pattern will sweep from 469.25 kHz to

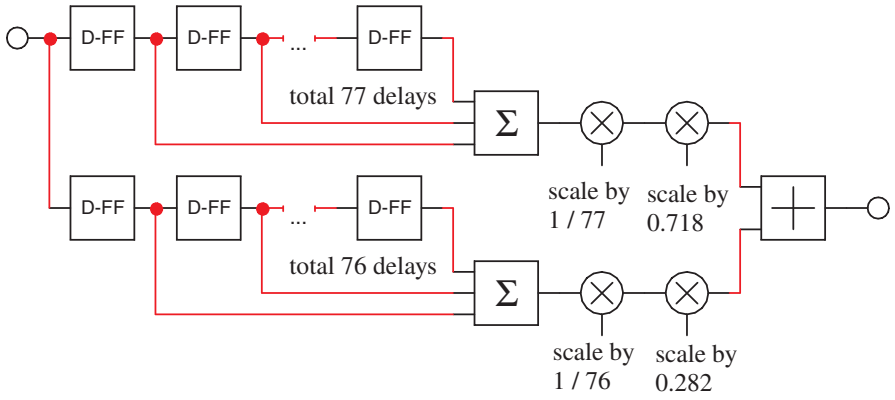

FIG. 8. (Color) Two CIC filters combined for a noninteger number of taps (here 76.718).

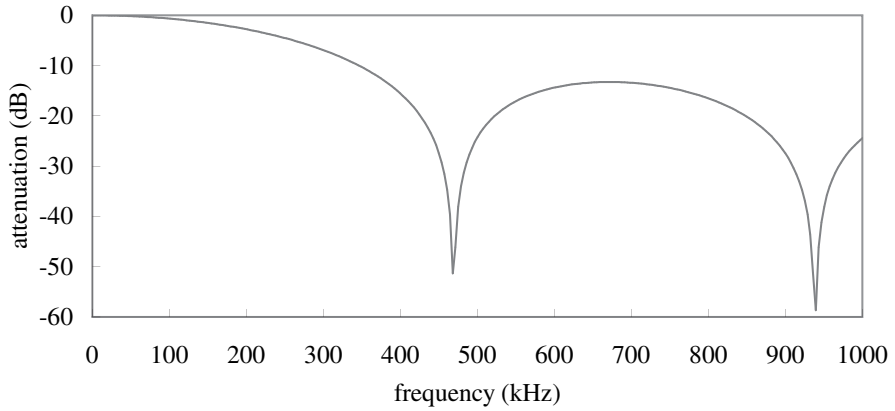

FIG. 9. The transfer function of the two combined CIC filters in Fig. 8: 76 taps and 77 taps at $f_{\mathrm{clk}} = 36$ MHz. The first notch is at 468 kHz, the next at 939.6 kHz.

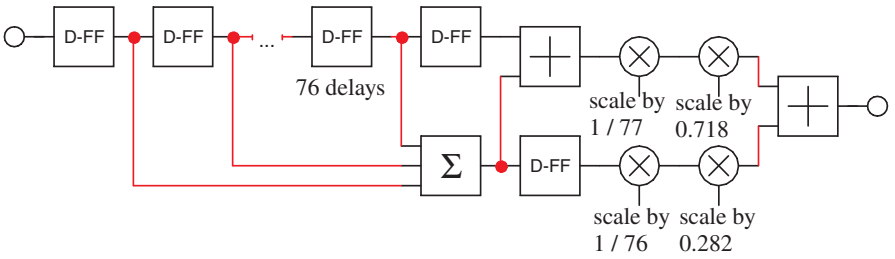

FIG. 10. (Color) Optimized version of 2 combined CIC filters of Fig. 8.

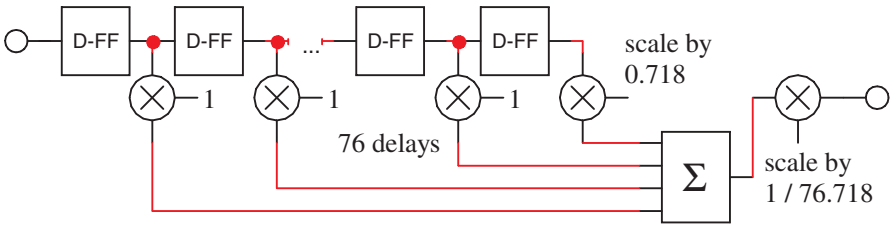

FIG. 11. (Color) FIR equivalent version of Fig. 10 where 76 coefficients are unity, and the last coefficient is variable.

approximately 835.866 kHz. In a later stage, when the injector LINAC will be upgraded to 400 MeV, the injection frequency of RCS will rise to 613.690 kHz, which is included in the filter operating range. For the expected sweep, the factor between revolution frequency and clock frequency $k_{\mathrm{opt}} = f_{\mathrm{clk}}/f_{\mathrm{rev}}$ decreases from 76.718 at 181 MeV injection to 43.069 at 3 GeV extraction. In case of 400 MeV injection, the factor k_{opt} varies between 58.662 at injection and 43.069 at extraction. In order to be prepared for changes in the future, and for testing purposes, the factor k_{opt} is defined with some safety margin. The chosen valid range for k_{opt} is between 40 and 80. The delay structure is composed of a fixed delay and a variable delay. For a fixed delay of 32 taps, which is easy to realize in a tree structure, the remaining variable delay will be changeable from 8 to 48 taps. The number of delays k_{int} is an integer number, with $k_{\mathrm{int}} = \mathrm{int}(k_{\mathrm{opt}}) = \mathrm{int}(f_{\mathrm{clk}}/f_{\mathrm{rev}})$ from Eq. (6). The corresponding circuit is shown in Fig. 12.

The function is explained by an example. The revolution frequency is assumed to be $f_{\mathrm{rev}} = 816.326$ kHz. Then $k_{\mathrm{opt}} = 36\ \mathrm{MHz}/0.816\,326\ \mathrm{MHz} = 44.1$, $k_{\mathrm{int}} = 44$, and $k_{\mathrm{frac}} = 0.1$. The fixed delay of 32 taps and the variable delay of 12 taps result in a total of $k_{\mathrm{int}} = 44$ delays. As k_{opt} is nearer to 44 than 45, the interpolated CIC-filter transfer function is expected to be close to the transfer function of a single CIC filter with 44 taps. In the upper signal path, the sum of 45 taps is scaled by (1/45). In the next multiplier, it is scaled by $(k_{\mathrm{frac}}) = 0.1$.

In the lower signal path, the sum of 44 taps is first scaled by (1/44). In the next multiplier, it is scaled by $(1 - k_{\mathrm{frac}}) = 1 - 0.1 = 0.9$.

III. IMPLEMENTATION DETAILS OF THE INTERPOLATED CIC FILTER

A. Scaling factors (k_{frac}) and (1-k_{frac})

For implementation of the filter, the scaling factors have a limited definition range. The scale factor (k_{frac}) in the upper filter path of Fig. 12 is defined for positive numbers from zero up to, but not including "1". The scale factor (1-k_{frac}) in the lower part of the filter is defined for positive numbers slightly bigger than zero (zero is not included) up to including 1. To avoid floating-point operation, fixed-point arithmetic is implemented, where the scaling factors are stored in a pattern memory.

The sum of these scaling factors $(k_{\mathrm{frac}}) + (1\text{-}k_{\mathrm{frac}})$ is always 1, therefore it is sufficient, to store only one of them in the pattern memory. As a straightforward implementation, the number k_{opt} is stored as a fixed-point number in a 16-bit wide pattern with 40 000 memory locations. This is compatible with ramping function generation for the low-level rf system of RCS [17], where for example the voltage is defined by pattern memories with 40 000 entries, so that each microsecond a new value is available during the 40 ms RCS machine cycle. The upper 6-bit (MSB) contain the integer part $(k_{\mathrm{int}} - 32)$. The value 32 is subtracted for the fixed delay of 32 taps, and to keep the number within 6-bit range. The remainder $k_{\mathrm{frac}} = k_{\mathrm{opt}} - k_{\mathrm{int}}$ is multiplied by 1024, which results in a 10-bit positive integer number between 0 and 1023 (LSB). Table I gives examples for the pattern as function of frequency. The data format is given in Table II.

The full range of the table for f_{rev} from 444.445 to 900.000 kHz was checked for consistency. The momentum of RCS will cycle like

$$p(t) = \frac{p_{\mathrm{top}} + p_{\mathrm{inj}}}{2} - \frac{p_{\mathrm{top}} - p_{\mathrm{inj}}}{2} \cos(2 \cdot \pi \cdot 25\ \mathrm{Hz} \cdot t) \tag{8}$$

within 20 ms from $p_{\mathrm{inj}} = 610.259\ \mathrm{MeV}/c$ to $p_{\mathrm{top}} = 3824.87\ \mathrm{MeV}/c$, so that the kinetic energy increases from 181 to 3000 MeV. Near injection, the lowest bit of the filter pattern will change when the revolution frequency changes by 6 Hz. The first change will occur at 16 μs. Near extraction, the lowest bit of the filter pattern will change when the revolution frequency changes by 12 Hz. The last change during the 20 ms acceleration time happens at 19.854 ms. Between 2 and 4 ms, the revolution frequency changes 37 . . . 49 Hz per μs. Then the pattern value for the CIC filter changes by the value 5 or 6 each microsecond step.

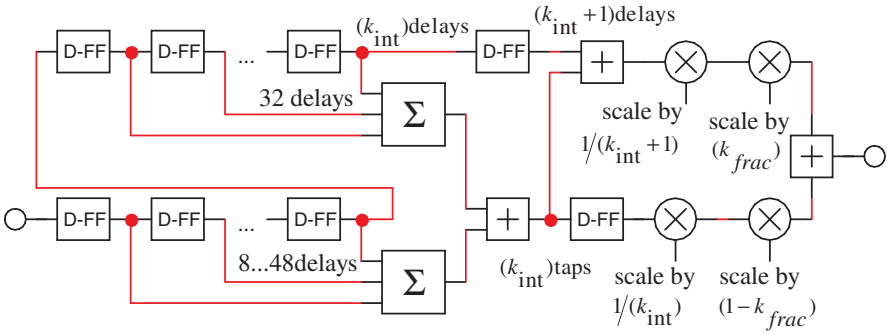

FIG. 12. (Color) The interpolated CIC filter for variable relation k_{opt} between 36 MHz clock frequency and revolution frequency.

TABLE I. Examples of the filter pattern for selected frequencies f_{rev}.

f_{rev} (kHz)	k_{opt}	k_{int}	$k_{\mathrm{int}} - 32$	$k_{\mathrm{int}} - 32$ (MSB)	k_{frac}	Int(1024 k_{frac})	Remain (LSB)	Pattern (hex)
444.445	80.999 899	80	48	C000	0.999 899	1023	03FF	C3FF
450.000	80	80	48	C000	0.0	0	0000	C000
469.250	76.718 167	76	44	B000	0.718 167	735	02DF	B2DF
500.000	72	72	40	A000	0.0	0	0000	A000
613.691	58.661 44	58	26	6800	0.661 44	677	02A5	6AA5
750.000	48	48	16	4000	0.0	0	0000	4000
835.867	43.069 05	43	11	2C00	0.069 05	70	0046	2C46
900.000	40	40	8	2000	0.0	0	0000	2000

TABLE II. The data format of the 16-bit filter pattern.

Upper 6-bit (MSB)	Lower 10-bit (LSB)
$k_{\mathrm{int}} - 32$	Int(1024 kfrac)

The connection of the pattern to the filter is shown in Fig. 13. Brackets "[ ]" indicate the word length. The 6-bit value ($k_{\mathrm{int}} - 32$) selects the number of delays. The 10-bit value Int($1024k_{\mathrm{frac}}$) is for the scaling multiplier in the upper path of Fig. 12. The sign bit [bit 15] of this multiplier input is set to zero. [Bit 14 . . . bit 5] of the multiplier input are connected to the 10-bit from the pattern. [Bit 4 . . . bit 0] of the 16-bit multiplier are set to zero. For the scaling multiplier in the lower path of Fig. 12, ($1 - k_{\mathrm{frac}}$) is computed by subtracting the scaled number int($1024k_{\mathrm{frac}}$) from 32 768. The value of 32 768 at the A input of the subtracter (A-B) in Fig. 13 is a 17-bit number in 2's complement. Therefore the multiplier for scaling needs a 17-bit input. Alternatively, the number could be changed to 32 767, because the resulting error is small, so that a 16-bit input is sufficient.

B. Scaling with the number of taps

The circuit shown in Fig. 12 contains one multiplier to scale by $1/(k_{\mathrm{int}} + 1)$ and another to scale by $1/(k_{\mathrm{int}})$. This is shown in detail in Fig. 14. For digital signal processing with integer arithmetic, one tries to avoid division operations. As the number of integer values for k_{int} is limited to the interval [40,80] in case of RCS frequency range, we use a table containing approximate reciprocal values. The approximate values are calculated by dividing the 22-bit value $2^{22} = 419\,430\,4$ by k_{int}. After rounding to the next integer, an 18-bit positive 2's complement number is obtained. Table III lists the numbers. For the multiplier output, finally a scaling with a 22-bit-shift of $2^{22} = 419\,430\,4$ is necessary, which is implemented by selected the appropriate multiplier outputs. Finally, 3 CIC filters as shown in Fig. 12 will be cascaded. Therefore the scaling table has

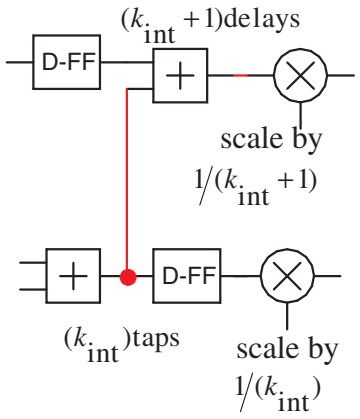

FIG. 14. (Color) Filter scaling to dc unity gain by integer number of taps (detail of Fig. 12).

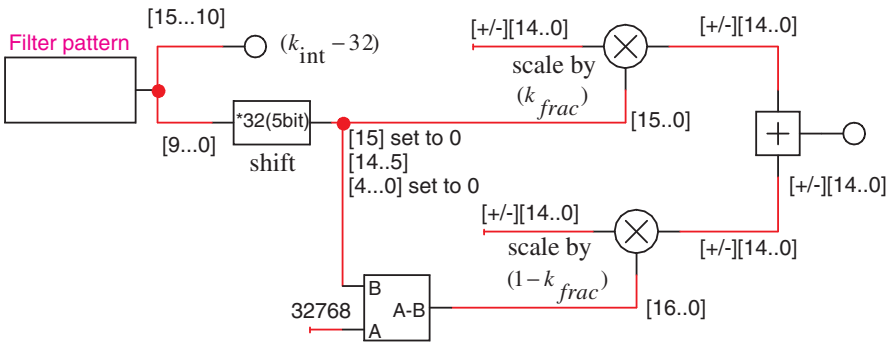

FIG. 13. (Color) The data flow from memory pattern to filter (a detail to Fig. 12).

TABLE III. Selected values of the table for the scaling factor $(1/k_{\text{int}})$.

k_{int}	$2^{22}/k_{\text{int}}$	18-bit signed	Hex
40	104 857.6	104 858	1999A
43	97 541.953 49	97 542	17D06
58	72 315.586 21	72 316	11A7C
76	55 188.210 53	55 188	0D794
80	52 428.8	52 429	0CCCD

TABLE IV. Explanation of the selection switches in Fig. 15.

$k_{\text{int}} - 32$	Switch matrix condition
48	All switches S9 to S48 are closed
47	Switches S9 to S47 are closed. S48 is open
...	...
10	S9 and S10 are closed
9	Only S9 is closed
8	None of the switches are closed

several "read" outputs. For addressing the table, we use $(k_{\text{int}} - 32)$, which is defined between 8 and 48.

C. The structure of the variable delay

The variable delay generates the 22-bit wide sum of 8 ... 48 samples. The number of samples is defined by the pattern value $(k_{\text{int}} - 32)$. The structure is shown in Fig. 15. The inputs of the adder stages of open switches are set to zero. For a frequency sweep going up, the function is explained in Table IV. The switching of S9 ... S48 is synchronized by appropriate delays with the scaling at the multipliers.

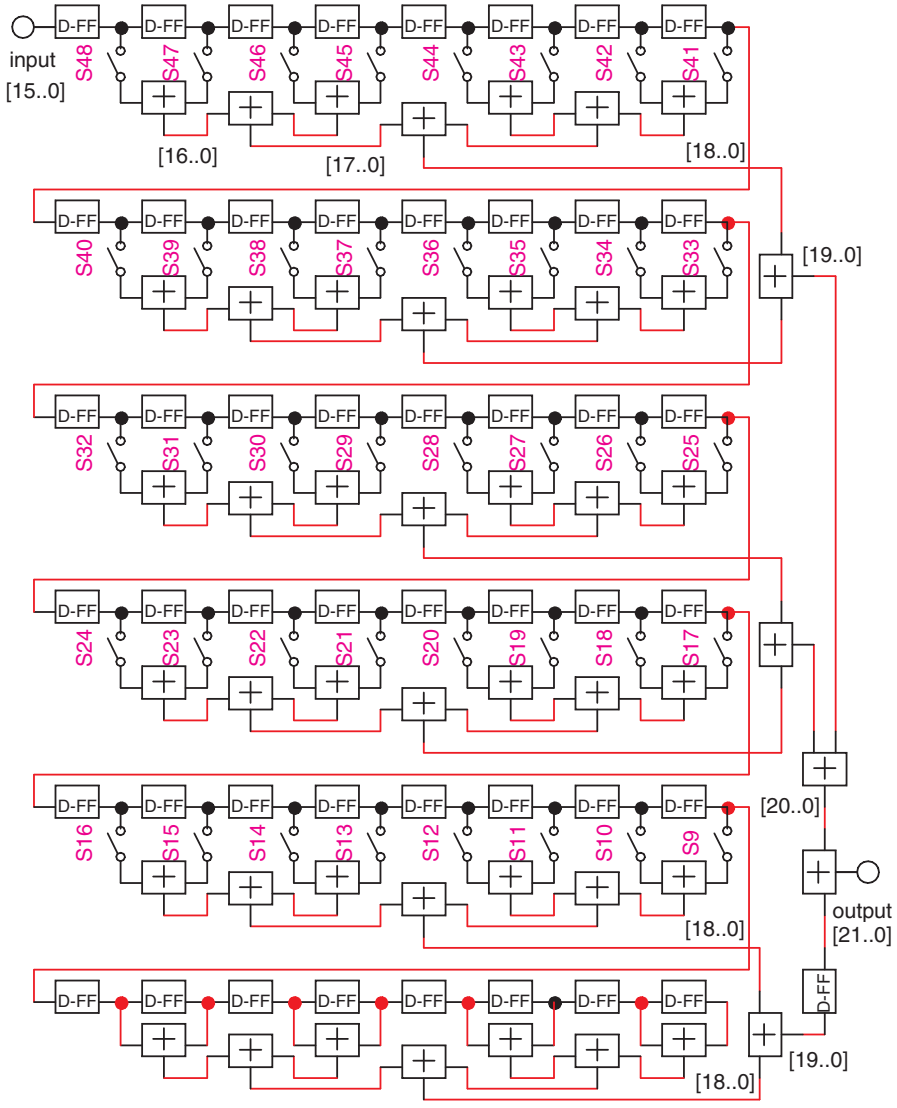

FIG. 15. (Color) The structure of the variable delay. For low frequency at RCS injection the switches S9 to S44 are closed.

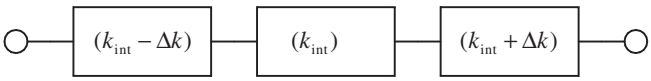

FIG. 16. Cascading 3 CIC filters with different k_{int} in series.

D. Cascading 3 interpolating CIC filters

Using one of these interpolating CIC filters is not sufficient for good suppression of unwanted signals. For the digital receiver subsystem, which is operating with 16-bit arithmetic, we expect attenuation in the order of 80 dB or better. Also the notch width is not wide enough, using the maximum synchrotron frequency of RCS (approximately 6 kHz) as criterion. Increasing the number of filters put in series improves the notch depth. Selecting a different number of taps for each of the cascaded filters increases the notch width. As a good compromise between total delay and desired transfer function, in total 3 filters with different variable delay are put in series. According to Fig. 16 the original delay variable (k_{int}) is replaced by either ($k_{int} - \Delta k$) or ($k_{int} + \Delta k$).

The value Δk depends slightly on the revolution frequency as is shown in Fig. 17. Near RCS injection, at low frequency, the filter stop band is narrow. There $\Delta k = 3$ is chosen. For revolution frequencies higher than 600 kHz, $\Delta k = 2$ gives better performance.

This criterion can be expressed as function of k_{int}:

For a value of $k_{int} \leq 60$, choose $\Delta k = 2$.

For a value of $k_{int} > 60$, choose $\Delta k = 3$.

In case the injection energy of RCS is upgraded to 400 MeV, the value $\Delta k = 2$ will stay constant during the whole RCS cycle.

IV. DISCUSSION OF RESULTS

A. Simulation of the 3 filters in series

The filter structure, shown in Fig. 16 was simulated with SCILAB [18]. For the case $k_{int} = 76$ and $\Delta k = 3$ at injection, the filter length in total sample points is $(76 - 3 +$

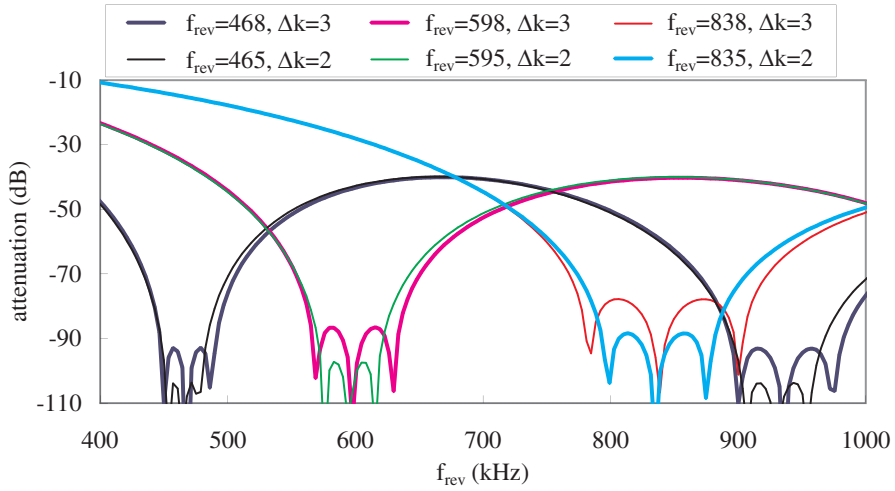

FIG. 17. (Color) The choice of Δk influences the performance of the 3 variable CIC filters in series.

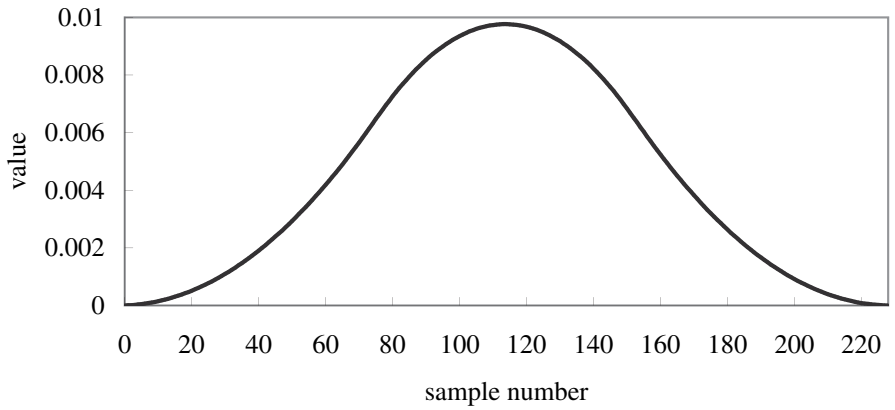

FIG. 18. The impulse response of 3 interpolating CIC filters in series for $k_{int} = 76$ and $\Delta k = 3$ has a length of 228 samples (equivalent to 228 clock cycles).

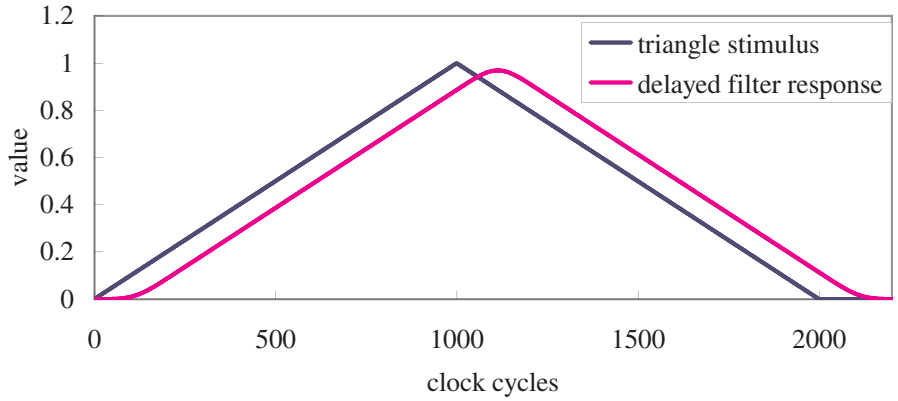

FIG. 19. (Color) The delay of 3 cascaded CIC filters with variable number of taps, arranged as $(k_{\text{int}} - 3)$ (k_{int}) $(k_{\text{int}} + 3)$ at 469 kHz for $k_{\text{int}} = 76$ is 114 clock cycles $\Leftrightarrow$ 3.166 μs.

$76 + 76 + 3) = 228$ taps. The impulse response is shown in Fig. 18. In the real circuit, the delay is slightly longer due to latches in the adder trees.

When a ramp with a rise time of 1000 clock cycles = 27.75 μs is applied as stimulus to the filter, the delay of the filter is half the number of total taps. At 50% signal level, the answer of the filter is delayed by 114 clock cycles or 3.166 μs. This is shown in Fig. 19. For higher revolution frequency, the number of taps goes down, but the delay will not become shorter, because the delay flip-flops are still in the signal path. This way, the behavior of the phase loop, where the variable CIC filter is used, does not change so much during the acceleration cycle. The resulting filter function at injection is shown in Fig. 20.

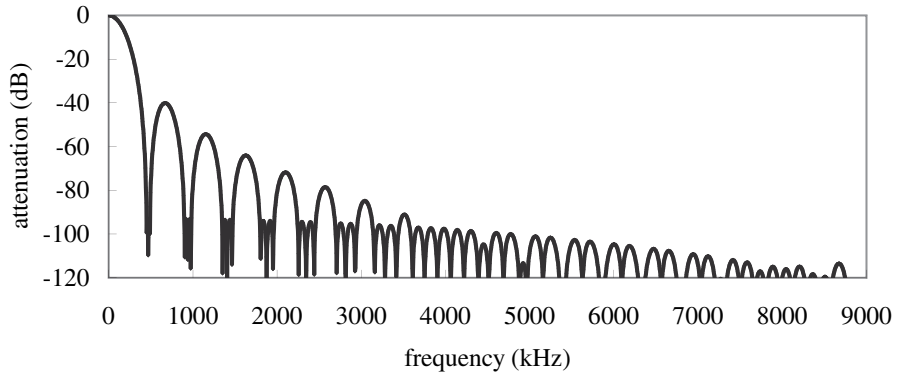

FIG. 20. CIC-filter function in frequency domain at injection for $\Delta k = 3$.

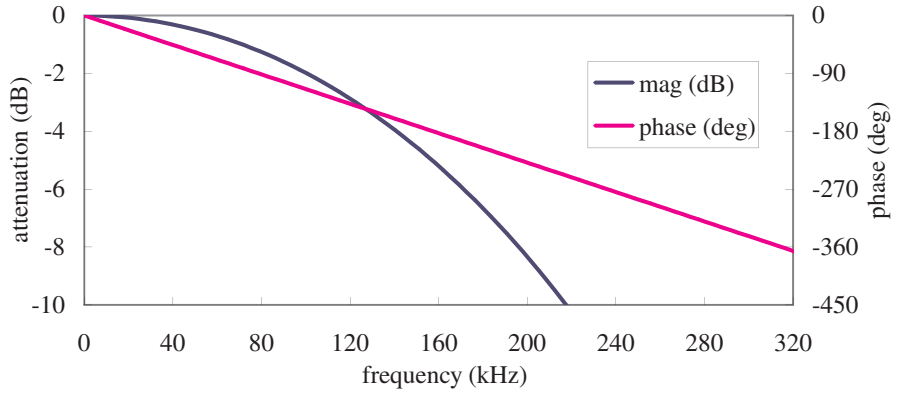

FIG. 21. (Color) Pass band of the combined CIC-filter function at 469 kHz for $\Delta k = 3$. The phase is $-90°$ at 79 kHz, $-140°$ at 122.4 kHz (3 dB point), and $-360°$ at 315 kHz.

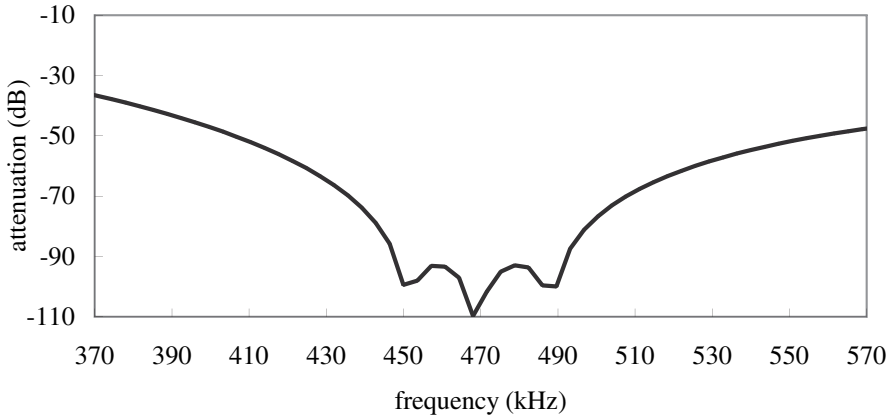

FIG. 22. Suppression of next harmonic of cascaded CIC filter for $\Delta k = 3$ at injection.

Then Fig. 21 shows the pass band, and Fig. 22 the suppression of the next revolution harmonic, which is better than 90 dB.

B. Comparing with a standard FIR filter

The digital low-pass filter for amplitude control in RCS [19] uses a combination of 3 CIC filters with 8 taps each (Fig. 23) for down sampling from 36 MHz clock to 9 MHz clock followed by a 63 tap FIR filter running at 9 MHz. The FIR filter has 2 delays between each coefficient, so that the length of the FIR filter is equivalent to $63 \cdot 8 = 504$ clock cycles at 36 MHz clock. The FIR-filter coefficients are shown in Fig. 24. To allow for troubleshooting, the well-tested FIR filter for amplitude control is also available for the phase-control circuit as a back-up solution. Both, the FIR and the variable CIC filter are realized in the same FPGA and are selected at boot time of the FPGA for phase control.

Figure 25 shows the response of the FIR-filter function in Fig. 24 to a ramp as stimulus. The same type of stimulus

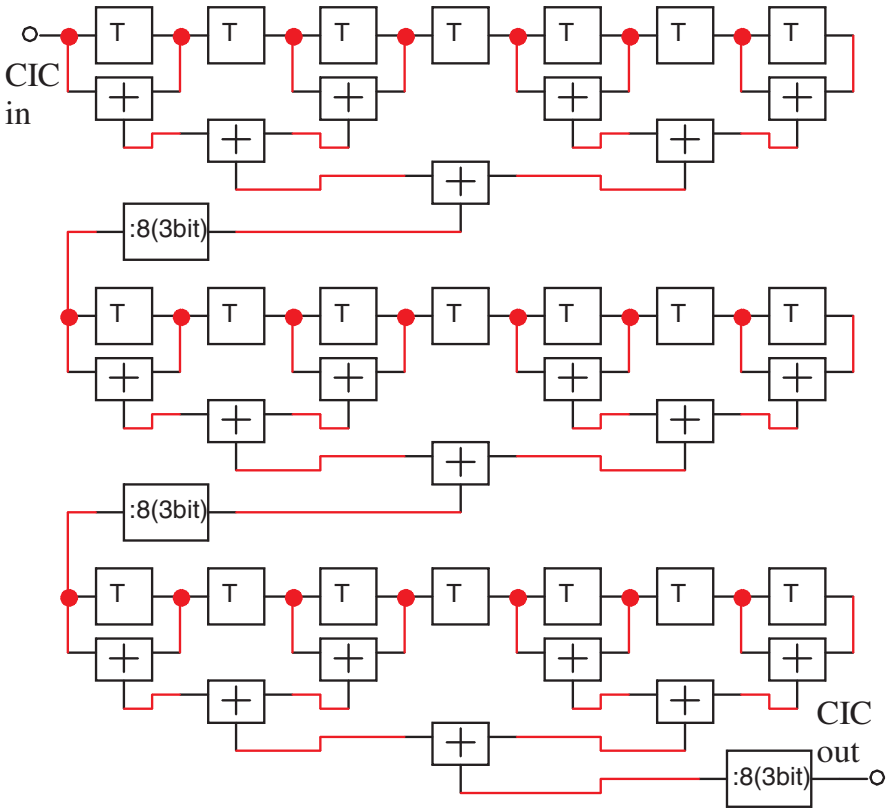

FIG. 23. (Color) Three CIC filters with 8 taps each for down sampling from 36 to 9 MHz.

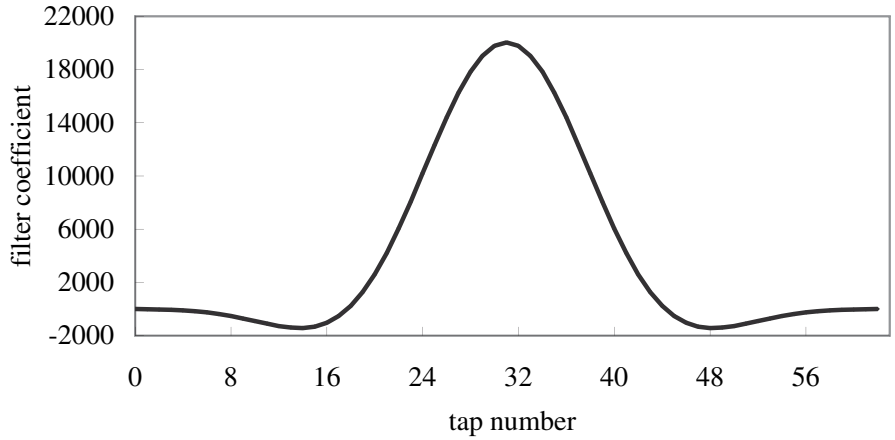

FIG. 24. FIR-filter coefficients for RCS amplitude control: 63 symmetric taps at 9 MHz clock with 2 delays between each tap (equivalent to 504 cycles at 36 MHz clock).

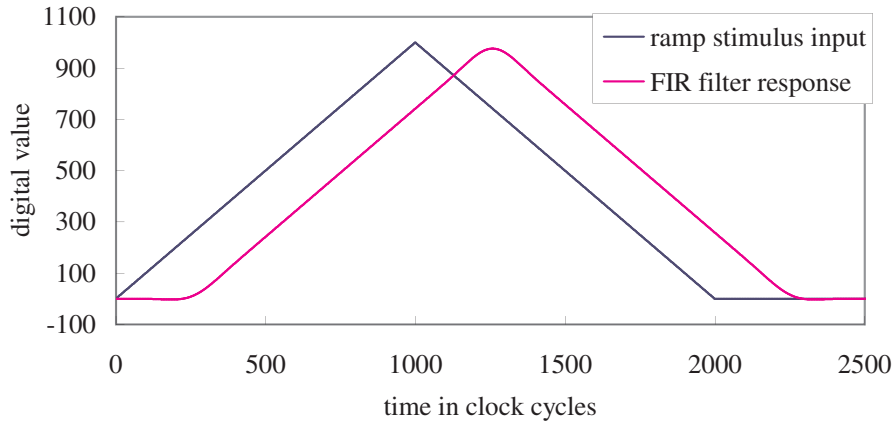

FIG. 25. (Color) Delay of the FIR filter with effectively 504 taps at 36 MHz clock. Stimulus is a 1000-point ramp (up/down) at 36 MHz clock with 27.77 μs rise time. At half pulse height the delay is 258.5 clocks = 7.18 μs.

as in Fig. 19 for the variable CIC filter is applied. The FIR-filter delay is more than twice compared to the variable CIC filter in Fig. 19. The frequency characteristics of the FIR filter combined with the CIC filter for down sampling are shown in Fig. 26(a) from dc to the Nyquist frequency limit. The FIR filter is clocked with 9 MHz, therefore Fig. 26(b) confirms, that the CIC down-sampling filter provides enough attenuation at multiples of 4.5 MHz. Then Fig. 26(c) shows the pass-band characteristic. The FIR filter has a longer delay, compared to the variable CIC filter, because the total frequency span that is attenuated is wider.

C. Simulation results with a phase loop

The digital phase loop for RCS is simulated with PSPICE to check the stability margin [20]. For 6 kHz synchrotron frequency, both control loops, either with FIR low-pass filter for down conversion [Fig. 27(a)], or with variable CIC filter [Fig. 28(a)] are stable. For an assumed synchrotron frequency of 30 kHz, the loop with the FIR filter [Fig. 27(b)] is near instability and shows strong ringing, while the phase loop with the variable CIC filter [Fig. 28(b)] is stable. The reason for the smaller stability margin of the FIR filter is the longer delay, which translates into a phase shift of $-90°$ at 33.89 kHz.

V. SAVING FPGA RESOURCES BY DOWN SAMPLING

One CIC filter will need 82 $\times$ 16-bit D-FF for the delays, 4 multipliers in the delay circuit, and 79 adders in the adder tree. For 3 of the variable CIC filters in series, running at 36 MHz clock, approximately 250 $\times$ 16-bit D-FF, 12 multipliers, 250 adders, and the table to look up for 40 scale values are needed. There are several possibilities to save resources.

A. Optimizing the circuit

The 3 filters in series in Fig. 16 have different numbers of taps, for example, $(k_{\text{int}} - 2)$, (k_{int}), and $(k_{\text{int}} + 2)$. The

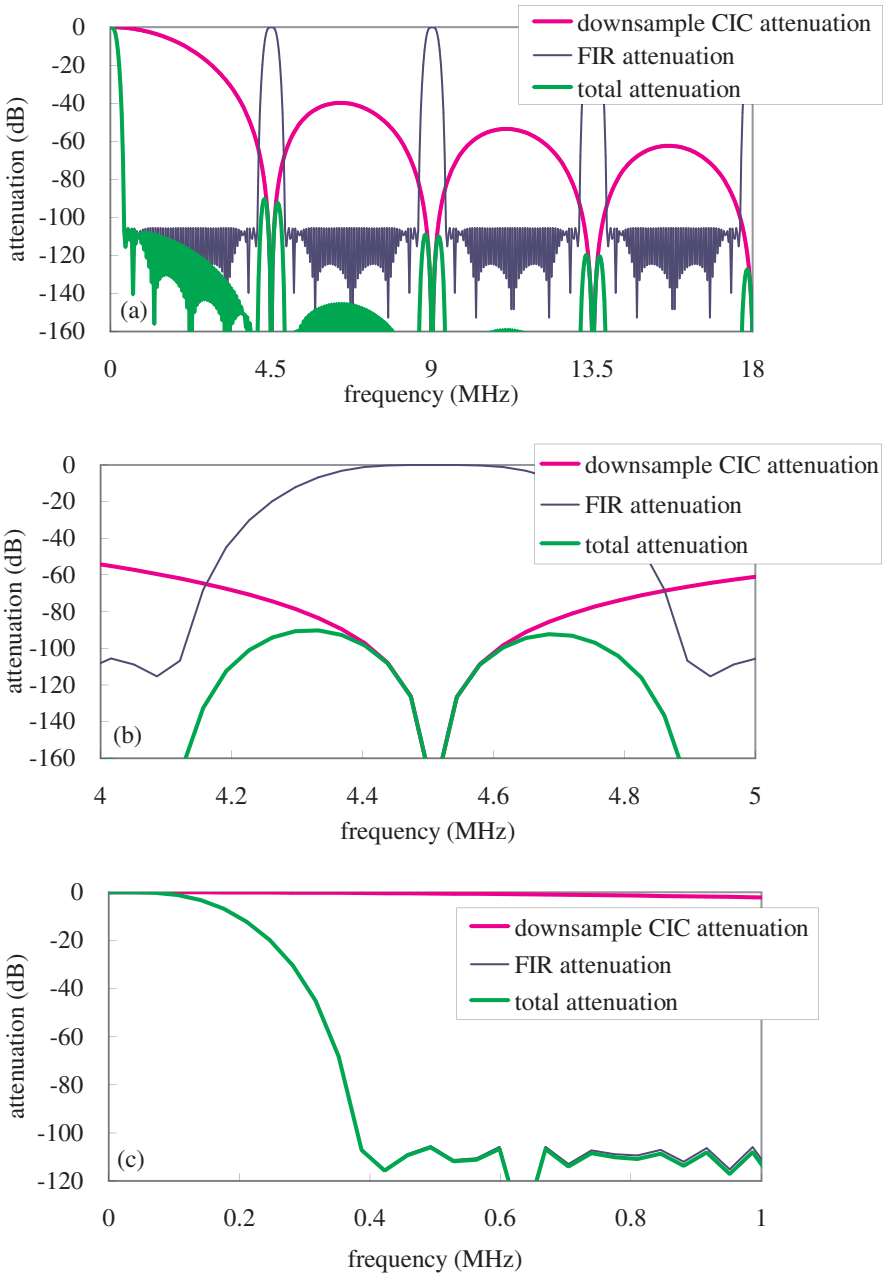

FIG. 26. (Color) (a) Transfer function of the low-pass filter for amplitude control, consisting of a 3×8 tap CIC for down sampling, and a FIR with 2 delays at each of the 63 taps at 9 MHz. (b) Attenuation at Nyquist rate of the FIR filter clocked at 9 MHz. Enlarged view of (a) around 4.5 MHz. (c) Pass-band characteristic of the Low-pass filter for amplitude control. Enlarged view of (a) from dc to 1 MHz.

maximum value for (k_{int}) is 76 at injection. It is possible to remove always unused taps in the filters with (k_{int}) and $(k_{\mathrm{int}} - 2)$. This way, $6 \ldots 8 \times 16$-bit D-FF can be saved. Also the total delay will be approximately 200 ns shorter. As a disadvantage, each CIC-filter stage will look different.

B. Down sampling to 9 MHz clock frequency

This approach is the same as reducing the resources for the FIR filter for amplitude control, shown in Fig. 24. The 3-stage CIC filter with 8 taps from Fig. 23 at the input sides provides low-pass filtering, so that the sample rate can be reduced to 9 MHz. However, for the 3 variable CIC filters in series, Δk has to be smaller than 1. In case of $\Delta k = 1$ the spacing between the harmonics for (k_{int}) and $(k_{\mathrm{int}} \pm 1)$ becomes too big. Therefore the difference in the number of taps between the filter stages Δk becomes noninteger. An example with $(k_{\mathrm{int}} \pm 0.5)$ is shown in Fig. 29. Some translation logic for the filter with $(k_{\mathrm{int}} \pm 0.5)$ is necessary, which makes the circuit

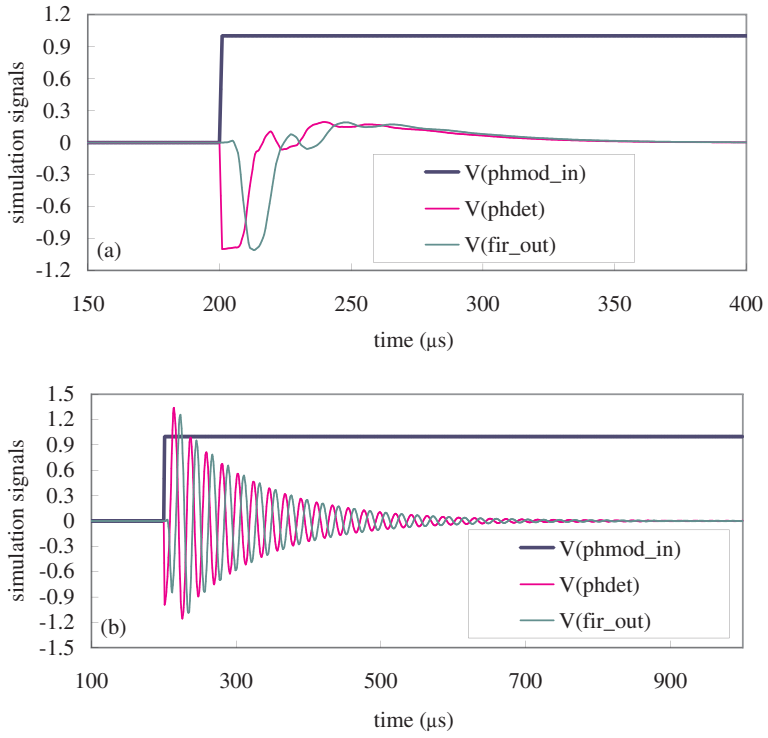

FIG. 27. (Color) (a) Simulated phase loop with FIR low-pass filter is stable at 6 kHz synchrotron frequency. (b) Simulated phase loop with FIR low-pass filter is near instability and shows ringing at 30 kHz synchrotron frequency. In both figures, the stimulus is a phase-jump with 1 μs rise time.

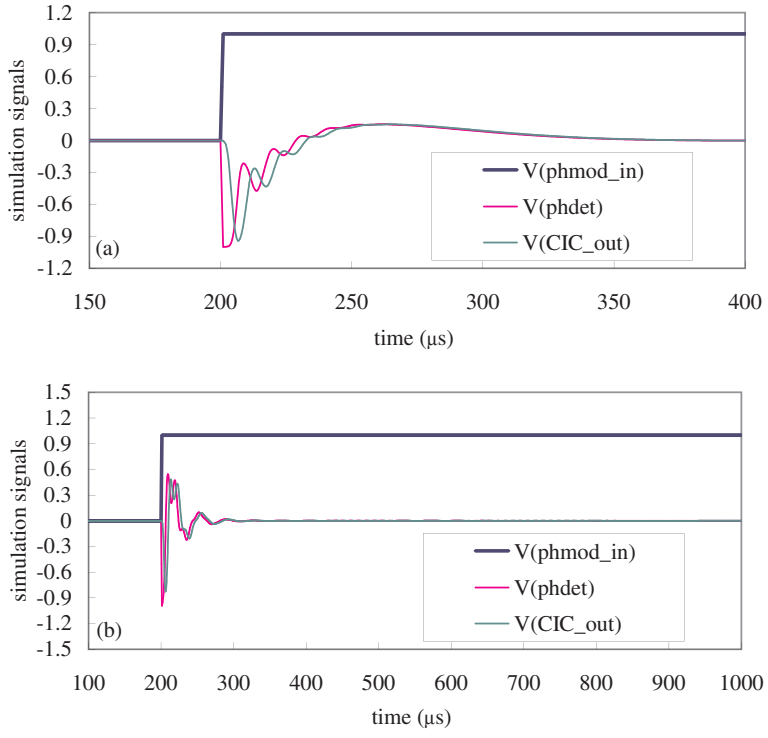

FIG. 28. (Color) (a) Simulated phase loop with variable CIC low-pass filter is stable at 6 kHz synchrotron frequency. (b) Simulated phase loop with variable CIC low-pass filter is stable at 30 kHz synchrotron frequency. In both figures, the stimulus is a phase-jump with 1 μs rise time.

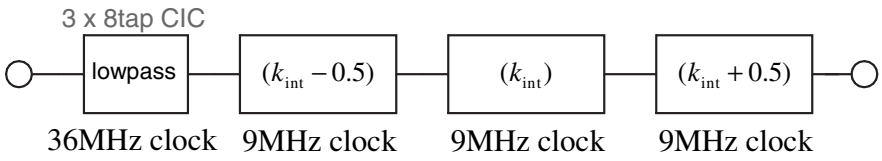

FIG. 29. Down sampling to 9 MHz to reduce resources results in noninteger Δk.

more difficult to understand, and less efficient in terms of used resources.

C. Down sampling to 18 MHz clock frequency

As in Sec. V B and Fig. 23, a 3-stage CIC filter with 8 taps is used as a prefilter. For the phase-feedback board [21] (PFB) it reduces the sample rate from 36 to 18 MHz (see Fig. 30). This prefilter introduces an additional delay of 36 clock cycles. 12 of these clock cycles are delays in the adder tree, and 24 of these delays are related to the filter taps. For slow signals like a ramp, the delays in the filter taps only contribute half. Then the 3-stage 8 tap CIC filter introduces a delay of $12 + 24/2 = 24$ clocks, or 666 ns for ramp signals as stimulus. This filter already exists in the FPGA for the FIR filter (Sec. IV B), which is the back-up solution—therefore its design is reused. One CIC filter will need approximately: 55 D-FF for the delays, 4 multipliers, and 41 adders for the delays. For the 3 CIC filters in series, running at 18 MHz clock, approximately 165 × 16-bit D-FF, 12 multipliers, and 123 adders, and the table to look up for 32 scale values are needed. The CIC-stages for down sampling need another 24 D-FF for delay, and 21 adders.

In discussions with the company, who is building the RCS digital low-level rf system, the structure in Fig. 30 was defined as the preferred filter for phase control in RCS. In the 36 MHz version, the variable Δk was either 2 or 3, depending on revolution frequency. In the 18 MHz version, Δk is constant with $\Delta k = 1$. The circuit for the single variable CIC filter then changes from Fig. 12 (36 MHz clock version) to Fig. 31 (18 MHz clock version).

With the reduced number of delays, the look-up table for $k_{int}(f_{rev})$ (Table I) is modified to Table V. Also the scaling factor (Table III) is changed according to Table VI. The 18-bit value for $k_{int} = 16$ is reduced by 1, so that it fits within 18-bit. Table VII shows the limits of $(k_{int} + \Delta k)$ for the 6 places where these values appear.

The transfer function of the 3 interpolated CIC filters (18 MHz version) is shown for 3 different revolution frequencies in Fig. 32. Figure 33(a) shows the attenuation of the combination of CIC prefilter and 3 variable CIC filters (the structure of Fig. 30) from dc up to 18 MHz—the Nyquist frequency for a 36 MHz clock system. Figure 33(b) gives an enlarged view of the frequency span from dc to 4.5 MHz. Thanks to the prefiltering, the suppression of the higher harmonics of the revolution frequency is 90 dB or better, which is an improvement

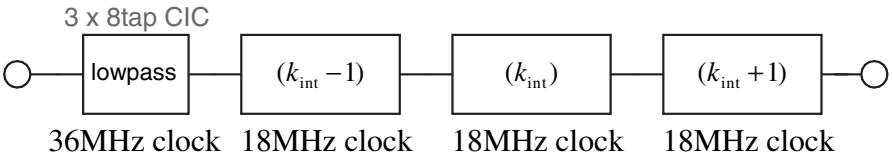

FIG. 30. Down sampling to 18 MHz clock reduces used resources. $\Delta k = 1$ is kept constant during the RCS frequency sweep.

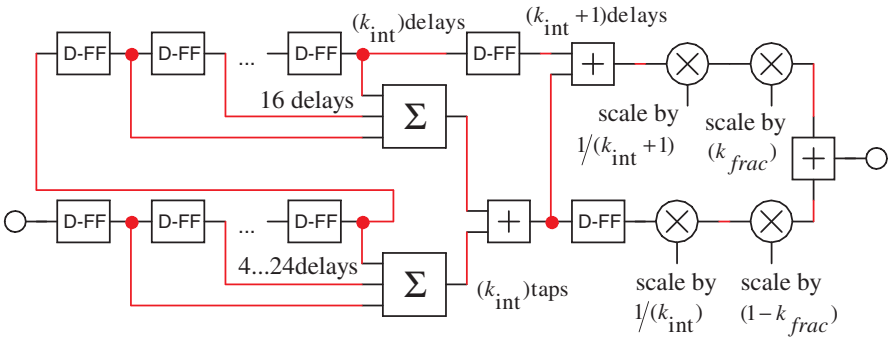

FIG. 31. (Color) The interpolated CIC filter for variable relation k_{opt} between 18 MHz clock frequency and revolution frequency.

TABLE V. Examples of the filter pattern for selected frequencies f_{rev} for the 18 MHz filter version.

f_{rev} (kHz)	k_{opt}	k_{int}	$k_{int} - 16$	$k_{int} - 16$ (MSB)	k_{frac}	Int(1024 k_{frac})	Remain (LSB)	Pattern (hex)
439.025	40.999 943	40	24	6000	0.999 943	1023	03FF	63FF
450.000	40	40	24	6000	0.0	0	0000	6000
469.250	38.359 084	38	22	5800	0.359 084	367	016F	596F
500.000	36	36	20	5000	0.0	0	0000	5000
613.691	29.330 72	29	13	3400	0.330 72	338	0152	3552
750.000	24	24	8	2000	0.0	0	0000	2000

TABLE VI. Selected values of the table for the scaling factor $(1/k_{int})$ for the 18 MHz filter version.

$k_{int} - 16$	k_{int}	$2^{21}/k_{int}$	18-bit signed	Hex
0	16	131 072.0	131 071	1FFFF
1	17	123 361.88	123 361	1E1E1
4	20	104 857.6	104 857	19999
24	40	52 428.8	52 428	CCCC
31	47	44 620.255	44 620	AE4C

compared to the 36 MHz version without down sampling in Fig. 17. Of course, an attenuation of 100 dB or more as shown in Figs. 32 and 33 is only possible with floating-point arithmetic. With 16 . . . 18-bit integer arithmetic used in the FPGA, the attenuation is limited to 90 . . . 100 dB.

VI. APPLICATION: 90° DELAY (HILBERT-TRANSFORMATION)

The basic idea for the interpolating CIC filter can be applied for solving the problem of generating a delay, that is proportional to the revolution period of a particle beam. This allows ''one-turn-delays'' [22] or 90° delays for Hilbert transformation to be realized with a fixed clock digital system.

Figure 34 shows the structure of a digital 90° phase shifter for Hilbert transformation that can follow the revolution frequency while operating at fixed clock. The optimum number of delays for 90° at harmonic h is

$$(k_{opt}) = \frac{f_{clk}}{4 \cdot h \cdot f_{rev}}. \quad (9)$$

The integer number of delays is $(k_{int}) = \text{int}(k_{opt})$. The corresponding scaling factors a_1 and a_2 are computed in

TABLE VII. Minimum and maximum for $(k_{int} + \Delta k)$ while accessing Table VI.

	Filter with $\Delta k = -1$		Filter with $\Delta k = 0$		Filter with $\Delta k = 1$	
	$k_{int} + \Delta k$	$k_{int} + \Delta k + 1$	k_{int}	$k_{int} + 1$	$k_{int} + \Delta k$	$k_{int} + \Delta k + 1$
Minimum	20	21	21	22	22	23
Maximum	37	38	38	39	39	40

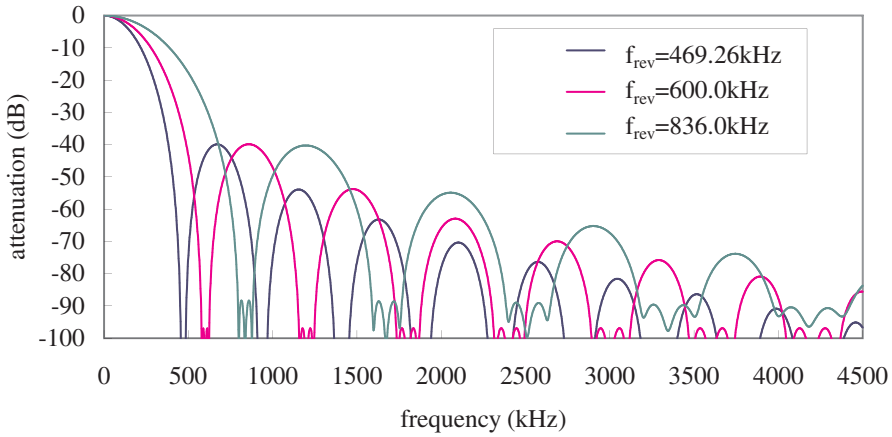

FIG. 32. (Color) Attenuation of 3 combined CIC filters with $\Delta k = (-1; 0; +1)$ at 18 MHz sample rate. The effect of the down-sampling CIC at the input is not included.

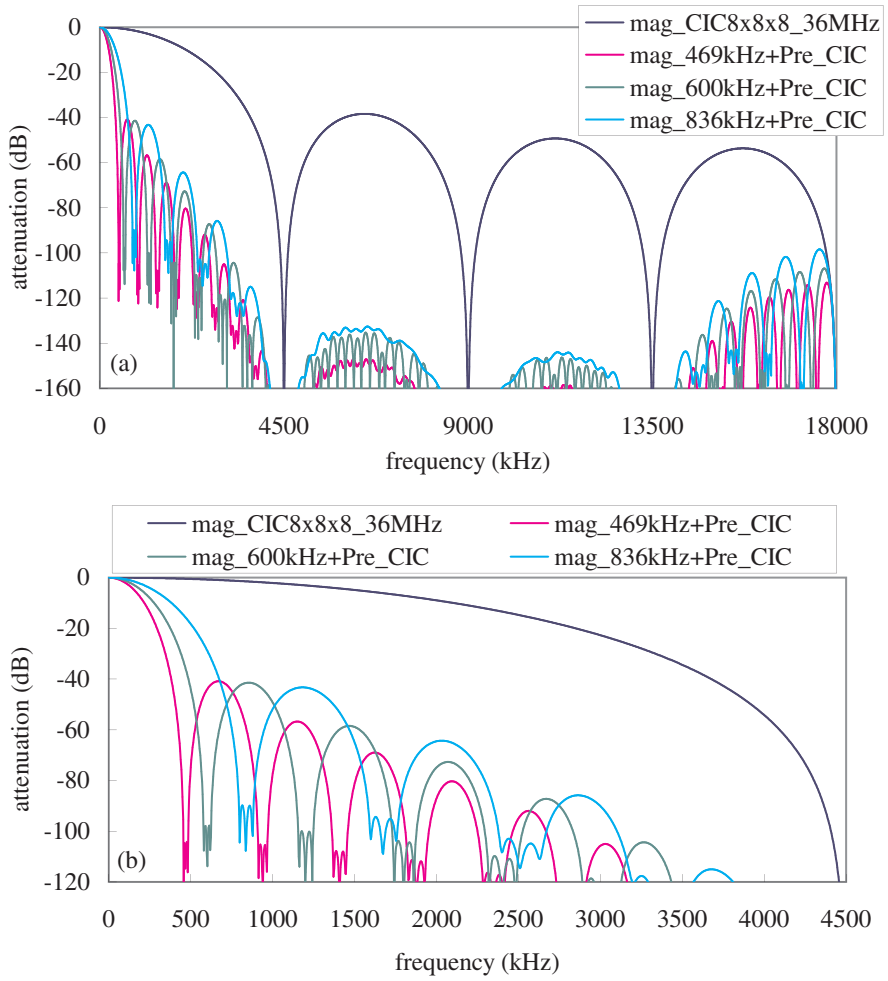

FIG. 33. (Color) (a) Attenuation of down-sampling CIC (to 18 MHz) combined with 3 variable CIC filters at 18 MHz sample rate. (b) The attenuation of the higher harmonics is shown in a reduced frequency span from dc to 4.5 MHz of (a).

a way, that the amplitude at the output follows the input amplitude and the phase between input and output is 90° as expected.

The output after (k_{int}) delays is a complex vector $z_1 = x_1 + jy_1$, and the output after ($k_{\text{int}} + 1$) delays is a complex vector $z_2 = x_2 + jy_2$. After scaling with the real numbers a_1 and a_2, we get the sum in frequency domain

$$S(f) = a_1 \cdot z_1 + a_2 \cdot z_2 = a_1(x_1 + jy_1) + a_2(x_2 + jy_2). \tag{10}$$

For a 90° phase shift, the real part has to be zero

$$a_1 \cdot x_1 + a_2 \cdot x_2 = 0, \tag{11}$$

and the amplitude has to be constant, e.g., 1.

$$(a_1x_1 + a_2x_2)^2 + (a_1y_1 + a_2y_2)^2 = 1. \tag{12}$$

Equation (11) inserted into (12) simplifies to

$$a_1y_1 + a_2y_2 = \pm 1. \tag{13}$$

Inserting Eq. (11) gives

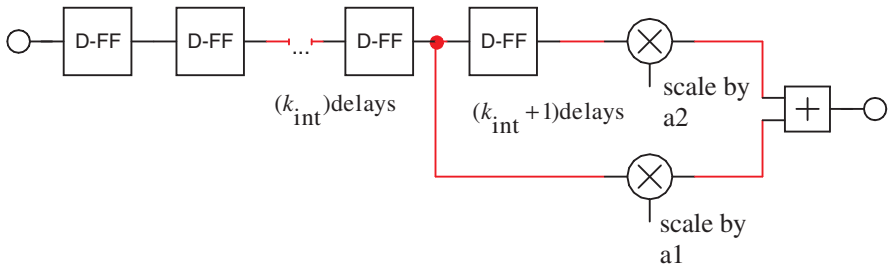

FIG. 34. (Color) Structure of a digital 90° phase shifter for Hilbert transformation.

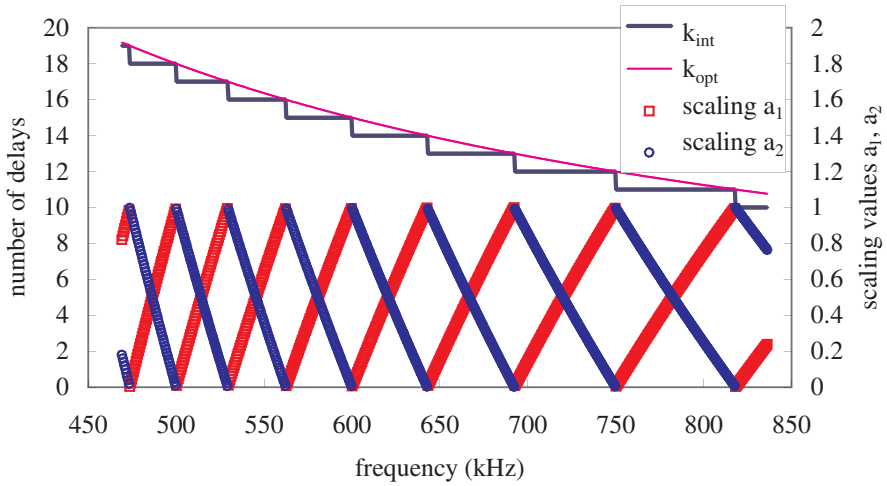

FIG. 35. (Color) Scaling factors to be stored in a pattern memory for a Hilbert transformer tracking the RCS cycle at ($h = 1$).

$$a_1 = \frac{\mp x_2}{y_2 x_1 - y_1 x_2}; \qquad a_2 = \frac{\pm x_1}{y_2 x_1 - y_1 x_2}. \tag{14}$$

Now we insert the transfer function of the delays

$$\begin{aligned} z_1 &= e^{-j2\pi h \cdot k_{\text{int}} \cdot f/f_{\text{clk}}} \\ &= \cos(-2\pi h \cdot k_{\text{int}} \cdot f/f_{\text{clk}}) \\ &\quad + j \sin(-2\pi h \cdot k_{\text{int}} \cdot f/f_{\text{clk}}), \end{aligned} \tag{15}$$

$$\begin{aligned} z_2 &= e^{-j2\pi h \cdot (k_{\text{int}}+1) \cdot f/f_{\text{clk}}} \\ &= \cos(-2\pi h \cdot (k_{\text{int}} + 1) \cdot f/f_{\text{clk}}) \\ &\quad + j \sin(-2\pi h \cdot (k_{\text{int}} + 1) \cdot f/f_{\text{clk}}). \end{aligned} \tag{16}$$

The variation of (k_{int}) and the amplitude scaling factors a_1 and a_2 for the frequency swing of RCS at ($h = 1$) is shown in Fig. 35. $z_1 = x_1 + jy_1$, and $z_2 = x_2 + jy_2$ from Eqs. (15) and (16) were inserted into Eq. (14), and the upper solution was used to obtain positive scaling factors a_1 and a_2. The scaling factors a_1 and a_2, and the variable delay selector (k_{int}) are put into a pattern memory, so that they can be accessed as function of revolution frequency—as in the case of the interpolated CIC filter.

VII. OUTLOOK

The filter structure explained in this document provides a way to translate the idea of a CIC filter for variable clock into designs for fixed clock. In this way, a recipe for notch filters which track a reference frequency is given. These filters have a shorter delay compared to standard FIR applications, so that the stability of loops using these filters is improved. This is important for the high intensity proton synchrotron RCS, where beam loss has to be kept as small as possible. Both filter types (FIR and variable CIC) are realized in FPGA technology, so that we are able to test both configurations in the commissioning phase of RCS. We plan to use this filter structure for the main-ring (MR) of J-Parc, too. In addition, this filter design method can be applied to generate a 90° delay for Hilbert transformation or a "one-turn delay" for fixed clock digital systems.

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