Effective Schottky barrier lowering in silicon-on-insulator Schottky-barrier metal-oxide-semiconductor field-effect transistors using dopant segregation

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We present an investigation of the use of dopant segregation in Schottky-barrier metal-oxide-semiconductor field-effect transistors on silicon-on-insulator. Experimental results on devices with fully nickel silicided source and drain contacts show that arsenic segregation during silicidation leads to strongly improved device characteristics due to a strong conduction/valence band bending at the contact interface induced by a very thin, highly doped silicon layer formed during the silicidation. With simulations, we study the effect of varying silicon-on-insulator and gate oxide thicknesses on the performance of Schottky-barrier devices with dopant segregation. It is shown that due to the improved electrostatic gate control, a combination of both ultrathin silicon bodies and gate oxides with dopant segregation yields even further improved device characteristics greatly relaxing the need for low Schottky barrier materials in order to realize high-performance Schottky-barrier transistors. © *2005 American Institute of Physics.* [DOI: 10.1063/1.2150581]

As scaling of field-effect transistor devices continues, Schottky-barrier metal-oxide-semiconductor field-effect transistors (SB-MOSFETs) are an attractive alternative to conventional-type devices with highly doped source/drain contacts. Due to metallic electrodes in direct contact with the channel, SB-MOSFETs exhibit low extrinsic parasitic resistances, offer easy processing, and allow for well-defined device geometries down to the smallest dimensions. Recent progress in silicidation has renewed the interest in SB-MOSFETs, and devices with excellent high-frequency operation were demonstrated.[1] However, due to the existence of the Schottky barrier (SB), SB-MOSFETs still do not reach the best intrinsic performance achievable in conventional-type devices. A high SB not only results in low on-currents but also causes poor subthreshold behavior. Therefore, intensive research has been devoted to the investigation of low SB silicides.[2] While PtSi provides reasonably low SB for *p*-type devices, an ideal candidate for *n*-type devices is still missing.

Recently, dopant segregation (DS) during silicidation has been used to improve Schottky contacts in SB-MOSFETs (Refs. 3 and 4) and to tune the workfunction of fully-silicided gates.[5] The advantage of DS is twofold: First, the silicidation is carried out at a low temperature; hence, thermally activated dopant diffusion is suppressed leading to steep doping profiles at the silicide-silicon interface (see Ref. 6 and references therein). Second, a very thin highly doped interface layer forms that significantly increases the tunneling probability of carriers through the SB. Here, we investigate the impact of arsenic segregation on the performance of silicon-on-insulator (SOI) SB-MOSFETs with varying SOI and gate oxide thicknesses. Devices with nickel silicide[7] as source/drain electrodes are fabricated that exhibit a significantly improved on-state and an almost ideal off-state. The effect of reducing the SOI and gate oxide thickness on the

effective SB height, and thus on the electrical device characteristics, is explored with simulations.

SOI wafers with a *p*-type doping of 1×10^{15} cm^{-3} are first thinned to ~25 nm by a cycle of dry/wet thermal oxidation and subsequent HF stripping. After mesa isolation, a 3 nm thick gate oxide is grown using a 600 °C wet thermal oxidation.[8] 200 nm *n*-doped polycrystalline silicon is deposited immediately afterward and the gate is formed using reactive ion etching. Only long-channel devices with a channel length of $L=2$ μm and a width of $W=40$ μm are fabricated in order to avoid any influence of short-channel effects. The source and drain areas are then implanted with arsenic [see Fig. 1(a)] at a dose of 1×10^{15} cm^{-2} and an energy of 5 keV. Control samples without any implantation are processed in parallel. Next, SiO$_2$ spacers are generated and nickel is deposited; the last steps include the silicidation and the removal of the superficial Ni [Fig. 1(b)]. For the silicidation, we chose a temperature of 450 °C for 20 s facilitating NiSi encroachment from the source/drain areas into the channel. This is a simple way to ensure that the silicide-silicon interface is well in the gated region without the need for ultrathin spacers. At the same time, the temperature is low enough to
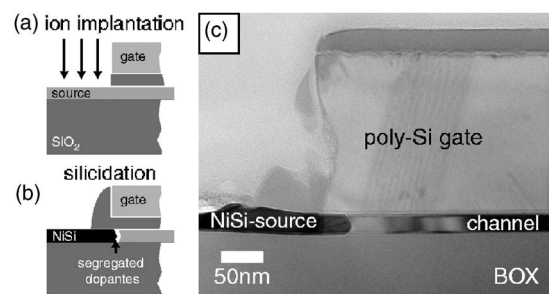

FIG. 1. Schematics of the SB-MOSFET fabrication. (a) Arsenic implantation into the contact regions, (b) spacer formation and silicidation, and (c) TEM image of a readily processed device.
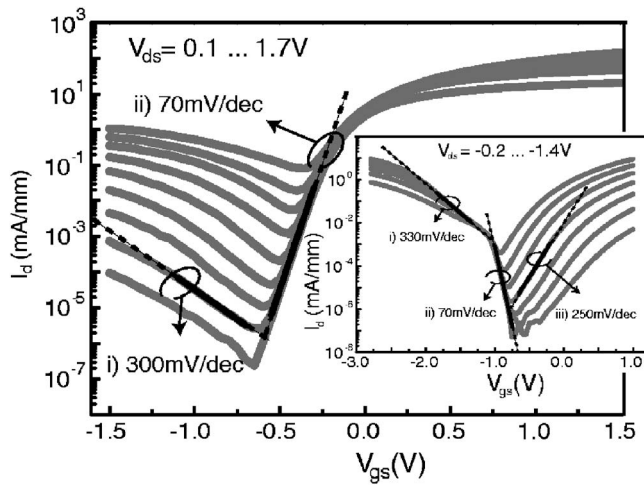
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FIG. 2. Transfer characteristics of a SB-MOSFET with DS. $L=2$ μm, W $=40$ μm, and $d_{ox}=3$ nm. The inset shows transfer characteristics of the same device without DS.

avoid dopant diffusion. Figure 1(c) shows a transmission electron microscope (TEM) cross section of the source region of a readily prepared device. One clearly sees the NiSi encroachment underneath the spacer into the channel region.

The inset of Fig. 2 shows transfer characterisics of a device without DS, exhibiting the typical ambipolar behavior[9] with almost equal current levels in the n-branch and the p-branch. A strong drain-induced-barrier-lowering like (DIBL) effect can be seen in the n-branch since the device is operated as a p-type SB-MOSFET with negative bias. Two different inverse subthreshold slopes with $S_{\text{i)}}$ $=330$ mV/dec and $S_{\text{ii)}}=70$ mV/dec can be extracted from the p-branch, whereas the n-branch exhibits only one slope with $S_{\text{iii)}}=250$ mV/dec. $S_{\text{ii)}}$ is close to the thermal limit meaning that the Fermi level is pinned more closely to the valence band instead of midgap, consistent with the expected SB height of 0.64 eV for electrons and 0.46 eV for holes.[10] The important point, however, is that in the n-branch $S_{\text{iii)}}$ significantly exceeds 60 mV/dec because the increase of current with changing gate voltage is determined by the change of the tunneling probability through the SB.[9,11] (Note, that the thermal part of the subthreshold characteristic of the n-branch is completely masked by the onset of hole conduction as the gate voltage decreases). In this sense, the SB-MOSFET is a "contact switching" device.

Transfer characteristics of SB-MOSFETs with DS are shown in the main panel of Fig. 2. The device still exhibits ambipolar conduction but now the hole branch is somewhat suppressed and the device behaves like an n-type transistor. In addition, the on-current in the n-branch has increased substantially. The most prominent feature of the transfer characteristics, however, is that the inverse subthreshold slope of the n-branch has changed dramatically from ~250 mV/dec to $S_{\text{ii)}}=70$ mV/dec, close to the thermal limit. This means that the device behaves like a "bulk-switching" conventional MOSFET; the reason being a decreased effective SB height due to the highly doped area at the silicide-silicon interface as will be discussed in detail below. It is important to note that since the device still exhibits ambipolar conduction, the DS layer cannot be larger than a few nanometers because otherwise the p-branch would be suppressed more effectively. This is expected from the steep doping profiles

achievable with DS during silicidation meaning that we expect a SB-MOSFET with DS to still offer excellent scalability and geometric control of the source/drain contacts.[12]

In order to gain a better understanding of the influence of DS and the impact of differing oxide and SOI body thicknesses on the device behavior, we have performed quantum simulations of SB-MOSFETs.[11] It has been shown that the electrostatics of fully depleted SOI devices are well captured by a modified one-dimensional Poisson equation.[13] This equation is given by

$$\frac{d^2\Phi_f}{dx^2} - \frac{\Phi_f - \Phi_g + \Phi_{\text{bi}}}{\lambda^2} = \frac{e[\rho(x) + N_{\text{seg}}]}{\epsilon_0\epsilon_{\text{si}}}, \quad (1)$$

where Φ_f, Φ_g, and Φ_{bi} are the surface potential, the gate potential and the built-in potential, respectively; $\lambda = \sqrt{\epsilon_{\text{si}}/\epsilon_{\text{ox}}d_{\text{ox}}d_{\text{si}}}$ is the relevant length scale on which potential variations are being screened. The effect of dopant segregation is accounted for by a step-function-like doping profile of spatial extension ℓ_{seg} and doping concentration N_{seg} right at the contact-channel interfaces. The charge $\rho(x)$ in and current through the channel is calculated employing the non-equilibrium Green's function formalism,[14] where the equation for the charge is solved self-consistently with Eq. (1). After self-consistency is reached, the current is computed according to

$$I_d = \frac{2e}{h}W\int T(E)[f_s - f_d]dE, \quad (2)$$

where $f_{s,d}$ are the Fermi distributions of source/drain and $T(E)$ is given by the Fisher–Lee relation.[15] Here, we assume that the first subband contributes most to the current, and hence the expressions for charge and current are averaged over the direction of W only (see Ref. 16 for details). Higher subbands are accounted for by a numerical factor as in Ref. 17. Finally, ballistic transport is assumed to give an upper estimate of the possible device performance. Although simple, the model reproduces the main experimental observations.

To verify the interpretation of a performance improvement due to an effective SB lowering and to investigate the impact of a varying body and gate oxide thickness on the transistor performance, we have simulated transfer characteristics of SB-MOSFETs with DS ($N_{\text{seg}}=2\times10^{20}$ cm^{-3}, $\ell_{\text{seg}}=2$ nm) and a fixed SB of 0.64 eV for two different body and oxide thicknesses, namely: (1) $d_{\text{ox}}=1$ nm, $d_{\text{si}}=5$ nm and (2) $d_{\text{ox}}=5$ nm, $d_{\text{si}}=25$ nm. A channel length of $L=60$ nm in case of (1) and $L=160$ nm in the case of (2) was found to be sufficient to ensure long-channel behavior. Having calculated $T(E)$, an effective SB height $\Phi_{\text{SB}}^{\text{eff}}$ can be determined by equating $\Phi_{\text{SB}}^{\text{eff}}$ with the energy E, where $T(E)$ has dropped to a specified value.[18] Figure 3(a) shows $\Phi_{\text{SB}}^{\text{eff}}$ as a function of gate voltage where we chose $T(E)=e^{-1}$ as the criterion to determine the effective SB height. The one-to-one change of $\Phi_{\text{SB}}^{\text{eff}}$ with V_{gs} for small gate voltages reflects the fact that $\Phi_{\text{SB}}^{\text{eff}}$ is smaller than the bulk potential in the channel; meaning that in this V_{gs} range, the device behaves like a bulk-switching transistor. This can also be inferred from the conduction-band profile for $V_{\text{gs}}=0$V, shown in Fig. 3(b). Here, the highly doped interface layer ensures that the bands strongly bend downward below the bulk potential barrier in both cases (1) and (2). Hence, an almost ideal off-state can be expected as is actually observed. However, for large gate
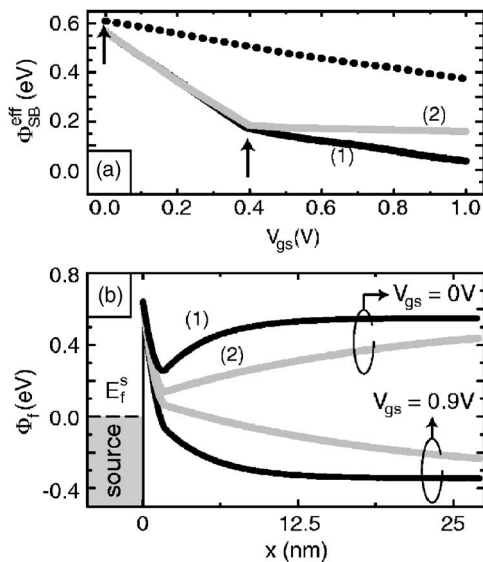
FIG. 3. Effective Schottky barrier height lowering due to DS. (a) Φ_{SB}^{eff} as extracted from the transmission function. The black line belongs to device (1), the gray line to device (2). For comparison, the black dotted line refers to a device of type (1) without DS. (b) The conduction-band profile for $V_{gs}=0$ V and 0.9 V at the source contact for devices (1) and (2).
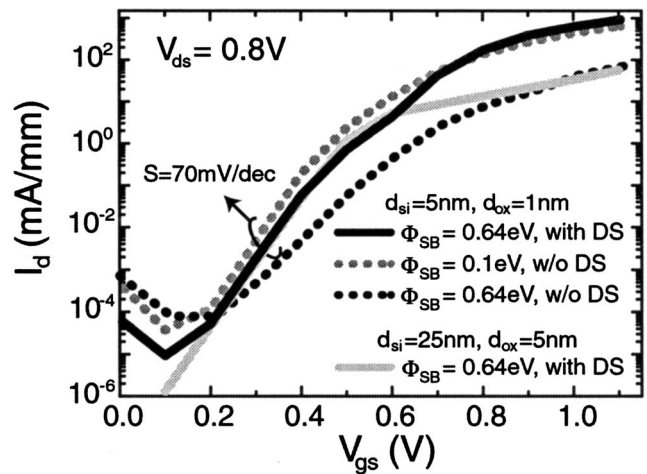

FIG. 4. Simulated transfer characteristics of Devices (1) (black line) and (2) (gray line). The dark gray dotted line belongs to a device of Type (1) without DS and a SB of 0.1 eV, the black dotted line belong to a device without DS and a SB of 0.64.

voltages, i.e., in the devices' on-state, Φ_{SB}^{eff} remains nearly constant in case of device (2). On the contrary, in case (1), Φ_{SB}^{eff} continuously decreases with increasing V_{gs} due to a much better gate control of the potential distribution of the SB in case of ultrathin bodies and oxides. This means that in case (1), a much better on-state can be expected. For comparison, we also plot Φ_{SB}^{eff} for a device of type (1) but without DS in Fig. 3(a) (black dotted line). The curve exhibits the same slope as the device with DS but begins at a much larger SB as indicated by the arrows. Thus, DS strongly reduces the effective SB height. However, the real Φ_{SB}^{eff} has to be determined by a direct comparison of SB-MOSFETs with DS to devices without DS but varying SB height. The reason for this is that DS leads to a change of the shape of the entire SB yielding an increased tunneling probability over a large energy range.

Figure 4 shows transfer characteristics of two devices of Type (1) with DS (black line) and without DS and a SB of 0.1 eV (dark gray, dotted line), along with a device of type (2) (gray line). Both devices with DS exhibit an almost ideal off-state showing that DS has effectively lowered the SB height. However, the on-state is significantly different with a much larger on-current in case (1) with an ultrathin body and oxide as anticipated from the discussion above. For comparison, a device of type (1) without DS and a SB of 0.64 eV (black dotted line) is shown as well, which exhibits an S much larger than 60 mV/dec and an on-current more than one order of magnitude less than the device with DS as expected. More importantly, owing to the increased transmission through the SB, device (1) with DS and $\Phi_{SB}^{e}=0.64$ eV exhibits approximately the same on- and off-state performance as the device without DS and a barrier of 0.1 eV only. As a result, the DS technique in combination with ultrathin body SOI and gate oxide greatly relaxes the requirements for low SB electrode materials and hence allows for high-performance n-type SB-MOSFETs.

In conclusion, we studied the impact of dopant segregation during silicidation on the performance of SB-MOSFETs with varying SOI and gate oxide thicknesses. It was shown that a drastic reduction of the effective SB height could be achieved. Experimental devices exhibited a significantly improved on- and off-state. Simulations show that the use of ultrathin body SOI and ultrathin gate oxides enables an even larger improvement due to a more substantial lowering of the effective SB height. Consequently, DS and ultrathin body/oxide devices allow to combine excellent intrinsic performance with the specific advantages of SB-MOSFETs.

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