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Hysteretic resistance concepts in ferroelectric thin films

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Hysteretic resistance effects based on a correlation between ferroelectric polarization and conductivity might become of particular interest for nonvolatile memory applications, because they are not subject to the scaling restrictions of charge based memories such as the ferroelectric random access memory. Two basic concepts, a metal-ferroelectric-metal structure and a metal-ferroelectric-semiconductor structure are discussed in the literature. This contribution discusses the principle of operation of those concepts in terms of the band model. A generalized model is proposed, which is based on a conductive metal-ferroelectric-semiconductor-metal structure. Here, the existence of a low and a high conductive state originates from a switch of the polarization in the ferroelectric layer and a resulting positive or negative polarization charge at the ferroelectric-semiconductor interface. Charge carriers in the film are attracted by or depleted at the interface giving rise to different local conductivities. By simulation, the effect of internal screening caused by mobile charge carriers on the hysteretic current-voltage behavior and the depolarizing field in the ferroelectric are estimated. The simulation discloses a switching ratio up to several orders of magnitude and a conductivity window, which scales with the donor concentration. It may also explain resistive switching in systems consisting only of one ferroelectric layer by assuming the presence of nonferroelectric interface layers. © *2006 American Institute of Physics*.
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INTRODUCTION

Over the past 15 years, nonvolatile random access memory concepts based on the ferroelectric effect have been studied as the most promising candidate for a future universal memory. Memory cells composed of ferroelectric capacitors unify fast read/write speeds and the random access properties of dynamic random access memory (DRAM) and static random access memory (SRAM) with nonvolatile information storage of flash.[1] Ferroelectric random access memories (FeRAMs) have to compete with other nonvolatile random access memory (NVRAM) concepts such as magnetic random access memories (MRAMs) and phase change random access memories (PCRAMs). The superior performance of state of the art FeRAMs concerning writing speed (some 10 ns), cycling endurance ($>10^{15}$), and power consumption can already be found in a number of commercially available products. The latter mostly address the low density flash and DRAM market segment as well as embedded applications. However, no product is currently available for high density applications. One of the key technological challenges for high density products is to solve scalability issues for the forthcoming FeRAM generations. As well known for charge based devices, in general, a reduction of the cell area of the ferroelectric capacitor is linked to a deterioration of the detectable charge. Since the (measured) charge amounts to twice the ferroelectric polarization times the area of the capacitor and is mostly independent of the thickness, a reduction of the capacitor thickness may not be required to increase the amount of charge. An estimation of the dependence between the minimum detectable charge on the order of 20–30 fC and the required capacitor area of 0.05 μm^2 (for $2P_S=40-60$ $\mu C/cm^2$) shows that the state of the art 64 Mbits FeRAM already approaches the size limit for *planar* capacitor geometries. For a higher level of integration, a three-dimensional (3D) conformal film deposition becomes indispensable, even if improved sensing schemes may shift this need to the forthcoming FeRAM generation. Below the prospected 22 nm technology node of the semiconductor industry, also the 3D concepts for FeRAM reach their limits because of the finite thickness of the ferroelectric and electrode layers.

Memories based on a resistance random access memory (RRAM) change do not exhibit these scaling limits. They might therefore have the higher potential to withstand the ongoing downscaling process compared to charge based memories. Two classes of nonvolatile resistive memories, the ferroelectric field effect transistor and the ferroelectric diode, are discussed in the literature. Here, the ferroelectric effect is used to switch the cell resistance between a high and a low resistive state. In the ferroelectric field effect transistor (FerroFET), the gate dielectric is replaced by a ferroelectric

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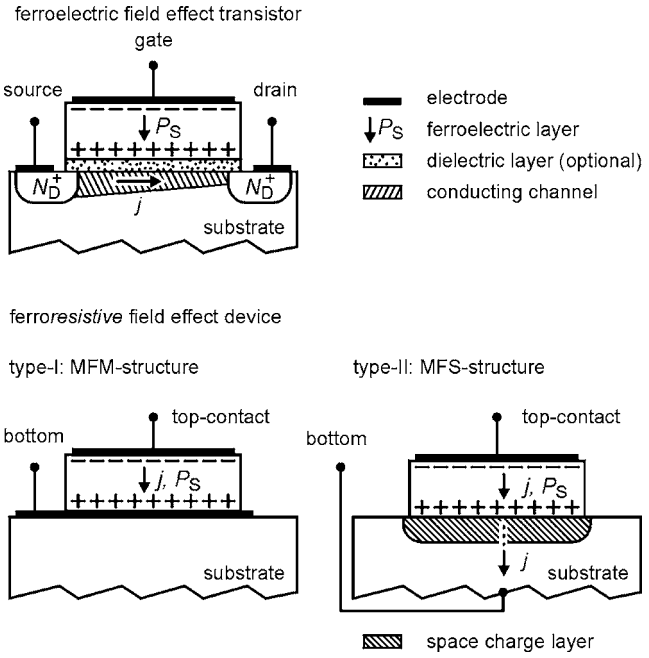

FIG. 1. Current path and ferroelectric polarization of a ferroelectric field effect transistor compared to the MFM structure and the MFS structure of a ferroresistive field effect device. In the field effect transistor, information storage and channel are separated locally; current density and polarization vector are orthogonal. In ferroresistive devices such as ferroelectric diodes, the ferroelectric both acts as storage and transport medium; current density and polarization vector point in parallel or antiparallel direction.

insulator.[2] A sketch of a FerroFET is illustrated in Fig. 1(a). Depending on the orientation of the ferroelectric polarization charge in the gate, charge carriers are attracted or an inversion layer is formed connecting drain and source by a conductive channel. Information storage (in the gate) and conducting path (channel at the substrate/gate interface) are situated in different areas of the device and interfere by the field effect. The polarization vector points *perpendicular* to the current density vector. For technological reasons, ferroelectric gate and substrate might be separated by an additional dielectric layer. However, it remains unclear if FerroFET performance can be improved to meet the requirements for technical applications.[3]

In contrast to the FerroFET, ferroelectric diodes, or more general, ferroresistive switches are two-terminal devices, where the ferroelectric is sandwiched between a bottom and a top electrode. An illustration of a ferroresistive switch is given in Fig. 1(b). Here, the ferroelectric acts both as information carrier and as conductive medium, so that current and polarization point in *parallel* or *antiparallel* direction. The requirements for the ferroelectric layer, namely, being a ferroelectric conductor rather than a ferroelectric insulator, significantly differentiate from those of the FeRAM and the FerroFET.

Our contribution will review the two basic concepts of ferroresistive switches. The third concept will be introduced and discussed on the basis of numerical simulation studies.

FERRORESISTIVE CONCEPTS

Already in 1971, Esaki *et al.*[4] suggested two concepts utilizing the ferroelectric effect in a resistance based memory. They claimed that the orientation of the ferroelectric polarization in a ultrathin ferroelectric bismuth niobate layer processed between two metal electrodes may affect the tunneling probability. As a consequence, an experimentally observed high and low resistive states were attributed to a polarization reversal in the ferroelectric. In a second approach, an ultrathin ferroelectric layer was placed between a metal and a semiconductor. Again, the current through the ferroelectric was assumed to be predominantly due to a tunneling process. The ferroelectric film was assumed to form a dipole layer between the metal and the semiconductor similar to the dipole layer created by interface states at the semiconductor surface and the respective image charge situated at the metal surface.[5] A change in the current-voltage (*I-V*) characteristic was expected from an increase or lowering of the effective contact potential caused by the orientation dependent potential drop over the ferroelectric dipole layer. Since those devices show, in principle, two stable *I-V* characteristics of a Schottky diode, they are often referred to as ferroelectric diodes.

In the early 1990s ferroelectric thin films became available. This development was mostly driven by the need for thin films with high remnant polarization and low leakage current for use in ferroelectric capacitor applications. Simultaneously, a variety of ferroresistive concepts based on high P_S ferroelectrics were developed. The main difference to the ferroelectric tunneling junction proposed by Esaki *et al.* is that the ultrathin ferroelectric layer was replaced by a thin weakly conductive ferroelectric layer. The dominant charge transport mechanism across the two-terminal device was then assumed to follow a drift diffusion or thermionic mechanism, rather than a tunneling related conduction. All devices can be classified in two general concepts. Devices where the ferroelectric is embedded between two metal electrodes will be referred to as type I or metal-ferroelectric-metal (MFM) structure. Devices where one metal electrode is replaced by a highly doped semiconductor will be referred to as type II or metal-ferroelectric-semiconductor (MFS) structure. In general, all devices are based on one principle: a modification of the device resistance is attributed to a change in the inner electric potential. A variation in the potential distribution is accompanied by a change in the charge carrier concentration, which in turn will affect the conduction properties.

Type-I ferroresistive device

Ferroelectric devices of type I consist of a conductive ferroelectric layer embedded between two metal electrodes. A hysteresis in the *I-V* characteristic has been reported for a variety of ferroelectric materials.[6–12] Most devices show a sudden change in the resistance of several orders of magnitude when exceeding a threshold voltage. A conductance change from the "on" to the "off" state or from the off to the on state depends on the polarity of the external voltage. Figure 2(a) displays a *I-V* hysteresis which is representative for most of this devices.

Although hysteresis in the *I-V* characteristic has been found in different ferroelectric material systems and the

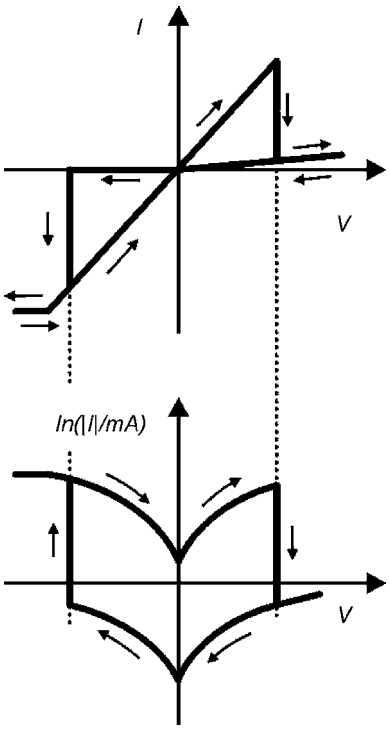

FIG. 2. Characteristic $I(V)$ hysteresis of a MFM structure (a) and a MFS structure (b). MFM structures show an abrupt resistance change of several orders of magnitude. The resistance change of MFS structures is less pronounced and a continuous rather than an abrupt resistance change is observed. Depending on the preparation conditions, a clockwise or counterclockwise sweep of the $I(V)$ curve has been reported.

change in resistance is in most cases several orders of magnitude, which makes the effect highly interesting for memory application as a well as for switchable interconnects. Unfortunately, only little is known about the underlying mechanism. There is an ongoing controversy concerning the nature of the *I-V* hysteresis. Blom *et al.* attributed the resistance change to a polarization and field-dependent dielectric constant. The latter leads to different screening lengths in the (doped) ferroelectric. As a result, different profiles of the inner electric potential and different local conductivities across the film give rise to a polarization dependent conductivity. In a recent paper,[13] we proposed a model of the resistive switching by taking into account nonferroelectric interfacial layers. The presence of nonferroelectric interface layers lead to an incomplete screening of the polarization charge. It was shown that the profile of the inner electric potential accompanies a local enrichment or depletion of charge carrier inside the multilayer stack. The formation of a potential well or potential barrier and the presence of a high or a low conductive state directly correlate with the orientation of the ferroelectric polarization.

The shape of the *I-V* hysteresis, however, observed for ferroelectric thin films is similar to that reported in metal-insulator-metal. In dielectric materials, many indications point to a localized charge transport effect rather than a volume controlled effect.[14,15] Therefore, it cannot ambiguously be excluded that resistive switching in type-I ferroresistive devices is not of ferroelectric nature. Since this question is still under investigation, one has to await the results of current studies.

Type-II ferroresistive device

In type-II ferroelectric device, one metal electrode is replaced by a heavily doped semiconductor.[16–18] A sketch of the a typical *I-V* hysteresis is drawn in Fig. 2(b). If the semiconductor is implemented as a conductive oxide such as *n*-type $SrTiO_3$, the typical charge carrier concentration of the semiconductor electrode might be in the order of 10^{20} cm^{-3}. As a consequence, the screening of the polarization charge at the ferroelectric/semiconductor interface is less efficient as compared to a metal electrode. An electric field penetrates into the semiconductor causing a band bending at the near-interface region. In the following we will discuss the experimentally observed switching in the *I-V* curve in terms of the band diagram. For the sake of simplicity, we will assume an ideal ferroelectric/metal contact, where the polarization charge is screened over an infinitely small distance. The ferroelectric will be treated as single domain. This implies that the polarization is stable even in the presence of a depolarizing field. We will further assume that interfacial trapped charges are negligible at the ferroelectric/semiconductor and metal/ferroelectric interfaces. The work function of the metal and electron affinity of the ferroelectric are chosen to form a highly resistive contact. Band gap, electron affinity, and dielectric constant of the semiconductor and the ferroelectric are identical. Electrons will be regarded as the majority mobile charge carrier. Electron holes will be neglected, unless explicitly mentioned. The above made assumptions might be appropriate to give a first order estimation of the band structure in ferroelectric diodes.

Band diagram

To get a first impression of the band diagram, we will first treat the ferroelectric as a dielectric. In a second step, the dielectric will be replaced by a ferroelectric. The band diagram and inner electric field of a metal-insulator-semiconductor (MIS) structure is illustrated in Fig. 3(a). E_L, E_V, E_G, and E_F denote conduction band, valence band, band gap, and Fermi energy, respectively. Φ_M is the work function of the metal and X_I and d_D refer to electron affinity and thickness of the ferroelectric layer.

If the insulator is replaced by a ferroelectric of the thickness d_F and the electron affinity X_F, an additional polarization charge $\rho_S = -\mathrm{div}\, P_S$ formed by an abrupt decay of the ferroelectric polarization at the ferroelectric/semiconductor interface has to be considered. Figure 3(b) displays the band bending of a MFS structure for a positive polarization charge at the ferroelectric/semiconductor interface ($P_S > 0$). Due to the accumulation of electrons at the ferroelectric/semiconductor interface, the conduction band of the ferroelectric and the semiconductor approaches the Fermi level and a degeneration layer is formed at the semiconductor/ferroelectric interface. As a consequence thereof, the ferroelectric charge is screened by electrons and the effective charge in the vicinity of the interface is reduced. A reduction of the effective interface charge hinders the Fermi energy from further entering the conduction band. A band bending caused by the enrichment of negative charge in a thin near-interface layer will affect the inner electric field as sketched

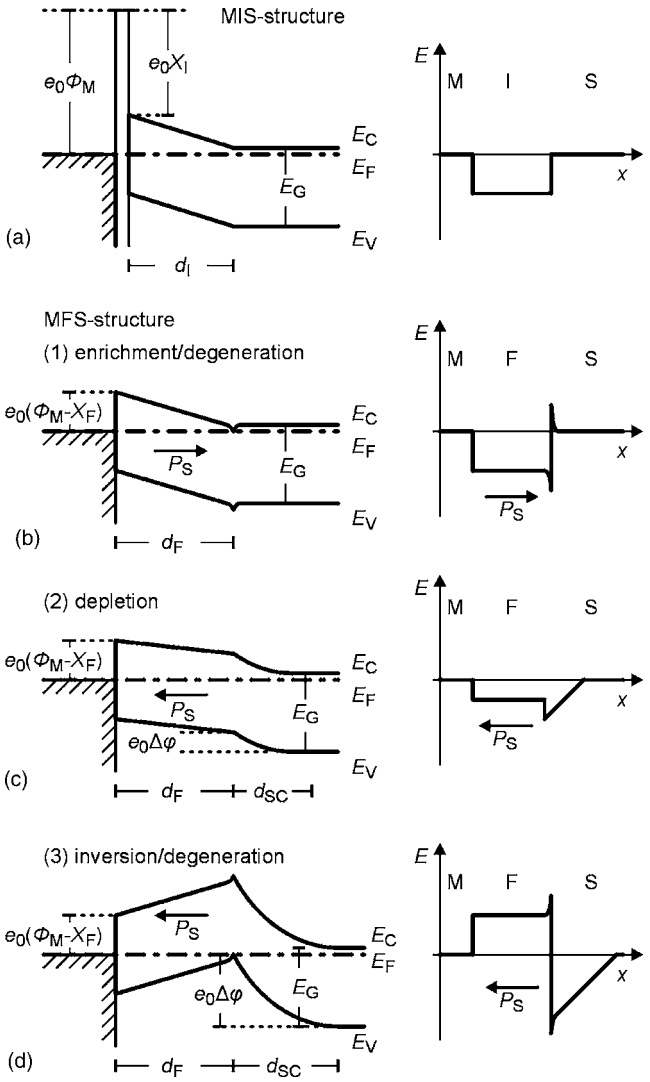

FIG. 3. Sketch of the band diagram and the inner electric field of a MIS structure (a) and a MFS structure for the case of charge carrier enrichment (b), charge carrier depletion, (c) and the formation of an inversion layer (d) at the ferroelectric-semiconductor interface.

in Fig. 3(b). However, only small changes of the potential and the field distribution are found compared to the MIS structure.

Figures 3(c) and 3(d) refer to polarization values of $P_S < 0$ or negative polarization charges at the ferroelectric/semiconductor interface. In contrast to the case discussed above, the interface charge is mainly screened by donor cores located in the semiconductor electrode. Since the screening effect is less efficient compared to an enrichment of electrons, the screening length and the field penetration into the semiconductor is sufficiently larger. Depending on the height of the energy barrier $e_0\Delta\varphi$ formed at the semiconductor surface, the compensation ranges from electron *depletion* or *inversion* to a *p*-type *degeneration* of charge carriers.

The shape of the inner potential displayed in Figs. 3(c) and 3(d) is estimated from Poisson's equation using the Schottky approximation for the space charge layer formed by donor cores. It is assumed that the polarization charge is exclusively compensated by a space charge layer in the semiconductor. Then, the band bending at the semiconductor/ferroelectric interface can be approximated by that of an *n*-type semiconductor surface in the presence of acceptor-type surface charges Q_{SC},

$$\Delta\varphi = \frac{Q_{SC}^2}{2e_0\varepsilon_0\varepsilon_{r,SC}N_D}. \tag{1}$$

N_D denotes the concentration of donors in the semiconductor, $\varepsilon_{r,sc}$ accounts for the dielectric constant of the semiconductor, and $\Delta\varphi$ is a measure for the band bending. Applied to the MFS structure, the surface charge Q_{SC} will be replaced by the spontaneous polarization P_S. For low values of P_S and high donor concentrations, an electron depleted layer is formed at the ferroelectric/semiconductor interface. The criterion for electron depletion in the semiconductor electrode is then given by

$$\frac{E_G}{2e_0} > \frac{P_S^2}{2e_0\varepsilon_0\varepsilon_{r,SC}N_D}, \tag{2}$$

where E_G is the band gap of the ferroelectric. The criterion for charge carrier inversion in the semiconductor is

$$\frac{E_G}{2e_0} < \frac{P_S^2}{2e_0\varepsilon_0\varepsilon_{r,SC}N_D}. \tag{3}$$

For charge carrier inversion/degeneracy, the following condition must be met:

$$\frac{E_G}{e_0} < \frac{P_S^2}{2e_0\varepsilon_0\varepsilon_{r,SC}N_D}. \tag{4}$$

Reasonable values for the spontaneous polarization of ferroelectric thin films amount to $P_S = 10-50\ \mu C/cm^2$. If heavily *n*-doped $SrTiO_3$ is used as a semiconductor electrode, typical values for the donor concentration and the dielectric constant are in the order of $\varepsilon_{r,sc}=300$ and $N_D=10^{20}\ cm^{-3}$ (e.g., Pt/PZT/*n*-STO system). The respective band bending amounts to 100 meV for $P_S=10\ \mu C/cm^2$ or exceeds half the band gap for $P_S > 35\ \mu C/cm^2$, if we assume a band gap of the ferroelectric is on the order of $E_G=3$ eV at room temperature.[19] However, these values might be underestimated, since the dielectric constant of the electrode will be reduced in the presence of high inner electric fields. Depending on the particular material properties and material combinations, either electron depletion, inversion, or inversion/degeneration of the semiconductor might therefore be realistic scenarios.

For nonvolatile memory applications, a large change of the resistance is desired upon polarization reversal. A change in the barrier height at the ferroelectric/semiconductor interface, however, does not necessarily lead to drastic conductivity changes. The reason therefore is twofold. First, the barrier at the ferroelectric/semiconductor interface $\Delta\varphi$ has to compete with a second barrier being present at the ferroelectric/metal interface. The latter is given by the difference of the metal work function and the electron affinity of the ferroelectric. Only for $\Delta\varphi > (\Phi_M - X_F)$ a significant change in conductivity might be expected at least for small external voltages. If a metal with a high work function such as Pt is chosen, the contact barrier might dominate over the internal barrier. A change in the internal barrier height might

then only have a minor impact on the conductivity. Secondly, for internal barriers $\Delta\varphi$ exceeding half the band gap, variations in the barrier height might not cause significant changes in the resistance. If an inversion layer is present at the interface, a decrease of the electron concentration will coincide with an increase of the electron hole concentration leading to a non-negligible hole conductivity. An effective resistance change upon polarization reversal might therefore only be achievable for

$$\varphi_M - X_F < \frac{P_S^2}{2e_0\varepsilon_0\varepsilon_r N_D} < \frac{E_G}{2}. \quad (5)$$

The formation of an inversion layer at the ferroelectric/semiconductor electrode was reported by Wünfel and Batra.[20] They quoted that a loss of polarization at high frequencies is due to a slow support of charge carriers in the inversion layer to screen the polarization at the ferroelectric/semiconductor interface. This hypothesis was supported by illumination experiments. It could be demonstrated that an optically induced increase of the charge carrier generation rate will restore the ferroelectric properties observed in MFM systems. The formation of an inversion layer might therefore not be favored in ferroelectric diodes, if high switching kinetics are wanted. This is especially the case, if a broad band semiconductor electrode such as donor-doped $SrTiO_3$ is used.

Experimentally, ferroelectric diodes show rather high resistances both for the on and the off state and require high programing voltages. Only small changes in the resistance are reported upon polarization reversal. This phenomenon might either originate from the high contact potential at the metal/ferroelectric interface or from an instability of the spontaneous polarization itself. Most ferroelectric diodes are composed of a lead zinconate titanate (PZT) thin film and a Pt top electrode. If one assumes an electrode work function of $\varphi_{Pt}=5.3-5.5$ V and an electron affinity of the semiconductor of $X_F=3.8-4.2$ V, the contact barrier amounts to approximately 1.5 V. At the contact interface, the Fermi energy might then be located in the middle of the band gap. As discussed in the last paragraph, this configuration might not be favorable, if a polarization switch should significantly change the conductivity. Another reason for the small resistance change might be the instability of the ferroelectric polarization due to depolarizing internal electric fields.

Stability of the ferroelectric polarization

From the band diagram representation, another issue of the ferroelectric diodes becomes obvious, namely, the presence of large electric fields in the ferroelectric layer. A relevant question arising from this fact is whether the ferroelectric polarization is stable in such a configuration or if the field will destabilize the single domain state. The remnant polarization P_R of the ferroelectric layer might then be significantly lower compared to the spontaneous polarization P_S of the material. In general, an electric field present in the ferroelectric may either promote (field in parallel to the spontaneous polarization vector,$\mathbf{E}\uparrow\uparrow\mathbf{P}_S$) or destabilize a polarization state (field antiparallel to the polarization vector, $\mathbf{E}\uparrow\downarrow\mathbf{P}_S$). In the case of an unscreened ferroelectric (no electrodes), however, the inner electric field is formed by the macroscopic polarization charge of the ferroelectric itself, which points in opposite direction to the polarization. Since it destabilizes the ferroelectric polarization, it is referred to as depolarizing field E_{depol}. This depolarizing field can drastically be lowered if the surface polarization charge is screened by the electrodes. The screening efficiency will depend on the charge carrier concentration inside the electrode. A semiconductor electrode will show a lower screening efficiency as compared to a metal electrode. A nonferroelectric interfacial layer being present between ferroelectric and electrode will also reduce the screening. In our particular case, an additional in-build electric field must also be taken into account. It originates from different contact potentials of the metal and the semiconductor electrode giving rise to a gradient in the inner potential, as shown in Fig. 3(a).

For spontaneous polarizations $P_S>0$, no significant change in the potential will be expected. The estimated distribution of the electric field is displayed in Fig. 3(b). Although the field is formed by the contact potential of the electrodes rather than the polarization charges at the ferroelectric surfaces, it points in opposite direction to the polarization. To estimate the inner electric field, we will assume a ferroelectric layer of 100 nm thickness and a potential difference between work function and electron affinity of 1.5 V. Then, the inner electric field amounts to $E_{depol}=150$ kV/cm, which is in the order of the coercive field E_C of typically 20–200 kV/cm. Here, the destabilizing electric field originates from the difference in the work function of the metal and the electron affinity of the semiconductor, rather than from the polarization charges of the ferroelectric itself.

A configuration as shown in Fig. 3(b) might therefore not be stable. Additionally, the resistance might not be affected by the presence of the ferroelectric for small external voltages, since the potential barrier formed at the metal interface will dominate the charge transport characteristic.

For $P_S<0$ the in-build electric field points parallel to the polarization. It will therefore support the respective polarization state by reducing the depolarization field. The sign of the net inner electric field depends on the screening efficiency of the semiconductor. For the case of charge carrier depletion as sketched in Fig. 3(c), the electric field in the ferroelectric layer points in the direction of the polarization. This configuration will therefore be stable. However, only a weak change in the resistance might be expected if applying a small external voltages to measure the resistance, since the potential barrier at the metal/ferroelectric interface exceeds the barrier situated at the ferroelectric/semiconductor interface. If an inversion layer is formed in the semiconductor electrode as shown in Fig. 3(d), the net electric field in the ferroelectric points in opposite direction to the ferroelectric polarization vector. As a consequence, the single domain state will be destabilized and the net ferroelectric polarization will be reduced.

GENERALIZED FERRORESISTIVE CONCEPT

This paragraph will discuss a generalized ferroelectric diode concept, which may improve the memory performance

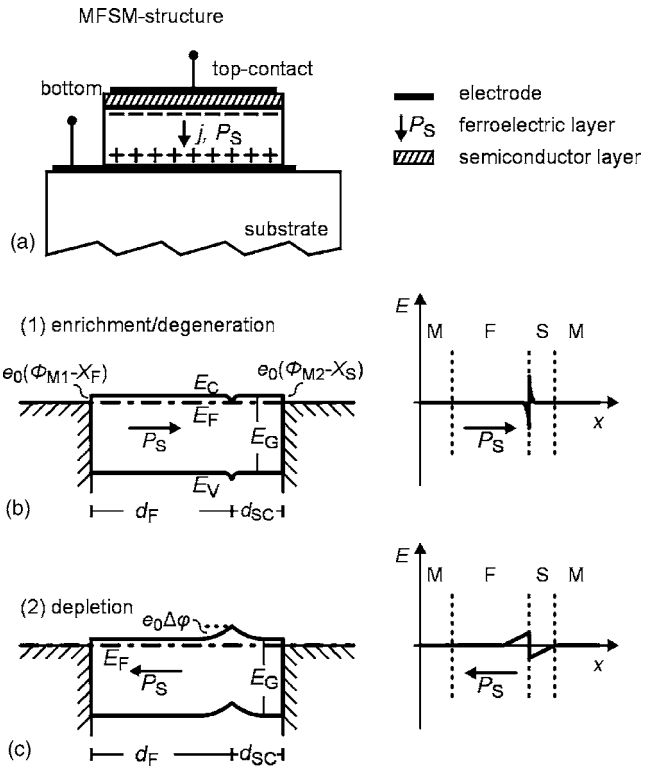

FIG. 4. Layer structure (a), band diagram and inner electric field for a MFSM structure for charge carrier enrichment (b), and charge carrier depletion (c) at the ferroelectric/semiconductor interface.

of ferroelectric diodes. Two main issues, the increase of the device conductivity and the resulting effect of internal screening, will be addressed. The suggested concept comprehends the following modifications.

- Reduction of the contact potential at the top contact to avoid the formation of a charge carrier inversion layer and to reduce the on and the off resistance of the device.
- Donor doping of the ferroelectric to reduce the device resistance and to lower the depolarizing field inside the ferroelectric.
- Replacement of the semiconductor electrode by a metal electrode in combination with a thin *n*-type conductive nonferroelectric layer to allow for an application of sufficiently high fields to the conductive ferroelectric layer.

A cross section [Fig. 4(a)] and a sketch of the band structure of the proposed metal-ferroelectric-semiconductor-metal structure (MFSM) is shown in Fig. 4 for different polarization states [Figs. 4(b) and 4(c)]. The conductivity of the ferroelectric semiconductor and the semiconductor layer results from a high concentration of electrons due to the presence of donors N_D in both layers. It is expected that the rectifying characteristic of the MFSM structure is less pronounced than in ferroelectric diode concepts. The latter is a consequence of the low contact potential at the top electrode and the use of a low work function metal at the bottom electrode. The device will be referred to as ferroresistive random access memory (FRRAM), rather than as ferroelectric diode.

As a consequence of the internal screening, the average depolarizing field in the ferroelectric is reduced, which may stabilize the polarization state. On the other hand, the internal screening will lower the potential barrier at the internal interface. The interface conductivity in the low conductive state will be increased and may deteriorate the switching performance by lowering the on to off ratio. Another question of interest is, how the device characteristic will evolve under large external electric fields as a function of voltage polarity. A finite differences method is applied to estimate the effect of internal screening, the large signal response of the MFSM structure as well as the amplitude of the resistance change.

Numeric model

To study the effect of internal screening more quantitatively, electron redistribution and current response are calculated as a function of the external voltage V_{ext} and the donor content N_D for a ferroelectric polarization parallel and antiparallel to the external electric field. The thicknesses of the ferroelectric and the semiconductor layer are set to 45 and 5 nm, respectively. The dielectric constant of both layers is assumed to be 300. The ferroelectric-semiconductor interface forms a homojunction. The value of the ferroelectric polarization amounts to 10 $\mu C/cm^2$. In a first approximation, the polarization is assumed to be single domain. A split up in a multidomain state and a partial switching of the polarization has not been considered yet. The charge carrier redistribution under the influence of the external and internal electric fields is calculated from the transport equation and the Poisson equation.[21] A drift-diffusion approach is used to estimate the electron current density. The electron mobility is set to 1 $cm^2/V\,s$, which is a reasonable value for the electronic mobility in perovskite-type ferroelectrics. The donor concentration is varied between 10^{17} and 10^{20} cm^{-3}. For the sake of simplicity, neutral contact conditions are applied. The equilibrium electron concentration at the contact interface may then be equal to the electron concentration inside the film, so that no space charge layer is formed due to a contact potential. For a detailed description of the model and the used set of equations, we refer to Refs. 22 and 23.

Electron redistribution at the ferroelectric/semiconductor interface under external field stress

Figure 5 illustrates the calculated redistribution of electrons as a function of the orientation of the ferroelectric polarization and an external voltage for a donor concentration of $N_D=10^{19}$ cm^{-3}. A positive polarization charge at the interface causes an enrichment of electrons. The negative space charge layer of approximately 5 nm is formed. The electron distribution only shows a weak dependency on the external voltage. Negative polarization charges lead to the establishment of an electron depletion layer, which is slightly larger than in the case of electron enrichment. Under external field stress, a significant redistribution of electrons is observed around the interface. The charge carrier concentration at the interface core is minimal, if no field is applied. It increases with voltage giving rise to a nonlinear current voltage char-

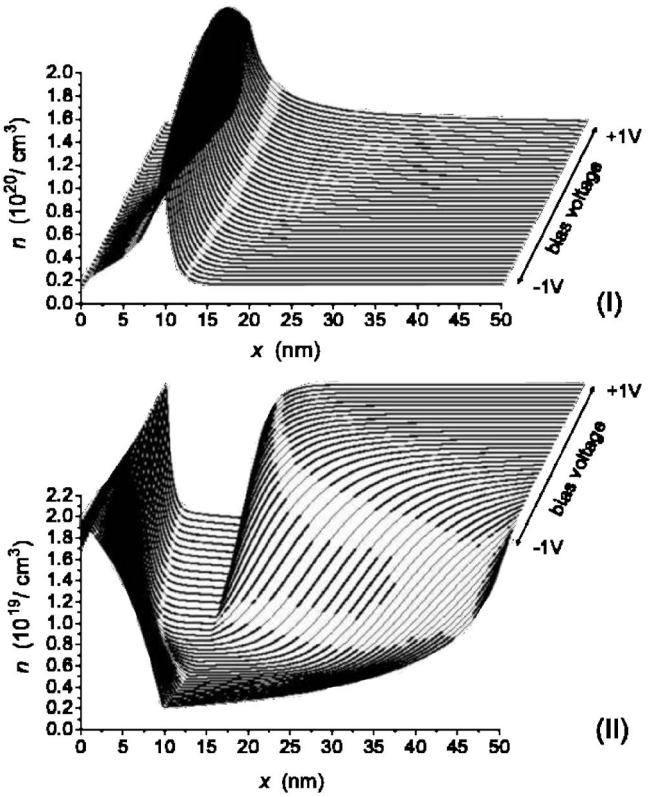

FIG. 5. Electron redistribution inside the MFSM structure at an external voltage of $1\ \mathrm{V} < V_{\mathrm{ext}} < 1\ \mathrm{V}$. For positive polarization charges at the ferroelectric-semiconductor interface (I), electrons are attracted and a negative space charge layer is formed in the vicinity of the interface. Due the enrichment of charge carrier, the conductivity across the structure is enhanced. Negative polarization charges at the interface lead to the formation of a positively charged space charge depletion layer. The depletion of electrons at the interface causes a reduction of the conductivity across the interface.

acteristic. Since the screening length depends on the concentration of fixed and mobile charge carrier in the system, different donor concentrations will show a more or less pronounced screening behavior.

Current voltage relation as a function of donor content

Depending on the screening efficiency at the ferroelectric/semiconductor interface, large (small charge carrier concentration) or moderate changes (large charge carrier concentration) in the resistance are expected. Figure 6 shows an estimation of the current voltage relation of the two-layer system calculated from the steady state drift-diffusion equation for orientations of the polarization parallel or antiparallel to the external field and for different donor contents. Very high charge carrier concentrations close to the degeneration limit of the ferroelectric ($N_D = 1.7 \times 10^{20}\ \mathrm{cm}^{-3}$) lead to an almost linear current voltage relation and small resistance changes in the order of 20%. An increase of the nonlinearity is observed for lower donor concentration of $N_D = 1.7 \times 10^{19}\ \mathrm{cm}^{-3}$. The nonlinearity is more pronounced in the low conductive state and for negative voltages. Here, electrons are injected from the top electrode close to the internal interface. If electrodes are injected from

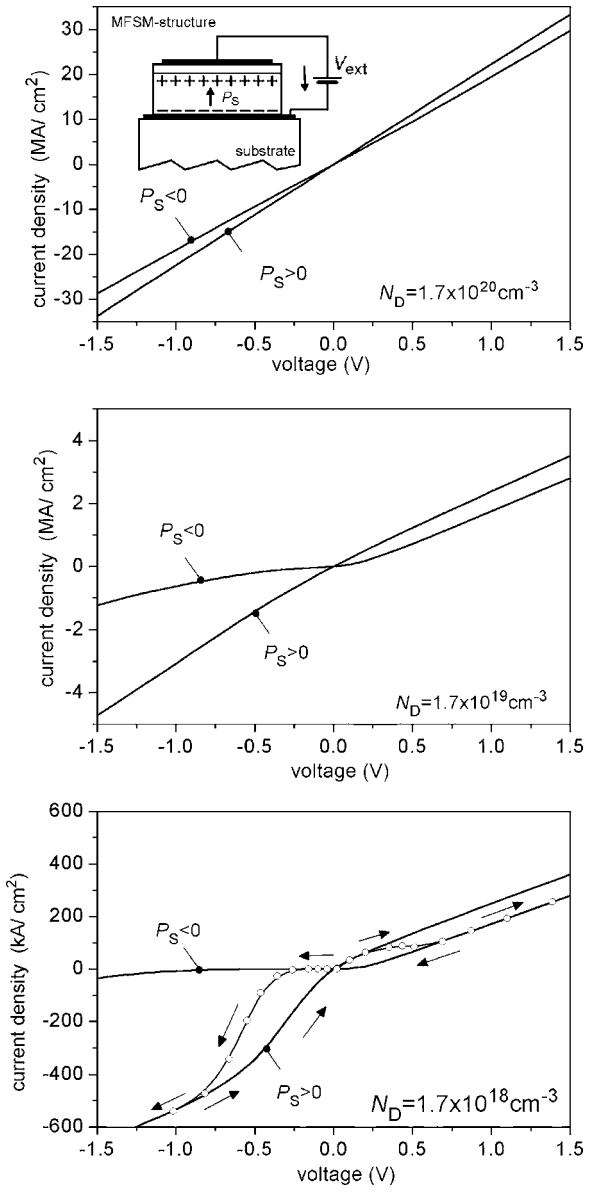

FIG. 6. Estimated $I(V)$ characteristic of the MFSM structure as a function of the ferroelectric polarization for heavy and moderate doping concentrations N_D of the ferroelectric and the semiconductor. The dashed lines and arrows indicate the expected resistance change and the $I(V)$ hysteresis for a voltage sweep under consideration of a polarization reversal.

the bottom electrode, the charge transport is less affected by the interface charge. A resistance charge of one to two orders of magnitude is found for negative voltages. Further reducing the donor content ($N_D = 1.7 \times 10^{18}\ \mathrm{cm}^{-3}$) causes a nonlinear $I(V)$ characteristic for both the high and the low conductive state. Again, the effect is more pronounced, if electrons are injected from the electrode closer to the internal interface. Resistance changes are calculated to several orders of magnitude for negative read voltages. The circles in the lower graph in Fig. 6 indicate the sweep direction expected transition from the low conductive to the high conductive state at negative voltages and from the high conductive state to the low conductive state at positive voltages, if a switching of the ferroelectric polarization is considered. The smooth transition results from the distribution of switching voltages observed in ferroelectric thin films. Although the

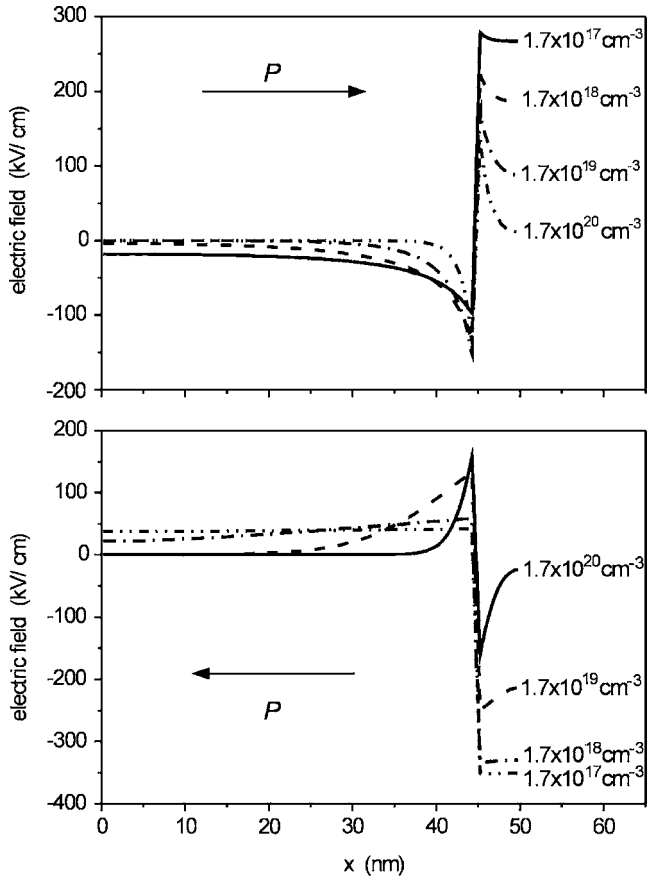

FIG. 7. Electric field inside the MFSM structure under zero bias condition for different polarization states as a function of the donor concentration.

switching ratios estimated here must be regarded as overestimated, since a partial switching of the polarization due to the presence of a depolarizing field in the ferroelectric layer has not been considered yet, experimental studies of a MFSM structure show a pronounced *I-V* hysteresis.[24] The current work is dedicated to the implementation of a more realistic modeling of the ferroelectric polarization, which describes the polarization as a function of the electric field in the ferroelectric.

Screening of the internal electric field as a function of the donor content

A partial back switching of the ferroelectric polarization and the related loss of remnant polarization even under short circuit conditions can be reduced by lowering the depolarization field in the ferroelectric. Figure 7 displays the electric field distribution inside the two-layer structure as a function of the polarization and the donor concentration, if no external field is applied. The field in the ferroelectric is found to be reduced for higher charge carrier concentration. The effect is more pronounced for polarization values $>$ *null* or enrichment of electrons. A large number of mobile charge carrier might therefore help to stabilize the polarization state.

SUMMARY AND CONCLUSIONS

This work addresses the concept of hysteretic resistance effects in ferroelectric thin film structures for memory applications. In particular, the operation principle of ferroelectric diodes and the impact of the ferroelectric polarization charge on the band structure is discussed. Based on the results, a ferroresistive device consisting of a conductive MFSM is proposed. Here, ferroelectric and semiconductor layers reveal a significant electric conductivity leading to an internal screening of the polarization charge at the ferroelectric-semiconductor interface. Numerical methods are applied to estimate internal charge carrier redistribution and the current-voltage relation as a function of the external voltage as well as the donor concentration. The inner electric field distribution and the evolution of the depolarizing field in the ferroelectric under short circuit conditions are studied for different donor contents. The results of this work may encourage experimentalists to study resistive switching in ferroelectric multilayer structures or ferroelectric diodes. It might also provide a better understanding of resistive switching phenomena in MFM structures by taking into consideration nonferroelectric interfacial layers.

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