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Citation: Appl. Phys. Lett. **92**, 122910 (2008); View online: https://doi.org/10.1063/1.2903707

View Table of Contents: http://aip.scitation.org/toc/apl/92/12

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Low current resistive switching in Cu-SiO₂ cells

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(Received 29 January 2008; accepted 9 March 2008; published online 27 March 2008)

Resistive switching in $Ir/SiO_2/Cu$ memory cells was investigated. The proposed switching mechanism is the formation and dissolution of a Cu filament. Under positive bias, Cu cations migrate through SiO_2 and are reduced at the counterelectrode forming a filament. The filament is dissolved under reverse bias. The write current can be reduced down to 10 pA which is four orders of magnitude below published values and shows the potential of extremely low power-consuming memory cells. Furthermore, a comparison of the charge flow in the high resistance state and the energy for writing is given for write currents between 25 pA and 10 nA. © 2008 American Institute of Physics. [DOI: 10.1063/1.2903707]

Nonvolatile memory cells based on anion or cation migration through a solid electrolyte are highly interesting due to the prospect of low power consumption, high scalability, and multibit data storage. Anion migration-based memory devices use, e.g., TiO₂, ^{2,3} NiO, ⁴ or Cr-doped SrZrO₃ (Refs. 5 and 6) as resistively switching material. Mainly, a filamentary switching mechanism based on mobile oxygen vacancies is proposed. Memory cells based on chalcogenides such as $Ge_x Se_{1-x}^{1-8} Ge_x S_{1-x}^{-9} Cu_2 S_{1}^{10}$ or $Ag_2 S$ (Ref. 11) belong to the group of cation migration-based devices. An oxidizable electrode metal such as Ag or Cu serves as cation source under positive bias. The metal ions move through the chalcogenide which acts as solid electrolyte and are reduced at the inert counterelectrode. From there, a metallic filament grows toward the oxidizable electrode and switches the initially high resistive cell to a low resistance state (on). Under reverse bias, the metallic filament is dissolved and the memory cell switches back to the high resistance state (off). Surprisingly, the same resistive switching effect was observed for SiO₂. Pure SiO₂ is typically not considered to be a solid electrolyte but it is used as an excellent insulator. Initially, a thermal forming step was required during which it was assumed that the metal partially dissolves in the SiO₂. ^{12,13} Here, we report about a SiO₂ system which does not show this requirement. In Ref. 13, unipolar or bipolar resistive switching was found depending on the write current. In the case of the bipolar switching, the characteristics are very similar to those observed in Ag-Ge-Se or Cu-Ge-S so that the same switching mechanism based on the electrochemical formation and dissolution of a Cu filament is also proposed for the Cu/SiO₂ cells.

In this study, we demonstrate very low current resistive switching in sputtered Cu/SiO₂ cells with switching voltages of several hundred millivolts and write currents down to 10 pA. The majority of devices could be formed during the first current-voltage (*I-V*) sweep with a current as low as 10 nA.

The memory cells were structured by optical lithography and a lift-off process in acetone. A 20 nm SiO₂ layer was deposited by radio-frequency sputtering at 600 W and

25 SCCM (SCCM denotes cubic centimeter per minute at STP) Ar flow on an Ir bottom electrode plug with a diameter of 86 nm. The Rutherford backscattering analysis showed that the SiO₂ layer was stoichiometric and its density did not significantly differ from that of thermally grown SiO₂. The 50 nm Cu top electrode was deposited by dc sputtering at 150 W and 10 SCCM Ar flow. A schematic of the cell structure is shown in Fig. 1. The electrical characterization was done on an Agilent B1500A semiconductor device analyzer and a Keithley 4200 semiconductor characterization system at room temperature.

Initially, the memory cells were in a high resistance state. Different from Cu/SiO2 devices with e-beamevaporated oxide and metal, ^{12,13} a thermal formation process was not necessary before resistive switching could be observed in the sputtered Cu/SiO₂ cells. Instead, the first (*I-V*) cycle can be regarded as a forming step. During this cycle, the write current could be as low as 10 nA to achieve a stable on state but the switching voltage for reaching the on state was higher than in the consecutive cycles. A possible explanation is that the Cu filament has to be formed once and later on switching takes place at the interface of the Cu dendrite and the Cu electrode. 14,15 Out of 30 measurements on one sample, 63% of the devices could be formed at 10 nA which is many orders of magnitudes lower than the forming currents necessary in other resistively switching materials, e.g., in TiO₂. The rest of the devices needed higher currents to achieve a stable on state and repetitive switching. After forming, the write current could be reduced again.

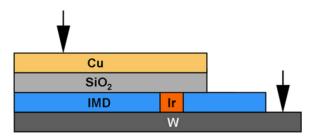


FIG. 1. (Color online) Schematic of the memory cell structure. The inter metal dielectric has a contact window with a diameter of 86 nm for the bottom electrode plug.

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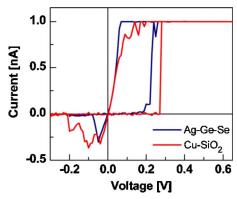


FIG. 2. (Color online) *I-V* characteristic of an $Ir/Cu-SiO_2/Cu$ electrochemical metallization cell written at 1 nA. The voltage was increased stepwise at a rate of 10mV/10 ms. The switching characteristic of a Pt/Ag-Ge-Se/Ag cell (Ref. 16) is shown for comparison.

A typical *I-V* characteristic for a write current of 1 nA is shown in Fig. 2. The switching voltages and the erase current level were very similar to Ag–Ge–Se cells¹⁶ which is shown as well for comparison. Therefore, the same switching mechanism based on the formation and dissolution of a metal filament between the electrodes is proposed for the Cu/SiO₂ cells. Similar to Ag–Ge–Se memory devices, the voltage did not immediately drop to a constant value as soon as the write current was reached under positive bias. ¹⁶ This shows that the on state was dependent on the charge supplied for the redox reactions.

A further reduction of the write current down to 10 pA could be achieved by increasing the time for the double I-V sweep from -0.5 V to 2.5 V to several minutes. This write current is four orders of magnitude smaller than the value reported in Ref. 13. The I-V characteristic for this extremely low write current is shown in Fig. 3. Even for a write current of 10 pA, the resistance ratio between off and on state at 80 mV was still \sim 10.

Figure 4 shows the charge flowing before the off-on transition for write currents varying from 25 pA to 10 nA. Even for the tolerant assumption of a cylindrical filament with a diameter of 25 nm, the charge flow before switching on with a write current of 25 pA was by a factor of $\sim\!100$ higher than expected if all charges were assumed to correspond to Cu ions forming the filament. Therefore, significant electronic leakage occurred, maybe due to tunneling via Cu clusters within the oxide. The leakage increased with increasing cycles and write currents. This tendency is shown in Fig. 4 by the vertical lines corresponding to the standard

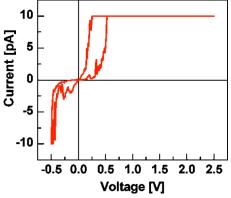


FIG. 3. (Color online) *I-V* characteristic of an Ir/Cu-SiO $_2$ /Cu cell written at 10 pA. The off-on resistance ratio at 80 mV is \sim 10.

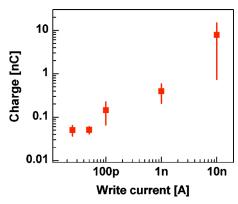


FIG. 4. (Color online) Charge flowing before off-on transition for various write currents. For higher write currents, the leakage current significantly increased after a few cycles. The vertical lines show the standard deviation on logarithmic scale.

deviation. For a write current of 10 nA, a properly erased device showed the same charge before the off-on transition as for a write current of only 25 pA. However, after a few cycles, the leakage current increased, probably due to remaining Cu within the oxide. The write energy was calculated by integration of the I-V characteristic before the off-on transition and multiplication with the elapsed time. An average energy of only 24 nJ was necessary for a write current of 25 pA, and due to leakage, the energy value increased to 3.3 μ J for a write current of 10 nA.

Resistive switching in $Ir/SiO_2/Cu$ memory devices was investigated. A forming cycle was necessary before repetitive switching could be observed. Devices with sputtered SiO_2 allowed for a reduction of the write current to 10 pA. For this very low write current, the off-on resistance ratio was still ~ 10 . The energy for writing was as low as 24 nJ for a write current of 25 pA. The evaluation of the charge flow before the off-on transition showed that not all charges corresponded to Cu atoms forming the filament in the on state. There was still electronic leakage maybe due to tunneling within the SiO_2 via Cu clusters.

This work was supported by IMI-NFG, Lehigh University, USA (NSF Grant No. DMR-0409588). The supply of wafers with prestructured bottom electrodes by Samsung Electronics, Korea is gratefully acknowledged.

¹R. Waser and M. Aono, Nat. Mater. **6**, 833 (2007).

²B. J. Choi, D. S. Jeong, S. K. Kim, C. Rohde, S. Choi, J. H. Oh, H. J. Kim, C. S. Hwang, K. Szot, R. Waser, B. Reichenberg, and S. Tiedke, J. Appl. Phys. 98, 033715 (2005).

³D. S. Jeong, H. Schroeder, and R. Waser, Appl. Phys. Lett. **89**, 082909 (2006)

⁴D. C. Kim, S. Seo, S. E. Ahn, D.-S. Suh, M. J. Lee, B.-H. Park, I. K. Yoo, I. G. Baek, H.-J. Kim, E. K. Yim, J. E. Lee, S. O. Park, H. S. Kim, U.-I. Chung, J. T. Moon, and B. I. Ryu, Appl. Phys. Lett. 88, 202102 (2006).
⁵A. Beck, J. G. Bednorz, C. Gerber, C. Rossel, and D. Widmer, Appl. Phys. Lett. 77, 139 (2000).

⁶C. Rossel, G. I. Meijer, D. Bremaud, and D. Widmer, J. Appl. Phys. 90, 2892 (2001).

⁷K. Szot, W. Speier, G. Bihlmayer, and R. Waser, Nat. Mater. 5, 312 (2006)

⁸M. N. Kozicki, M. Park, and M. Mitkova, IEEE Trans. Nanotechnol. 4, 331 (2005).

⁹M. N. Kozicki, M. Balakrishnan, C. Gopalan, C. Ratnakumar, and M. Mitkova, *Proceedings of the NVMTS*, 2005, Vol. D5, pp. 1–7.

¹⁰S. Kaeriyama, T. Sakamoto, H. Sunamura, M. Mizuno, H. Kawaura, T. Hasegawa, K. Terabe, T. Nakayama, and M. Aono, IEEE J. Solid-State Circuits 40, 168 (2005).

- ¹¹K. Terabe, T. Hasegawa, T. Nakayama, and M. Aono, Nature (London) 433, 47 (2005).
- ¹²M. Balakrishnan, S. C. Puthen Thermadam, M. Mitkova, and M. N. Kozicki, *Proceedings of the NVMTS*, 2006, pp. 104–110.
- ¹³C. Schindler, S. C. Puthen Thermadam, R. Waser, and M. N. Kozicki, IEEE Trans. Electron Devices **54**, 2762 (2007).
- ¹⁴K. M. Kim, B. J. Choi, Y. C. Shin, S. Choi, and C. S. Hwang, Appl. Phys. Lett. **91**, 012907 (2007).
- ¹⁵X. Guo, C. Schindler, S. Menzel, and R. Waser, Appl. Phys. Lett. **91**, 133513 (2007).
- ¹⁶C. Schindler, M. Meier, M. N. Kozicki, and R. Waser, *Proceedings of the NVMTS*, 2007, pp. 82–85.