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Lifetime estimation due to imprint failure in ferroelectric SrBi₂Ta₂O₉ thin films

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Two different failure modes for a ferroelectric memory cell caused by imprint, the read failure due to the loss of polarization, and the write failure due to the shift of the hysteresis loop are investigated. The quasistatic hysteresis loop allows us to distinguish which failure mode is dominating in a ferroelectric random access memory application and, hence, it can also be used as a powerful tool for lifetime estimation of ferroelectric thin films limited by imprint failure under operating conditions. The experimental results show that the write failure is only decisive for very low voltage operation ($V_p \le 1.25 \text{ V}$), whereas for the Pt/SrBi₂Ta₂O₉/Pt under investigation the read failure is the dominant failure mode for operating voltages exceeding 1.25 V. © 2000 American *Institute of Physics.* [S0003-6951(00)02503-1]

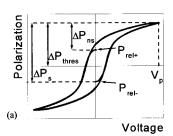
 $SrBi_2Ta_2O_9$ (SBT)¹⁻³ and Pb(Zr,Ti) O_3 (PZT)⁴ thin films are promising candidates for the use as ferroelectric materials in nonvolatile ferroelectric random access memories (FeRAMs). Besides fatigue and retention failure, imprint failure is one of the important failure mechanisms for these ferroelectric thin films. In general, two different mechanisms are discussed in the literature to explain the imprint effect in ferroelectric materials, the alignment of defect dipoles, ^{5,6} or the trapping of charges near the electrode thin film interface.^{5,7} Imprint affects the ferroelectric behavior of the thin films in two ways. On the one hand, a shift of the ferroelectric hysteresis loop on the voltage axis is observed and, on the other hand, imprint also leads to a loss of remanent polarization. Hence, imprint can lead to two different failure modes of a memory cell. First, the voltage shift might become too large so that the programming voltage cannot switch the ferroelectric capacitor (write failure). Second, if the loss of polarization is dominant the sense amplifier cannot distinguish between the two logic states (read failure). Many groups have reported imprint investigations on PZT and SBT thin films in the past by either evaluating the voltage shift or asymmetries in the pulse response.⁵⁻¹⁷ From a device point of view, it is most important to provide a method to estimate the lifetime of a ferroelectric capacitor limited by imprint under operating conditions. Hence, the question arises, which one of the two imprint effects (write or read failure) is dominating and leads to a cell failure and, more important, what is the precise criterion for cell failure?

Thus, the aim of this work is to evaluate the time dependence of both the voltage shift and the loss of polarization. Based on this analysis is a precise criterion for cell failure is defined and a tool for lifetime extrapolation is presented. Details about the sample preparation and the measurement procedures provided by the aixACCT Analyzer can be found elsewhere.16,18

In Fig. 1(a) the operation principle of a FeRAM cell is sketched. The two logic states can be assigned to the two opposite orientations of remanent polarization. To read out the stored information a voltage pulse (V_p) is applied to the ferroelectric capacitor, which drives the capacitor into the positive saturation $[P(V_p)]$. The sense amplifier uses the difference between $\Delta \dot{P}$ and a threshold polarization $(\Delta P_{\rm thres})$ to distinguish between the switching and the nonswitching case (i.e., stored "0" or "1")

$$\Delta P_s - \Delta P_{\text{thres}} > 0 \Rightarrow \text{switching case}$$
 (1)

$$\Delta P_{\rm ns} - \Delta P_{\rm thres} < 0 \Rightarrow$$
 nonswitching case. (2)



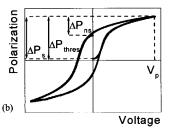


FIG. 1. (a) Hysteresis loop of a virgin ferroelectric capacitor showing the location of the coercive voltage (V_{c+}, V_{c-}) and of the relaxed remanent polarization $(P_{\text{rel}+}, P_{\text{rel}-})$; introduction of the threshold polarization $(\Delta P_{\text{thres}})$ and of the change of polarization in the switching and nonswitching case $(\Delta P_s, \Delta P_{ns})$. (b) Hysteresis loop of a capacitor after imprint treatment (150 °C 100 000 s, 2 V bias).

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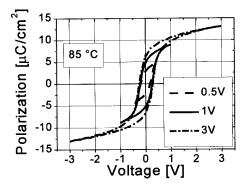


FIG. 2. Quasistatic hysteresis loops (85 $^{\circ}$ C) with varying driving voltage (SBT, 190 nm).

For a symmetrical initial hysteresis loop the threshold polarization is equal to the polarization value at the programming voltage $\Delta P_{\text{thres}} = P(V_p)$.

Notice that ΔP_s and $\Delta P_{\rm ns}$ are determined by the difference between $P(V_p)$ and the relaxed values of polarization $(P_{\text{rel}+} \text{ and } P_{\text{rel}-})$. These relaxed values of polarization are smaller than the dynamically measured ones, i.e., obtained under continuous triangular (100 Hz) voltage excitation. However, for the device operation this relaxation has to be taken into account. 18 Figure 1(b) shows an hysteresis loop of an SBT capacitor after imprint treatment (150 °C at +2 V bias for 100 000 s). Establishing a *positive* polarization leads to a loss of the negative relaxed polarization $P_{\text{rel}-}$ and, additionally, to a shift of the hysteresis loop to the left. The value of $P_{\rm rel-}$ even changed its sign. In that case the loss of the remanent relaxed polarization $P_{\text{rel}-}$ would lead to a read failure of the memory cell. Based on these considerations, the following criteria for the read and the write failure can be defined. (i) The read failure occurs when the sense amplifier cannot distinguish between the different polarization states. This happens when one relaxed remanent polarization $(P_{\text{rel}+}, P_{\text{rel}-})$ drops to zero. Hence, the failure criterion for the read failure can be defined as the point when the loss of polarization equals the value of the relaxed polarization states of the initial hysteresis loop. (ii) On the other hand, the write failure occurs when the ferroelectric capacitor cannot be switched sufficiently to the opposite polarization state. To switch a ferroelectric, a sufficiently high voltage V_{\min} has to be applied so that the resulting remanent polarization $P_{\rm rel}$ is high enough to meet the circuit design requirements. In the case of SBT V_{\min} amounts to approximately 1 V (Fig. 2). Hence, the failure point due to the write failure depends on the difference between the minimum required voltage (V_{\min}) of the thin film material and the programming voltage (V_p) of the memory device. If the voltage shift $(V_{c,\text{shift}})$ exceeds the difference between $\boldsymbol{V_p}$ and $\boldsymbol{V_{\min}}$ the ferroelectric capacitor cannot be switched sufficiently, resulting in a write failure. Hence, the precise failure criterion for the write failure can be defined as the point when the voltage shift $(V_{c,\text{shift}})$ equals the difference between the programming voltage of the memory cell and the minimum required voltage (V_p) $-V_{\min}$) of the ferroelectric capacitor.

Since the failure criteria are defined, a lifetime estimation due to imprint failure can be obtained by the analysis of the time dependence of these two effects and an extrapolation to the required lifetime of the device. In Fig. 3(a) the

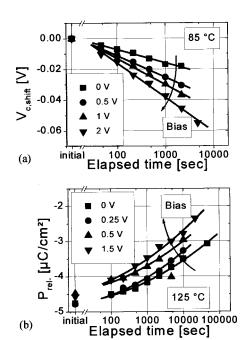


FIG. 3. Time dependence of imprint as a function of the applied bias: (a) linear time dependence (log scale) of the voltage shift ($V_{c,\rm shift}$). (b) Nonlinear time dependence of the loss of relaxed polarization ($P_{\rm rel}$) (SBT, 190 nm)

time dependence of the voltage shift is plotted for different applied biases during an imprint treatment. In good approximation a linear dependence is obtained on a log scale. Hence, the lifetime of the ferroelectric limited by the write failure can be easily estimated by extrapolating this linear dependence of the voltage shift ($V_{c,\text{shift}}$) to the failure criterion $V_p - V_{\min}$. However, for the read failure no linear dependence for the polarization loss versus time is observed [Fig. 3(b)]. Hence, the extrapolation for the read failure seems to be more difficult. A careful evaluation, however, reveals a correlation between the loss of polarization and the voltage shift. Plotting the relaxed values of polarization $[P_{\rm rel}(t)]$ versus the corresponding values of the voltage shift with reversed sign $[-V_{c,\text{shift}}(t)]$ reveals a correlation of these two effects in a way that $P_{\text{rel}}(t)$ vs $-V_{c,\text{shift}}(t)$ lie within the dynamically measured hysteresis loop. Taking the quasistatic hysteresis loop¹⁸ into account one finds that $P_{\rm rel}(t)$ vs $-V_{c,\rm shift}(t)$ fit very well on the quasistatic hysteresis loop [Fig. 4(a)]. This correlation becomes clearer by the following considerations: the relaxed values of polarization are the starting points of the dynamic hysteresis loop [Fig. 4(b)]. In good approximation the imprint treatment causes the same shift $(V_{c,\text{shift}})$ of the dynamic as well as of the quasistatic hysteresis loop. But still, after the imprint treatment the starting points of the shifted dynamic loop fit on the shifted quasistatic loop [Fig. 4(b)]. Hence, plotting $P_{\text{rel}}(t)$ vs $-V_{c,\text{shift}}(t)$ reveals the static hysteresis loop.

Now, with this correlation each value of the loss of polarization can be assigned to a certain voltage shift and thus the nonlinear time dependence of the polarization loss can be transformed to the linear time dependence of the voltage shift (in log scale). Most important, the failure criterion for the read failure ($P_{\rm rel}$ drops to zero) can be redefined by transforming the loss of polarization to the corresponding voltage shift: the relaxed value of polarization drops to zero when

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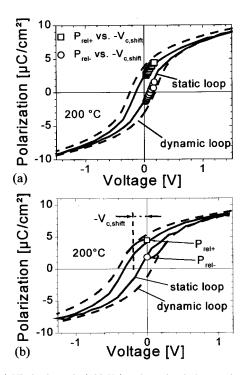


FIG. 4. (a) Virgin dynamic (100 Hz) and quasistatic hysteresis (relaxation time: 1 s) loop at 200 °C; symbols [$P_{\rm rel}(t)$ vs $-V_{c,\rm shift}(t)$] measured during imprint treatment (200 °C, +2 V) fit very well on the virgin quasistatic hysteresis loop. (b) Imprinted dynamic and quasistatic hysteresis loop (200 °C) both shifted by $V_{c,\rm shift}$ to the left (SBT, 1990 nm).

the corresponding voltage shift equals the coercive voltage of the quasistatic hysteresis loop. Thus, the lifetime of the ferroelectric capacitor can be estimated by extrapolating the time dependence of the voltage shift [Fig. 3(a)] to the coercive voltage of the quasistatic hysteresis loop. Since both failure criteria can be expressed by a maximum voltage shift, one can easily judge which failure mode is decisive by comparing the maximum voltage of each failure criterion. Note that it is important to use the quasistatic hysteresis loop for lifetime extrapolations: since the values of the remanent polarization and the coercive voltage of the dynamically measured loops exceed those of the quasistatic loop leading to wrong failure criteria an overestimation of the lifetime of the device is the result. In the following the lifetime of the device is estimated under operating conditions (85 °C). The coercive voltage $(V_{c,stat})$ of the quasistatic hysteresis loop is approximately 0.25 V for hysteresis loops with $V_p \ge 1$ V at 85 °C ($V_{c,\text{stat}} \ge 0.25 \text{ V}$, see Fig. 2) which yields a maximum voltage shift for the read failure of 0.25 V. Thus, the write failure is only dominating for a difference between the programming voltage and the minimum required voltage smaller than 0.25 V ($V_p - V_{min} < 0.25$ V). Since the polarization values of these SBT films meet the design requirements for voltages greater than 1 V (V_{\min} =1 V, Fig. 2) one finds that the write failure is only decisive for very low voltage operations ($V_p < 1.25 \text{ V}$), whereas the read failure determines the lifetime of the device for more realistic values of the operation voltage $V_p > 1.25 \text{ V}$). In Fig. 5 the lifetime extrapolation for an SBT capacitor at 85 °C is shown for two different conditions: (i) establishing and maintaining a remanent state of polarization $(+P_r)$ and (ii) applying a unipolar rectangular excitation signal ($V_{\text{peak}} = 3 \text{ V}, 100 \text{ kHz}$) to the ferroelec-

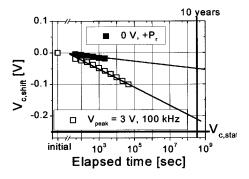


FIG. 5. Lifetime extrapolation at 85 °C for $+P_r$ established and for severe stress condition (unipolar rectangular voltage excitation: $V_{\rm peak}=3$ V, 100 kHz) reveal lifetimes of well over ten years (SBT, 190 nm).

tric which emulates a permanent read and write without changing the polarization state. In Fig. 5 it can be seen that for both cases, even for unipolar stress, a lifetime of well over ten years is estimated.

To summarize, the results presented above show that both failure modes, the read and the write failure, can affect the FeRAM operation. With the quasistatic hysteresis loop a tool is provided to estimate the dominance of each failure mode over the other and to estimate the lifetime of the device. For operation voltages ($V_p > 1.25 \, \mathrm{V}$) the read failure is found to be decisive. That means that at the present 5 V Si logic levels, imprint will limit the read operation but in the 1.1 V Si chips anticipated in the near future, imprint will decisively affect write operations. Lifetime extrapolation at 85 °C reveals a lifetime of the device of well over ten years even under severe unipolar voltage excitation stress.

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