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We report on the fabrication and characterization of lead titanate nanoislands on platinized silicon substrates embedded into a low-k dielectric. Our findings with Pt and Au as collective top electrodes are compared to previous results and thin films, and we discuss the coercive field and the remanent polarization with special care devoted to capacitive and leakage contributions of the nonpolar matrix. A direct electrical characterization of sub-100-nm ferroelectric nanoislands becomes feasible if they are measured in parallel, providing that the thin film material parameters of both ferroelectric and spin-on glass are independently determined. © *2008 American Institute of Physics.*
[DOI: 10.1063/1.2838346]

I. INTRODUCTION

The feasibility of ferroelectric perovskite oxides for application in next generation nonvolatile memory, piezoelectric actuator, or pyroelectric sensor devices strongly depends on their scalability. Therefore, the physical properties of these materials reaching the nanoscale regime are intensively studied at present.[1] Regarding technological issues, new fabrication routes were presented recently, demonstrating the production of large-area high density ferroelectric structure arrays in effective manners.[2–6] Appropriate characterization methods such as piezoresponse force microscopy[7] (PFM) were developed in parallel, capable of detecting piezoelectricity and domain structures with very high spatial resolution. Using PFM, ferroelectricity is detected indirectly in terms of piezoelectric hysteresis loops or piezoelectric phase switching. Hence, the quantification of the remanent polarization requires additional assumptions on the electrostriction and the permittivity of the sample, while the electrical field underneath the very tip is often insufficiently quantified to determine the coercive field. To directly characterize ferroelectric structures electrically and one by one, individual top electrodes are mandatory. The smallest freestanding capacitor structures achieved so far were in the range of 100 nm lateral cell size.[8,9] As the switching charge to detect drops below the background noise for ever shrinking structure dimensions, the smallest capacitors ever electrically characterized were 200×200 nm^2.[10,11]

In order to enable electrical characterization on nanoscale ferroelectric capacitors and to set a step toward further integration, our group recently presented self-assembled lead titanate [PbTiO$_3$ (PTO)] nanograins embedded in a layer of low-k dielectric spin-on glass (SOG) and equipped with collective gold top electrodes.[12] Electrical access to the grain tops was provided using a dedicated chemical mechanical polishing (CMP) step. Switching of the embedded PTO islands was detected, although the collective switching peaks were blurred and at relatively high coercive fields E_c of about 1.5 MV/cm. Using improved polishing parameters and a larger variety of embedding dielectric and electrode materials, we are now able to present *I-V* curves clearly demonstrating symmetric switching of the embedded ferroelectric islands at more reasonable values of E_c.

II. EXPERIMENT

The basic sample setup is shown in Fig. 1. PTO nanoislands are deposited by a modified 2-butoxyethanol based chemical solution deposition process on 1 cm^2 platinized silicon substrates. For details on the chemical synthesis route, see Refs. 13 and 14. A general description of the sample preparation can be found in Ref. 12. Only modifications in sample processing are discussed in the following. Two different low-k dielectric SOG materials, hydrogen silsesquioxane[15] (HSQ) and methyl silsesquioxane (MSQ),[16] are used to embed the ferroelectric islands. Dilution states and spin-coating conditions (e.g., the revolution speeds) are chosen to result in layer thicknesses completely covering the PTO islands (about 70 nm in height). The baking procedure for SOG reflow is carried out on hot plates at temperatures between 80 and 250 °C for 2 min each, depending on which
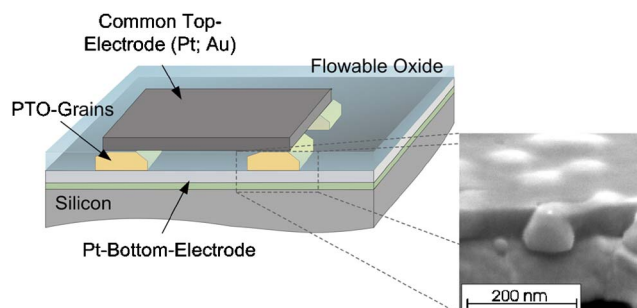

FIG. 1. (Color online) Sample setup of fully embedded PTO nanograins provided with collective gold or platinum top electrodes. The inset on the right shows a cross sectional scanning electron image of an embedded and polished PTO island of about 60 nm in height.

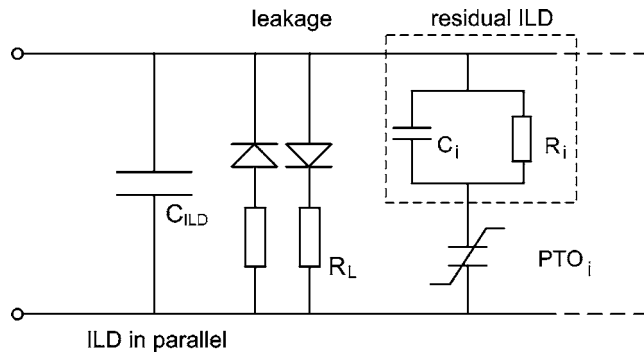a)Electronic mail: schneller@iwe.rwth-aachen.de.

FIG. 2. Equivalent circuit diagram for embedded ferroelectric grains. The exponential leakage current through the film is described by inverse diodes. C_{ILD} represents the total capacitive current through the dielectric materials in parallel to the PTO islands (PTO$_i$). Every distinct PTO island is subject to a residual dielectric layer or a defective boundary layer, leading to capacitive currents next to the ferroelectric switching currents within these in series elements.
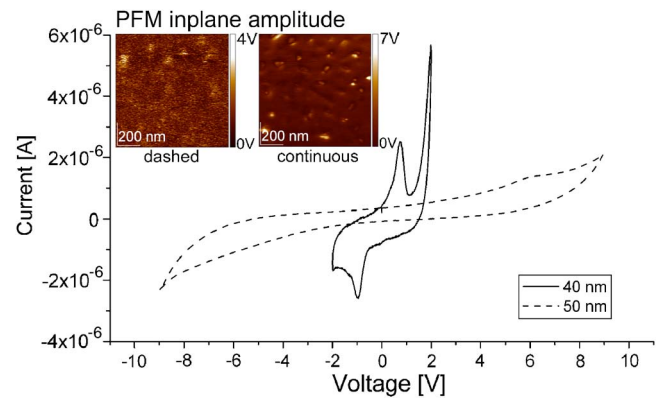

FIG. 3. (Color online) Current response of HSQ embedded PTO grains measured at 100 Hz. The PFM insets indicate a much better electrical contact to the PTO islands for the solid curve (layer thickness: $\approx$40 nm/200 μm diameter Pt electrode) than for the dashed curve (remaining layer thickness: 50 nm/75 μm diameter Au electrode). For comparability reasons, both measurements were conducted under equal settings using the same probe tip with 4 V at 7 kHz.

type of SOG is used. While the HSQ films are cured at 450 °C for 1 h in a rapid thermal processing tool, a diffusion oven is used to cure the MSQ films at a slightly lower temperature of 425 °C, both processes under ongoing nitrogen flow. The resulting surface qualities are comparable to those presented previously.[12] The CMP step used to uncover the PTO grain tops is only slightly modified; i.e., a new type of polishing pad is used,[17] resulting in an even more uniform material removal rate across the sample surface. The polishing rates for the HSQ films vary between 7 and 10 nm/min, and markedly elevated rates up to 30 nm/min are obtained for the MSQ films due to an increased polishing pressure. PFM measurements are carried out to check whether and to what extent the PTO islands are freed from the dielectric matrix after the CMP step by recording the percentage of piezoelectric activity on the sample surface. The polishing step itself is a tradeoff between achieving a good electrical contact to the grain tops congruent to a strong reduction in film thickness and the highly increased risk of going short circuit as the top electrodes are large compared to the remaining layer strength. Two kinds of electrodes are used, thermally evaporated gold and sputter deposited platinum electrodes, both with a minimum diameter of 75 μm. Platinum is chosen to improve the sample and, therefore, switching current symmetry. Electrical characterization measurements are carried out on an AixACCT TFAnalyzer 2000 ferroelectric test system with a FE module. Triangular voltage curves, varying in amplitude and frequency, are applied to the samples, and the current response is recorded. Different contributions to the overall current response become apparent upon inspection of the equivalent circuit diagram in Fig. 2. The ferroelectric switching current is superseded by capacitive and leakage currents through the SOG and PTO grain networks.

III. RESULTS AND DISCUSSION

The importance of removing the SOG layer entirely from the top of the PTO grains in order to obtain clear switching peaks is illustrated in Fig. 3. Here, *I-V* curves were measured on samples polished to different extents. The thin-

ner sample (solid curve) shows increased leakage and capacitive currents, as evidenced by the widening of the curve. Geometrical reasons, the use of larger top electrodes and the reduced sample thickness, as well as the slightly different HSQ and PTO distribution, should result in an about 15 times increased capacitive current. Regarding the dependence of the capacitive current contribution on the derivative of the applied voltage over time, this solely geometrical factor has to be divided by 5, confirming the detected current difference at zero voltage. At the same time, the switching peaks move toward lower coercive fields and are not as smeared out as peaks that appear when the sample is only slightly polished. While for the dashed curve the coercive field can be calculated to 1.2 MV/cm, it decreases to 250 kV/cm in the case of the solid curve, approaching values for PTO thin films.[18]

In order to determine the influence of the dielectric SOG layer in between the nanograins, the solid *I-V* curve already presented in Fig. 3 is compared to an *I-V* curve measured on a PTO thin film in Fig. 4. The PTO thin film was fabricated using the same chemical synthesis route for the precursor solution, applying a precursor dilution of $0.25M$ and four coatings. For details on the PTO thin film processing, see Ref. 18. At large, both measurements show an analog curve progression, varying only in details. As explained for the curves in Fig. 3, the different top-electrode sizes and layer thicknesses and the reduced dielectric permittivity for the HSQ as well as the respective voltage amplitudes used to limit the leakage current lead to the detected current variation factor of about 2 at zero voltage here. Regarding the switching peaks, for the PTO thin film they are more asymmetric, but with a slightly reduced coercive field E_c. A comparison of the respective switching charge, obtained by the integration over the switching peaks, indicates that in the case of the embedded islands, about 5% of the area under the collective top electrode switches (assuming that for the continuous film, 100% of the film contributes to the switching process). Taking the correspondent PFM measurements into account, this value is confirmed. Regarding the leakage cur-
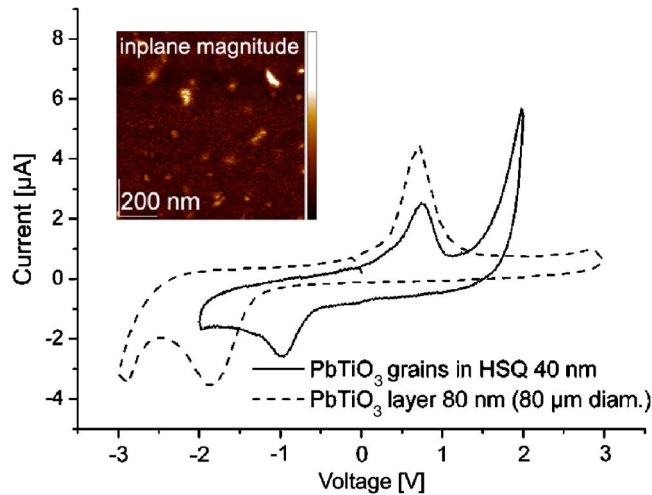
FIG. 4. (Color online) *I-V* curves of HSQ embedded PTO grains (solid) and an about 80 nm thick PTO thin film (dashed) measured at 100 Hz using Pt top electrodes of 200 μm (grains) and 80 μm (thin film) in diameter. The PFM inset on the top left displays the percentage of piezoelectric activity on the embedded PTO grain surface.

rent contribution, it is clearly asymmetric for both samples. In the case of the PTO thin film, leakage can be strongly reduced by post annealing the sputter deposited Pt top electrodes at 700 °C. For embedded PTO grains, a postannealing step results in thermal decomposition of the SOG and the formation of amorphous silicon oxide.[19] The collapse of the porous HSQ or MSQ network involves an increase in refractive index and film shrinkage. Besides, enhanced lead diffusion into the dielectric matrix might result in lead deficient grains and formation of a lead silicate interface layer. Therefore, it was desisted from postannealing the embedded PTO grain samples so far. Nevertheless, it is possible to compensate *I-V* measurements for leakage current numerically. From all appearing current contributions, leakage is the only one that is independent of frequency. Compensated *I-V* curves can be obtained by subtracting curves that are measured at different frequencies according to Ref. 20. Figure 5 displays
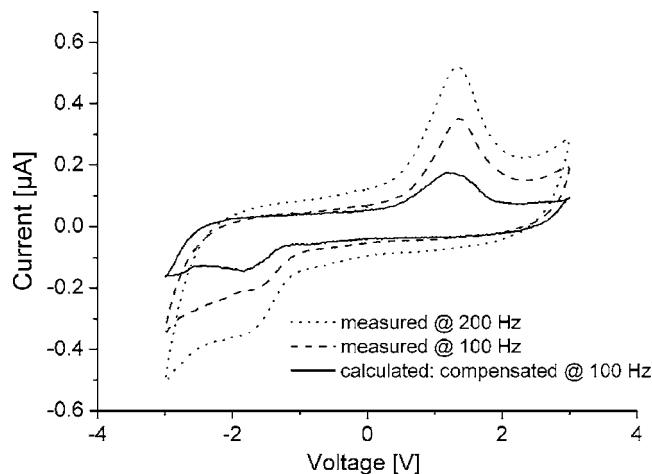

FIG. 5. *I-V* curves of MSQ embedded PTO islands with a remaining layer thickness of about 45 nm measured at different frequencies (dotted/dashed) and calculated compensated curve for the lower frequency of 100 Hz (solid). The measurements were performed under collective Pt top electrodes of 100 μm in diameter.

two measured curves for PTO nanoislands that are embedded and polished in a layer of MSQ (dotted/dashed). As the measurements were performed at 100 Hz and doubled frequency, the compensated curve for 100 Hz is obtained by solely subtracting the recorded *I-V* loops. The outcome is a curve representing the compensated current amount for the lower frequency, in this case for 100 Hz (solid line). As expected, the leakage compensated *I-V* curve is flat, only consisting of a capacitive current contribution resulting in a constant widening of the curve and two switching peaks. Nevertheless, a "leakagelike" current amount remains uncompensated, becoming apparent when regarding the slight increase in current on the negative voltage loop. While the capacitive current contribution results in a slope for the corresponding hysteresis loop that can easily be subtracted, even marginal amounts of leakage inflate it. This hampers an exact identification of ferroelectric parameters such as remanent polarization for the embedded PTO grains at this point, although a first estimation is facilitated. A closer investigation of the frequency dependent and therefore not compensated current contributions through the grain-dielectric matrix network is currently under way.

IV. CONCLUSIONS

In summary, we demonstrated distinct electrical switching peaks for ferroelectric PTO nanostructures. The given results obtained from the optimization of sample processing prove the eligibility of the applied integration route presented previously.[12] *I-V* curves were recorded, only slightly differing from curves that are obtained for continuous PTO thin films. While values for the coercive field can be directly extracted from the *I-V* curves, leakage current compensation enables a first estimation of remanent polarization for ferroelectric nanostructures.

ACKNOWLEDGMENTS

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