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$SmScO_3$ thin films as an alternative gate dielectric

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Samarium scandate thin films deposited on (100) Si have been investigated structurally and electrically. Rutherford backscattering spectrometry and transmission electron microscopy results show that the films are stoichiometric, amorphous, and smooth. X-ray diffraction analysis indicates that $SmScO_3$ starts to crystallize at 900 °C. Capacitance and leakage current measurements reveal *C-V* curves with negligible hysteresis, a dielectric constant around 29 for 6 nm thick films, low leakage current densities in the range of 10^{-7} A/cm^2, an effective oxide charge density of $\sim 5 \times 10^{11}$ (cm^{-2}), and an interface trap density of 4.5×10^{11} (eV cm^2)$^{-1}$. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2968660]

The dielectric SiO_2 has been the key to the tremendous improvements in Si-based metal-oxide-semiconductor (MOS) device performance over the past four decades. It has, however, reached its limit in terms of scaling since it exhibits a leakage current density higher than 1 A/cm^2 and does not retain its intrinsic physical properties at thicknesses below 1.5 nm.[1,2] In order to overcome these problems and keep Moore's law ongoing, the use of higher dielectric constant (κ) gate oxides has been suggested. These high-κ materials must satisfy numerous requirements including high κ, large band gap and band offsets, low leakage current density, low interface trap density, high breakdown strength, acceptable reliability, and additionally thermal stability in contact with silicon. Recently, Intel reported the first 45 nm microprocessors using a hafnium-based gate oxide together with an appropriate metal gate material. The transistors in these microprocessors exhibit an order of magnitude lower gate leakage than transistors with an SiO_2 gate dielectric.[3] Tomida *et al.* observed that $Hf_{(1-x)}Si_xO_2$ shows different κ values depending on the crystallization phase.[4] They observed that amorphous $Hf_{(1-x)}Si_xO_2$ shows a κ value around 20; however, for monoclinic phase, the κ value is 15 and as they increased the temperature and changed the crystallization phase from monoclinic to tetragonal the κ value increased to 27. Moreover, Böscke *et al.*[5] and Migita *et al.*[6] obtained a κ of 36 and an even higher κ value for tetragonal and cubic HfO_2, respectively. However the κ of amorphous hafnium-based oxides varies between 10 and 20.[7,8] In contrast, rare earth (RE) scandates ($REScO_3$, RE=Gd, Dy, La) show higher κ and, therefore, have attracted significant attention for high-κ applications.[9–13] The amorphous RE scandates have κ between 20 and 30 and the crystalline phases have κ over 30.[12] Christen *et al.* observed band gaps higher than 5.5 eV for these $REScO_3$ oxides and varying crystallization temperatures depending on the RE atomic number and the Goldschmidt tolerance factor.[12] According to their results, the crystallization temperature of $SmScO_3$ (750 °C) lies intermediate between those of $LaScO_3$ (650 °C) and $GdScO_3$ (800 °C), however, among them it has the highest κ when crystallized. So far there are no experimental results about the application of amorphous $SmScO_3$ as a gate dielectric. The aim of this paper is therefore to establish the properties of amorphous $SmScO_3$ thin films concerning the above-mentioned requirements for high-κ materials.

$SmScO_3$ films with thicknesses ranging from 6 to 62 nm were deposited by pulsed-laser deposition (PLD) using a stoichiometric ceramic target. RCA cleaned *p*-type (100) Si wafers were used as substrates. Prior to film deposition the wafers were heated to 400 °C and the deposition was carried out in 2×10^{-3} mbar O_2 with a fluence of 2.5 J/cm^2 and a pulse rate of 10 Hz from a 248 nm (KrF) excimer laser. After the deposition, the structure, stoichiometry, and thermal stability of the films were investigated using Rutherford backscattering spectrometry (RBS), transmission electron microscopy (TEM), and x-ray diffraction (XRD).

For electrical characterization, MOS capacitors were fabricated. 70 nm thick Pt top contacts were deposited by electron beam evaporation through a shadow mask with areas between 2×10^{-4} and 11.5×10^{-4} cm^2. An Ohmic backside contact was realized by depositing 120 nm Al. Finally, the samples were annealed in forming gas (90% N_2 +10% H_2) for 13 min at 450 °C to improve their electrical properties.

High frequency *C-V* measurements were carried out using an impedance analyzer (HP 4192A) at 100 kHz. The work function of the metal gate and the effective charge density in the oxide were obtained from the high frequency *C-V* results. The density of the interface trap states (D_{it}) was calculated using Terman's method.[14] Finally, leakage current measurements were performed using a semiconductor parameter analyzer (HP 4155B).

The stoichiometry and thickness of the films were determined by RBS. Simulation of the RBS data using the rump program[15] reveals that the films have the desired stoichiometry with a ratio of Sm:Sc:O=1:1:3.

A cross-sectional TEM image of a 49 nm thick $SmScO_3$ film on Si (100) (Fig. 1) shows an amorphous and smooth film on Si. The figure also indicates the existence of an interfacial layer between the silicon and the high-κ dielectric

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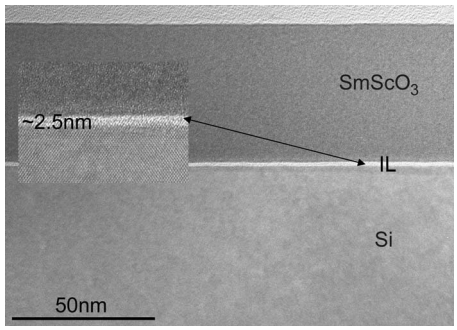

FIG. 1. Cross-sectional TEM micrograph of a 49 nm thick $SmScO_3$ film deposited on (100) Si. The inset shows a close-up of the interlayer, which has a thickness of about 2.5 nm.

with a thickness of 2.5 nm. The growth of the interfacial layer is probably related to the oxidation of the silicon surface during PLD growth.

In order to study the thermal stability of the $SmScO_3$ grown at 400 °C, rapid thermal annealing in ultrapure N_2 was performed at atmospheric pressure and different temperatures ranging from 700 to 1100 °C for 10 s. Figure 2 shows the XRD patterns of a 22 nm thick $SmScO_3$ film for different annealing temperatures. It is apparent that the as-deposited film is amorphous, in agreement with the TEM results. The film remains amorphous up to 800 °C and the crystallization of the orthorhombic $SmScO_3$ phase starts at 900 °C, as indicated by the arrows identifying $SmScO_3$ reflections. The value for the onset of crystallization is higher than that for HfO_2 (Ref. 16) and comparable to Hf silicates.[17] It is, however, lower than for $DyScO_3$ and $GdScO_3$.[10]

Figure 3 shows the capacitance normalized to the gate area versus gate voltage for $SmScO_3$ films with different thicknesses. The *C-V* curves are smooth and free of humps. Double sweep measurements from inversion to accumulation and back were carried out at a frequency of 100 kHz with a 3 s hold time for each measuring point. Negligible counter clockwise hysteresis indicates that these samples contain a low density of positive trap charges, Q_{ot}, in the range of $\sim 10^{10}$ cm^{-2}, as estimated from the simple formula, $Q_{ot} = (C_{ox}/q)\Delta V_{FB}$,[18] where C_{ox} is the accumulation capacitance normalized to the gate area, q is the electron charge, and ΔV_{FB} is the voltage shift from the reverse bias measurement to the forward one.

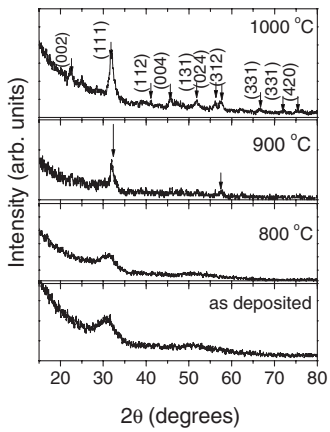

FIG. 2. XRD patterns of a ~22 nm thick, as deposited $SmScO_3$ film grown on (100) Si, together with those after annealing at different temperatures in 1 atm N_2 gas for 20 s.

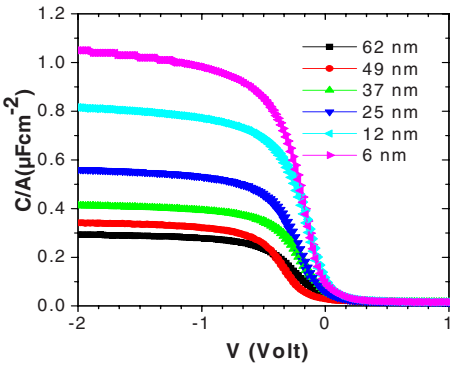

FIG. 3. (Color online) Capacitance normalized to the gate area vs gate voltage of Pt/$SmScO_3$/Si MOS capacitors with different oxide thicknesses.

Using the curves shown in Fig. 3, the capacitance equivalent thickness (CET) was extracted from the capacitance in the accumulation region C_{acc} as CET $= A\varepsilon_o\kappa_{SiO_2}/C_{acc}$, where A is the gate area, ε_o is the permittivity of vacuum and κ_{SiO_2} the dielectric constant of SiO_2. Figure 4 shows a plot of the CET versus oxide thickness t_{ox}. From the slope of the linear fit, it is possible to extract the dielectric constant of the films disregarding the contribution of the interfacial layer. The κ thus obtained for amorphous $SmScO_3$ is ~29. The intercept of the line with the CET axis represents the electrical thickness of the lower-κ interfacial layer, which is found to be 2.5 nm. This value is in agreement with the physical interfacial layer thickness observed by TEM indicating that this layer has a κ comparable to SiO_2 and thus likely is SiO_2.

The flatband voltage (V_{FB}) of the samples has been extracted from the comparison between the ideal *C-V* curves and experimental ones obtained from the capacitors exposed to forming gas annealing at 450 °C. The sample with a 6 nm thick $SmScO_3$ oxide layer has a −0.1 V flatband shift and as the thickness of the oxide layer increases the flatband voltage shifts to more negative voltages. In order to evaluate the effective oxide charge density (N_{eff}) and the effective work function of the Pt metal gate ($\Phi_{m,eff}$), $V_{FB}+\Phi_s$ versus CET was plotted in Fig. 5, where Φ_s is the work function of the silicon. V_{FB} can be expressed as[19]

$$V_{FB} = \Phi_{m,eff} - \Phi_s - qN_{eff}CET/\varepsilon_o\kappa_{SiO_2},$$

where N_{eff} does not change with the oxide layer thickness.

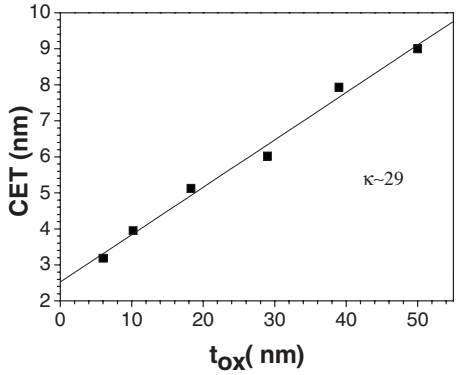

FIG. 4. Calculated CET vs t_{ox} of Pt/$SmScO_3$/Si MOS capacitors. The slope of the best-fit line indicates that $\kappa \sim 29$ and its intercept at 2.5 nm on the CET axis corresponds to the electrical thickness of the lower-κ interfacial layer.

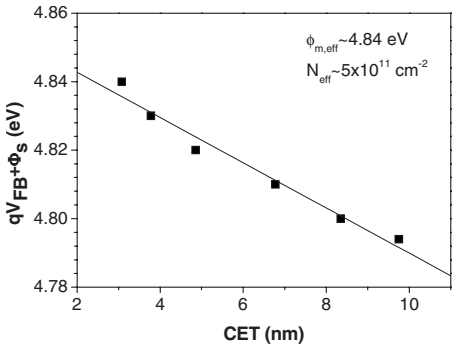

FIG. 5. $V_{FB}+\Phi_s$ vs CET. The intercept of the best-fit line on the $V_{FB}+\Phi_s$ axis gives $\Phi_{m,eff}$ and the slope N_{eff}.

From the intercept of the $V_{FB}+\Phi_s$ axis, $\Phi_{m,eff}$ was found to be 4.84 eV. This value satisfies the work function requirement for a *p*-type MOS field-effect transistor. From the slope of the curve N_{eff} was evaluated to be 5×10^{11} cm^{-2}. Such a low charge density indicates a low concentration of defects in the oxide layer.

Another important issue for MOS capacitors is the quality of the high κ/Si interface. To evaluate the quality of the Si/$SmScO_3$ interface after forming gas annealing, D_{it} levels were calculated using Terman's method. The values are $\sim4.5\times10^{11}$ $(eV\ cm^2)^{-1}$ and do not show a clear dependence on the oxide thickness, as expected. Finally, the leakage current density of the samples was measured. For the sample with a 6 nm thick $SmScO_3$ it is in the range of 10^{-7} A/cm^2 and, for thicker films, it is even below the detection limit of the measurement system for the contact size used.

We have investigated the thermal stability and electrical properties of $SmScO_3$ thin films and their interface to Si (100). The films remain amorphous on Si up to 800 °C and start to crystallize at 900 °C. The results indicate low oxide charge and interface trap charge densities in the range of 5×10^{11} cm^{-2} and 4.5×10^{11} $(eV\ cm^2)^{-1}$, respectively. Very smooth *C-V* curves with negligible hysteresis were recorded and a κ value of ~29 was extracted from the electrical measurements. The films reveal low leakage current densities in the range of 10^{-7} A/cm^2 for 6 nm thick film. It can be concluded that amorphous $SmScO_3$ shows promising properties as an alternative high-κ gate dielectric, which might allow it to be used in future integrated circuits.

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