

Large array of GFETs for extracellular communication with neuronal cells

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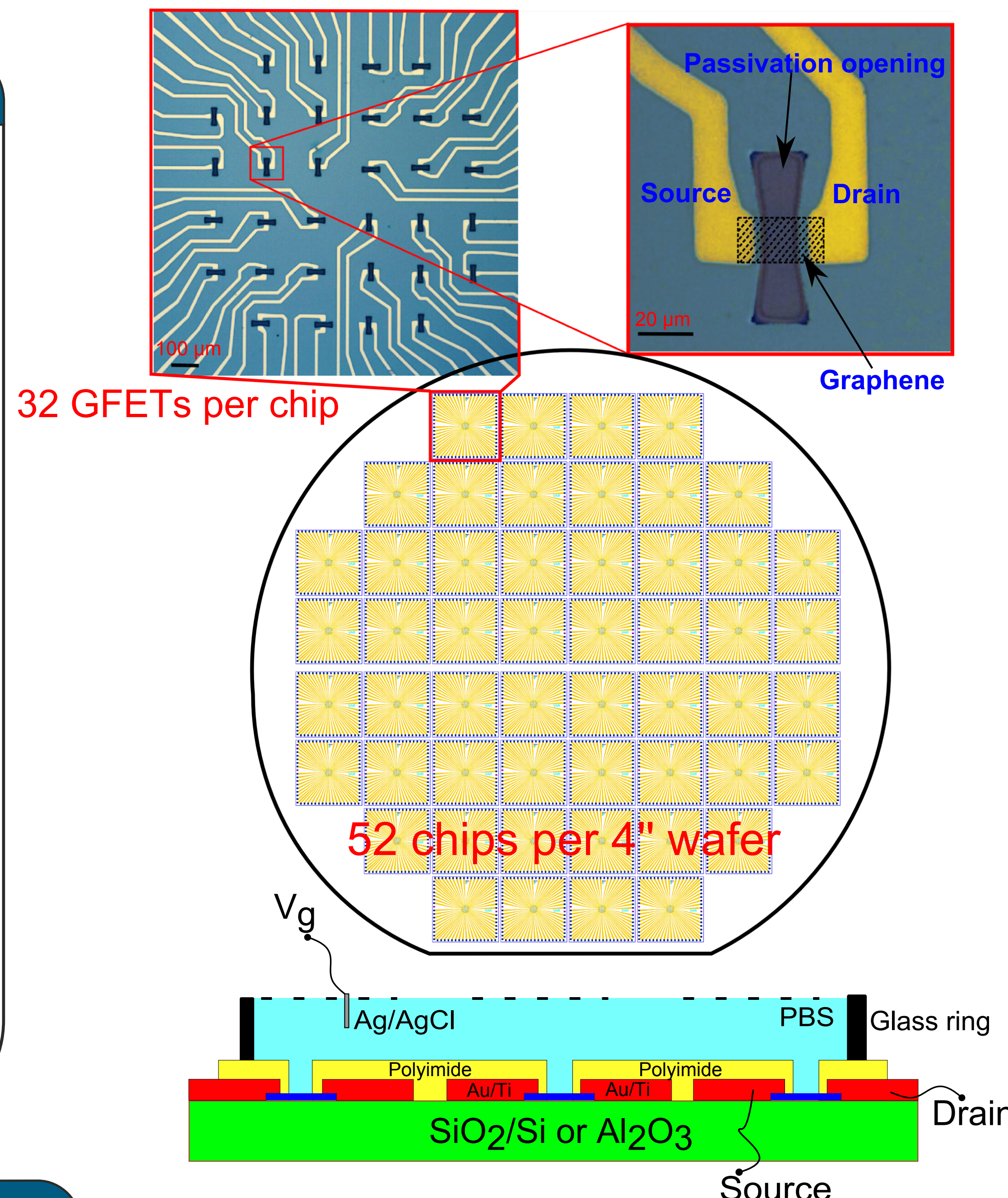
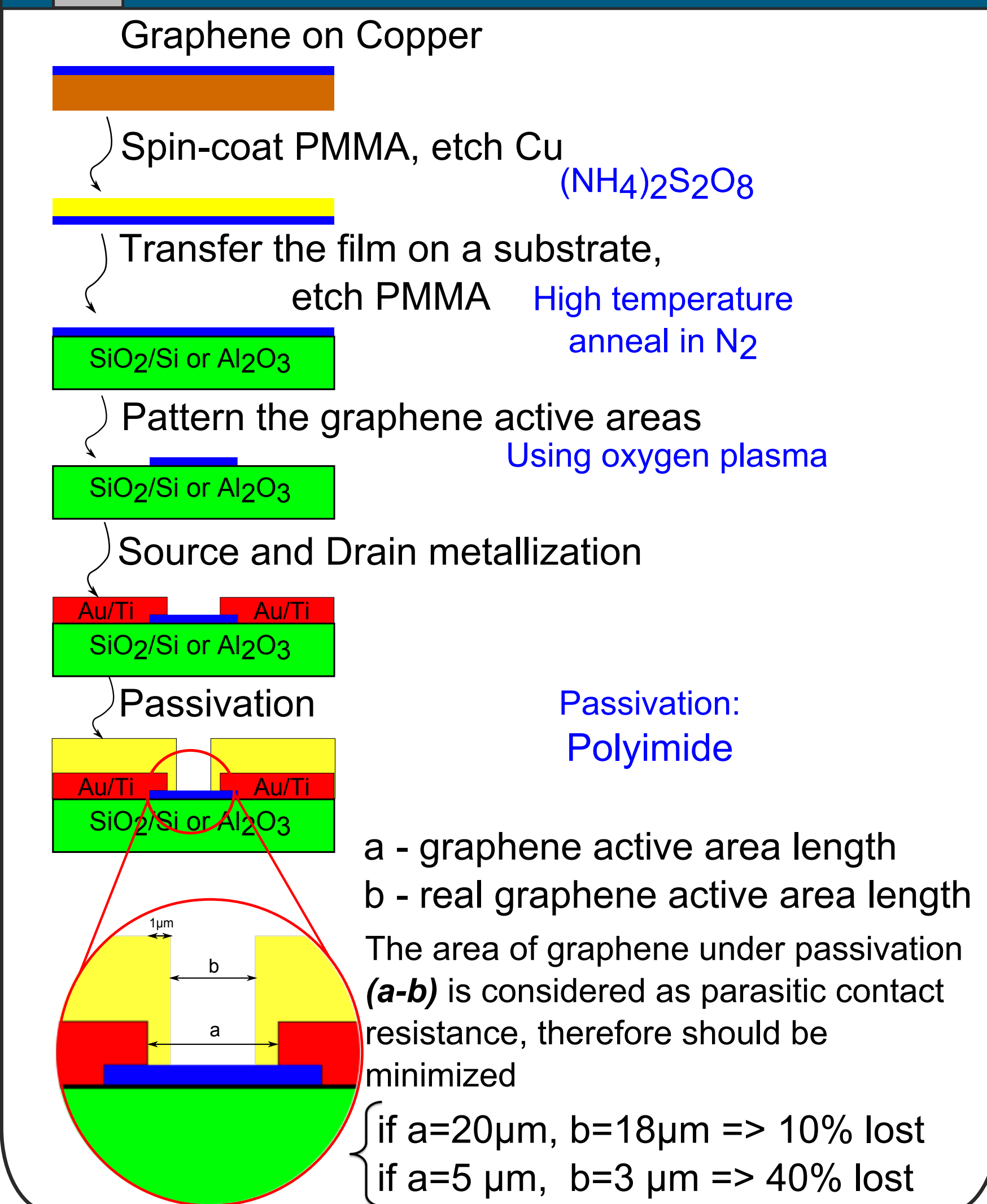
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1 Introduction

In the last years, graphene-based devices have demonstrated their potential for molecular biosensing applications. More recently, the high sensitivity of solution-gated graphene field effect transistors has been exploited for cell-based biosensing applications, such as the recording of cellular activity [1]. Due to their biocompatibility in combination with good signal-to-noise ratio, such devices are excellent candidates for extracellular measurements [2]. However, cell experiments do require a large number of reliable devices to generate statistically significant data, which is difficult to obtain with conventional graphene device technology.

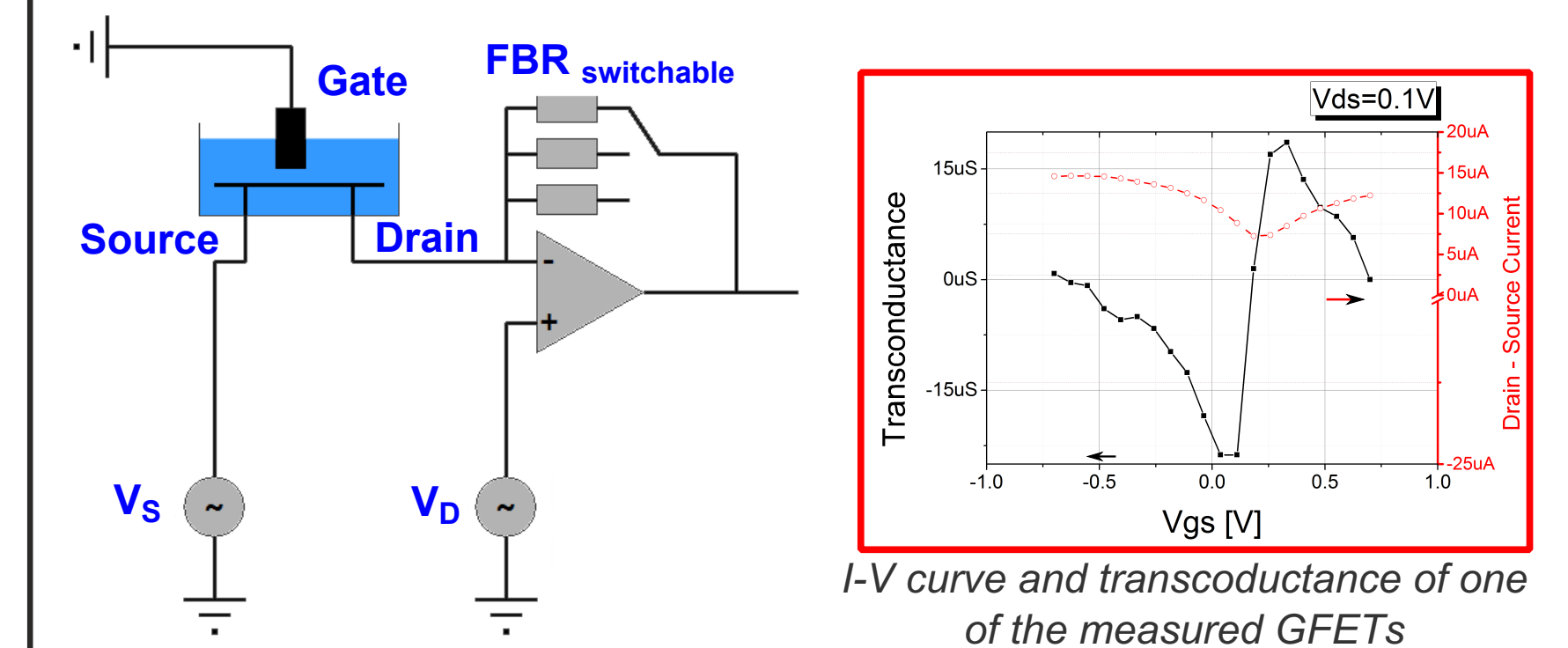
The aim of this work is to establish a large-scale, high-throughput fabrication process in order to use graphene as a transducer of biological information into electrical signals. We fabricate our devices on 4" wafers, each yielding in 52 chips, 11 by 11 mm size. Every chip contains an array of 32 GFETs. The active area of the chip (for further cell growth) is around 2 mm², while each GFET's channel size differs between 6 and 360 μm² with altered configurations. We have developed a multichannel measurement system that allows us to measure all 32 transistors on a chip simultaneously. This approach makes it possible to measure not just discrete spikes, but even propagation of the action potential through the neuronal network.

2 Fabrication

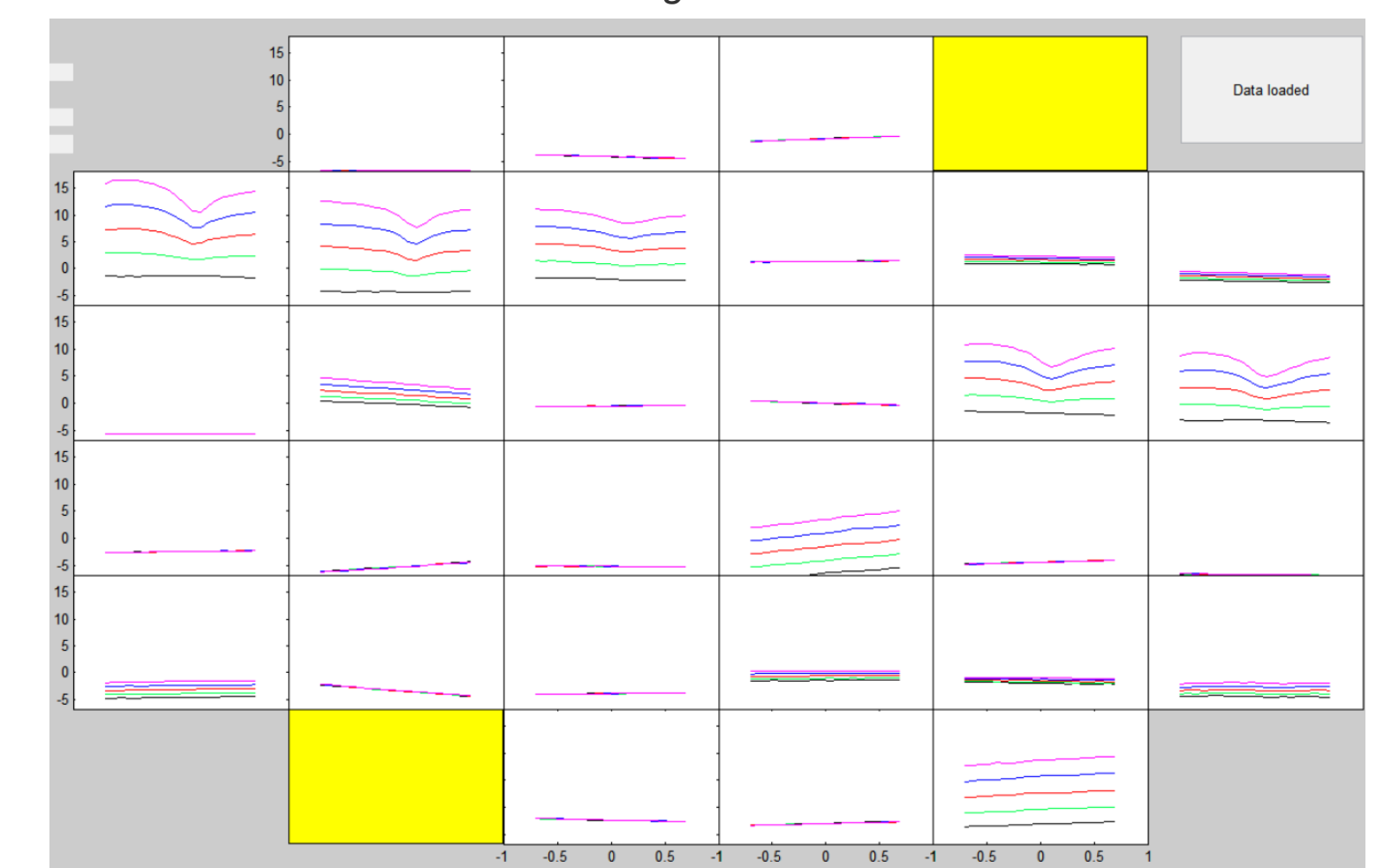


3 Parallel measurements

A schematic of the BioMAS multichannel measurement system



Typical output result of the parallel measurement from a chip with only 5 (out of 32) working transistors:

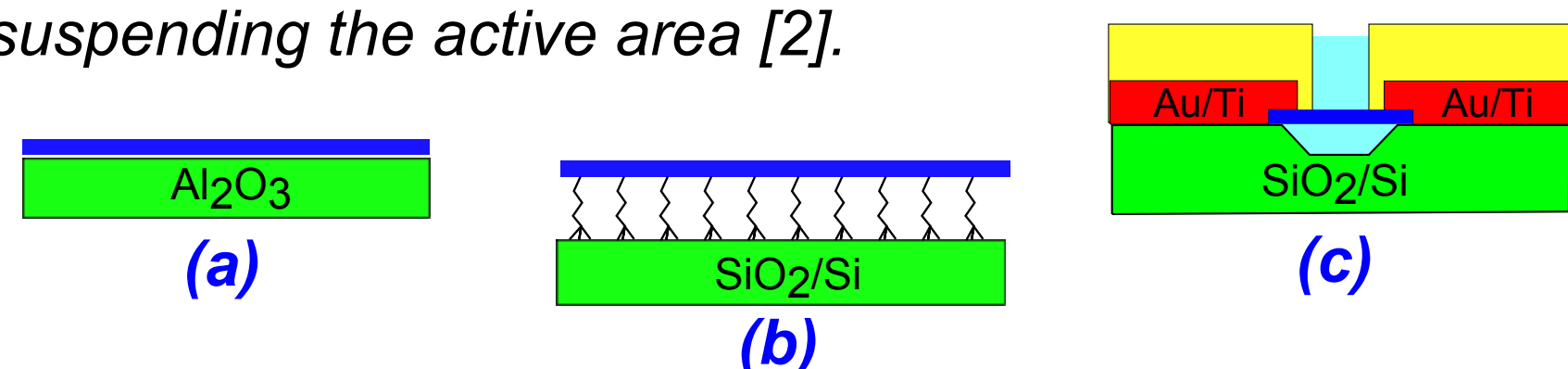


4.1 Graphene-Substrate Interface

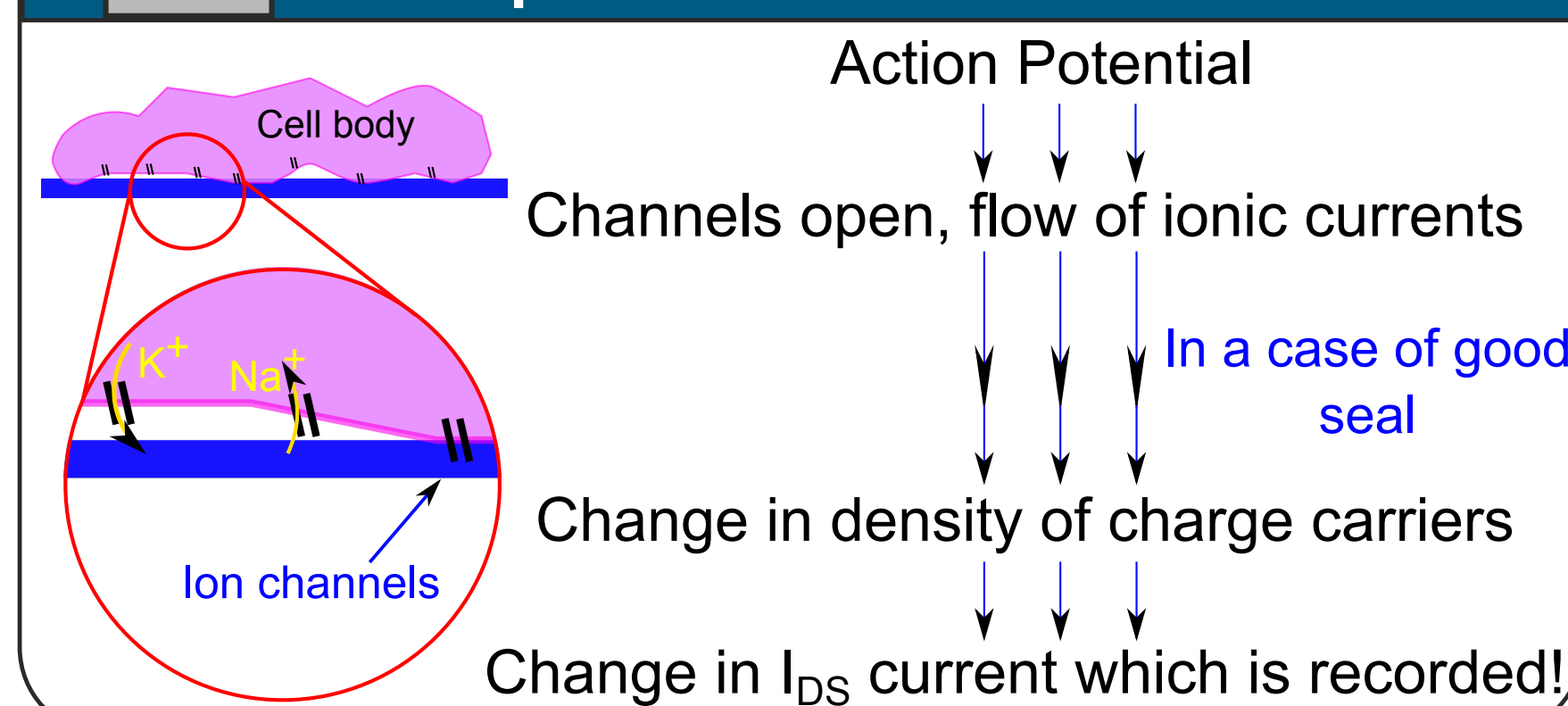
Silicon dioxide is not the best dielectric for interaction with graphene. Its dangling bonds and charge traps result in direct doping graphene and disturb the superior properties of the pure graphene itself [3].

There are several ways we are working on in order to overcome this issue:

- Use more appropriate substrates: BN, sapphire [1];
- Use SiO₂/Si wafers, modified with self-assembled monolayers, i.e. OTS, APTES [4];
- Eliminate the graphene-dielectric interface by suspending the active area [2].



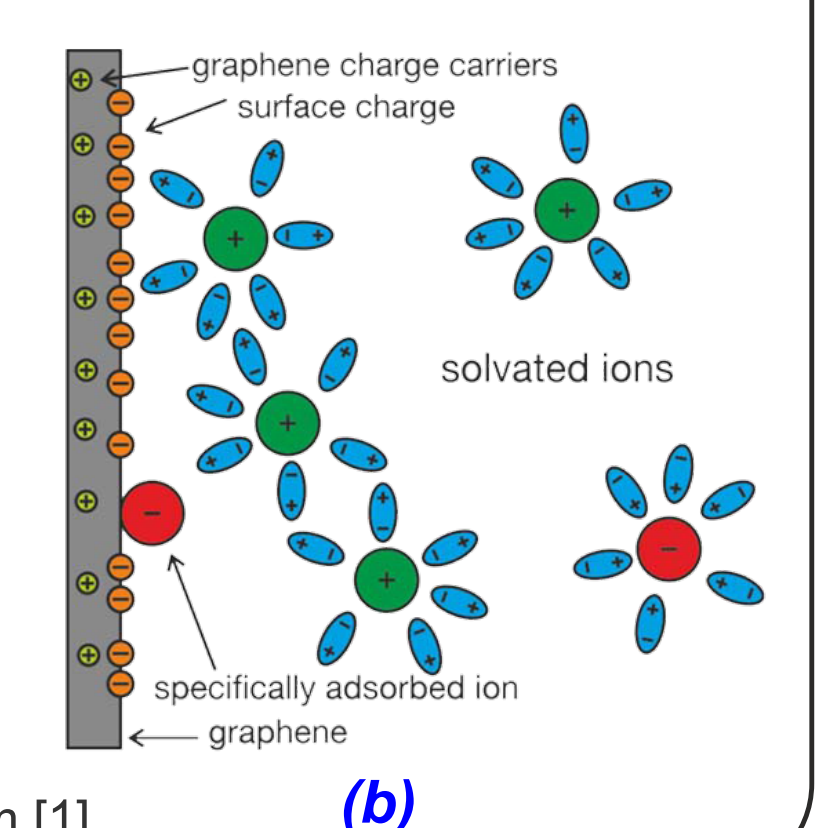
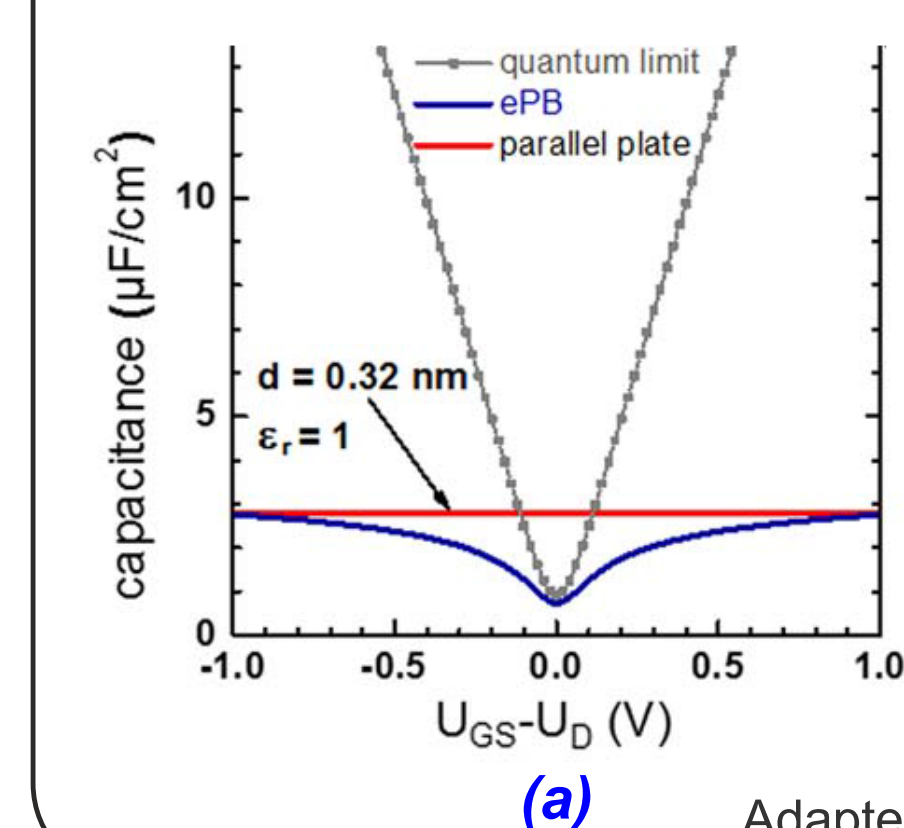
4.3 Graphene - Cell Interface



4.2 Graphene-Liquid Interface

Electrolyte gating of GFET is not straightforward and quite different from a typical FET gating. There are two main components of electrolyte-induced gating:

- C_Q - quantum capacitance - due to density of states in graphene;
- Double-layer capacitance



5 Experimental scenario

Assume a real case: a cell is "sitting" on a GFET. The GFET is biased with V_{GS} and V_{DS}, and I_{DS} is recorded. If an action potential occurs across the cell, this will induce local surface potential changes. This small variation in I_{DS} will be detected.

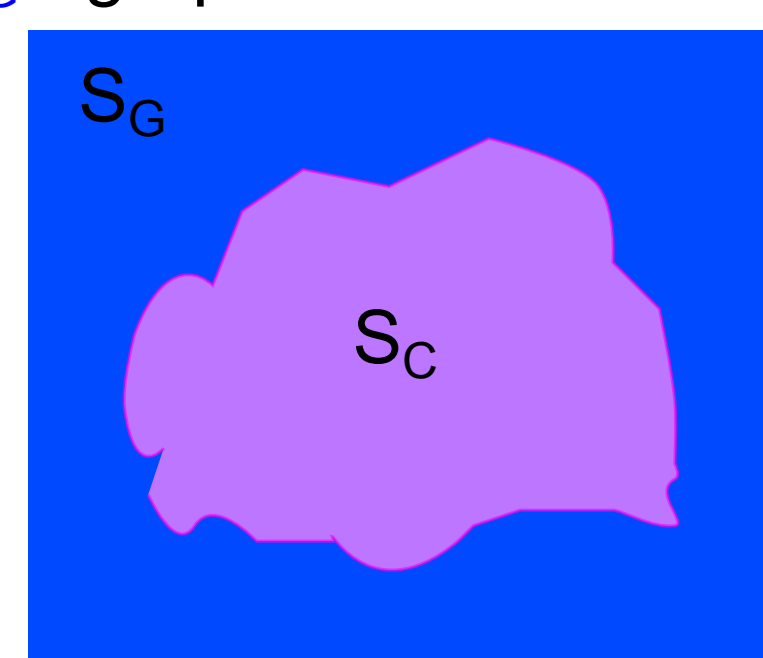
Nevertheless, there is still a trade-off between the size of the graphene active area compared to the size of cells:

- If GFET's area is too big, the higher the chance of having a cell on it, but also higher current fluctuation and lower gating modulations.
If GFET's area is small, the chance of having cell on it decreases but the gating characteristics and noise fluctuations are much better.

S_C - cell body surface area

S_C : 25 to 400 μm²

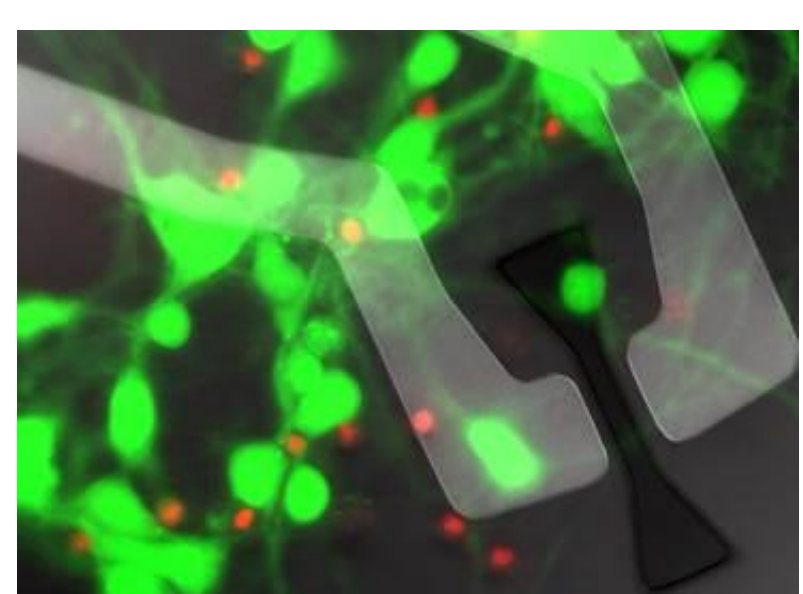
S_G - graphene surface area



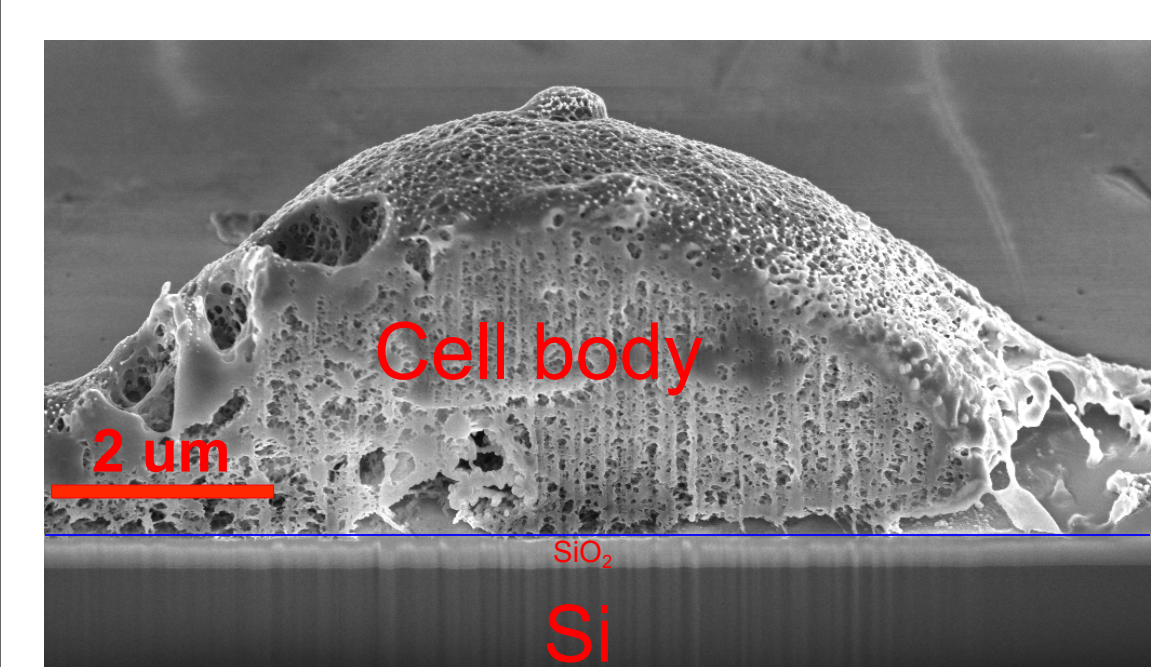
Combinations of S_G, μm²

Width, μm	2	5	10	20
Length, μm				
3	6	15	30	60
8	16	40	80	160
18	36	90	180	360

- S_G >> S_C : Noise
- S_G ≥ S_C :
- S_G ≈ S_C :
- S_G ≤ S_C : Good seal
- S_G << S_C : Single ion channels?



Green - live cell, stained with Calcein;
Red - dead cells, stained with EtHD.



SEM image of the FIB cut of a neuronal cell on top of the graphene-SiO₂-Si stack. The cell was fixed, stained in advance to the FIB cut.

6 Conclusions and Outlook

A wafer-scale fabrication of graphene FET arrays has been introduced. The measured transconductances (20-25 μS) are an order of magnitude smaller than high-performance GFETs [5], which gives us the motivation for further improvements. The improvements are comprised of:

- using SAMs to adjust dielectric-induced doping;
- optimizing the GFET's size in terms of SNR;
- improving the graphene-substrate interface by using other fabrication designs

7 References

- (1) L. Hess, M. Seifert, J. Garrido, *Proceedings of the IEEE*, **101** (7), 1780-1792 (2013)
- (2) Z. Cheng et al., *Nano letters*, **13** (6), 2902-2907 (2013)
- (3) J. Chen, C. Jang, S. Xiao, M. Ishigami and M. Fuhrer, *Nature nanotechnology*, **3** (4), 206-209 (2008)
- (4) A. Nourbakhsh et al., *ECS Transactions*, **50** (14), 83-90 (2012)
- (5) D. Khodagholy et al., *Nature communications*, **4**, 2133, 1-6 (2013)