Analysis and Design of Amplitude Error Detector and Digital Control Loop to Increase Reliability of PLL

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***Abstract*—A digital control loop scheme for a high speed PLL is suggested to detect amplitude errors at the output of the oscillator. Reliability specifications of the PLL are likely to be violated in case of excessive output swing in the oscillators. In addition, low amplitude swings will have negative influences on the phase noise of LC oscillators. As a result, the performance and reliability of the PLL will be reduced. The design includes a novel amplitude error detector. The amplitude error detector generates a digital word to show the situation of the amplitude error. The structure is implemented in 65nm CMOS technology. The power consumption of one amplitude error detector from 1V power supply is 0.76mW.**

***Index Terms*—Digital control loop, amplitude error detector (AED), reliability, LC oscillator, Phase locked loop (PLL).**

I. Introduction

Phase locked loops (PLLs) provide the fundamental function of clock generation in many electronic systems. Voltage controlled oscillators (VCOs) as sub-blocks in the PLLs are important to produce low phase noise clocks with high stability. The PLL covered by this work is applied to generate clocks for a digitizing and data pre-processing chip in the receiver chain of the Jiangmen Underground Neutrino Observatory (JUNO) neutrino detector [1]. The priority goal of the detector that contains 20 kton of liquid scintillator is the determination of the neutrino mass hierarchy. Figure 1 (right) shows a conceptual drawing of the central detector that will be installed in an underground water pool as shown in figure 1 (left). It comprises 20,000 20-inch photomultiplier tubes (PMTs) as well as a complimentary 3-inch PMT system for improved accuracy. Receiver electronics, including the digitizing chip, are attached to and potted within the 20-inch PMTs. Since the electronics are inaccessible during the lifetime of the experiment, stringent reliability requirements need to be fulfilled. One critical issue in this respect is the output swing of the LC-VCO in the PLL that can exceed the power supply due to inductive loading.

An LC based VCO shows superior phase noise compared to ring oscillator structures [3]. Voltage swings exceeding the supply limits increase the channel electric field that is already high for 65 nm CMOS and may lead to sufficiently high energy carriers which can create trap states at the gate oxide interface or trapped charge carriers in the bulk oxide.

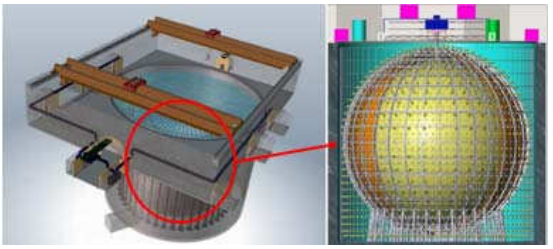

Figure 1. Conceptual drawing of the central detector [2].

These hot-carrier effects might degrade the long-term performance of the device and manifest themselves in a reduction of mobility and transconductance as well as a drift of the threshold voltage over time [4]. Furthermore, when a high gate voltage is applied across the thin gate oxide of a transistor, the breakdown (BD) phenomenon is more likely to happen. This effect expands conducting paths through the gate oxide and reduces the gate capacitance which may cause failure in the operation of the MOS devices [5]. Increasing the output swing of the oscillator above breakdown limitations at the gate oxide of transistors provokes reliability challenges in their design.

On the other hand, reduction of the output swing restricts signal to noise ratio (SNR) and deteriorate phase noise characteristics of the oscillators. Since the oscillator signal strength should be adequate to drive the following block of the PLL, an optimum value for the oscillator amplitude is necessary to insure both reliability and signal capability.

In this paper, a novel high precision amplitude error detector (AED) is introduced. The amplitude limit is controlled to stay within a range defined by two reference levels – a low and a high one. The error detection and modification of the amplitude is conducted by employing a digital control loop scheme in the PLL. Several previous works have investigated some aspects of the PLL design such as charge pump fault detection [6], and jitter transfer function [7]. Our proposed design is intended to increase the system reliability. Section II of the paper explains the effect of breakdown on the circuit performance. In section III, the digital control loop procedure in the PLL is described. Then, the design of the AED will be presented in section IV. The design implementation is discussed in section V. Finally, section VI concludes the paper.

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II. EFFECT OF BREAKDOWN ON PERFORMANCE

The conventional LC-VCO consists of an LC tank which is formed by a symmetric inductor and varactors. Cross-coupled transistors that constitute a negative resistance are inserted to compensate resistive losses in the tank circuit. By applying control voltage to the MOS varactors, the VCO frequency can be tuned. The required voltage is regulated in the way that the output signal of a frequency divider that is attached to the VCO output is in phase with a reference clock.

In the LC-VCO, the output voltage amplitude can be above the power supply limits, so that the amplitude cannot be controlled by setting the supply voltage. This additional stress applied to the gates of transistors increases current leakage as a result of conductive paths formed by generated traps within the oxide [8]. A possible breakdown in the LC-VCO because of high amplitude will be observed by its effects on the MOS varactors and the two cross-coupled active devices. In a MOS varactor, capacitance is formed between the gate and the common drain and source terminals (D=S). For understanding of the breakdown effect, it is worth to review the quality factor of the MOS varactors in the strong inversion region. The quality factor of the varactor is expressed as [9]

$$Q_{var} = \frac{1}{2\pi f R_s C}, \quad (1)$$

where C is the varactor capacitance, and R_s is the parasitic series resistance of the varactor given by:

$$R_s = \frac{L}{12\mu_n C_{ox} W (V_{GS} - V_{tn})}, \quad (2)$$

where μ_n is the mobility of electrons, C_{ox} is the oxide capacitance, and V_{GS} and V_{tn} are the gate-(drain=source) voltage and the threshold voltage of the NMOS varactors, respectively. A decreased mobility and an increased threshold voltage as a result of breakdown make the series resistance larger which degrades the quality factor. This has a negative effect on the phase noise of the VCO due to the noise contribution of the varactors. Considering the effect of breakdown on the quality factor of the varactors, the degraded overall quality factor of the LC tank is as (3):

$$Q = \frac{1}{\frac{1}{Q_{var}} + \frac{1}{Q_{ind}}}. \quad (3)$$

This quality factor decay causes VCO amplitude reduction. The basic phase noise model of Leeson [10] reveals the adverse effect of this phenomenon on VCO phase noise. In addition, the tuning range of the oscillator is affected by the breakdown effect. The tuning range has to be sufficient to guarantee the proper operation of the VCO in the PLL, even in case of process and temperature variations. A possible limitation of this capability is revealed by the VCO gain that describes the oscillation frequency variation induced by control voltage changes as:

$$\frac{\partial f_{osc}}{\partial V_{cntrl}} = \frac{1}{4\pi\sqrt{L}(C_v)^{1.5}} \times \frac{\partial C_v}{\partial V_{cntrl}}, \quad (4)$$

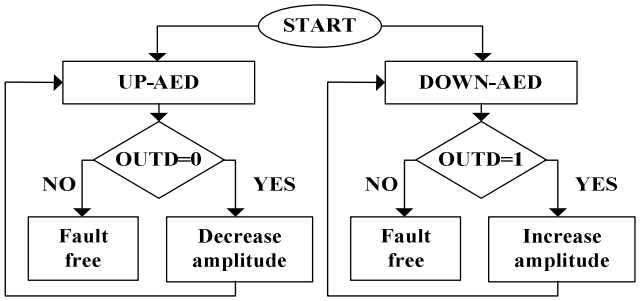

Figure 2. Digital control loop algorithm.

where C_v is considered to be the equivalent capacitor of the varactors and parasitics. The impact of the varactor capacitance changes is important since the tuning range affects the PLL characteristics including loop bandwidth, settling behavior and noise transfer function.

Finally, in this PLL design, the VCO is followed by frequency dividers. A current mode logic (CML) structure which is suitable to be driven by high frequency clock is used as a divider [11]. The condition of the self-oscillation ($g_{mL}R_L > 1$) has to be fulfilled by the latches in this frequency divider to operate in case of low amplitude clocks. R_L and g_{ml} are consecutively load resistance and transconductance of the cross-coupled pair. The condition of the self-oscillation can be violated by the reduction of the transconductance as a result of a prolonged breakdown effect owing to the changes in the threshold voltage and the mobility of the transistors.

In awareness of all these aspects, limits for the minimum and maximum voltage swing are introduced. This task is fulfilled by the digital control loop presented in the next section.

III. DIGITAL CONTROL LOOP PROCEDURE

The control flow of the digital control loop in the PLL to regulate the amplitude of the VCO outputs is presented in figure 2. For the digital control loop, a digital counter and two AEDs with different reference levels, which are used to specify limits for the maximum and minimum levels of the VCO output, are added to the PLL structure. The outputs of the AEDs, which are binary signals, are given to the digital counter. Eight bits at the output of the digital counter are generated to set the VCO amplitude. Binary weighted current sources are added to the VCO to adjust the voltage at the center tap of the inductor (V_I) that is used to bias the VCO as presented in figure 3. The control word generated by the counter tunes the amplitude by changing V_I.

As the amplitude grows beyond the reference level, the output voltage of the UP-AED tends to zero. Dependent on the output, the digital counter reduces the decimal value to lower V_I.

In the opposite case, when the amplitude falls below a minimum value, the DOWN-AED causes its output voltage to go toward one. In this case, the digital counter increases the control word and thus V_I.

When the digital control loop is enabled, a default value is assigned to the control bits to start the amplitude regulation. The digital control loop is only active during the regulation time to set the VCO amplitude to the optimum value. This will guarantee the stability in the operation.

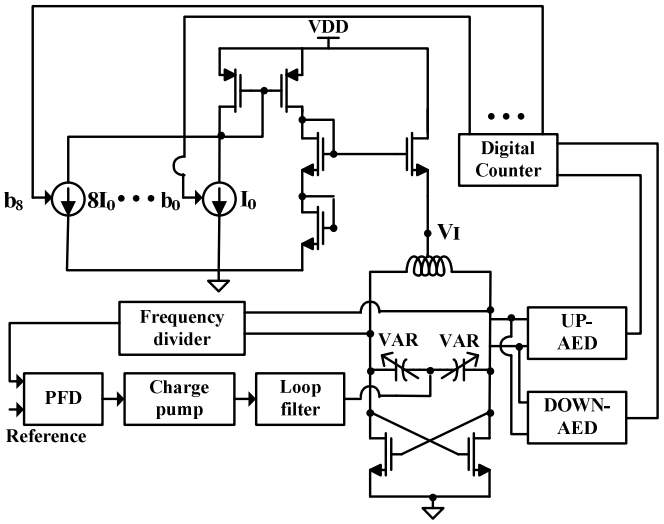

Figure 3. Digital control loop in the PLL.

IV. AMPLITUDE ERROR DETECTOR DESIGN

The proposed differential topology of an AED used in the digital control loop is shown in figure 4. In an AED, the amplitude of the VCO outputs is compared with an input reference level. The input reference level is a DC voltage that is provided form a digital to analog converter (DAC). The gates of the transistors M_1 and M_2 receive the inputs from two differential sinusoidal outputs of the VCO, whereas M_3 takes from the constant DAC output.

If the amplitude of the VCO is below the reference level, i.e. in the default mode of operation, no current flows in M_1 and M_2 and the tail current of M_0 passes through M_3. This means that a certain fraction of the drain-current of M_5 is subtracted from the current entering the source of M_9. The latter causes the voltage drop V_X across M_7 that is regulated to $V_{ref\text{-}amp}$ by the action of the feedback amplifier. Since all the drain-current of M_4 enters the source of M_8 in this mode, the voltage drop across M_6 is higher than V_X.

If the input voltage peaks rise above the reference level, M_1 and M_2 start to conduct, whereas the current through M_3 is reduced. The feedback amplifier counteracts a corresponding rise of V_X by increasing V_{GL}. This reduces the drain-current of M_4 from which, in addition, the drain-currents of M_1 and M_2 are subtracted. The difference current entering the source of M_8 is well reduced compared to the current in the default mode. This causes the drain voltage of M_6 to fall below V_X. A regenerative output buffer is attached to the drain node of M_6 to ensure a proper '1' or '0' binary output signal for the next steps of the amplitude control flow. It has a simple structure with rail-to-rail output swing.

The slow changes in V_X are the result of gradual variations in the VCO amplitude. The AED block can easily track these changes. Using differential outputs of the VCO ensures a symmetrical loading of VCO.

V. DESIGN IMPLEMENTATION

The structure was fabricated in 65nm CMOS technology.

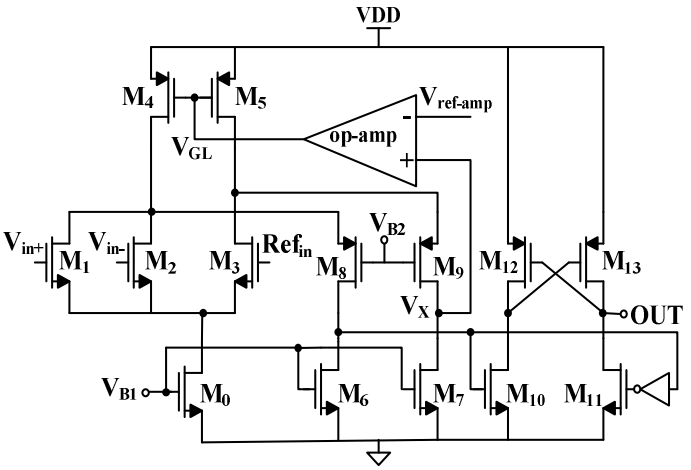

Figure 4. Proposed amplitude error detector design.

The chip including PLL (left) and AED layout (right) is shown in figure 5. The area of one of the detector circuits is 81μm×46μm on chip. The reference levels (Ref_{in}) for the DOWN-AED, UP-AED and op-amp are set to 0.85V, 1V and 0.3V, respectively.

The post layout simulations approve the functionality of the proposed design over different process corners and temperatures from -40˚C to 120˚C. The default value for the 8 control bits of the binary weighted current sources is equal to 128 in decimal value. The differential input clock signals to the AEDs are generated through the PLL at 4GHz oscillation frequency. The post layout simulation results using these settings are presented in figure 6. When the oscillation starts, the VCO amplitudes are lower than the reference level and the output of UP-AED tends to '1' to indicate this situation. As soon as the amplitude of the VCO outputs grows above the reference level, the output of UP-AED goes to '0'. V_X is kept at the amplifier reference ($V_{ref\text{-}amp}$) which approves the operation of the feedback amplifier. The outputs of VCO are applied to the DOWN-AED as well to ensure an amplitude of more than 0.85V.

In this regard, an optimum range for the VCO amplitude between 0.85V and 1V is obtained that guarantees the reliability and low phase noise operation. The minimum difference between the input reference and the VCO amplitude required for a full switching of the detectors is more than 3.8% of the input reference. As the probability of breakdown strongly depends on time, a short overshoot of the VCO amplitude over power supply limits at the gates of M_1 and M_2 in the AED can be ignored since it is corrected by the control loop. Considering the supply voltage of 1V, the power consumption of each detector is 0.76mW which complies with the application requirements.

The phase noise characteristic of the VCO is extracted by subtracting the simulated phase noise contributions of charge pump, clock reference and loop filter from the measured phase noise of the PLL. There is 3dB difference between the simulation and measurement results of the VCO phase noise at 1MHz offset frequency. The difference comes as the result of extra imposed parasitic in the fabrication process and measurement setup.

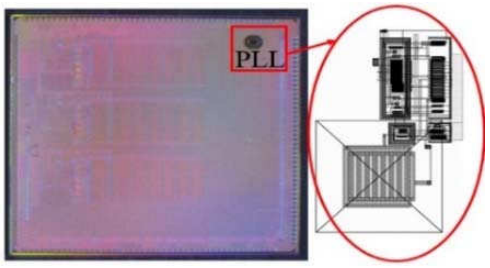

Figure 5. Chip micrograph.

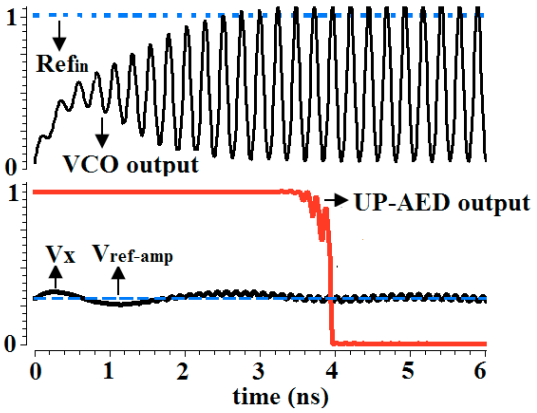

Figure 6. Simulation results of UP-AED.

The negative effect of breakdown on the VCO performance can be simulated by a modification of the transistor model. According to [8], 100 kΩ are applied between gate and drain/source of the MOS varactors. Then, compared to the original phase noise spectrum, there is a 4.4dB phase noise difference at 1 MHz offset frequency from the 4GHz carrier in this simulation. A similar or even worse phase noise degradation is expected for the measured phase noise data when the breakdown effect occurs.

VI. Conclusion

In this paper, the effect of hot carriers and gate oxide breakdown on the operation of the LC-VCO and frequency divider in a PLL is investigated. A novel structure of an amplitude error detector is presented which tracks the amplitude difference of the LC-VCO compared to a reference level. The control flow of a digital control loop is introduced to address the reliability concerns of the PLL related to the excursion of VCO output amplitude beyond the supply voltage. However, excessive reduction of LC-VCO amplitude leads to increased phase noise. Using the proposed method, VCO oscillation amplitude is restricted to an appropriate range that is an optimum spot regarding the PLL phase noise and reliability. The comparison of phase noise for the original and degraded VCO gives the phase noise difference of 4.4dB at 1MHz offset frequency from 4GHz carrier. The same or even worse impact of degradation on measured data is expected.

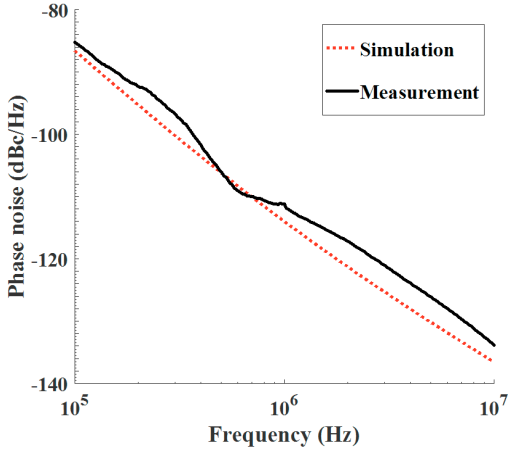

Figure 7. VCO phase noise characteristic.

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