CMOS based scalable cryogenic Control Electronics for Qubits

C. Degenhardt[1], L. Geck[1], A. Kruth[1], P. Vliex[1] and S. van Waasen[1,2]
[1]Central Institute of Engineering, Electronics and Analytics, Electronic Systems,
Forschungszentrum Jülich GmbH, Jülich, Germany
[2]Faculty of Engineering, Communication Systems, University of Duisburg-Essen, Germany
c.degenhardt@fz-juelich.de

***Abstract*—The feasibility of using commercial CMOS processes for implementing scalable cryogenic control electronics for universal quantum computers is investigated. Using a systems engineering approach, we break the system down into sub-systems and model the individual components down to transistor level. First results for area demand and power consumption indicate that even with a standard CMOS process, it should be possible to operate hundreds of qubits. Using dedicated low power processes with reduced supply voltage, this number could be further increased in the long term by four or more orders of magnitude, allowing the control of millions of qubits.**

Keywords—quantum computing; electronics; cryogenic; CMOS; systems engineering

I. INTRODUCTION

During the last two decades, there was tremendous effort in increasing the number of controllable qubits in order to pave the way towards a universal quantum computer. Today, nearly 20 qubits can be operated in parallel. Most approaches use 'brute force' scaling of room temperature electronics or FPGA based cryogenic electronics[1]-[4]. Both routes are very valuable in building quantum computers with up to around hundred qubits to show quantum supremacy by implementing first useful algorithms. Although there are several investigations on system architectures for quantum computers[5]-[8], up to now there are only very few attempts to develop scalable integrated approaches for the electronics that control the qubits[9]-[12]. Only truly scalable solutions will enable the use of millions of qubits needed for a universal quantum computer.

In this paper, we investigate the feasibility of building control electronics using commercial CMOS processes. We model the system down to the transistor level and derive values for area demand and power consumption.

II. METHODOLOGY

The methodology follows the V-model of systems engineering. The system under consideration is decomposed into sub- and sub-sub-systems in a top-down fashion and implemented bottom-up. On every level, the performance of the (sub-)systems is verified against the requirements. As the control electronics itself is only a sub-system within the overall architecture of the quantum computer, it is very important to define the interfaces to the systems the control electronics is connected with (see Fig.1).

The individual subsystems are modeled down to the level of logical gates in case of digital circuitry and down to the device level (transistor, capacitor, etc.) for analog circuitry. All system building blocks are modeled with MATLAB and/or Cadence Virtuoso and validated by Virtuoso Schematic at room temperature. For individual components like the Digital-to-Analog Converter (DAC), transient behavior and noise figures were simulated using Cadence Spectre.

Since truly scalable control electronics has to be placed as close to the qubits as possible, the main figures of merit to compare different implementations are area demand and power consumption. The estimation of area demand is done differently for digital and analog circuitry. For digital circuitry, the number and types of logic gates used is derived from the circuit schematics. With the knowledge of number of transistors for each of the logical gates, the total number of digital transistors can be calculated. As a reference, we consider a commercial 65 nm CMOS process that needs an area for a simple minimum sized transistor of $A_{MOS} = 0.23\ \mu m^2$. The area demand for analog circuitry is mainly dominated by transistors and capacitors. For both, an effective density is extracted for the considered CMOS technology. Effective means that additional area for terminals is included. The capacitive density is approx. $1.75\ fF/\mu m^2$ and the sheet resistance approx. 600Ω/sq at room temperature.

The dynamic power loss is estimated by

$$P_{dyn} = 0.5 \times \sigma \times f \times (V_{dd})^2 \times C. \quad (1)$$

In case of charged based DAC, $\sigma=1$, V_{dd} is the reference voltage, C the total capacitance of the DAC and f the sample rate. For the digital parts, $\sigma \in [0;1]$ denotes the switching activity, V_{dd} the digital supply voltage and C_{gate} the gate capacity that needs to be loaded. For simplicity, we neglect static power consumption and short circuit charge which are estimated to contribute approximately 10% to the total power consumption at room temperature and transistor leakage is further decreasing at lower temperatures.

III. IMPLEMENTATION

Fig.1 gives a high level overview of the system architecture of the considered quantum computer. On the one hand, the control electronics is connected to the error correction and quantum execution system of the quantum computer. On the other hand, it is connected to the qubits. The control electronics will translate gate sequences that are generated by the quantum execution systems into corresponding pulses to let the qubits perform the desired operations.

The top-level of the control system is depicted in Fig.2. The interface to the higher layers of the quantum computer is realized by a digital control unit. The digital control unit receives and decodes commands and data from the higher level interface, manages the local memory, controls the DACs generating DC biases and RF pulses that are used to control the qubits and manages the local clocking. The local memory stores the bias gate voltages and the pulse shape of the RF pulses. The memory is made out of serial to parallel registers. The registers are written serially which takes several clock cycles but can be read out in parallel in one clock cycle to allow fast gate sequence generation. Since memory values don't have to be frequently changed, the readout is nondestructive to reduce power consumption.

The requirements for the DACs are given by the qubits they control. Therefore, a concrete implementation of qubits has to be considered here. As an example, we take the requirements of GaAs double dot spin qubits into account. Those spin qubits need five to eight DC bias signals to tune the qubit and additional two RF signals to control the state of the qubit. Table I summarizes the requirements.

As a low power implementation, we choose a capacitor based charge scaling DAC as a first promising DAC topology to be investigated and evaluated, illustrated in Fig.3. It is composed of capacities that are multiples of the unit capacitor C_u. An additional so called attenuation capacitor C_a is used to reduce the number of needed capacitors by a factor of $2^{N/2}$, with N as the number of bits, and to reduce the requirements on capacitor matching.

TABLE I. REQUIREMENTS ON THE CONTROL DAC FOR GAAS DOUBLE DOT SPIN QUBITS

	DC DAC	RF DAC
Amplitude	1V	4mV
Stability	10µV	1µV
Resolution	12bit	10bit
Sample rate	NA	300 MHz

IV. RESULTS

Fig.4 and Fig.5 show the dependence of the area demand on the resolution of the DC DAC and RF DAC, respectively. For resolutions up to 16 bit, the area demand of the DC DAC is comparable to the area demand of the rest of the control electronics. For the RF DAC, the area demand is comparable to the rest of the circuits for resolutions up to 14 bit. Therefore, efforts to reduce the area of the electronics should not only focus on the DACs, but comprise all components of the control electronics.

In order to reduce the area demand, the DACs are charged in a stepwise manner (see Fig.6). This initial charging only has to be done during the initialization phase. Therefore, it is not a time-critical process. Once the DAC is charged to its setpoint, the charging only has to compensate for leakage. The power consumption of the DAC is shown in Fig. 7. It depends on the actual DAC setting and varies between 5µW and 25µW.

V. CONCLUSIONS

Overall, the area consumption of the control electronics as investigated here is still considerably larger (on the order of 100µm × 100µm) than the size of the qubits. However, the investigated structures were not yet optimized for area demand and there is the possibility to use smaller process nodes than the 65nm process considered in this paper. In addition, the use of multiplexing techniques will allow to steer multiple qubits with the same DAC.

With respect to the power consumption, approximately 20µW per DAC channel sound promising. The DAC was not yet optimized for power consumption and multiplexing techniques will again allow to share one DAC between multiple qubits. Taking into account the cooling power of dilution refrigerators around 100mK (the typical operating temperature of GaAs qubits) of approximately 1mW, the approach shown here should allow to operate on the order of hundred qubits, even with today's available commercial CMOS processes. With the use of dedicated cryogenic electronics using supply voltages on the order of 10mV instead of 1V, the power consumption could be reduced by another factor 10.000, $(1V/10mV)^2$.

In summary, using standard CMOS processes seems a viable way to implement cryogenic control electronics for qubits as a starting point towards a truly scalable universal quantum computer. It will allow the implementation of quantum computers using hundreds of qubits.

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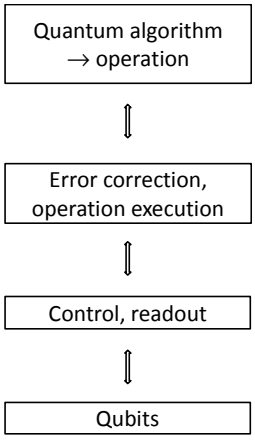

Fig. 1. Simplified system diagram of the considered quantum computer. The control electronics considered here constitutes an interface between the quantum operation execution and the qubits.

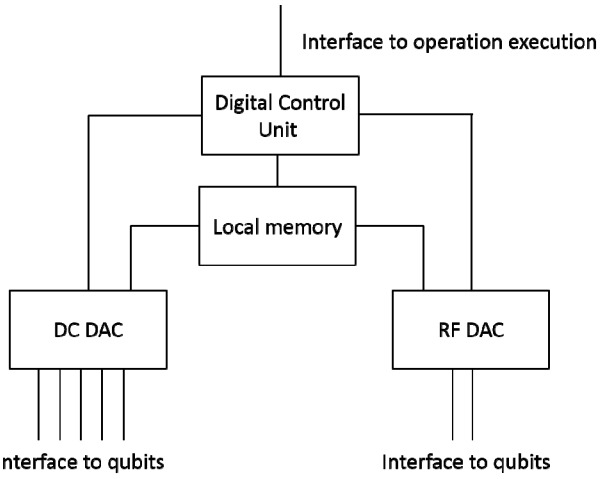

Fig. 2. Top level of the control system. It consists of a digtial controller that constitutes the interface to the higher layers of the quantum computer (error correction and quantum operation execution) and the individual components of the control electronics like memory and digital-to-anaolog-converters (DAC).

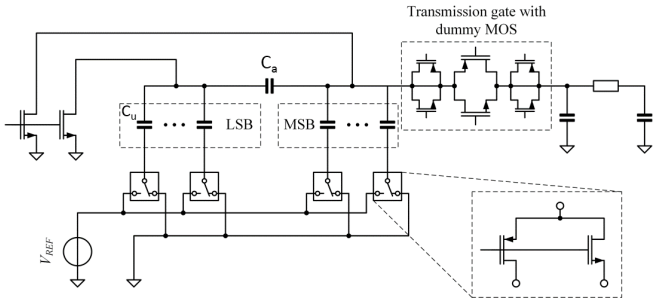

Fig. 3. DAC implementation.

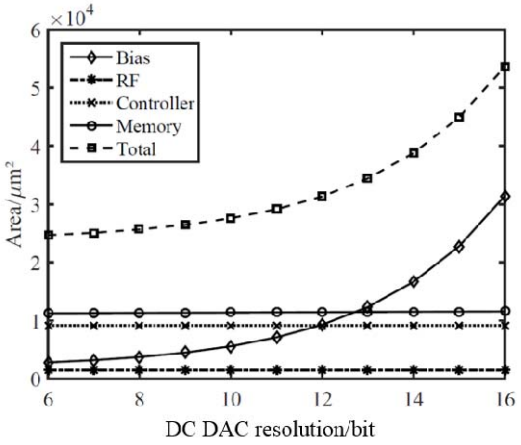

Fig. 4. Dependence of area demand on DC DAC resolution. The RF DAC resolution was kept constant at 12 bit.

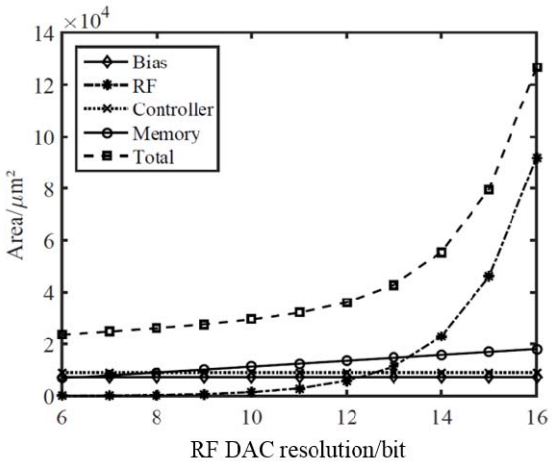

Fig. 5. Dependence of area demand on RF DAC resolution. The DC DAC resolution was kept constant at 10 bit.

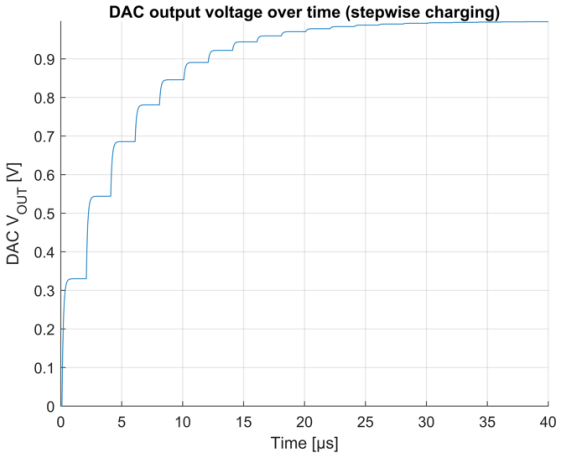

Fig. 6. Charging behavior of the charge-redistribution DAC. Only capacitive losses for the input capacity have been taken into account.

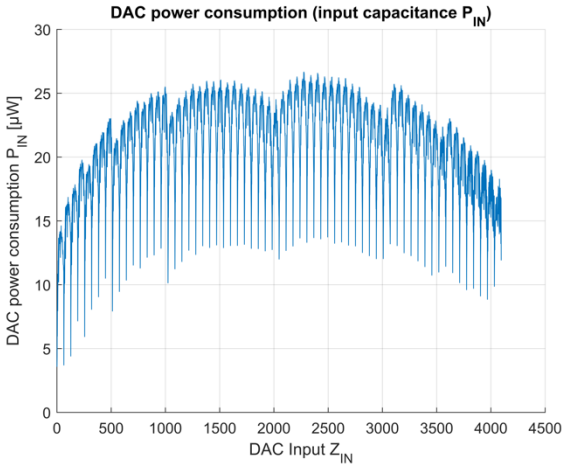

Fig. 7. Power consumption of the charge division DAC