Investigating CMOS Based Local Bias Voltage Generation for Solid-State Qubit Potential Well Creation

Patrick Vliex[1], Carsten Degenhardt[1], Lotte Geck[1], Andre Kruth[1], Dennis Nielinger[1], Stefan van Waasen[1,2], Stefan Heinen[3]

[1]Central Institute of Engineering, Electronics and Analytics, ZEA-2 Electronic Systems, Forschungszentrum Jülich GmbH,
[2]Communication Systems Department (NTS), University of Duisburg-Essen
[3]Chair of Integrated Analog Circuits and RF Systems, RWTH Aachen University

Goals & Motivation

Quantum Computer needs millions of physical Qubits[1,2]

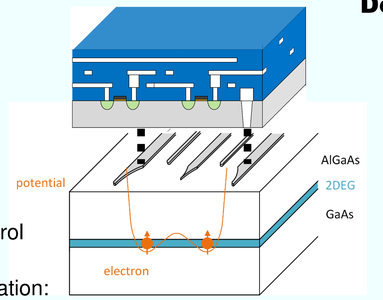
- Qubits operated inside a dilution refrigerator
- Number of Qubits need to increase by several orders of magnitude to build a universal quantum processor
  - Need for a completely scalable solution
  - Technology operable at cryogenic temperatures, 4 K down to 20 mK

→ Integrated semiconductor based devices are promising candidates in order to meet these criteria, i.e. modern CMOS process technology

Integrate Local Classical Control Electronics with Qubits

- Long-term scalability calls for local classical control electronics:
  - Reduce number of wires fed into the fridge
  - Reduce bandwidth by pre-processing data
  - (Partly) local quantum error correction possible
- Electronics should include: bias voltage DACs, control pulses generation, readout, data pre-processing
- Top-down system design and bottom-up implementation:

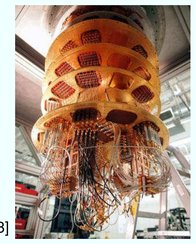
→ Investigate system partitioning (RT, 4 K and Qubit stage)
→ Design specialized ICs for cryogenic temperature



State of the Art

"Brute Force" Scaling

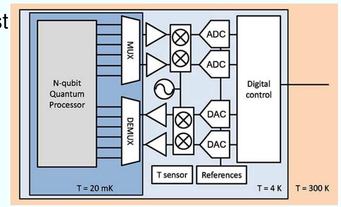
- Increase the no. of wires to connect as many Qubits as possible
- 7 x 7 qubits are targeted to be operated[3]
- No full scalability to millions of Qubits



[3]

4 K Stage Control Electronics[4]

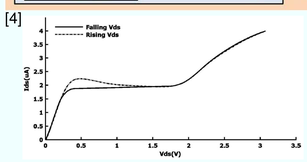
- Ongoing research activity in order to bring control electronic into the dilution refrigerator, including use of FPGAs, ASICs and off-the-shelf components
- Only limited number of devices operated at the lowest temperature stage (e.g. MUX and DEMUX)
- Considerably more cooling power available on 4 K stage, but interconnect to Qubits via cables required
- Multiplexing used to reduce the required number of cables



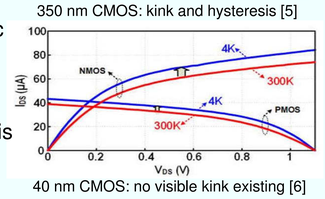
[4]

CMOS Cryogenic Operation

- Ultra low temperatures lead to MOSFET behavior anomalies e.g.:[5]
  - Kink effect
  - Dopant freeze-out (<30 K)
  - V_{TH}-shift
  - I_D-Hysteresis
- Rapid increase of noise below 50 K, due to cryogenic anomalies (in 350 nm CMOS)[5]
- Reduced kink for CMOS process nodes < 100 nm[6]
  → Use small technology nodes
- No standard model for cryogenic MOSFET behavior is commercially available[6]
- Modeling and fitting of CMOS parameters is required



350 nm CMOS: kink and hysteresis [5]

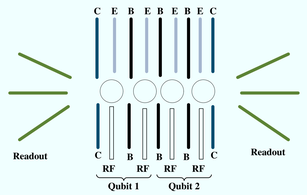


40 nm CMOS: no visible kink existing [6]

System Level Considerations

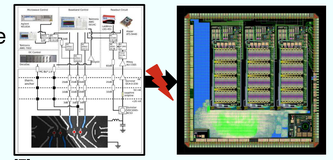
IC for Bias Voltage Generation

- Generate bias voltages for Quantum Dot (potential well for electrons)
- Update times in the range of milliseconds
- 5-10 DC voltages needed for one Qubit
  - Bias tee used for RF electrodes
- Voltage digital-to-analog converter (DAC)



Design Challenges

- Cryogenic operating conditions
- Ultra-low power consumption: ca. 1 mW total cooling budget at lowest cooling stage
- Extremely stable output voltages: uncertainties of less than 30 µV
- Scalable architecture (e.g. multiplexing)
- Quantitative design specifications still premature
- Include various options to tune circuit

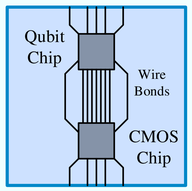


[7]

→ Novel IC circuit architectures and approaches enabling solutions not applicable without CMOS technologies

Cryogenic IC Qubit Control Demonstrator

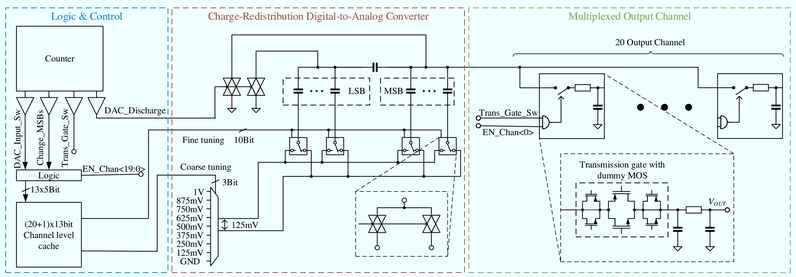
- Design of a proof of principle demonstrator in commercial CMOS 65 nm technology
- Operation on the same interposer as the Qubits
  - Lowest temperature regime of dilution refrigerator (<100 mK)
  - First step: DC biasing DACs for potential well creation
  - Test structures support fitting of device model parameters to cryogenic environment
  - Prove feasibility of using commercial CMOS to control a Qubit and develop system concepts for full scalability



Implementation

Charge-Redistribution DAC Topology

- Utilize reduced thermal noise at cryogenic temperatures: $\overline{V}_{N,RMS} = \sqrt{\frac{k_B \cdot T}{C}}$ [8]
- Iterative charging concept implemented
- Periodical refresh needed to compensate leakage currents
- Reduce power consumption by coarse tuning reference voltages
- Multiplexing of output channels to further enhance power and area efficiency
- Passive low-pass filtering of output signals

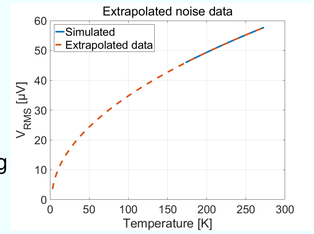


Voltage Stability

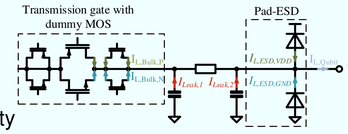
- Simulated static operating point noise in one output channel and extrapolated data

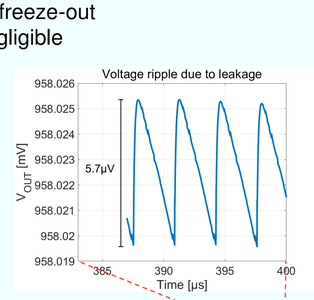
$$\overline{V}_{RMS} \propto \sqrt{\underbrace{T/I_D}_{} + \underbrace{T \cdot I_D + T^2 \cdot I_D^2}_{}}$$ [9]

Noise source: **Thermal** Channel



- Small I_D due to low current flow for refreshing (range of 5-10 nA)
- Thermal noise is main contributor
- Simulated noise at 100 mK: $\overline{V}_{N,RMS} \approx 1.3\ \mu V$ close to $\sqrt{\frac{k_B \cdot 0.1K}{1\ pF}} = 1.17\ \mu V$
- Leakage currents causing voltage drop on the capacitors
  - Tradeoff: power vs. voltage stability
  - Max. 10 µV (with process variations and mismatch)
    → ~300 kHz refresh frequency per channel
  - Simulation models do not include dopant freeze-out
    → Leakage at 100 mK expected to be negligible
    → Decreased refresh rate possible





Power Consumption

- System speed defined by transmission gate "on"-time (4 ns → 125 MHz clock rate)
- Major part of power dissipated in digital logic and buffers for transmission gate control
  - $P_{Dig} \propto V_{DD}{}^2$
  → Reduce supply voltage
  → Dedicated cryogenic CMOS technology operating at few mV supply
- Reuse control signals for multiple DACs

No. DACs	No. channels	Power per channel
1	20	4.2 µW
5	100	2.7 µW

→ DAC architecture and global signals promise further reduction of power consumption

Conclusion and Outlook

- Promising early noise simulations indicate the potential of cryogenic ICs
- Promising early power simulations encourage the feasibility to operate multiple Qubits within given power budget
- Investigate the influence of parasitics on the supplied voltages
  - Need for ultra-low noise supply and reference voltages
- Decide on interface protocol (robustness, efficiency)
- Integration of ADC for DAC output verification on demonstrator

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[4]F. Sebastiano *et al.*, "Cryogenic CMOS interfaces for quantum devices," *2017 7th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI)*, Vieste, 2017, pp. 59-62.
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[6] E. Charbon *et al.*, "15.5 Cryo-CMOS circuits and systems for scalable quantum computing," *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, 2017, pp. 264-265.
[7]Tim Botzem, „ Coherence and high fidelity control oftwo-electron spin qubits in GaAs quantum dots," PhD Thesis, p. 36, Figure 4.2.: Schematic setup. Online: http://publications.rwth-aachen.de/record/689507, 14.08.2017
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