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Strained Silicon Complementary TFET SRAM: Experimental Demonstration and Simulations

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ABSTRACT A half SRAM cell with strained Si nanowire complementary tunnel-FETs (TFETs) was fabricated and characterized to explore the feasibility and functionality of 6T-SRAM based on TFETs. Outward-faced n-TFETs are used as access-transistors. Static measurements were performed to determine the SRAM butterfly curves, allowing the assessment of cell functionality and stability. The forward p-i-n leakage of the access-transistor at certain bias configurations leads to malfunctioning storage operation, even without the contribution of the ambipolar behavior. At large V_{DD}, lowering of the bit-line bias is needed to mitigate such effect, demonstrating functional hold, read and write operations. Circuit simulations were carried out using a Verilog-A compact model calibrated on the experimental TFETs, providing a better understanding of the TFET SRAM operation at different supply voltages and for different cell sizing and giving an estimate of the dynamic performance of the cell.

INDEX TERMS SRAM, static noise margins, tunnel FET.

I. INTRODUCTION

Supply voltage V_{DD} scaling is needed to reduce the power dissipation in digital electronics. In this scenario Tunnel-FETs (TFETs) emerged as energy efficient switches: the exploitation of band-to-band tunneling allows for sub-threshold swing (SS) steeper than 60 mV/dec at room temperature [1], [2] resulting in high on-current to off-current ratios (I_{ON}/I_{OFF}) at small voltages. In recent years, many groups succeeded in fabricating TFETs showing sub-60 mV/dec switching operation [3]–[5]. Among the different device architectures, experimental Si TFETs show competitive results in comparison to III-V and Ge TFETs, as indicated by the benchmarks of drain current I_D vs. SS [3]–[6] and I_{ON}/I_{OFF} [7], [8]. So, although the large (and indirect) band-gap of silicon may discourage its use for band-to-band tunneling devices, Si TFETs exploit the mature CMOS technology which enables the easy processing of p- and n-type devices on the same technology platform and thus the adoption of circuits based on complementary TFETs (CTFETs). In fact, first fabricated logic circuits employing TFETs were Si CTFET inverters [9]–[11] and Si TFET current mirrors [12].

TFETs show peculiar electrical characteristics with respect to conventional MOSFETs. The implications of these characteristics on TFET-based circuits need to be investigated but one cannot rely just on single device characterization. So far, evaluation of the performance of various digital and analog building blocks employing TFETs has been mainly analyzed by means of mixed-mode device/circuit TCAD simulations [13]–[17] and with Verilog-A models based on look-up tables for the TFETs [18], [19].

The static-random-access-memory (SRAM) cell, being one of the most important digital building block widely used as data caches in processors, is an important circuit vehicle to assess the advantages of TFETs over conventional MOSFETs. Early analysis based on simulation mainly relied on idealized TFET templates [13]–[19], neglecting fundamental aspects of experimental devices, such as parasitic phenomena leading to ambipolarity and to forward p-i-n leakage. As regards the ambipolar behavior, it was shown

that it needs to be suppressed to enable robust SRAM stability in retaining the data [16]. This can be addressed by various engineering techniques at device level [11]. On the other hand, the unidirectional conduction of TFETs is the main hindrance for the pass-transistors used as access transistor (AT), that are required to conduct current from source to drain and vice versa. Several modified SRAM topologies have been proposed in the literature to circumvent this issue using outward (O-AT) or inward faced (I-AT) AT configurations and/or adding more transistors to enhance the operation stability [13]–[19]. Recent simulation results with idealized TFETs as well as templates calibrated on experimental TFETs [16] suggested acceptable static performances of the simple 6T-SRAM design with outward ATs provided that the read operation is performed with a bit-line (BL) precharge at $0.5 \times V_{DD}$, but no experimental verification has been reported so far (to our knowledge). In this regard, the purpose of this paper is to experimentally explore the operation of 6T-SRAM employing TFETs by characterizing a half SRAM (HSRAM) cell composed by strained Si NW TFETs.

The reminder of this paper is organized as follows. Section II details the TFET fabrication process, with emphasis on the device engineering strategy to reduce the ambipolarity. Section III presents the fabricated HSRAM cell with the related device characteristics; experimental SRAM static-noise-margins are discussed in that section. Section IV extend the analysis by exploring various cell sizing and V_{DD} levels by means of supporting simulations; dynamic performance are also estimated. Finally, Section V concludes this paper.

The present paper is an extended version of the results presented at the *47th European Solid-State Device Research Conference* [20].

II. STRAINED SILICON NANOWIRE TFETS

A. FABRICATION PROCESS

Nanowire (NW) TFETs were fabricated on 15 nm thick biaxial tensile strained sSOI ($\varepsilon_{biax} = 0.8\%$) substrates with 145 nm BOX using electron beam lithography and dry etching. HF is then used to underetch the patterned silicon, thus creating suspended NWs (Fig. 1a). The nanowires have a cross-section of $45 \times 5nm^2$. A 3 nm thick HfO_2 layer was grown by atomic layer deposition (ALD), followed by atomic vapor deposition (AVD) of 40 nm TiN around the NWs as gate material (Figs. 1c). Then 70 nm PECVD SiO_2 was deposited and patterned to create the spacer on the drain side (Fig. 1b) for suppression of the ambipolar behavior. Epitaxial $NiSi_2$ layers at source/drain (S/D) areas were formed by annealing a very thin Ni layer at 700°C in forming gas for 30 seconds. Excessive Ni was removed by selective wet etching. Such a $NiSi_2$ formation exhibits good alignment with no encroachment of the silicide into the channel region [9]–[11]. The S/D region were defined by ion implantation with boron (1.5 keV, 5×10^{15} cm^{-2})/phosphorous (3 keV, $10^{15} cm^{-2}$) ions under a tilt angle of 45° into the preformed silicide. For each step of implantation, the opposite side was covered with PMMA to prevent intermixing of dopants. Doped pockets close to the $NiSi_2$/Si interface, resulting in very steep tunnel junctions [9]–[11], were obtained by driving the dopants into the Si NW by means of a low temperature anneal (500° C for 10s in RTP in N_2/H_2 environment).

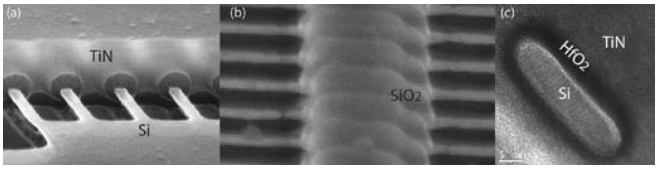

FIGURE 1. (a,b) Array of NWs constituting a TFET, showing the gate-drain underlap and the SiO_2 drain spacer. (c) Cross sectional TEM images for a single NW wrapped by the HfO_2/TiN gate stack.

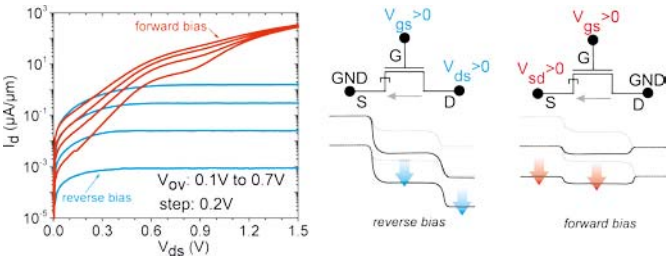

FIGURE 2. I_D-V_{DS} output characteristics of an n-TFET reported for both positive (blue) and negative (red) V_{DS}, for an overdrive voltage V_{OV} ranging from 0.1V to 0.7V with a step of 0.2V ($V_{OV} = V_{GS}$-V_{OFF}, where V_{OFF} is defined as the V_{GS} at which the I_D-V_{GS} for $V_{DS} = 0.5V$ reaches its minimum point). When $V_{DS} > 0$ the p-i-n diode operates in reverse bias, and the conduction is controlled by the gate voltage (TFET mode). When $V_{DS} < 0$ the p-i-n diode is forward biased and shows a conduction current only barely controlled by the gate terminal.

B. AMBIPOLAR AND UNIDIRECTIONAL CONDUCTION OF TFET

Ambipolarity (conduction also for opposite V_{GS}) and unidirectional conduction (different current at $V_{DS} > 0$ and $V_{DS} < 0$) are peculiar behavior of TFETs and need to be analyzed when considering TFETs as an alternative to conventional MOSFETs.

As regards unidirectional current conduction, Fig. 2 illustrates the I_D-V_{DS} output characteristics of an experimental n-TFET emphasizing that a non-symmetric current transport can be observed rather than *unidirectional conduction*. In fact, a positive V_{DS} voltage (i.e., positive voltage at the n-region) leads to reverse biasing of the p-i-n band structure and results in the desired transistor behavior with saturated currents (blue curves). In contrast, when a high potential is applied at the source terminal (i.e., $V_{SD} > 0.5V$), the TFET exhibits large current flow due to forward biasing of the p-i-n structure (red curves). In comparison with operation at $V_{DS} > 0$, this forward p-i-n leakage current is barely controlled by the gate voltage. Furthermore, the curves at different V_{GS} converge for $V_{SD} > 1.2V$, meaning that the gate loses control of the channel and the current is controlled only by V_{SD}. In order to prevent

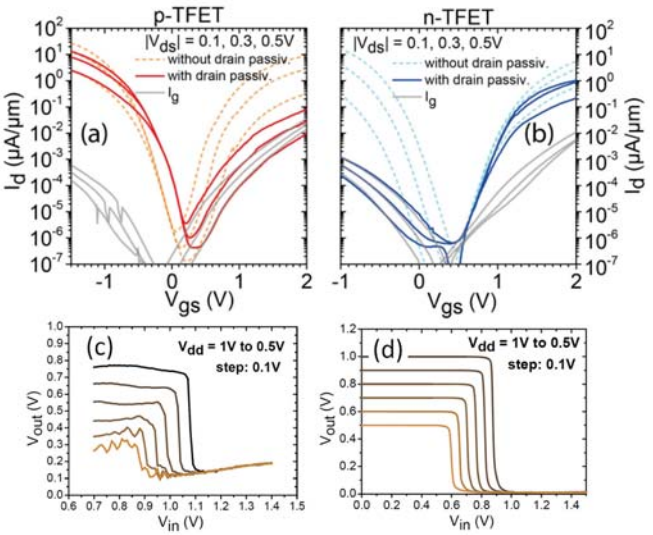

FIGURE 3. **I_D-V_{GS} transfer characteristics of (a) p- and (b) n-TFETs with sSi GAA NWs with (solid lines) and without (dashed lines) gate-drain underlap created through the SiO_2 spacer at the drain side (see Fig. 1b). Experimental C-TFET inverter VTCs implemented with (c) ambipolar devices and (d) devices with drain spacer for $V_{DD} = 0.5 \cdots 1$ V (step 0.1 V). Due to the ambipolar behavior of the devices, the high output level of the inverter VTC in (c) does not reach the nominal high and low voltages, i.e.,V_{DD} and 0 V respectively.**

uncontrolled large parasitic currents, the forward biasing configuration needs to be avoided [18] although this is not possible in the SRAM cell, as we will see in the following.

As regards ambipolar conduction, Fig. 3 shows the I_D-V_{GS} transfer characteristics of experimental n-TFETs (a) and p-TFETs (b). Solid lines are related to wafers processed with the full process steps, while dashed lines are related to wafers where the drain spacer creation has been skipped. The comparison of these two device sets emphasize the impact of the spacer on the ambipolarity suppression (note that the small degree of ambipolarity of the devices with spacer is caused by the gate leakage, and not by the parasitic band-to-band tunneling at the drain side as for devices without gate-drain underlap). It is important to remark that such a drain-gate underlap results in an intrinsic Si region between the channel and the silicide at the drain side, which increases the series resistance, as demonstrated by the lower I_{ON} (see Fig. 3a-b).

C. CHARACTERIZATION OF INVERTERS

Fig. 3c and d report the voltage transfer characteristics (VTCs) of two inverters implemented with CTFETs with and without ambipolar behavior, respectively. The inability of the ambipolar TFET inverter to feature rail-to-rail output swing (Fig. 3c) proves the importance to keep the ambipolarity of the devices under control. This becomes even more crucial for the SRAM operation since with ambipolar ATs, the cell in "hold" state cannot be isolated from the bit-lines (see [16]).

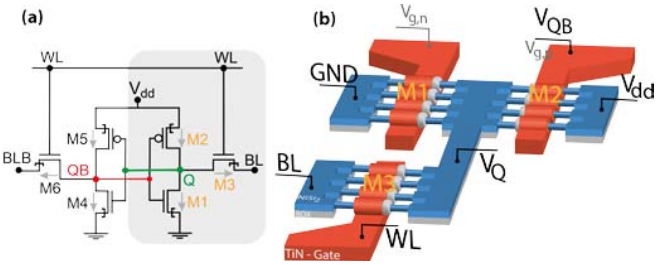

FIGURE 4. **(a) Symmetric 6T SRAM design composed of two cross-coupled inverters and two access transistors in outward configuration. (b) Sketch of the fabricated half SRAM layout composed of three strained Si NW TFETs (M1-M3) to investigate the 6T-SRAM static operation.**

III. FABRICATED HALF SRAM

The symmetric six-transistor (6T) structure shown in Fig. 4a is the most common and simple topology for CMOS SRAM cells. The core of the cell are the two cross-coupled inverters that store a differential logical level in the Q and QB nodes. The potential at nodes Q and QB can be accessed (read) and manipulated (write) with the bit-lines (BLs) through the ATs depending on the word-line signal (WL). Otherwise, the voltage level in Q and QB is preserved during the hold state.

The layout of the fabricated TFET HSRAM is sketched in Fig. 4b. The half-cell allows for the measurement of the inverter VTC as deformed by the presence of the AT, considering various WL and BL conditions, in order to reconstruct the butterfly curves for each SRAM operation. From the butterfly curves one can then extract the static noise margins (SNMs) for the hold, write and read operations (HSNM, WSNM and RSNM, respectively). Each TFET consists of an array of 60 NWs with a width of 30 nm and thickness of 10 nm (30×10 nm^2 cross-section). The gate length is about 100 nm.

We selected the outward orientation for the ATs, based on the simulations in [16], which suggest that O-AT is preferable with respect to the I-AT. In fact, the I-AT configuration does not allow for stable write and read operations for a given cell sizing.

Instead of a common gate for the pull-up (PU) and pull-down (PD) TFETs (M1 & M2 in Fig. 4a), we keep them independent in order to compensate for possible threshold voltage mismatch due to the limitations of our fabrication process (note the independent gates G_n and G_p in Fig. 4b). This workaround makes it possible to electrically adjust the threshold voltage of each device, by adding a voltage offset to the applied input voltage V_{QB}.

Fig. 5 presents the I_D-V_{GS} transfer characteristics measured for the three devices that compose the fabricated cell: the PU p-TFET (a), the PD and outward-AT n-TFETs (c and d, respectively). The reported devices feature reduced ambipolar current, as pointed out when discussing Fig. 3. The full suppression of the ambipolarity of the AT (Fig. 5d) with respect to the other devices (along with the reduced I_{ON} and the shifted threshold voltage) indicates a large process

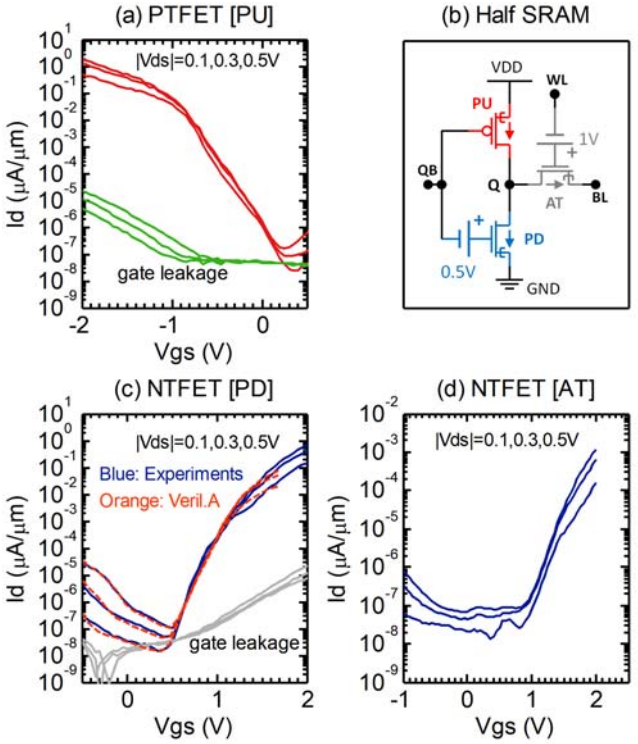

FIGURE 5. **I_D-V_{GS} transfer characteristics of the (a) p-TFET and (c) n-TFET used as pull-up and pull-down transistors of the inverter, and of the (d) n-TFET used as AT. (c) displays the experimental I_D-V_{GS} (blue) as well as the current from the Verilog-A model that will be used in Section IV (orange). (b) Schematic of the half-SRAM including the voltage corrections needed to compensate for the threshold-voltage mismatch. Note that since the rising part of the I_D-V_{GS} for both PD and AT takes place for positive V_{GS}, the voltage sources needed to shift these curves to the left have the '+' terminal connected to the gates.**

variability, likely related to the SiO_2 drain spacer as well as to other electrostatics knobs (e.g., gate oxide thickness and metal gate workfunction). For the devices in Fig. 5, we extract the minimum off-current I_{OFF} at $|V_{DS}| = 0.5$ V as 0.11 pA/μm, 0.2 pA/μm, 0.15 pA/μm for M1, M2 and M3, respectively. The on-current I_{ON} corresponds to 0.06 μA/μm, 0.01 μA/μm, 1.1 nA/μm at a gate overdrive $V_{OV} = 1$ V, and the minimum SS is 100, 160, 220 mV/dec. The relative small on-current compared to the devices shown in Section II is due to the larger NWs cross-section resulting in worse electrostatics.

Fig. 5b sketches the equivalent HSRAM topology, including the gate voltage corrections to compensate for the threshold voltage mismatch of the PD and AT devices. The gate voltage offset needed to match the device threshold voltage is 0.5V for the PD n-TFET (M1, see Fig. 5c), 1V for the AT n-TFET (M3, see Fig. 5d), whereas the PU p-TFET (M2) does not need any correction. The high/low gate voltage levels applied to the various devices are summarized in Table 1 considering $V_{DD} = 0.8$V.

In the following, the static performance of the HSRAM is presented for various BL and WL voltage levels in order to observe the behavior of the node Q as a function of QB

TABLE 1. **Definition of the low and high voltage levels considering $V_{DD} = 0.8$V.**

Device	$V_{G,Low}$	$V_{G,High}$
(M1) n-TFET, PD	0.5V	1.3V
(M2) p-TFET, PU	0V	0.8V
(M3) n-TFET, AT	1V	1.8V

under different SRAM operations for $V_{DD} = 0.8$ V. The experimental setup and the HSRAM topology do not allow for time-domain measurements. This has been done by simulation, used to estimate read and write delays that will be shown in Section IV-B.

A. CHARACTERIZATION OF THE CELL IN HOLD

In the presence of ambipolar/unidirectional conduction, the HSNM cannot be computed by looking at the inverters alone, since the ATs are not really behaving as an open circuit [16].

To mimic a write operation of a neighboring cell within the same column, we set WL = $V_{G,low}$ for the AT while keeping the BL and BLB respectively to V_{DD} and 0. In both cases, the AT should be ideally off, screening the cell from the influence of the BL voltages. This is true for the HSRAM VTC taken at BLB = 0 (dotted red curve in Fig. 6a, note that this VTC is flipped since is expressed in the form QB=f(Q)), that is very close to the VTC of an inverter. The resulting VTC for BL = V_{DD}, instead, is strongly distorted (solid black curve in Fig. 6a), the reason being the forward p-i-n leakage in the AT, as explained in Section II. Since the high potential of the BL is applied at its source terminal, a significant current flow is established, which pulls up the potential of node Q and hence lift up the low level of the VTC. The distorted VTC does not allow for any static noise margin, i.e., HSNM = 0, meaning that the cell cannot operate. Only reducing the BL(B) to $0.5 \times V_{DD}$ mitigates the parasitic current and results in a VTC (dashed black curve in Fig. 6a) which gives margin for hold (HSNM = 213 mV, square in Fig. 6a).

The same analysis has been repeated for the hold condition under read of the neighboring cells: we force the BL/BLB pair to V_{DD} while keeping the WL low. Again, as demonstrated by the solid curves in Fig. 6b, the BLs at V_{DD} results in a hold fail, while the cell stability is guaranteed if the high BL potential is set to $0.5 \times V_{DD}$ (dashed curves in Fig. 6b) giving an HSNM of 224 mV (square in Fig. 6b).

Since we found that the cell in hold can preserve the logic state only when the BL(B) voltages are lower than $0.5 \times V_{DD} = 0.4$V, we continue the analysis by setting $0.5 \times V_{DD}$ as high logic level at the bit-lines for both read and write operations.

B. CELL UNDER WRITE AND READ OPERATIONS

Under write operation, the butterfly curves shift apart from the inverter case due to the large distortion of the VTC of

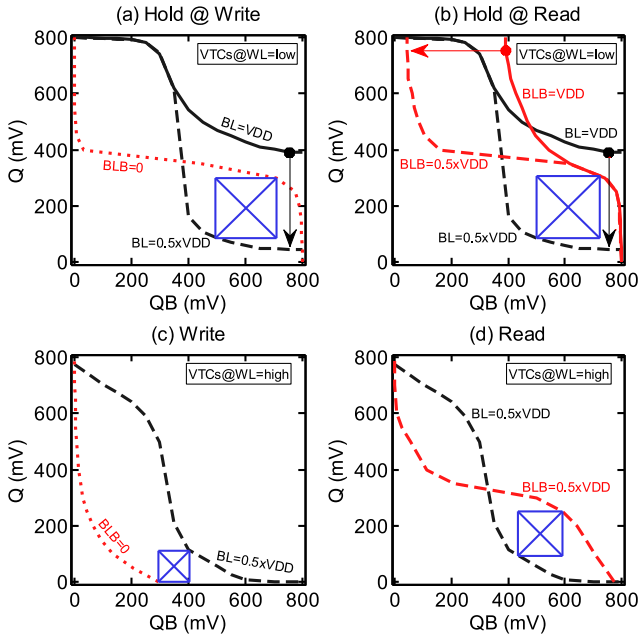

FIGURE 6. Experimental butterfly plots for SNM calculations: hold operations during a write (a) and during a read (b) of a cell sharing the same bit-lines of the cell under test. Write (c) and read (d) operations. The measured SNMs assuming a $BL_{High} = 0.5 \times V_{DD}$ for both read and write are: HSNM@W = 213 mV, HSNM@R = 224 mV, WSNM = 110 mV, RSNM = 156 mV. V_{DD} = 800 mV. The arrows in the plots show the VTC change due to lowering of BL_{High} from V_{DD} to $0.5 \times V_{DD}$.

the half-cell whose bit-line is connected to the low potential with active AT (see Fig. 6c). Such strong deformation results from the pull-down action of the AT forcing the storage node to follow the BLB = 0V potential. Consequently, the write butterfly curves have only one crossing point, which corresponds to the logical value that has to be written. In the write condition, the static noise margin is evaluated by considering the separation between the two VTCs [16]. In our case the extracted WSNM amounts to 110 mV (square in Fig. 6c).

The read is performed by applying a high potential at both BL(B) = $0.5 \times V_{DD}$ (bit-line precharge) and activating the AT with WL = $V_{G,AT,high}$. Compared to the hold state where the AT is switched OFF, the wings of the butterfly curve in Fig. 6d is compressed but still preserve the three crossing points. The extracted RSNM is about 156 mV (square in Fig. 6d).

C. DISCUSSION

The reported experimental HSRAM characterization has allowed us to highlight the importance of the forward p-i-n leakage and to explore alternative biasing of the BL to limit it. On the other hand, the analysis cannot be considered exhaustive as it is strongly limited by several factors affecting the devices constituting the HSRAM cell: (1) the large process variability reducing the probability of fabricating three same functional TFET devices in one cell; (2) the p-i-n leakage being comparable (or even larger) than band-to-band tunneling current; (3) the process variability leading to threshold voltage mismatch, requiring a compensation based on independent gates; (4) the small current and larger SS of the AT (as a result of the large V_{GS} levels needed to virtually compensate for the threshold voltage shift) that limited the analysis to relatively high V_{DD} (800 mV).

IV. SIMULATIONS

In order to extend the analysis at different V_{DD} values and estimate the dynamic performance of the cell, we have implemented a Verilog-A model based on a look-up-table calibrated against the n-TFET drain current shown in Fig. 5c, shifted by 500 mV in V_{GS}. This allows us to make the assumption of having perfectly repeatable n-TFETs (same characteristics for PD and AT, differently from the currents in Fig. 5), as well as symmetric p-/n-devices. In fact, the same look-up-table has been mirrored in order to obtain a perfectly symmetric virtual p-TFET. The analysis is carried out for a wide range of V_{DD} and cell sizing.

A. STATIC OPERATION

The simulated butterfly curves presented in Fig. 7 corresponds to the same situations (biasing and device size) shown in Fig. 6 (i.e., extracted from experiments). The main trends of the experiments are basically captured by the simulated cell: the p-i-n leakage contribute to the distortion of the butterfly in hold conditions, but this effect can be counteracted by lowering the nominal high voltage of the BL ($BL_{high} = 0.5 \times V_{DD}$). The fact that the read HSNM improves by moving from V_{DD} to $0.5 \times V_{DD}$ further supports the fact that the p-i-n leakage is dominant. This effect was not observed in our previous TCAD analysis [16], since the model (based on the devices in [9] and [21]) featured much higher band-to-band tunneling compared to p-i-n leakage, a better situation than in the experimental devices considered here.

The same analysis as in Fig. 7 has been repeated by scaling the V_{DD} down to 300 mV. Fig. 8 reports the SNMs normalized to the corresponding V_{DD} in order to enable a quick comparison among different V_{DD} values. The main message of Fig. 8 is that, with $BL_{High} = 0.5 \times V_{DD}$, all SNMs scale almost linearly with V_{DD}. This is not the case for the RSNMs which is reduced more than linearly with V_{DD} scaling, mainly due to the negative impact of the degradation of the VTC voltage gain with V_{DD} scaling. On the other hand, read with $BL_{High} = V_{DD}$ is not possible for any of the V_{DD} considered here, given that the obtained RSNM is close to 5% of V_{DD}.

The increase of the HSNMs (for $BL_{High} = V_{DD}$) with V_{DD} scaling in Figs. 8a-b is a sign of a lower deformation of the VTC, and this is due to the stronger dependence on V_{DD} of the p-i-n leakage (I_D at negative V_{DS}) than of the band-to-band tunneling current (I_D at positive V_{DS}).

This suggest that SRAM cell with optimized devices featuring a band-to-band tunneling current much larger than

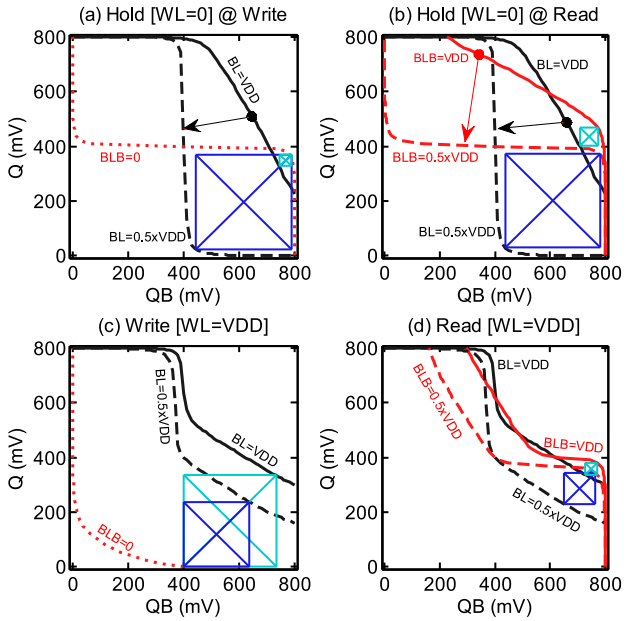

FIGURE 7. 6T TFET SRAM cell simulated with symmetric p/n-TFETs calibrated against the PD device in Fig. 5c . Hold SNM butterfly plots while (a) writing and (b) reading a cell sharing the same BLs. (c) Write butterfly plots. (d) Read butterfly plots. V_{DD} = 800 mV. Solid (dashed) lines refer to $BL_{High} = V_{DD}$ (or 0.5 × V_{DD}). The extracted SNMs assuming a $BL_{High} = V_{DD}$ (or 0.5 × V_{DD}) for both read and write operations are: HSNM@W = 40 (342) mV, HSNM@R = 66 (342) mV, WSNM = 333 (237) mV, RSNM = 43 (113) mV. V_{DD} = 800 mV.

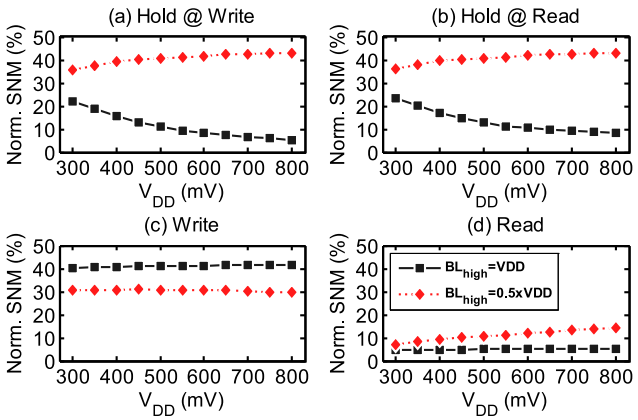

FIGURE 8. Simulated HSNMs during a write (a) and during a read (b) of a cell sharing the same BLs. (c) WSNMs. (d) RSNMs. The SNMs are extracted by assuming two possible definitions for BL_{High} : V_{DD} or 0.5 × V_{DD}. The margins are normalized to V_{DD}.

p-i-n leakage, may operate with $BL_{high} = V_{DD}$ during write '1'. In any case the read might be performed with the precharge at $0.5 \times V_{DD}$ due to TFET becoming unidirectional at low V_{DD} as suggested by simulations [16].

Fig. 9 reports the simulated SNMs for the write (WL='1', BL='1', BLB='0') and read (WL='1', BLs precharged at $0.5 \times V_{DD}$) operations as a function of the number of parallel NWs used to implement the AT, the PU and the PD. The figure considers V_{DD} = 400 mV and shows that there is, as expected, a trade-off between write and read SNM based on the number of NWs in the PU and in the AT: a weak PU is

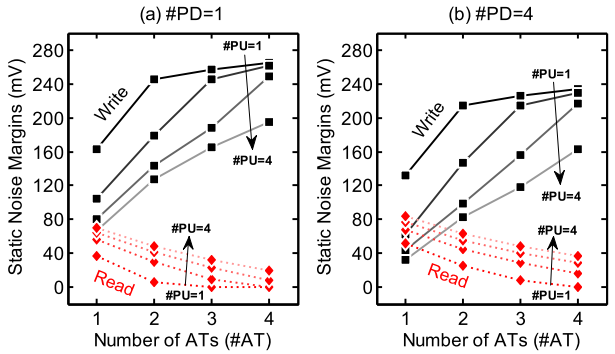

FIGURE 9. RSNMs and WSNMs as a function of the number of access-transistor NWs (#AT) and of pull-up transistor NWs (#PU) for (a) 1 single pull-down transistor NW and for (b) 4 PD NWs, of a 6T TFET SRAM cell simulated with symmetric p/n-TFETs calibrated against the n-TFET in Fig. 5c (M1 in Fig. 4). V_{DD} = 400 mV.

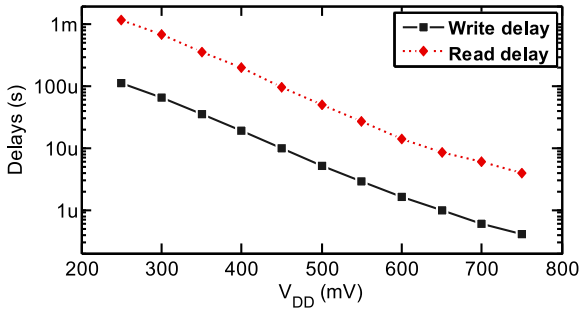

FIGURE 10. Read and write delays estimated for a virtual 6T TFET SRAM cell implemented with symmetric p/n-TFETs calibrated against the PD device in Fig. 5c. #PU = #PD = #AT = 1 NW. C_{BL} = 20 pF. Pre-charge during read is at 0.5 × V_{DD}, while write is performed with V_{DD} as BL_{High} value. The read delay is extracted at the time when a voltage difference of 10% of V_{DD} is detected between the BL nodes precharged at the same level (i.e., 0.5 × V_{DD}). The write delay is extracted at the time when the difference between the Q and QB nodes reach the 90% of V_{DD} during the switching.

good for write but bad for read, while a strong AT is good for write and bad for read. The effect of the PD is less relevant.

B. DYNAMIC PERFORMANCE

This section provides a rough estimation of the dynamic performance that a cell would have devices with a current drive as shown in Fig. 5c. In order to perform transient simulations, the compact model has been augmented with look-up-tables for gate to drain (C_{GD}) and gate to source (C_{GS}) capacitances. Since extracting the intrinsic capacitances from experimental C-V curves in such a small nanowire is essentially unfeasible, we have relied on TCAD simulations by considering a TFET nanowire template with physical and geometrical parameters (materials, doping, EOT, geometry) similar to the experimental one. Thus, C_{GD} and C_{GS} have been extracted by performing AC simulations for any V_{GS} and V_{DS} in the −0.8V to 0.8V range (step 10 mV). Furthermore, we assume an equivalent bit-line capacitance of 20 pF.

Fig. 10 reports the simulated write and read delays. The slow transient is in line with the low I_{ON} of the devices employed in this analysis. In fact, simulations of SRAM cells

built with aggressively scaled TFETs and FinFETs [16] show read and write delays more than three orders of magnitude lower than the delays in Fig. 10.

V. CONCLUSION

The first experimental HSRAM based on strained Si NW gate-all-around complementary TFETs with suppressed ambipolar behavior has been fabricated and characterized. Although the considered TFET devices turned out to be somehow underperforming (SS $>$ 60 mV/dec), they have allowed us to perform a systematical analysis on the static figures of merit of the 6T cell topology using TFETs. On the base of the butterfly curves, we have shown that with outward faced n-TFETs as ATs, functional operation for hold, read and write can be achieved when the high voltage potential at the bit-lines BL(B) is limited to $0.5 \times V_{DD}$. This requirement diminishes the impact of the forward p-i-n biasing of the O-AT by minimizing parasitic current leakage and thus reduces distortion of the resulting butterfly curves. The experimental analysis is restricted to static figures of merit. The study has been completed by relying on simulations (calibrates on the experimental n-TFET implementing the PD device) in order to provide an estimate of the behavior of a SRAM cell when implemented with symmetric and stable devices. In this case, the performance improve and the static behavior is satisfying also at low V_{DD}. About the read and write times, devices with higher on-current would be needed for fast operation.

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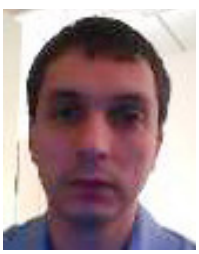

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