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The benefits of a gate-normal tunneling architecture in enhancing the on-current and average subthreshold swing of tunneling field-effect transistors were scrutinized in experiment through careful physical analysis of a $Si_{0.50}Ge_{0.50}$/Si heterostructure. In accordance with theoretical predictions, it is confirmed that the on-current is governed by line tunneling scaling with the source-gate overlap area of our devices. Our analysis identifies the early onset of parasitic diagonal tunneling paths as most detrimental for a low average subthreshold swing. By counter doping the channel, this onset can be shifted favorably, permitting low average subthreshold swings down to 87 mV/dec over four decades of drain current and high on-off current ratios exceeding 10^6. *Published by AIP Publishing.* https://doi.org/10.1063/1.4996109

In the search for low power alternatives to metal-oxide-semiconductor field-effect transistors (MOSFETs), tunneling FETs (TFETs) have become an extensive field of research in recent years.[1,2] The advantage of TFETs lies in the current transport mechanism based on band-to-band tunneling (BTBT), allowing subthreshold swings (SS) of less than 60 mV/dec at room temperature. This implies that TFETs may be operated at lower supply voltages, resulting in lower overall power consumption.[1,2] However, soon after the fabrication of the first TFETs consisting of simple lateral pin-structures, it was realized that they cannot reach on-current values as high as MOSFETs.[3] As a potential solution, the idea of "vertical" or "gate-normal" tunneling emerged, in which the tunneling direction is parallel to the electric field of the gate.[4,5] For this purpose, the source is extended to underneath the gate (undercut). A thin pocket of opposite dopants is added in the undercut region between the source and the gate forming a vertical pn-junction. However, lateral tunneling may cause severely increased off-state leakage and heavily degraded turn-on abruptness. A solution proposed by Agarwal *et al.*[3] consists of thinning the channel on the drain side by pushing up the buried oxide and hence suppressing lateral tunneling to a very large extent. This approach was used with altered geometry in combined experimental and theoretical studies on a III/V platform.[6–8] Further theoretical studies investigated different materials, effects of quantum corrections, and parasitic diagonal tunneling.[9–11] Even though a lot of theoretical work has been published on the topic, few experimental results are available, especially for Si-based technology.

In the scope of our study, we expand the distinct tunneling paths present in gate-normal tunneling FETs continuing our efforts from previously published work.[12,13] The fabricated TFETs comprise a vertical SiGe/Si hetero-tunneling junction and use an air bridge design to prevent lateral leakage. In the experimental section of our paper, we identify distinct TFET operation followed by an analysis of the on-current, confirming that tunneling takes place over the whole source-gate overlap area as expected from theory. The main focus of this paper lies on the interplay of gate-normal tunneling on a 2D line (line tunneling) and parasitic diagonal tunneling.[11,14] We devote particular attention to an early gate voltage onset of the latter and the negative consequences of this on the average subthreshold swing. The details of the TFET geometry and channel doping are analyzed in comparison with Technology Computer Aided Design (TCAD) simulations in order to merge line and diagonal tunneling components closely and circumvent a degraded average SS. The simulations identify a higher resilience of counter doped TFETs against fringing fields as the reason for the much-improved performance statistics found in experiment.

The layers used in our experiments were grown by reduced pressure chemical vapor deposition (RP-CVD) on a 200 mm SOI substrate with 145 nm buried oxide (BOX) and 55 nm Si. The 55 nm Si layer was thinned down to about 10 nm by repeated oxidation and HF etching before growth. About 13 nm of $Si_{0.5}Ge_{0.5}$ with a boron doping of about 5×10^{19} cm^{-3} followed by a ~7 nm Si cap layer were subsequently grown. Substrates with intrinsic and slightly n-doped (counter doped) (3×10^{18} cm^{-3}) cap layers were grown with high quality [Fig. 1(a)]. The device concept is based on an air bridge design, where the p-type $Si_{0.5}Ge_{0.5}$ source and the n-type Si drain are connected via a thin Si channel over an air gap [Fig. 1(b)]. The air bridge is created by selective wet etching of SiGe with respect to Si[15] [Fig. 1(c)]. During this process, the acid attacks the exposed SiGe sidewalls of a rectangular mesa from all sides, etching inwards for about 200 nm. Less than 5 nm of Si are etched latterly in the same time. The top of the mesa is protected with SiO_2 and resist so that the Si cap layer is not thinned down during this step. After wet-chemical removal of the protection layers, the Si cap layer has bent down onto the SOI due to capillary forces. Bonding between the Si cap and the SOI is improved by a forming gas anneal (FGA) at 400 °C in H_2/N_2 for 10 min. The Si channel is covered by a 5 nm HfO_2/50 nm TiN gate stack extending from source to drain. The drain contact is

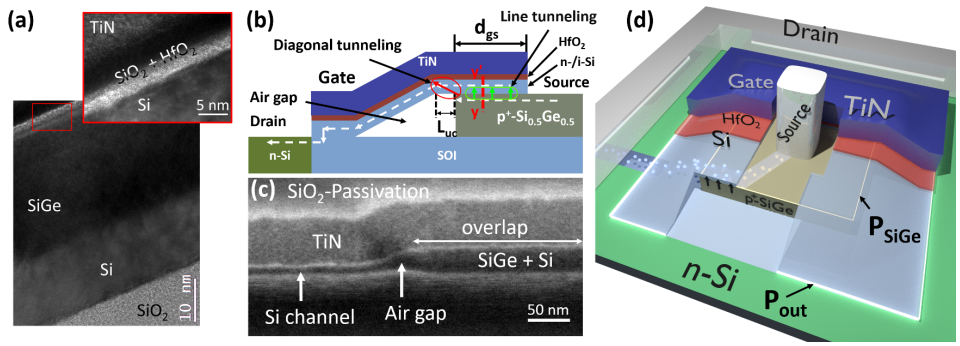

FIG. 1. (a) TEM cross-section of the layer stack in the source-gate overlap region. (b) 2D conceptual drawing. A current path from source (right) to drain (left) is illustrated. Line and parasitic diagonal tunneling are indicated by green and red arrows, respectively. Undercut L_{uc} and cutline y-y′ are illustrated. (c) SEM micrograph, showing the source-gate overlap area, the air bridge, and the Si channel leading towards the drain contact. (d) 3D model showing the geometry of devices. The source contact is formed in a recess area in the center of the gate. Perimeters P_{out} and P_{SiGe} are highlighted. (b) and (d) are not to scale.

formed on the gate-surrounding SOI layer by ion implantation of phosphorus at 2 keV to a level of 10^{19} cm^{-3}. The tunneling junction extends over an area of a few μm^2 where the channel and the gate overlap the SiGe source. The tunneling direction is parallel to the electric field induced by the gate. An essential requirement for our structure is a channel thickness of a few nm or less so that the electrostatic control of the tunneling junction through the gate is efficient. The current is injected at the source contact into SiGe in a recess area in the center of the gate [Fig. 1(d)]. In the overlap area of the channel and the source, carriers tunnel towards the gate as depicted by green arrows in Fig. 1(b). Importantly, the tunneling junction is located at a SiGe/Si hetero-interface, which allows low off-currents and small SS. Diagonal tunneling occurs as a consequence of elevated electric fields due to edge effects.[16]

Supporting 2D simulations were performed with the Sentaurus TCAD environment.[17] Band-to-band tunneling (BTBT) carrier generation was taken into account through the dynamic non-local path BTBT model, which is the most advanced BTBT model incorporated in Sentaurus TCAD.[17] Strained Si/SiGe band diagrams, including effective density of states and carrier effective masses used for the calculation of BTBT model constants, have been obtained by means of a 30-level k.p model.[18]

Figures 2(a)–2(c) motivate the purpose of the air-bridge geometry in avoiding direct source-drain leakage. As evident from the transfer characteristics (a), the "simple" device geometry suffers from much higher off-current than the "air-bridge" design. By contrast, for $V_g > 0.5$ V, both curves match closely because the gate-normal tunneling junction with an extent of 250 nm is identical for both devices. In the off-state, however, the p$^+$-SiGe layer below the gate in (b) cannot be depleted due to the high doping so that carriers injected at the source (right) can leak along the red-dashed line to the left and tunnel into the n-Si drain. This can be seen from a region at the drain with strong electron BTBT (eBTBT) carrier generation at $V_g = 0.1$ V and $V_d = 0.25$ V. Under the same conditions, a transistor with an air-bridge [Fig. 2(c)] shows hardly any eBTBT generation. This results in significantly lower off-current in the transfer characteristics below 0.5 V as shown in Fig. 2(a). While it is crucial to diminish the connection between the source and the drain, e.g., by the etching process described above, the size, geometry, and a partial filling of the air gap do not alter the ability to block direct leakage fundamentally. However, they may have a significant influence on the shape and character of the onset, as described in a later section.

In Fig. 3, the transfer characteristics (a) and the corresponding SS vs. I_d plot (b) of an experimental device are shown. The smallest slopes are obtained close to the onset of the transistor and may be caused by a modulation of the tunneling length. For all data points displayed in Fig. 3(b), including the ones marked by arrows [compare Fig. 3(a)], I_s and I_d are in good agreement, and any influence of the gate leakage current I_g can be excluded because I_d is at least one order of magnitude larger than I_g. Note that a sign change occurring between the n- and p-branches of the transfer characteristics could have an impact on the data points at the transition, leading to exaggeratedly small values of SS. Nevertheless, SS values ~60 mV/dec were reached. Additionally, the output characteristics of the same device as displayed in Fig. 3(c)

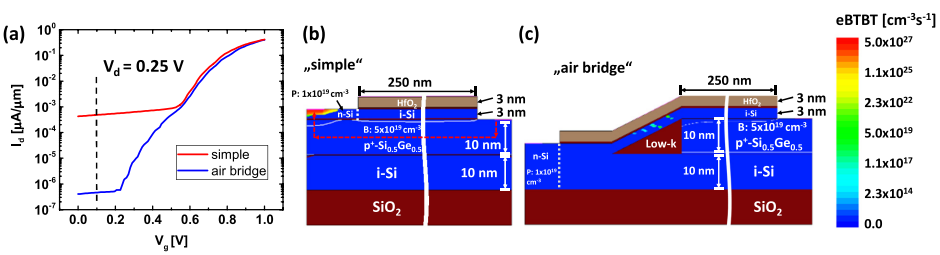

FIG. 2. (a) Simulated transfer characteristics of two devices with and without air-bridge design. As evident from the contour plots of the eBTBT generation rate (b) and (c) at $V_g = 0.1$ V and $V_d = 0.25$ V, direct source-drain leakage [red dashed line in (b)] is strongly reduced in the off-state due to the air bridge design, where the p$^+$-SiGe and the n-Si regions (connected to the source and drain terminals, respectively) do not form a pn-junction but are separated by the i-Si region, different from the "simple" design.

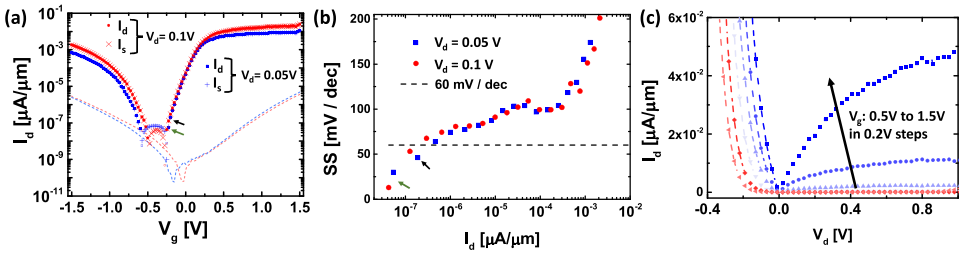

FIG. 3. (a) and (b) Transfer characteristics (I_d and I_s) and corresponding SS vs. I_d plot showing a region with SS < 60 mV/dec in a device with counter doping, a channel thickness of ~5 nm, and $A_{gs} = 33\mu m^2$. At the points in the sub-60 mV/dec region which are marked by (green/black) arrows, I_s and I_d are in good agreement. Data points at lower current are neglected in (b). (c) Output characteristics exhibiting a linear onset and strong current increase in reverse bias characteristic to TFETs.

exhibit typical TFET features. At positive V_d, the current first increases linearly and starts to saturate towards higher voltage, a behavior well known for MOSFETs. In contrast to MOSFETs, the opposite doping of the source and the drain leads to an exponential increase in current at negative V_d since the pin-diode is biased in the forward direction.

The main purpose of our structure is to examine line tunneling in the source-gate overlap area (A_{gs}). In the on-state, line tunneling is expected to contribute predominantly to I_d, which can be confirmed by checking for a dependence of I_d on A_{gs} as shown in Fig. 4. A dispersion of the on-current (I_{on}) becomes apparent in the n-branch of the I_d-V_g characteristics, which vanishes by normalizing to A_{gs}. The normalized currents match perfectly for $V_g > 0.5$ V, confirming that line tunneling is dominant in this region. While diagonal tunneling close to the air gap plays an important role in the early onset of the transistor as explained later (see Fig. 6), it can safely be excluded as the largest contributor to I_{on}. Its contribution is proportional to the outer perimeter of the SiGe Source P_{SiGe} [see Fig. 1(d)], which increases by a factor of about 1.35 (27 μm, 36 μm, and 50 μm) to the next bigger transistor size, while A_{gs} roughly doubles. Therefore, it is obvious that the dispersion in the I_d-V_g characteristics cannot originate solely from diagonal tunneling close to the air gap. Unlike that, the ambipolar current (p-branch) originates from tunneling parallel to the gate (point tunneling) at the drain-channel junction with a length equal to the outer gate perimeter P_{out} [see Fig. 1(d)].

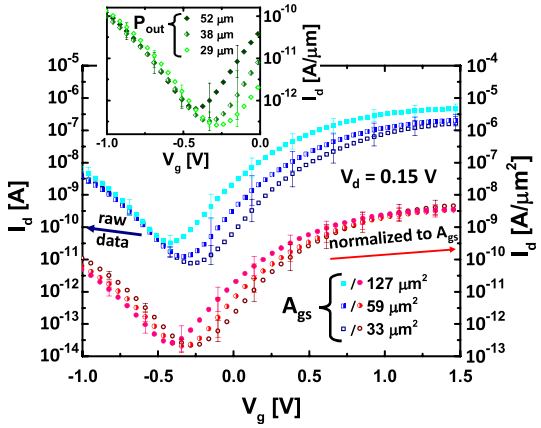

FIG. 4. Measured transfer characteristics of TFETs exhibiting higher I_{on} for transistors with larger gate-source overlap A_{gs} in the raw data. The dispersion vanishes when the data are normalized to A_{gs}. In contrast to that, the current of the ambipolar branch scales with P_{out} (inset).

Proof for this is provided by normalizing the current to P_{out}, where no dispersion remains below $V_g = -0.5$ V (inset of Fig. 4). Our findings demonstrate that the proposed thin channel geometry with a source-gate overlap embodies a means to efficiently use a large fraction of the transistor area in order to scale I_{on}.

Although it is not the intention of our work to reach record I_{on}, one may wonder about the main cause preventing I_{on} from reaching high values of 100 μA/μm or more targeted by the semiconductor industry.[3] With large d_{gs}-values of 4.5 μm, 7.25 μm, and 9.25 μm for transistors increasing in size, series resistance (R_s) in the channel could play a role. Other sources of R_s are source/drain contacts (no silicide used) and the contact between the underetched channel and the SOI because of insufficient intermixing, despite FGA at 400 °C. Yet, judging from the relation $I_{on} \propto A_{gs}$ and I_{on}-values of roughly the same order in experiment [Figs. 3(a) and 6(a)] and simulations (where R_s is neglected) (Fig. 5, $d_{gs} = 2500$ nm), the tunneling resistance appears to be dominant even in the on-state.

Even though a sufficiently high value of I_{on} is very important, a TFETs' great strength lies in the subthreshold regime due to their steep slope switching capability. Hence, it has to be guaranteed that a low average SS is achieved over many orders of magnitude of I_d. In any TFET geometry where line tunneling is present, electrostatic non-idealities or fringing fields will occur at the edges of the tunneling layer, leading to unwanted current contributions. A severe consequence of a premature onset of parasitic diagonal tunneling compared to line tunneling is a heavily degraded average SS. This issue is addressed in Fig. 5 showing a simulated I_d-V_g curve with an interrupted turn on. This is caused by a shifted onset of diagonal and line tunneling, with the first setting in at $V_g \approx 0.2$ V and the latter setting in at $V_g \approx 0.5$ V. As discussed in the previous paragraph, the line tunneling contribution to I_d scales with A_{gs} (in simulation, the overlap distance d_{gs} is sufficient), whereas diagonal tunneling close to the air gap and hence I_d in the range $0.2\,V < V_g < 0.5\,V$ are not affected by d_{gs} at all. Ideally, both onsets are close enough together so that no transition becomes evident in the I_d-V_g characteristics.

Consequently, for the optimal performance, such a mismatch between the onset of the tunneling contributions must be avoided. In this sense, devices with a counter doped channel have achieved by far better results compared to devices with an intrinsic channel (Fig. 6). As evident, no hump and

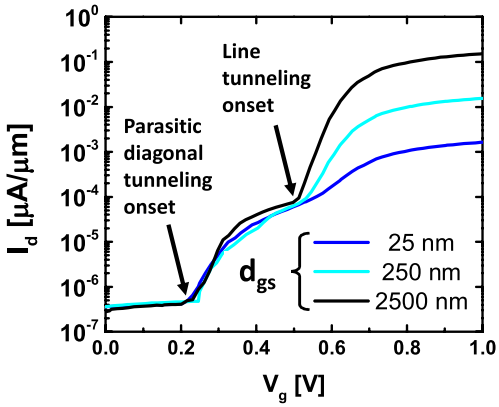

FIG. 5. TCAD simulated transfer curves for different gate-source overlap lengths d_{gs} at $V_d = 0.05$ V for a TFET as shown in Fig. 2(c), comprising a 3 nm thick i-Si channel. The onsets of diagonal and line tunneling are clearly distinguishable. The line tunneling current scales with d_{gs}.

therefore no considerable premature tunneling onset are present in the former. SS values of 87 mV/dec over 4 orders of magnitude of I_d are achieved. Unlike that, in transistors with an intrinsic channel, two distinct onsets can clearly be distinguished, resulting in much larger average SS (250 mV/dec) as seen in Fig. 6(a).

Figure 6(b) shows the simulated doping and band profile along the cutline y-y′ in Fig. 1(c) for a TFET with intrinsic and n-doped channels at $V_d = 0.05$ V and $V_g = 0$ V. In both cases, the boron doping profile of the source decays into the Si channel. Phosphorus used as a counter dopant compensates the decaying dopants from the source, leading to a sharp dip close to the SiGe/Si interface. By this mechanism, under the same bias condition ($V_g = 0$ V and $V_d = 0.05$ V), the bands in the channel of a counter doped device are bent further down. Therefore, a conduction-valence band overlap can be achieved at reduced bias with respect to the first onset of tunneling. Furthermore, based on a decrease in the tunneling length, the tunneling probability increases and thus I_{on}.

One key aspect of achieving good average SS in experiment is illustrated in Fig. 6(c). In real devices, fringing fields at edges of a line tunneling region depend heavily on the specific geometry of the edge. Even small geometric variations can lead to distinct changes in the transfer characteristics. In TCAD simulations, this can be triggered, e.g., by changing the undercut length L_{uc} [Fig. 1(c)] of the transistor from 0 to 7 nm as shown in Fig. 6(c). With decreasing L_{uc}, the shoulder in the I_d-V_g characteristics stemming from parasitic tunneling becomes more obvious and the average SS increases. The most important observation is that for a counter doped channel, the variance stemming from different L_{uc} values is only half of that of a device with an intrinsic channel. The enhanced stability against fringing fields is a consequence of an earlier onset of line tunneling with respect to diagonal tunneling. In experimental devices, small geometric non-idealities are always present. Thus, the improved performance of devices with counter doping seen in Fig. 6(a) is a direct consequence of the higher resilience against geometric variations of any kind. While our simulations can clearly capture the general trend, completely accurate simulations are beyond the scope of this work. Therefore, we refer to other theoretical studies such as Ref. 19, where the V_g-onset of Si and Ge line tunneling FETs with counter doping pockets is examined in detail, theoretically. The authors show large onset shifts for devices without counter doping when varying the physical oxide thickness, gate alignment, and tunnel layer thickness, including quantum corrections. Other studies focusing on quantum corrections show that a reduction or suppression of parasitic diagonal tunneling leads to an increase in onset voltage.[11,16,20] A situation as found in our experiment where $V_{g,onset}^{intrinsic} < V_{g,onset}^{counter-doped}$ is never explicitly shown in the cited references but may well be the result of a combination of all the above stated influences shifting the onset. Even though no plateau or hump is obvious in the transfer characteristics of devices with a counter doped channel, it may be beneficial for the SS to delay the onset of diagonal tunneling even further, e.g., by workfunction tuning with a dual metal gate as proposed by Cui *et al.*[21]

In summary, we have shown the feasibility of a vertical TFET structure in which I_{on} is line tunneling dominated and

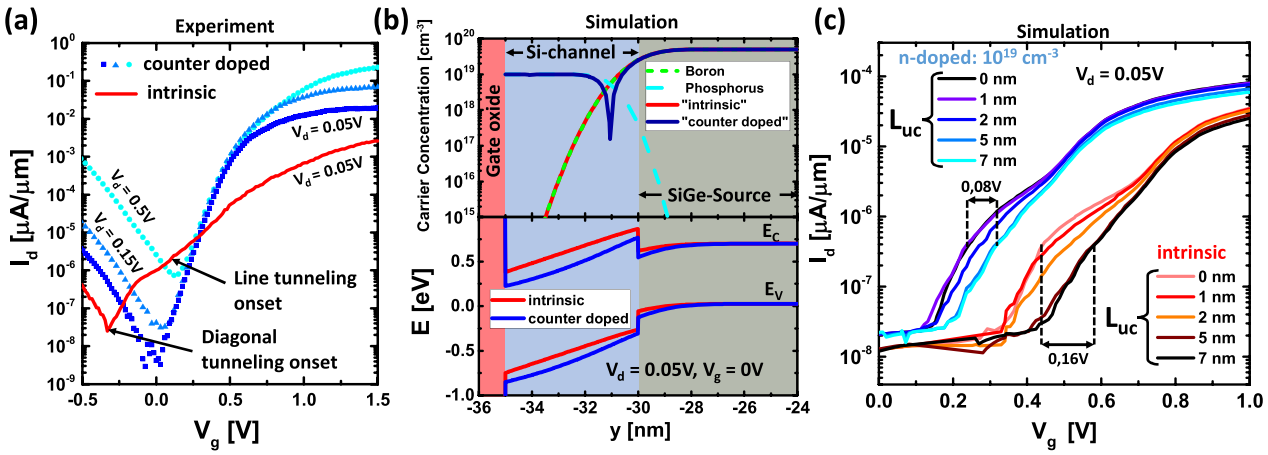

FIG. 6. (a) Comparison of typical experimental transfer characteristics of TFETs with and without counter doping, where the former exhibit no kink, better SS, and higher I_{on}. Both devices have a channel thickness of ~4–5 nm and $A_{gs} = 127$ µm^2. (b) Simulated doping profile and band structure along the cutline y-y′ in Fig. 1(c). In the "intrinsic" case, boron doping from the source decays into the Si-channel. In the case of counter doping, phosphorus compensates boron in the channel, leading to much stronger band bending (lower panel) at $V_g = 0$ V and therefore to enhanced tunneling probability. (c) Varying the underlap L_{uc} [Fig. 1(c)] shows that the persistence of the counter doped TFETs against fringing fields is better. Based on this robustness, much better results can be achieved in experiment.

scalable with the source-gate overlap area. As predicted by simulations, we have found evidence for a premature diagonal tunneling onset based on conceptually inherent electrostatic edge effects. By carefully engineering the tunneling layer thickness and using counter doping, these non-idealities can be effectively circumvented. The benefit of counter doping turns out to be twofold. First, it leads to a sharpening of the tunneling junction and thus higher tunneling probabilities, and second, it contributes to merging the onsets of all tunneling paths. In accordance with these measures, our best devices are well comparable with leading publications in terms of average SS, achieving values of 87 mV/dec over four orders of I_d.

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