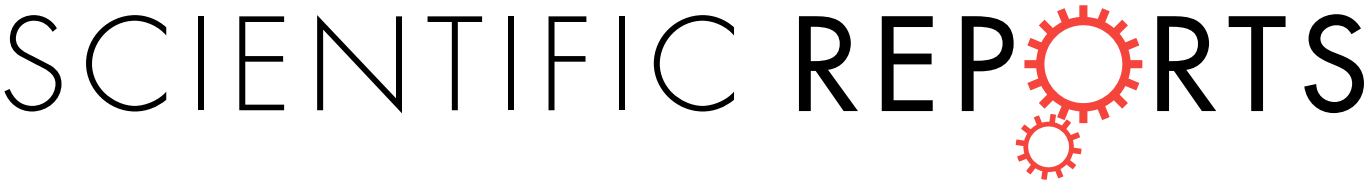

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A Steep-Slope Transistor Combining Phase-Change and Band-to-Band-Tunneling to Achieve a sub-Unity Body Factor

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Steep-slope transistors allow to scale down the supply voltage and the energy per computed bit of information as compared to conventional field-effect transistors (FETs), due to their sub-60 mV/decade subthreshold swing at room temperature. Currently pursued approaches to achieve such a subthermionic subthreshold swing consist in alternative carrier injection mechanisms, like quantum mechanical band-to-band tunneling (BTBT) in Tunnel FETs or abrupt phase-change in metal-insulator transition (MIT) devices. The strengths of the BTBT and MIT have been combined in a hybrid device architecture called phase-change tunnel FET (PC-TFET), in which the abrupt MIT in vanadium dioxide (VO_2) lowers the subthreshold swing of strained-silicon nanowire TFETs. In this work, we demonstrate that the principle underlying the low swing in the PC-TFET relates to a sub-unity body factor achieved by an internal differential gate voltage amplification. We study the effect of temperature on the switching ratio and the swing of the PC-TFET, reporting values as low as 4.0 mV/decade at 25 °C, 7.8 mV/decade at 45 °C. We discuss how the unique characteristics of the PC-TFET open new perspectives, beyond FETs and other steep-slope transistors, for low power electronics, analog circuits and neuromorphic computing.

Complementary metal-oxide semiconductor (CMOS) technology has been the core of micro/nanoelectronics industry for decades. In the Dennardian scaling era of MOS transistors, extraordinary improvements in terms of switching speed, device density, functionality and cost have been achieved by the additive application of several technology boosters such as substrate engineering, strain, multi-gate, high-k/metal gate stacks and high-mobility channel materials. However, the concept of a metal-oxide-semiconductor field-effect transistor (MOSFET) remained unchanged. Recently, aggressive scaling of the gate length dimensions down to few tens of nanometers is facing major challenges in terms of process variability, high leakage power, unscalable voltage supply and degraded current switching ratios[1].

The quest for a new beyond CMOS switch, addressing essentially leakage power and voltage scaling, encompasses new device concepts and materials, capable to complement MOSFETs and to be integrated on advanced CMOS platforms[2,3]. A fundamental target is the reduction of the subthreshold swing SS ($=dV_g/d\log I_d$), which in a conventional MOSFET is limited to 60 mV/decade at room temperature ($T = 300$ K) due to the thermionic carrier injection mechanism[4]. A steep-slope switch, with $SS < 60$ mV/decade, would allow to scale down the supply voltage and to enable future low-power computing[5]. Different steep-slope device principles have been proposed for this purpose, exploiting negative capacitance[6], movable electro-mechanical gates[7], impact ionization[8] and tunnel field-effect transistors (TFETs) based on quantum mechanical band-to-band tunnelling[9] (BTBT). TFET is currently considered the most promising steep-slope solid-state switch among alternative technologies, with experimentally demonstrated SS values of the order of 30 mV/decade at room temperature[10] mainly limited into a range of low currents. However, the tunnelling conduction mechanism limits the device performance in terms of 'on' current, I_{ON}, and the frequency of operation.

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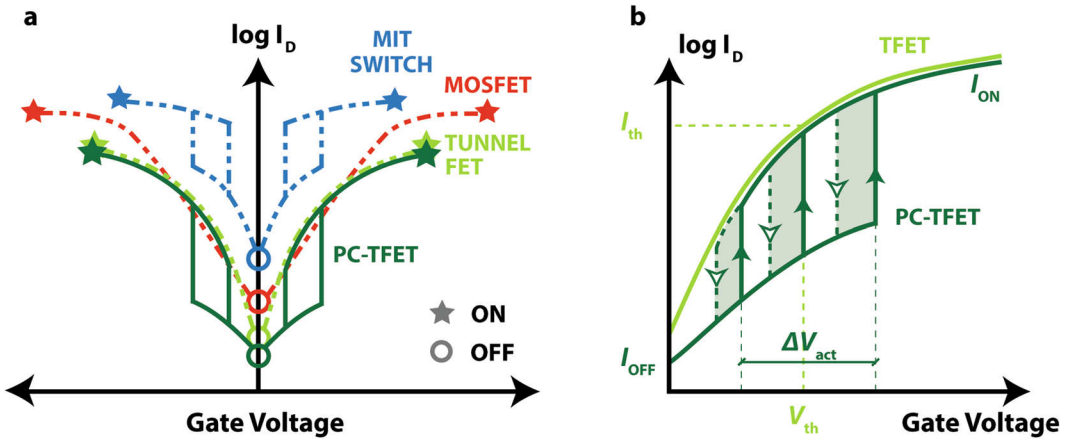

Figure 1. Comparison of three steep-slope switches: TFET, MIT and proposed PC-TFET. (**a**) Transfer characteristics for the PC-TFET and other steep-slope switches (TFET, MIT switch) achieving lower subthreshold swing than the MOSFET. (**b**) PC-TFET characteristics for different values of the MIT switch threshold voltage V_{act}, compared to the transfer characteristics of the TFET component with threshold voltage V_{th}. The hysteresis areas for three different values of V_{act} are highlighted by the shaded regions.

Recently, phase change materials such as correlated functional oxides have been proposed as a promising solution for beyond CMOS electronics. External excitations applied to phase change materials can induce a phase transition accompanied by a drastic change in their conduction properties[11–19]. One of the most studied phase change materials is vanadium dioxide (VO_2), which exhibits a metal-insulator transition (MIT) corresponding to a structural phase transition at a critical temperature T_{MIT} (340 K in bulk VO_2[20–22]). When VO_2 temperature is increased above T_{MIT}, the material transitions from a monoclinic phase to a tetragonal rutile structure, concomitant with the closing of an energy gap $E_g \approx 0.6$ eV in the 3d conduction band and a steep decrease in resistivity, up to 5 orders of magnitude in bulk VO_2. When the VO_2 temperature is decreased, the transition back to the monoclinic phase is observed for values below T_{MIT}, giving rise to a hysteresis with width depending on the quality of the material. VO_2 holds great potential for beyond CMOS electronics because the MIT can be induced by electrical excitations, enabling applications based on volatile resistive switching. The VO_2-based MIT switch in 2-terminal configuration shows interesting properties such as abrupt increase in current with applied voltage[23–31], fast switching time[32–34], high reliability[35,36], negative differential resistance[37–40], memristive switching[41,42] and low temperature dependence of transition dynamics[43,44]. However, the main drawback of the 2-terminal MIT switch is the relatively high leakage current I_{OFF} due to the small bandgap of VO_2 in the insulating state. While this problem can be mitigated by VO_2 doping[45], the most effective solution would be the development of 3-terminal switches in which a VO_2 channel undertakes a gate-driven phase change. The development of such a device was attempted first with standard MOSFET structures using VO_2 as the semiconducting material[46], but the observed conductance modulation by gate voltage was limited to a small percentage[47–50]. This encouraged the investigation of the use of electrolyte gating to obtain very high electric fields at the interface between VO_2 and an ionic liquid[51,52], inducing a higher channel conductance modulation due to the creation of oxygen vacancies[53–55] or protonation[56] but with a much slower switching time[57,58].

In order to overcome these issues, the phase-change tunnel FET (PC-TFET) has been proposed[59] as a hybrid design integration of a tunnel FET and a 2-terminal MIT switch, combining the strengths of the two devices and resulting in the first solid-state VO_2-based 3-terminal switch with simultaneous very low I_{OFF} current, high I_{ON}/I_{OFF} ratio and ultra-steep subthreshold swing (Fig. 1a), performance that cannot be individually achieved by a TFET or a MIT switch. The transfer characteristics of the PC-TFET are qualitatively compared to the ones of the TFET used as a component part in Fig. 1b. The main working principle of the PC-TFET is to feedback (by an appropriate gate or source connection) the ultra-abrupt switching in the MIT material into a TFET characteristic, used to block the current in the OFF state. The phase change in the MIT switch corresponds to the actuation voltage V_{act} (tunable by the design of the MIT component) allowing to switch from a high resistance state to a low resistance state, in which the current follows the transfer characteristics of the TFET. For ideal performance, the V_{act} of a 2-terminal MIT switch should be aligned with the TFET threshold voltage V_{th} (defined by the constant current method). Figure 1a and b also depict the resulting hysteretic behaviour of the PC-TFET, inherited from its MIT component. In this work, we discuss in detail the PC-TFET principle, its integration and the method of extraction of the body factor. Moreover, we further characterize the PC-TFET to discuss its temperature dependence and possible applications for analog circuits and neuromorphic computing.

Results

Hybrid PC-TFET: principle. The principle of the PC-TFET steep slope hybrid device is to simultaneously use two physical mechanisms to lower the subthreshold swing factors m and n, respectively the body factor

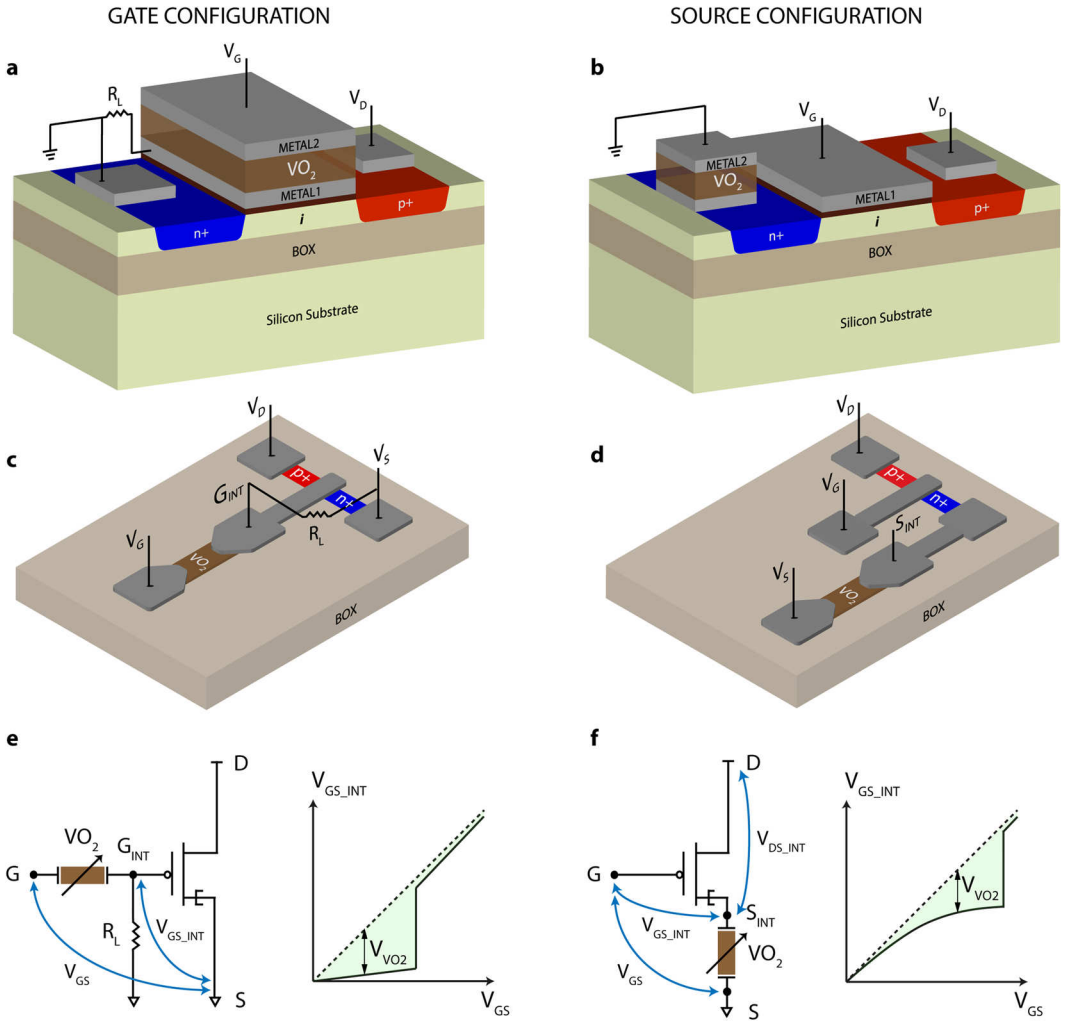

Figure 2. Phase change TFET integration in gate and source configuration. (**a**,**b**) 3D schematic diagrams of the PC-TFET integrating vertical VO_2 switches. (**c**,**d**) 3D schematic diagrams of the PC-TFET integrating planar VO_2 switches. (**e**,**f**) Equivalent circuits showing the internal TFET gate voltage V_{GS_INT} amplified by the MIT switch phase change, induced by the external gate voltage V_{GS}.

(mirroring the differential amplification of surface potential) and the carrier injection mechanism in the conduction channel (by band-to-band-tunnelling in a gated p-i-n junction):

$$SS = \frac{dV_{GS}}{d(\log_{10} I_{DS})} = \overbrace{\frac{dV_{GS}}{dV_{GS\_INT}}}^{m} \overbrace{\frac{dV_{GS\_INT}}{d\Psi_S}}^{} \overbrace{\frac{d\Psi_S}{d(\log_{10} I_{DS})}}^{n} \quad (1)$$

while the use of band-to-band tunnelling is intrinsically offering a straightforward solution to a potentially lower than 60 mV/decade n-factor, for lowering m, in contrast with any other previous reports, we do not use any negative capacitance principle but a simple circuit technique exploiting the abrupt switching in a 2-terminal MIT device connected in a voltage divider placed in the gate or in the source of a TFET. It is worth noting that reducing the body factor, m, of a TFET below 1, corresponds to a less explored approach (previously proposed by Ionescu[60]) to boost the abruptness of subthreshold characteristics of a TFET.

In the following, we study two PC-TFET designs, in which the MIT switch is connected to the gate (Fig. 2a,c,e, "gate configuration") or to the source (Fig. 2b,d,f, "source configuration") terminal of the TFET. In both cases the state of the MIT switch is controlled by the gate voltage V_{GS} and the phase change induces an internal differential amplification of the voltage drop V_{GS_INT} between the gate and source terminals of the TFET ($dV_{GS\_INT}/V_{GS} >> 1$) resulting in a steep increase in current I_{DS}.

Figure 2a shows the hybrid design integration of a 3-terminal TFET and a 2-terminal VO_2 switch to obtain the PC-TFET gate configuration. A VO_2 thin film is deposited and patterned on top of the gate terminal of the TFET, and a second metal layer is used to contact it and define the gate electrode of the PC-TFET. The same design can be adapted to the source configuration, shown in Fig. 2b, where the VO_2 switch is built on top of the source terminal of the TFET. An alternative design exploiting planar VO_2 switches is reported in Fig. 2c for the gate configuration and Fig. 2d for the source configuration.

Figure 2e presents the equivalent circuit and voltage distribution for the PC-TFET in gate configuration. A load resistance R_L is used to allow a current flow high enough to reach the power threshold of the VO_2 switch[43]. The value of R_L is selected in order to have $R_{VO2\_OFF} >> R_L >> R_{VO2\_ON}$, where R_{VO2_OFF} is the resistance of the MIT switch in the insulating state and R_{VO2_ON} is the resistance in the metallic state. As V_{GS} is ramped up in this configuration, the VO_2 material is initially in the highly resistive state, hence most of the voltage drops on the MIT switch ($V_{VO2} \approx V_{GS}$) and V_{GS_INT} stays low. Once the voltage is high enough to induce the metallic state in VO_2, V_{VO2} drops to a very low value and V_{GS_INT} experiences a steep transition to a value approaching V_{GS}.

Figure 2f presents the equivalent circuit and voltage distribution for the PC-TFET in source configuration. In this case the MIT switch is connected to the internal source terminal of the TFET and both the internal voltage drops V_{GS_INT} and V_{DS_INT} are changing while sweeping V_{GS} depending on V_{VO2}, such that $V_{GS} - V_{GS\_INT} = V_{DS} - V_{DS\_INT} = V_{VO2}$. For low values of V_{GS}, the VO_2 material is in its insulating state but the TFET channel resistance is much higher, effectively blocking the leakage through the MIT switch and keeping a low I_{OFF} current. Hence V_{GS_INT} follows V_{GS}. Increasing V_{GS}, the tunnelling current increases steadily until the TFET resistance becomes comparable with R_{VO2_OFF}. At this point the rise in V_{GS_INT} decreases and the MIT switch approaches its power threshold. Once VO_2 switches to its metallic state, V_{GS_INT} jumps abruptly to values near V_{GS}. It is clear that the source configuration is very suitable for the lowest power consumption and aggressive scaling as it does not require any additional load resistor (which is the TFET itself) and there is no power dissipation in such a load. However, as it will be shown later, the gate configuration is particularly interesting for its steeper characteristics.

The source configuration is similar to a previously reported solution based on III–V FinFET transistors and VO_2 switches[61]. However, that work exploited classical FinFETs with thermionic subthreshold swing and with very high leakage current to induce the phase change in VO_2, and as a consequence the I_{ON}/I_{OFF} ratio was limited to 4×10^2 and the region of abrupt switching was observed over less than a decade of current, whereas the PC-TFET achieves simultaneously low I_{OFF} and high I_{ON}/I_{OFF} ratio.

PC-TFET in gate configuration. The experimental demonstration of the PC-TFET has been achieved by fabricating and characterizing TFETs and VO_2 switches connected as explained in the previous section (Fig. 2e,f). During the experimental tests, the gate voltage is doubly swept and the voltage of the internal node is recorded with a high impedance voltmeter in the whole range of device operation. This allows us to carefully derive the internal amplification and the effect of the MIT transition point on the TFET characteristics by extracting its intrinsic gate and drain voltages.

The TFETs used in this work are based on a strained silicon gate-all-around (GAA) nanowire (NW) technology[62,63] with a NW cross section of $40 \times 5\,nm^2$ and a gate length of 350 nm. In order to enable a low power design of the PC-TFET, it is necessary to minimize the power threshold of the MIT switch. Based on an electrothermal model considering Joule heating as the triggering mechanism for the abrupt MIT transition[26,64], a convenient device geometry is achieved by reducing the VO_2 volume between the two electrodes of the MIT switch[65]. In this work such a low power actuation of a MIT switch is achieved by fabricating nanogap planar switches on a Si/SiO_2 substrate, limiting the VO_2 volume between the electrodes to values as low as $200 \times 100 \times 100\,nm^3$ (see Supplementary Fig. 1 for details on the process flow and Supplementary Fig. 2 for images of a final device).

Figure 3a shows the I_{DS}-V_{GS} characteristics of a TFET for different values of V_{DS}, ranging from −0.25 V to −1 V. The TFET biased at $V_{DS} = -0.75$ V exhibits very low $I_{OFF} = 69.1$ pA, very good $I_{ON}/I_{OFF} = 1.0 \times 10^7$ ratio, low gate leakage $I_G < 8$ nA up to $V_{GS} = -2$ V (see Supplementary Fig. 3), and a good average subthreshold slope over 4 decades of current: $SS_{TFET} = \partial V_{GS}/\partial \log_{10}(I_{DS}) = 112$ mV/decade. Figure 3b shows the I–V characteristics of a VO_2 switch at different temperatures, ranging from 25 °C to 55 °C. A 1 kΩ resistor is connected in series to the MIT switch in order to limit the current in the metallic state and prevent excessive overheating of the device. The switch design has been optimized for its use in the PC-TFET, presenting a low actuation voltage $V_{act} = -0.93$ V at room temperature, steep slope of the transition ($SS_{VO2} = 18.7$ mV/decade) and capability to drive high I_{ON} current. The transition presents limited hysteresis width (<0.2 V at room temperature) when the voltage is removed and the switch reverts to the OFF state. Increasing temperature, the actuation voltage decreases while the I_{ON} and the slope remain stable ($SS_{VO2} = 17.7$ mV/decade at 35 °C, 23 mV/decade at 45 °C) until reaching values near T_{MIT}, where the sharp transition is lost. This behaviour can be explained by an electrothermal actuation model based on Joule heating[66].

Figure 3c shows the I_{DS}-V_{GS} characteristics of the PC-TFET in gate configuration at different temperatures, biased at $V_{DS} = -0.75$ V and using a load resistance $R_L = 1$ kΩ. Different values of R_L allow to shift the V_{GS_act} level necessary to induce the phase transition (as described by additional measurements reported in Supplementary Fig. 4). Once VO_2 undergoes the phase transition to the low resistivity state, we observe a sharp rise in I_{DS} current up to values approaching the ones of the TFET at the same biasing conditions. The PC-TFET at room temperature has lower $I_{OFF} = 29.5$ pA (12.3 pA/μm normalized by the TFET width) than the TFET, comparable I_{ON}/I_{OFF} ratio (5.5×10^6) and a subthreshold slope vastly superior to the ones of state-of-the-art TFET devices reported to date: $SS_{PC\_TFET} = 4.0$ mV/decade at 25 °C, 7.8 mV/decade at 45 °C. This is due to the internal amplification of V_{GS_INT}, reported in Fig. 3d, in which we observe a very steep transition from low voltage levels to values near the TFET threshold voltage (e.g. from −0.14 V to −0.49 V at room temperature within a $V_{GS} = 10$ mV step). The output characteristics of a PC-TFET in gate configuration are reported in Supplementary Fig. 5. Due to the relatively significant power consumption in the resistive divider at the gate terminal, practically dictated by the VO_2 actuation (see Fig. 3b), the PC-TFET in gate configuration is not providing substantial advantages for low power electronics. However, the very abrupt transition in the PC-TFET in gate configuration can be exploited for analog circuit applications such as a voltage-controlled buffered oscillator (see Supplementary Fig. 6).

PC-TFET in source configuration. Figure 4a shows the I_{DS}-V_{GS} characteristics of the TFET component used to implement the PC-TFET in source configuration for different values of V_{DS}, ranging from −0.25 V to

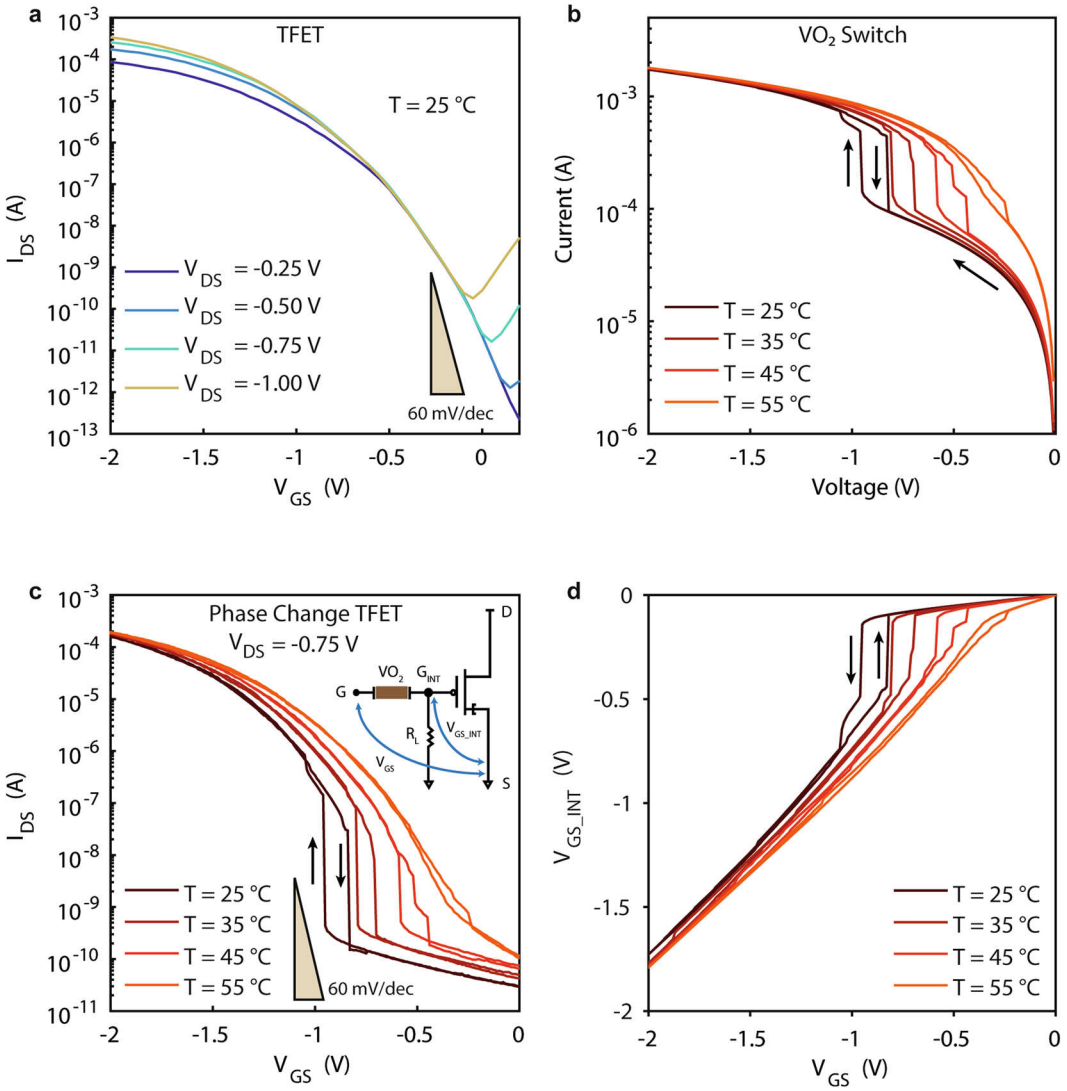

Figure 3. Experimental demonstration of Phase Change TFET in gate configuration. (**a**) I_{DS}-V_{GS} transfer characteristic of the TFET for different applied V_{DS}. (**b**) I-V characteristic of the VO_2 switch measured at different temperatures with a series resistance of 1 kΩ. (**c**) I_{DS}-V_{GS} obtained combining (a) and (b) in gate configuration with a load resistance of $R_L = 1$ kΩ between the gate terminal and ground and an applied $V_{DS} = -0.75$ V. (**d**) Internal gate voltage V_{GS_INT} biasing the TFET in function of the external applied V_{GS}.

−1.5 V. The TFET measured at $T = 55$ °C and biased at $V_{DS} = -0.75$ V presents an average subthreshold swing $SS_{TFET} \approx 180$ mV/dec and a current ratio of 6.3×10^5 in a 2 V gate voltage window. Figure 4b shows the I-V characteristics of the VO_2 switch used in this case, with a series resistance of 3 kΩ. The actuation voltage decreases with temperature from −2.61 V at 25 °C to −1.19 V at 55 °C, while the steep slope is preserved up to values approaching T_{MIT} ($SS_{VO2} = 11.9$ mV/decade at $T = 25$ °C, 22.3 mV/decade at $T = 55$ °C).

Figure 4c depicts the I_{DS}-V_{GS} characteristics of the PC-TFET in source configuration. The V_{DS} has been increased to −2 V and the measurement is reported at 55 °C in order to reach the current levels necessary to induce the transition at $V_{GS} < 4$ V. The PC-TFET in source configuration combines the strengths of the two component devices, presenting a high I_{ON}/I_{OFF} ratio, a low I_{OFF} current and a low I_G gate leakage comparable to the TFET, while the subthreshold slope is similar to the one of the VO_2 switch ($SS_{PC\_TFET} = 20.6$ mV/dec). The subthermionic (<60 mV/dec) value for the slope at the phase change transition is due to a similar internal gate voltage amplification mechanism exploited for the gate configuration, with the difference that both the intrinsic gate and drain voltages are simultaneously switching abruptly: $V_{GS\_INT} = V_{GS} - R_{VO2} \cdot I_D$ and $V_{DS\_INT} = V_{DS} - R_{VO2} \cdot I_D$ (see Fig. 4d). However, as shown in Fig. 4d, in this case the amplification occurs for values of V_{GS_INT} above the TFET threshold (from −2.54 V to −3.31 V within a $V_{GS} = 10$ mV step), resulting in a less abrupt increase in I_{DS}. Moreover, our experiments show that the V_{DS_INT} change while sweeping V_{GS} is quantitatively less important than the effect of dV_{GS_INT}/dV_G amplification (see Supplementary Fig. 7).

The output characteristics of a hybrid PC-TFET in source configuration are reported in Fig. 5a, pointing out a very particular behaviour that could be further exploited in energy efficient logic or neuromorphic circuits.

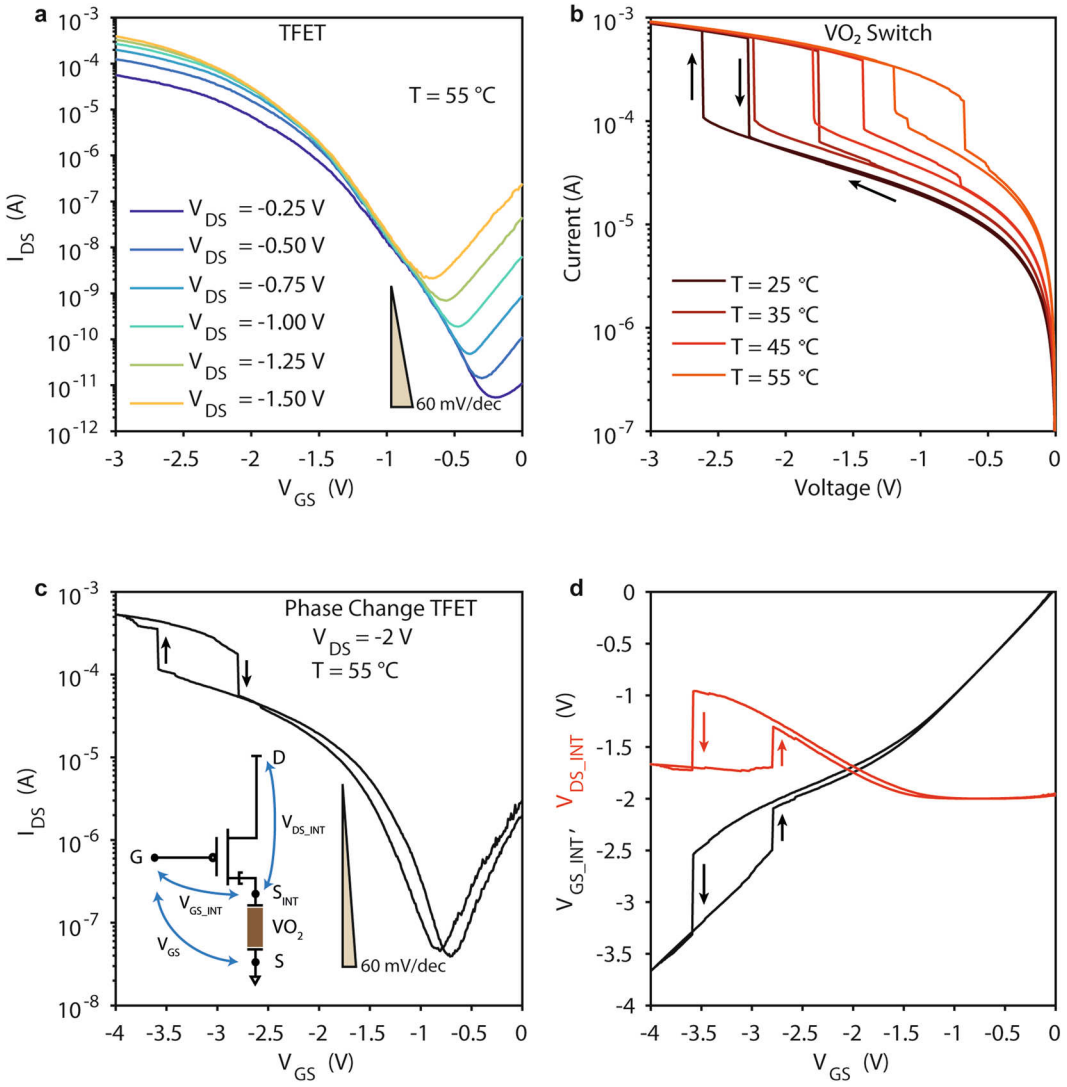

Figure 4. Experimental demonstration of Phase Change TFET in source configuration. (**a**) I_{DS}-V_{GS} transfer characteristic of the TFET component for different applied V_{DS} measured at $T = 55$ °C. (**b**) I-V characteristic of the VO_2 switch measured at different temperatures with a series resistance of 3 kΩ. (**c**) I_{DS}-V_{GS} of PC-TFET obtained introducing the VO_2 switch in the TFET source terminal; measurements performed at $T = 55$ °C with an applied external $V_{DS} = -2$ V. (**d**) Intrinsic TFET gate voltage V_{GS_INT} and drain voltage V_{DS_INT} versus applied V_{GS}.

The VO_2 phase change induces a very abrupt switching in the PC-TFET output characteristics, corresponding, in absolute values, to a *higher* V_{GS_INT} and a *higher* V_{DS_INT}, as pointed out by Fig. 5b. The output characteristics of PC-TFET inherit from the MIT transition points a hysteretic behaviour, which has a direct consequence on the effective drive current (because of the different trajectory on the output characteristics in logical switching) if such device is used for building CMOS inverters. Moreover, the low leakage current in the PC-TFET, negligible with respect to the drain current over the whole domain of operation (see Supplementary Fig. 8), makes it promising for energy efficient implementations of neuromorphic circuits based on relaxation oscillators[67,68].

Body factor reduction in PC-TFET. The deep subthermionic switching in the PC-TFET can be explained by its sub-unity body factor due to the internal gate voltage amplification. The relation between the subthreshold slope and the body factor has been captured in equation (1), with the transistor body factor $m = dV_{GS}/d\Psi_S$ expressed as the inverse of the differential amplification of the surface potential with respect to the extrinsic gate voltage. In a conventional MOSFETs the body factor is dependent on a capacitance ratio between the gate oxide capacitance, C_{ox}, and the depletion capacitance, C_d, $m = 1 + C_d/C_{ox}$, resulting in a lower bound, $m \geq 1$. Here, we show that this limit is overcome in the PC-TFET because the body factor m can be expressed in function of V_{GS_INT} and becomes:

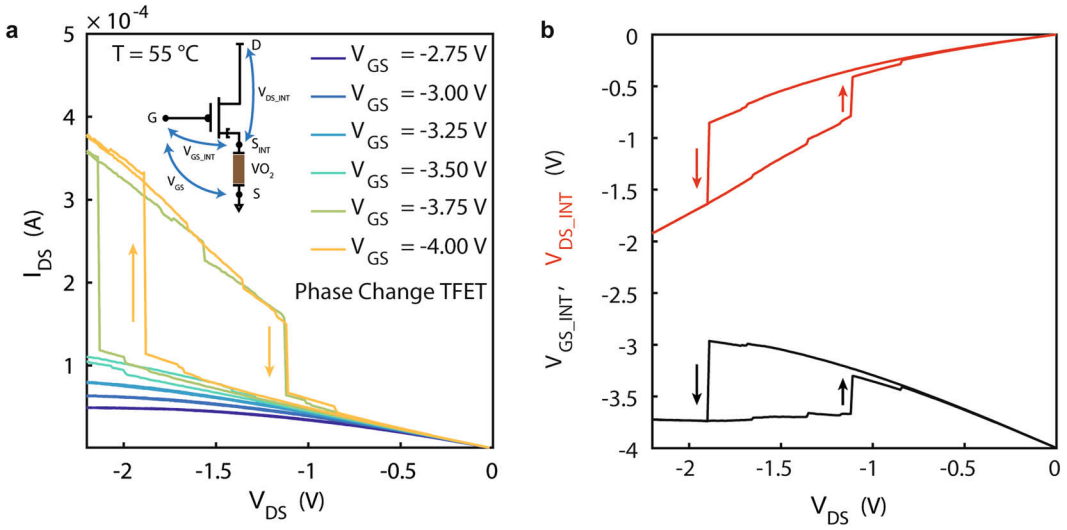

Figure 5. Output characteristics and drain voltage switching of Phase Change TFET in source configuration. (**a**) Output characteristics of PC-TFET in source configuration for different applied V_{GS} (ranging from −2.75 V to −4 V) measured at $T = 55$ °C. (**b**) Intrinsic TFET gate voltage V_{GS_INT} and drain voltage V_{DS_INT} versus applied V_{DS}.

$$m = \left[\frac{d\Psi_S}{dV_{GS\_INT}}\frac{dV_{GS\_INT}}{dV_{GS}}\right]^{-1} = \left(1 + \frac{C_d}{C_{ox}}\right)\frac{dV_{GS}}{dV_{GS\_INT}} \quad (2)$$

hence, when maximizing the internal gain of the PC-TFET, $G = dV_{GS\_INT}/dV_{GS} >> 1$, and given that in fully depleted body devices $(1 + C_d/C_{ox}) \sim 1$, it follows that $m << 1$, showing that the body factor is a booster of the TFET subthreshold swing. We extract the body factor from our experimental results, starting from calculating the surface potential as a function of V_{GS} as shown in Fig. 6a, for the gate configuration, and Fig. 6b, for the source configuration. On the same figures we include the measured internal gain, G, whose experimental values are used to extract m, using equation (2). The values of $\Psi_S(V_{GS})$ are obtained by means of technology computer-aided design (TCAD) simulations of NW-TFETs identical to the fabricated structures, biased with the experimental values of V_{GS_INT} and V_{DS} for the gate configuration (Fig. 3d), V_{GS_INT} and V_{DS_INT} for the source configuration (Fig. 4d). We observe a steep change in Ψ_S (resulting in a very low m) in correspondence of the V_{GS} values for which a high internal gain amplification is recorded, highlighting the key role of the internal gain in the steep switching characteristics of the PC-TFET.

Figure 6c,d show m in function of the measured I_{DS}, respectively for the gate and source configurations. In both cases the experimentally extracted body factor shows a less than 0.1 value in the transition region. The PC-TFET in gate configuration presents a value of m of ~0.05 (<<1) for more than two decades of current, from 0.43 nA to 142.3 nA in the OFF to ON transition and from 27.5 nA to 0.15 nA in the OFF to ON transition. The PC-TFET in source configuration shows similar values of m (0.025 in the OFF to ON transition, 0.5 in the ON to OFF). It is worth noting that the low-m region is extended for more decades of current in the gate configuration due to the better alignment of the internal gain peaks and the TFET threshold region.

Discussion

We reported the PC-TFET as a novel hybrid steep-slope electronic switch, combining two steep switching mechanisms in a single device, and its detailed characterization in a broad range of temperatures up to values approaching the transition temperature of VO_2. The unique combination of BTBT in TFET and MIT in VO_2 leads to excellent figures of merit for digital electronics such as an I_{on}/I_{off} ratio better than 5.5×10^6 and a subthreshold swing lower than 10 mV/dec over 3 decades of currents. We observe low dependence on temperature of the swing of the PC-TFET in gate configuration, ranging from 4.0 mV/dec at room temperature to 7.8 mV/dec at 45 °C. Moreover, we have demonstrated that the underlying mechanism for the abrupt switching behaviour is the internal gate voltage amplification, leading to a sub-unity equivalent body factor. Such lower-than-1 body factor to achieve subthermionic switching is a much more general design criterion than the previous principle of negative capacitance, serving as a performance booster for both TFETs and MOSFETs. The PC-TFET represents an important step forward for beyond CMOS electronics, exploiting for the first time the full potential of the VO_2 MIT in in an electrically gated 3-terminal architecture and opening new perspectives for low power electronics and neuromorphic computing.

Methods

Fabrication of experimental devices. VO_2 nanogap switches were fabricated on a silicon substrate with a 200 nm thick SiO_2 layer on top. The VO_2 layer was deposited by reactive magnetron sputtering at 600 °C of a pure

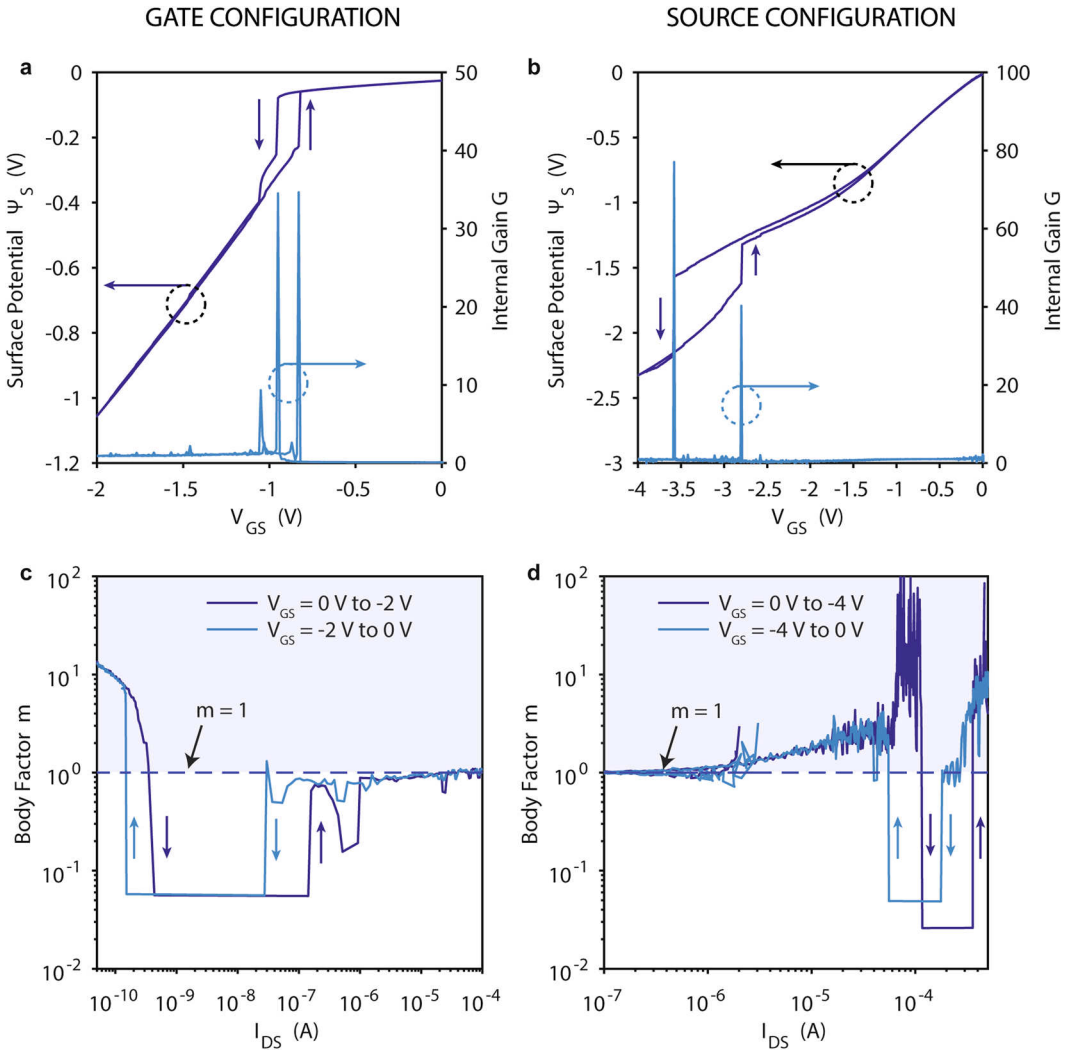

Figure 6. Surface potential and body factor in Phase Change TFET. (**a**,**b**) Dependence on V_{GS} of the surface potential, Ψ_S, and internal gain, $G = dV_{GS\_INT}/dV_{GS}$, for gate and source configurations. The reference level for the surface potential is taken at the source terminal. (**c**,**d**) Body factor as a function of I_{DS} for gate and source configurations; the dashed lines represent the $m \geq 1$ limit overcome thanks to the internal V_{GS_INT} amplification.

vanadium target, with detailed experimental conditions reported elsewhere[69]. Electrical contacts were defined by electron beam lithography on PMMA/MMA and lift-off of a 100 nm thick platinum film deposited by sputtering. The VO_2 areas around the switch are then removed by electron beam lithography on ZEP and ion beam etching. Strained silicon GAA TFETs have been fabricated on a silicon on insulator substrate using a process based on doping segregation from $NiSi_2$[70].

TCAD simulations for surface potential extraction. TCAD simulations were performed using Sentaurus TCAD Suite 2014.09. We simulated a strained silicon double gate TFET with channel thickness $T_{CH} = 5$ nm, oxide thickness $T_{OX} = 3$ nm with HfO_2 ($\varepsilon_r = 22$) gate metal workfunction of $\phi_m = 4.1$ eV corresponding to TiN. The source doping is $N_S = 1 \times 10^{20}$ cm^{-3} and the drain doping is $N_D = 1 \times 10^{19}$ cm^{-3} with abrupt junctions. Since the semiconductor layer is extremely thin, we have enlarged the bandgap by 70 meV, corresponding to the quantized state of the [100] ellipsoids. However, this increase is cancelled out by the strain on the nanowires, which results in an overall bandgap reduction of $\Delta E_g = -25$ meV. All the simulated surface potential values reported in this work are taken from 0.1 Å below the semiconductor-oxide interface. The surface potential plots in function of V_{GS} (Fig. 5a,b) are taken at the tunneling junction, while the full potential profile across the channel is reported in Supplementary Fig. 9.

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Author Contributions

W.A.V., E.A.C. and A.B. performed the experiments. W.A.V., E.A.C. and C.A. analyzed the data. T.R. designed and simulated the circuit applications. A.K. and A.S. deposited the VO_2 films. E.A.C. fabricated the VO_2 switches. G.V.L., Q.-T.Z. and S.M. designed and fabricated the TFETs. W.A.V. and A.M.I. wrote the manuscript. All authors discussed the results and commented on the manuscript. A.M.I. directed the overall research project.

Additional Information

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