



SQUBIC1: AN INTEGRATED CONTROL CHIP FOR SEMICONDUCTOR QUBITS

11.09.2018 | D. NIELINGER, V. CHRIST, C. DEGENHARDT, L. GECK, C. GREWING, A. KRUTH, D. LIEBAU, P. MURALIDHARAN, P. SCHUBERT, P. VLIEX, A. ZAMBANINI AND S. VAN WAASEN

OVERVIEW

- General Introduction
- Scalability
- Electrical control of qubits
- Prototype chip SQuBiC 1
 - Bias Voltage DAC
 - Qubit Gate DAC
- Next steps
- Discussion & Questions



GENERAL INTRODUCTION

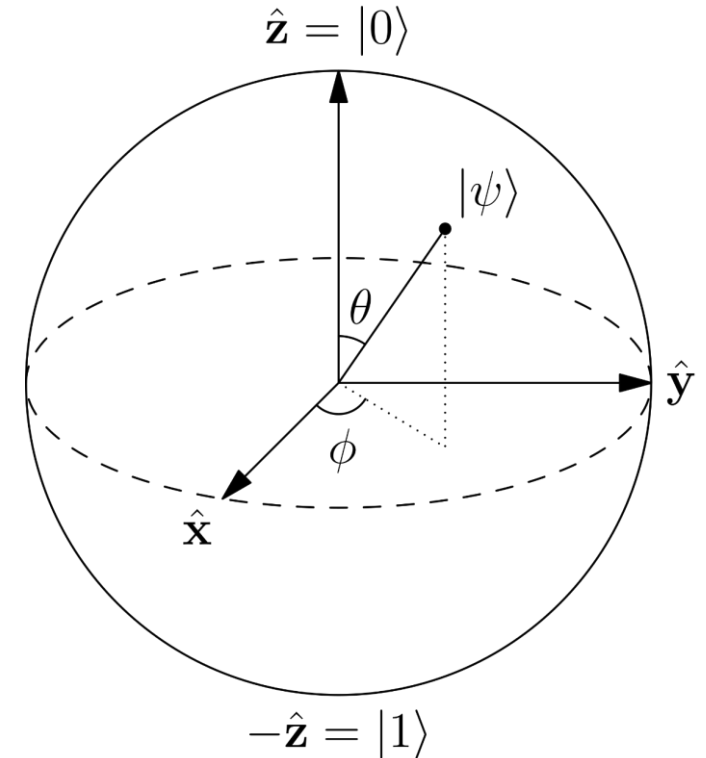
Quantum Computing

- Possible exponential speed up for certain tasks:
 - Shor's algorithm for factoring integers
 - Grover's algorithm for search in unordered databases
 - Quantum chemistry: Simulate new molecules and catalysts utilizing quantum mechanics
 - Quantum(-enhanced) machine learning
- Requirements for a quantum computer:
 - Large number (10^6 - 10^9) of physical Qubits operated in a cryogenic environment ($< 1\text{K}$)
 - Room temperature electronics to communicate with the Qubits
 - Scalable control and read-out electronics

GENERAL INTRODUCTION

What are Qubits?

- Two-state quantum-mechanical system with exactly 2 orthogonal distinct states
- Because of its wave nature the state of a Qubit is described by : $|\Psi\rangle = \alpha|0\rangle + \beta|1\rangle$
- α and β are complex coefficients constrained by normalization : $|\alpha|^2 + |\beta|^2 = 1$
- $|\Psi\rangle = \cos\left(\frac{\theta}{2}\right)|0\rangle + e^{i\phi}\sin\left(\frac{\theta}{2}\right)|1\rangle$
- N entangled Qubits represent 2^N classical bits

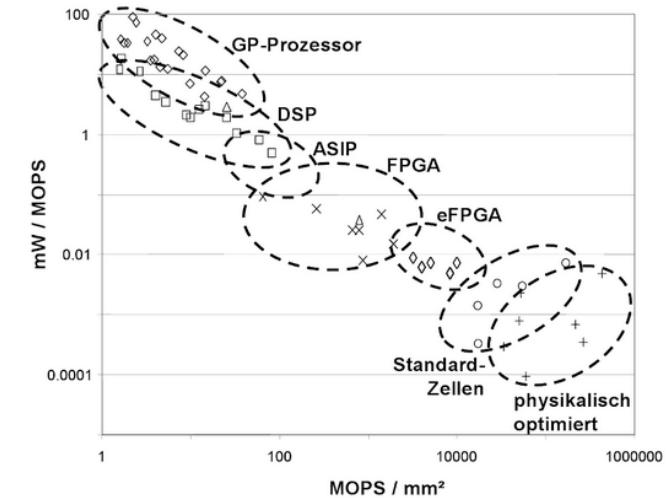
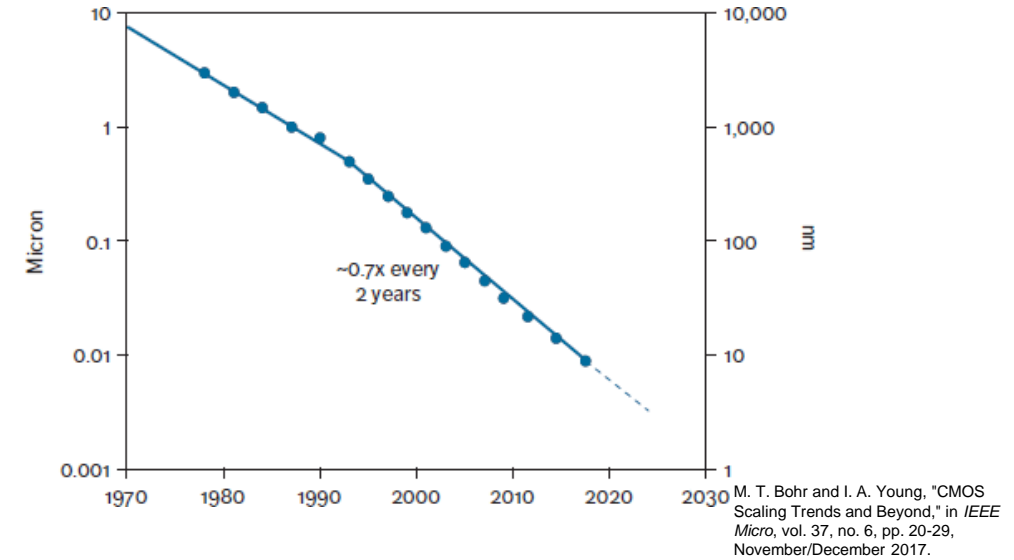


By Gloser.ca – Own work: Bloch sphere

SCALABILITY

Integrated CMOS

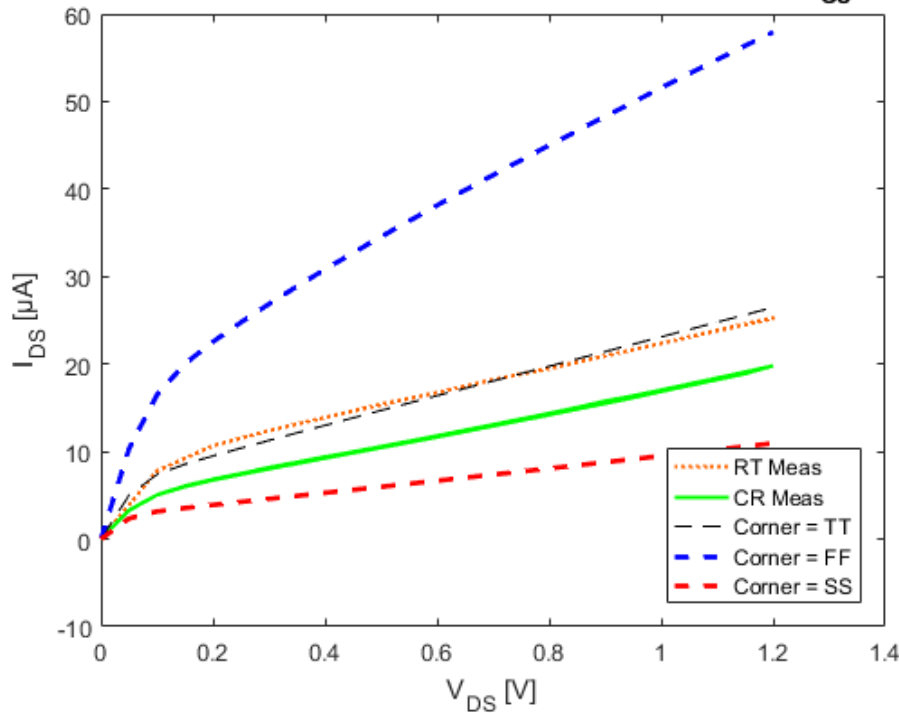
- Integrated CMOS scaling is unmatched over the last 50 years (Moore's law)
- The best approach for a scalable system is an application specific solution with reduced flexibility
- Using state of the art CMOS with prospect of using dedicated cryo-CMOS in the future



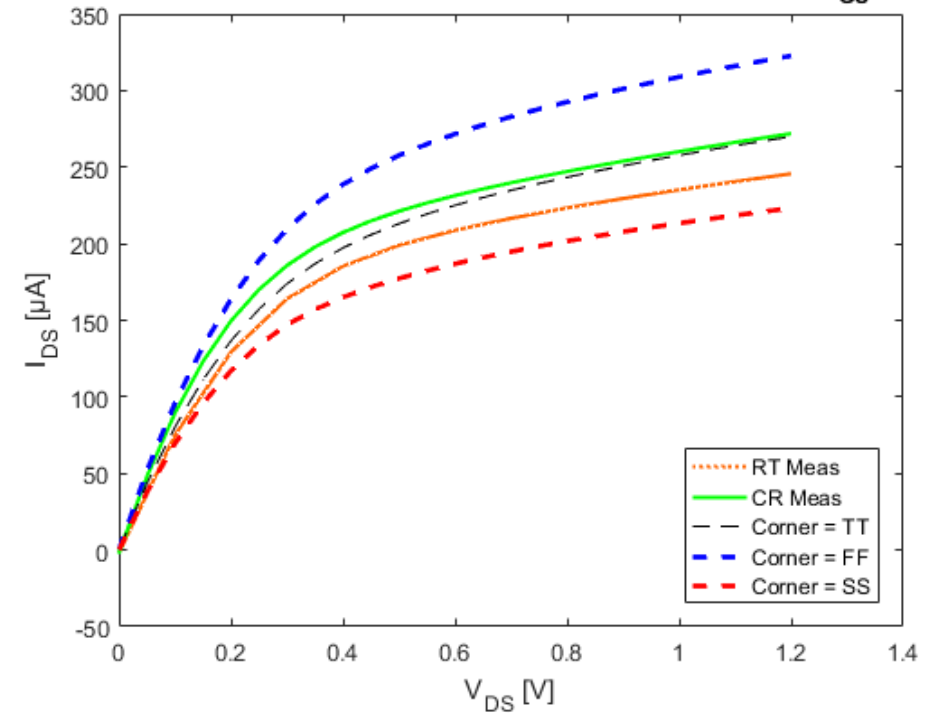
CRYOGENIC CMOS

Measurement Results for Transistors at Cryogenic Temperatures (CR) and Room Temperature (RT)

d048 measurement (RT and CR) against simulation @ 27°C $V_{GS} = 0.6\text{ V}$



d048 measurement (RT and CR) against simulation @ 27°C $V_{GS} = 1.2\text{ V}$

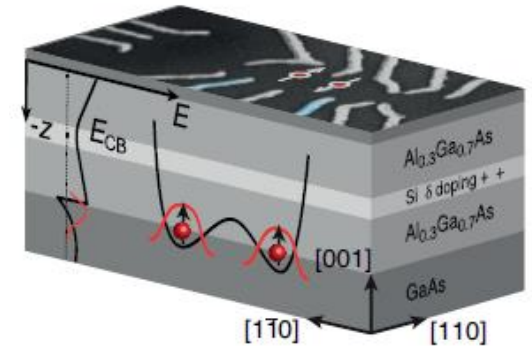


- Device: NMOS Core Bulk 1.2V V_{DD} 480nm/60nm ($V_{BS} = 0\text{ V}$)
- I²C Interface validated for liquid helium temperature

ELECTRICAL CONTROL OF QUBITS

Requirements GaAs Spin Qubits

- Up to 8 uncorrelated bias voltages per Qubit, forming potential wells
- 2 pulse electrodes for Qubit operation
- Key performance indicator: fidelity of Qubit Gate



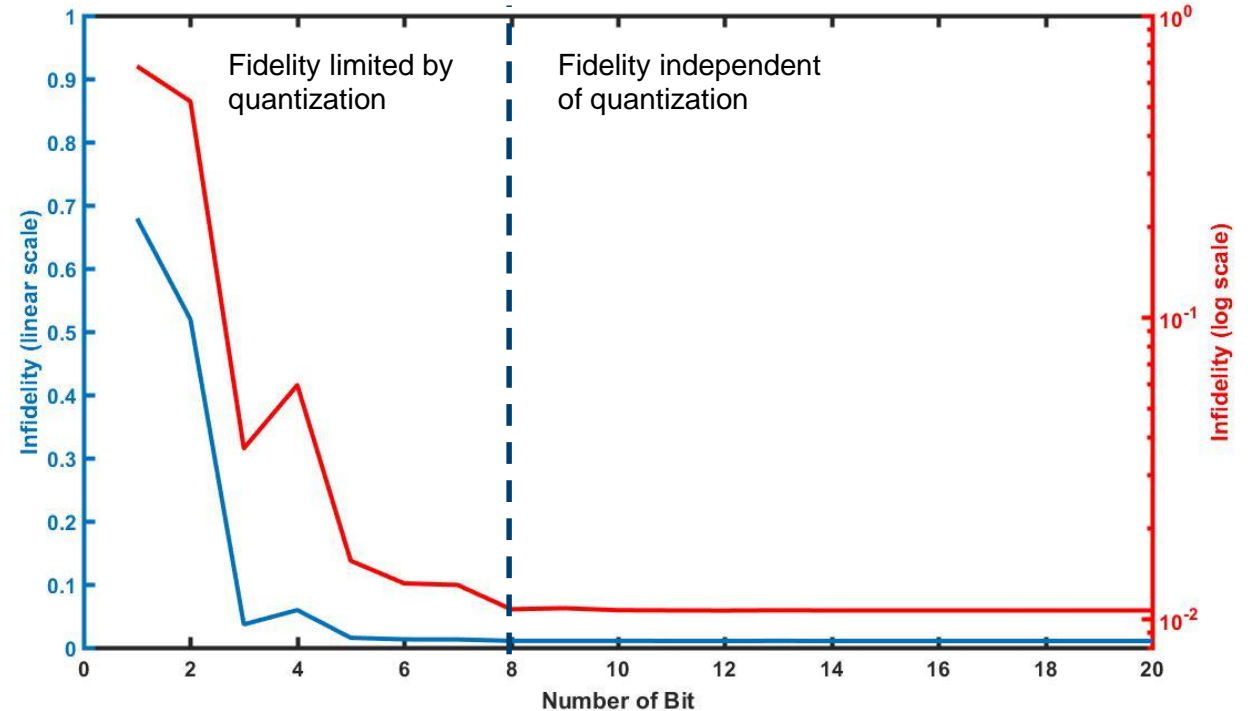
Tim Botzem, "Coherence and high fidelity control of two-electron spin qubits in GaAs quantum dots," PhD Thesis, p. 7, Figure 2.2.: Device Layout. Online: <http://publications.rwth-aachen.de/record/689507>, 14.08.2017

Characteristic	Specification
DC voltage range	-1 V to 0 V
DC voltage stability (1V range)	$\lesssim 20 \mu\text{V}$
DC Stepsize	250 μV ($\triangleq 12$ bit)
Pulse voltage range	± 4 mV
Pulse sampling rate	250 MHz
Pulse resolution (8mV range)	30 μV ($\triangleq 8$ bit)
Cooling power budget @ 100 mK	<1 mW

QUBIT GATE DAC (PULSE DAC)

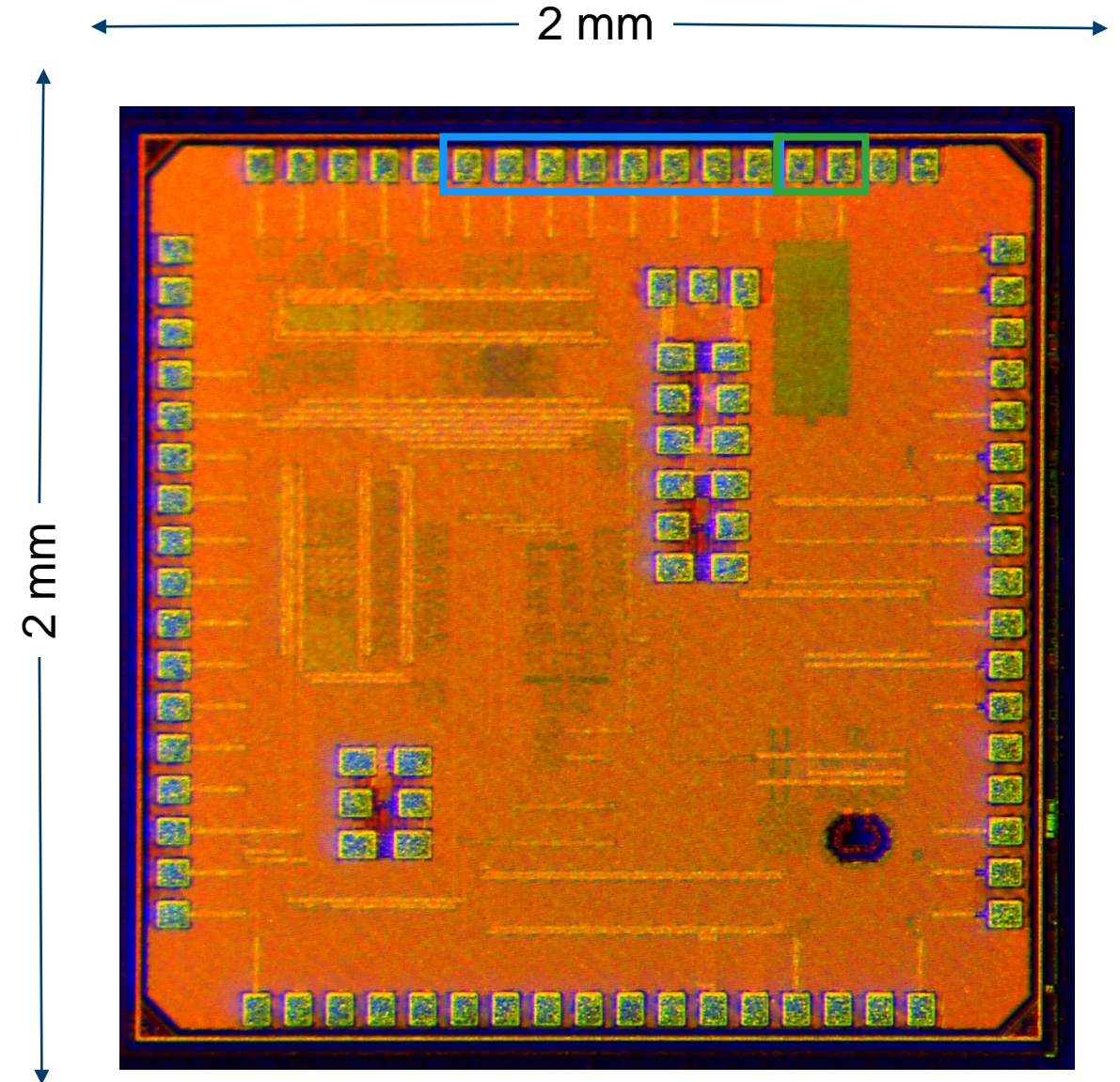
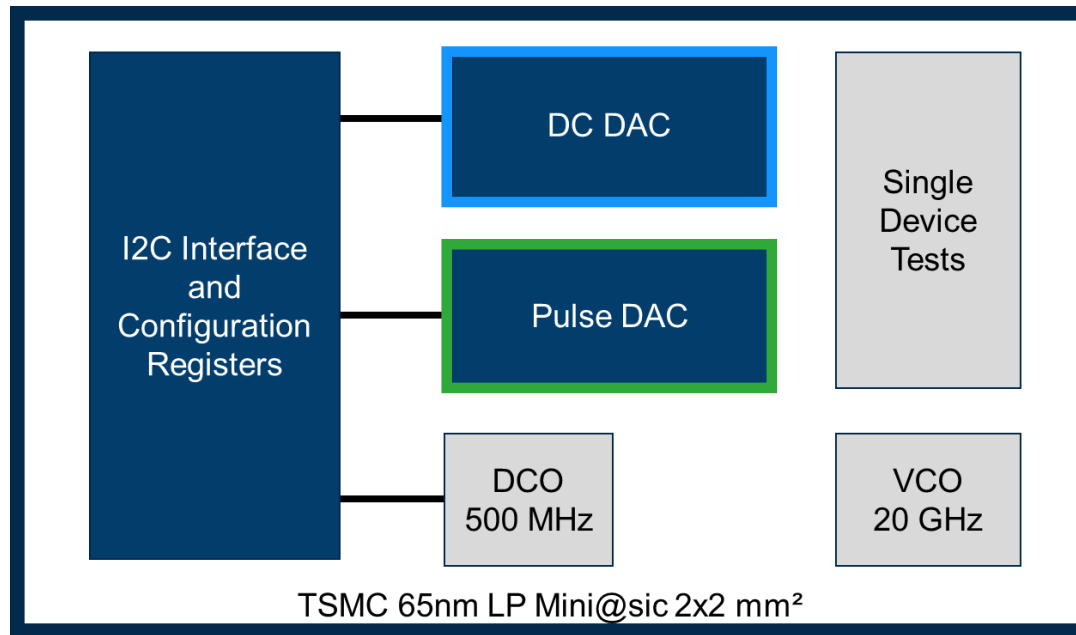
Quantization influence

- Pulse shapes were obtained by using a Matlab model
- After optimizing the pulse shape, quantization is applied and the fidelity is evaluated
- Beyond a certain number of bits, quantization is no longer the limiting factor for fidelity



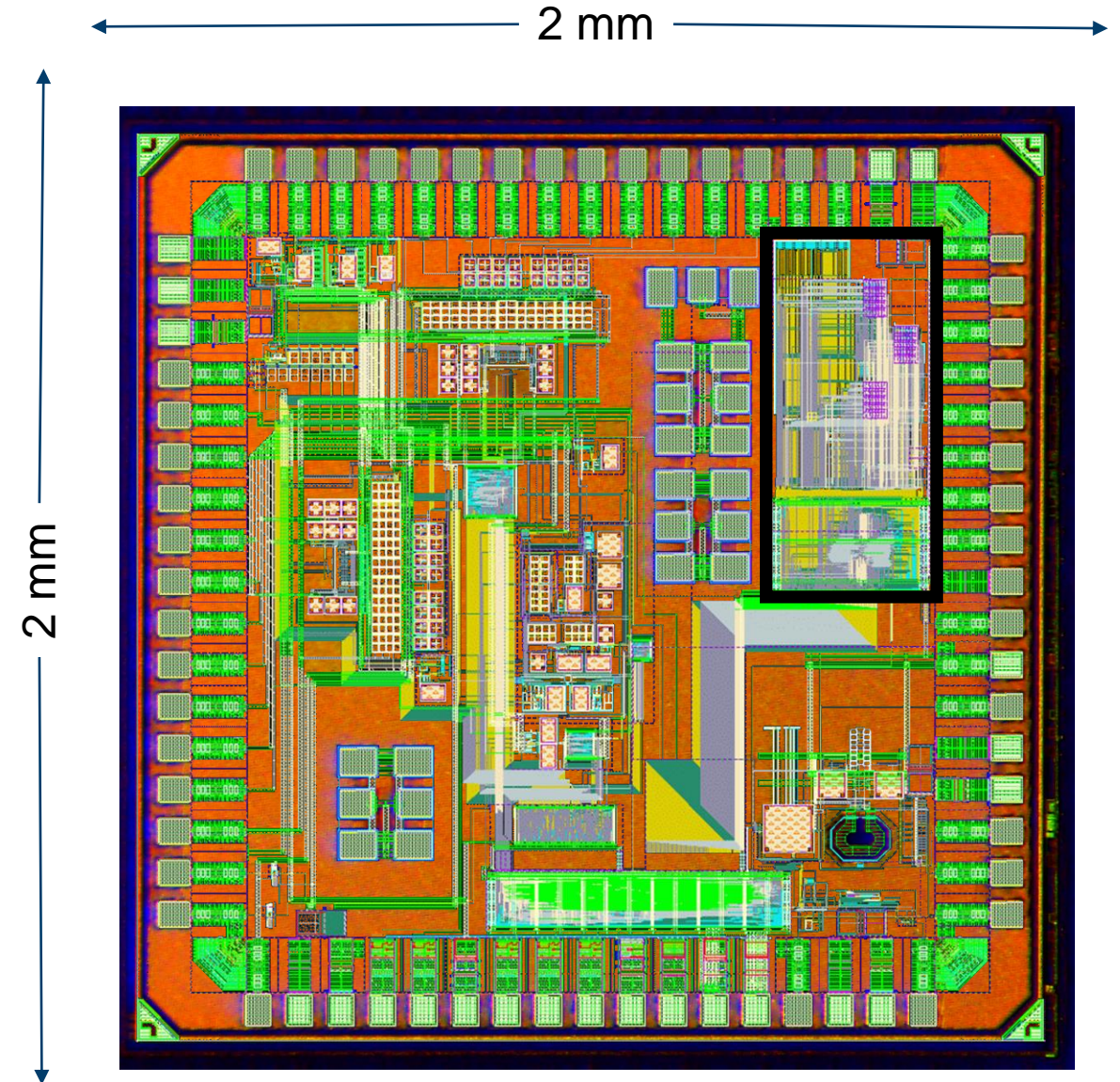
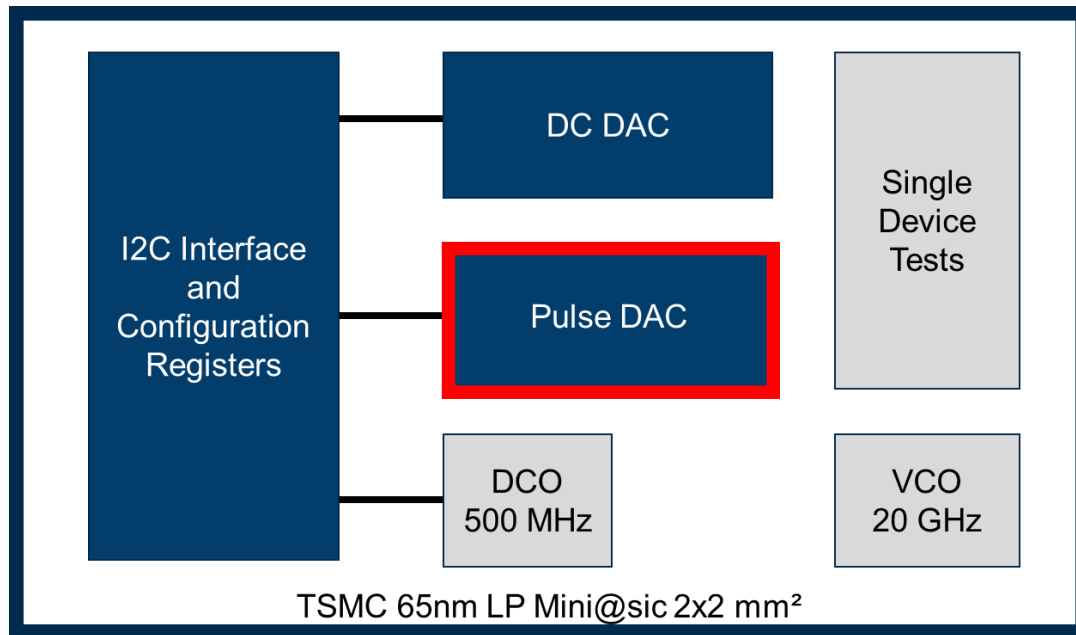
SQUBIC1

- Scalable Quantum Bit Control
- All infrastructure to operate a GaAs Qubit



QUBIT GATE DAC

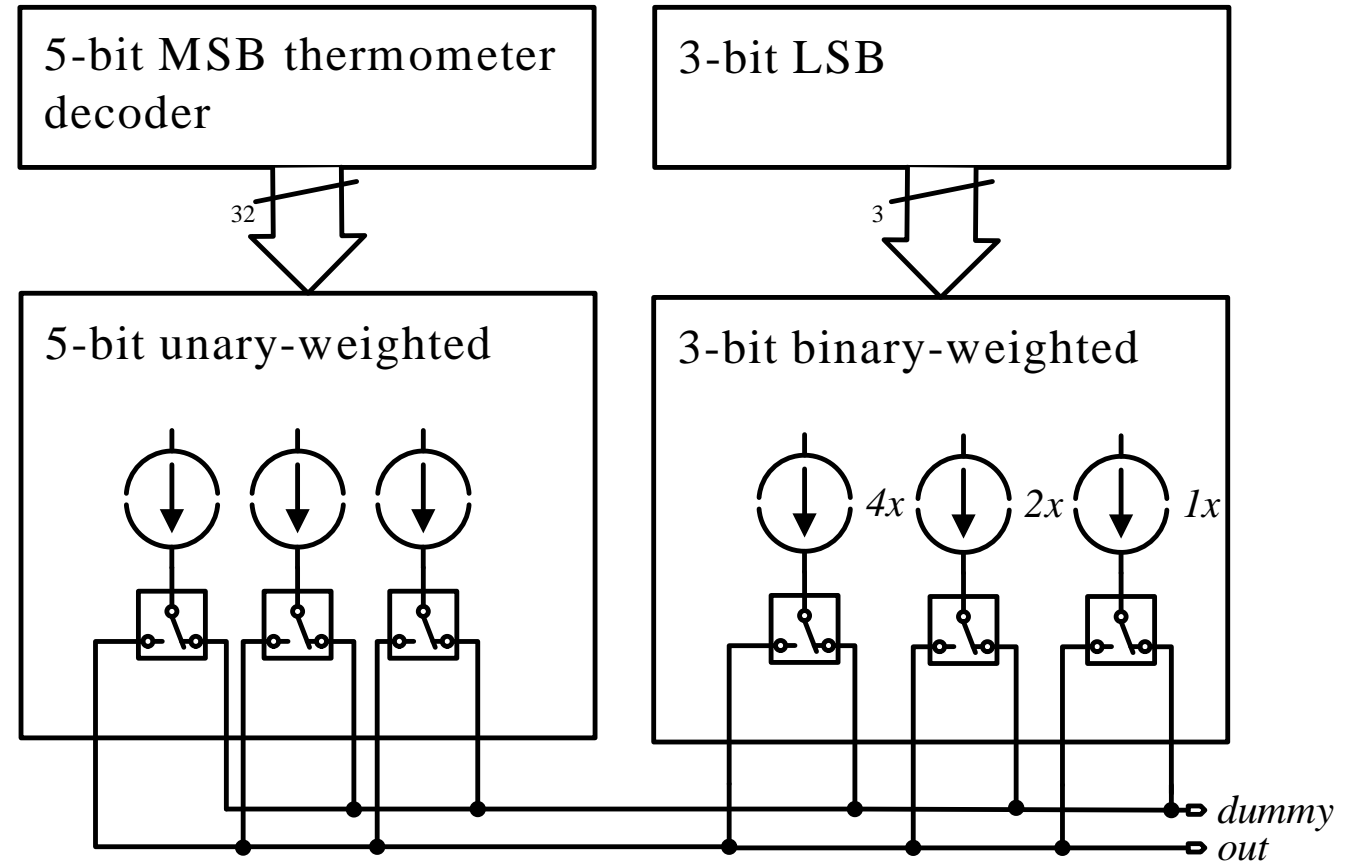
- Scalable Quantum Bit Control
- Qubit Gate DAC



QUBIT GATE DAC

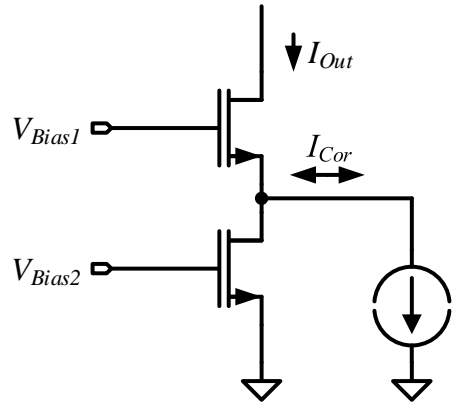
Current Steering

- Segmented current steering topology
- 5-bit unary weighted
- 3-bit binary weighted

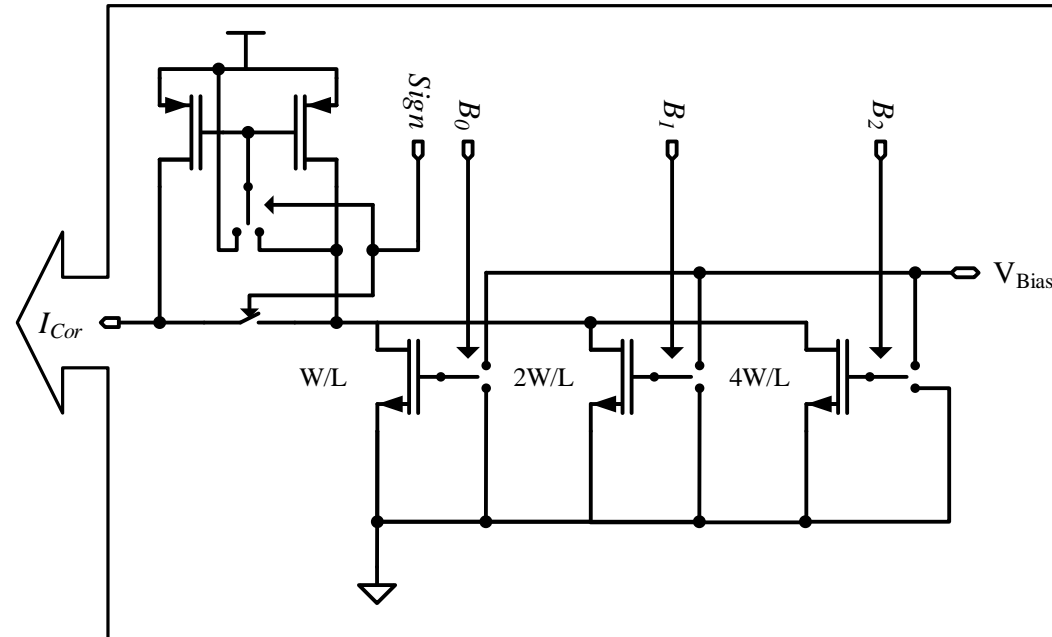


QUBIT GATE DAC

Current Calibration



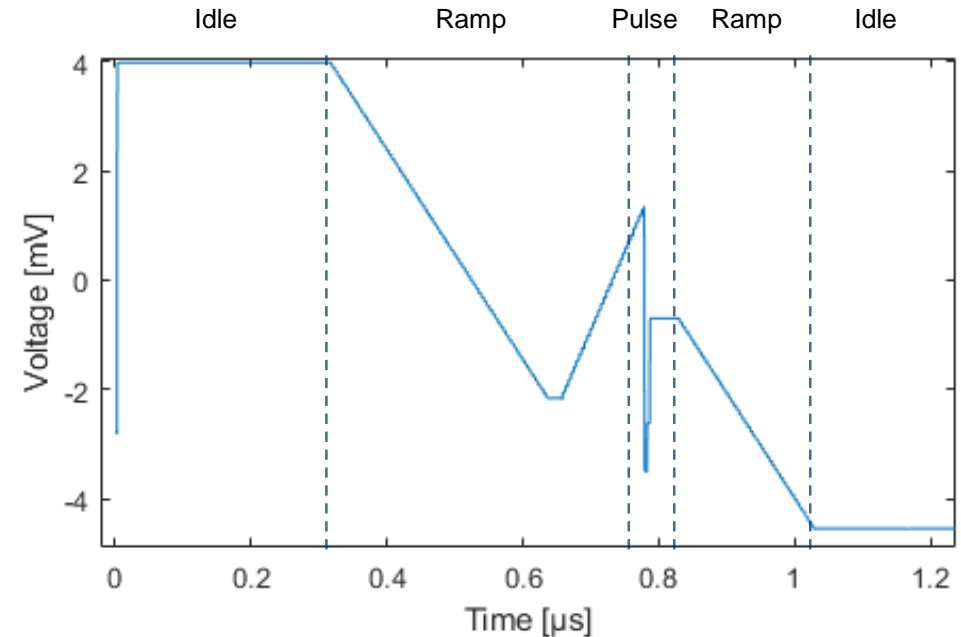
- Digital current injection calibration
- Small calibration DAC 3-Bit amplitude 1-Bit Sign
- Calibration for each current cell



QUBIT GATE DAC

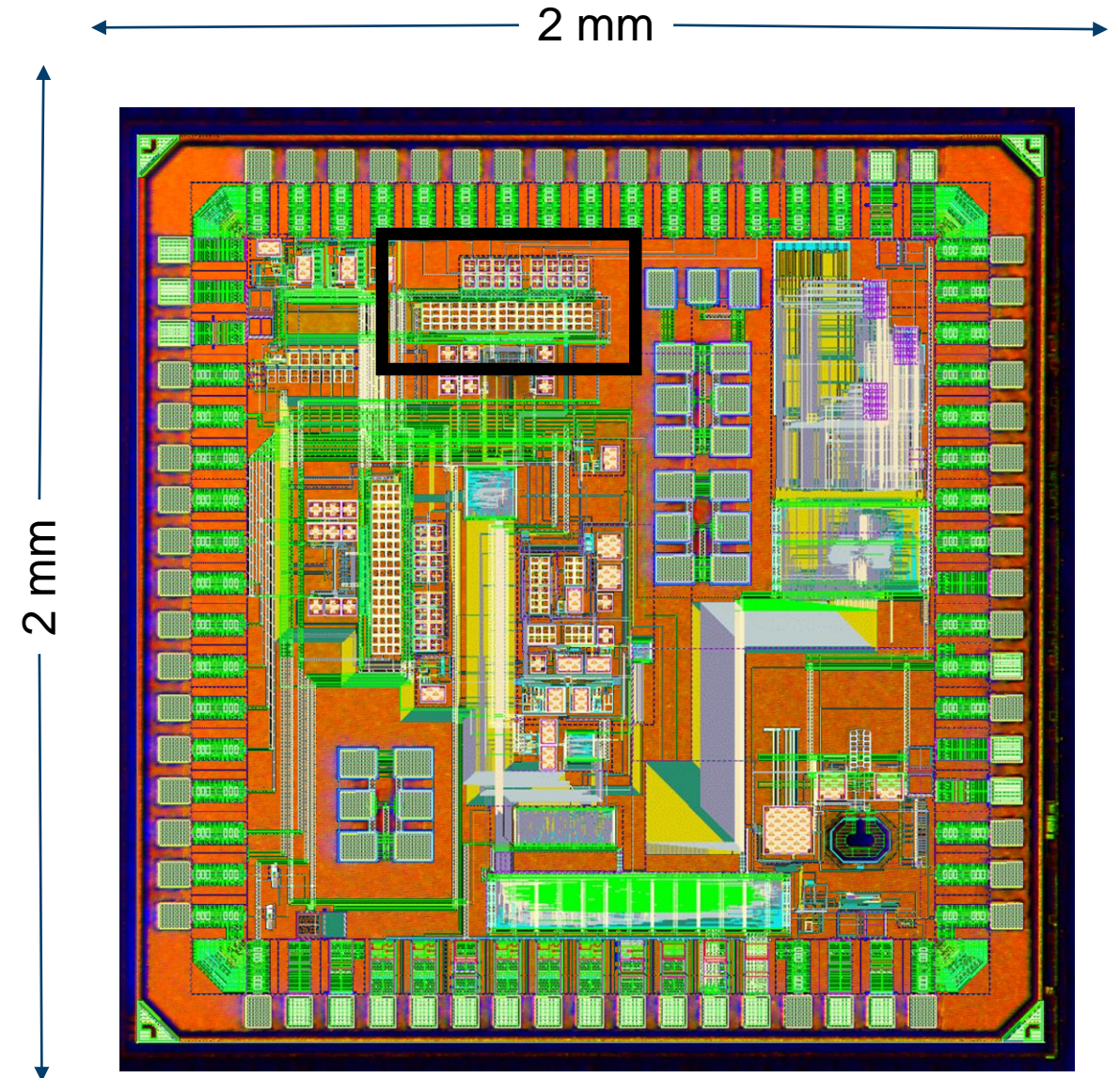
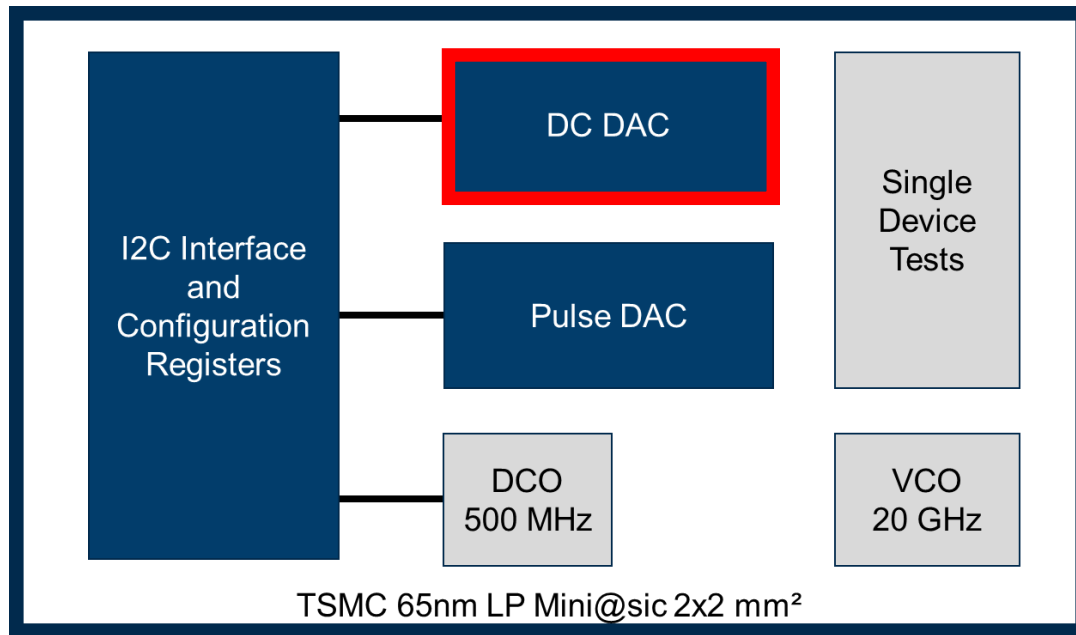
Pulse Encoding

- Problem: Huge difference in time constants for
 - Initializing the Qubit (Slow ramps, idle times)
 - Operating the Qubit (Fast pulses)
 - Read-out (Slow ramps, idle times)
- Solution: First order linear representation



BIAS VOLTAGE DAC

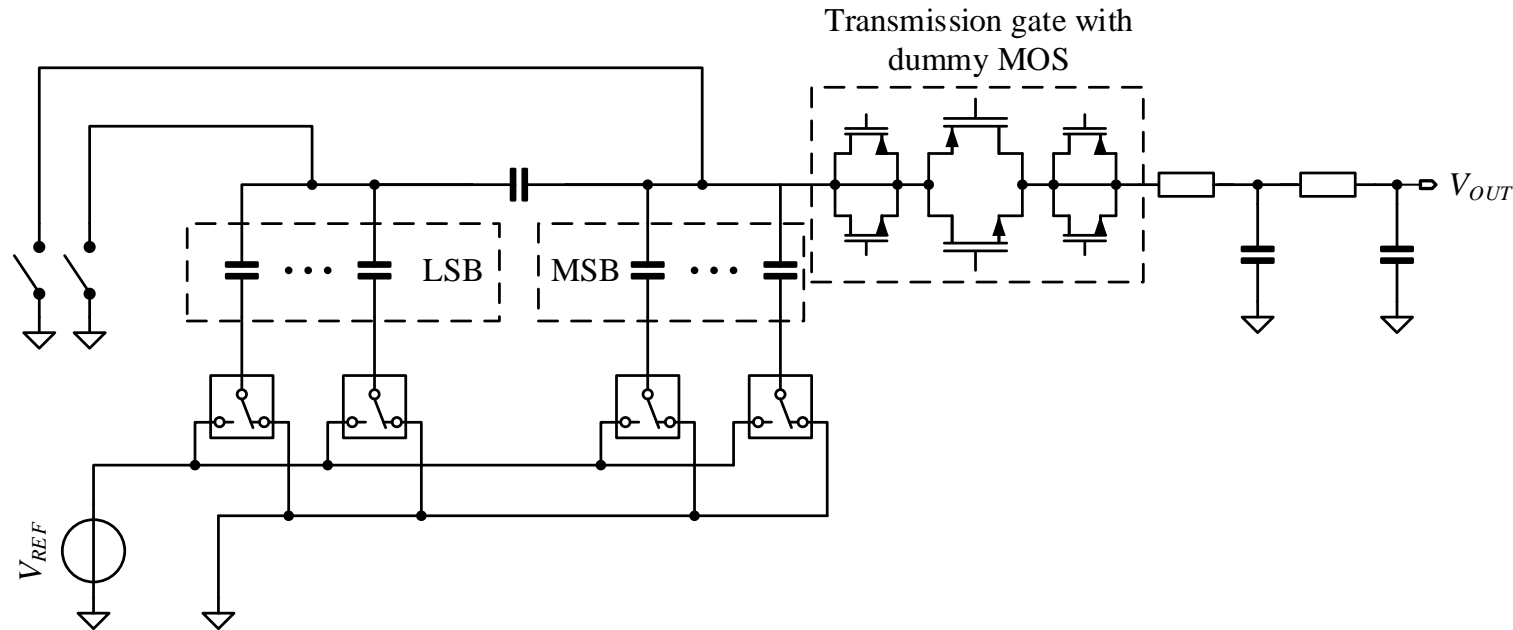
- Scalable Quantum Bit Control
- DC DAC



BIAS VOLTAGE DAC

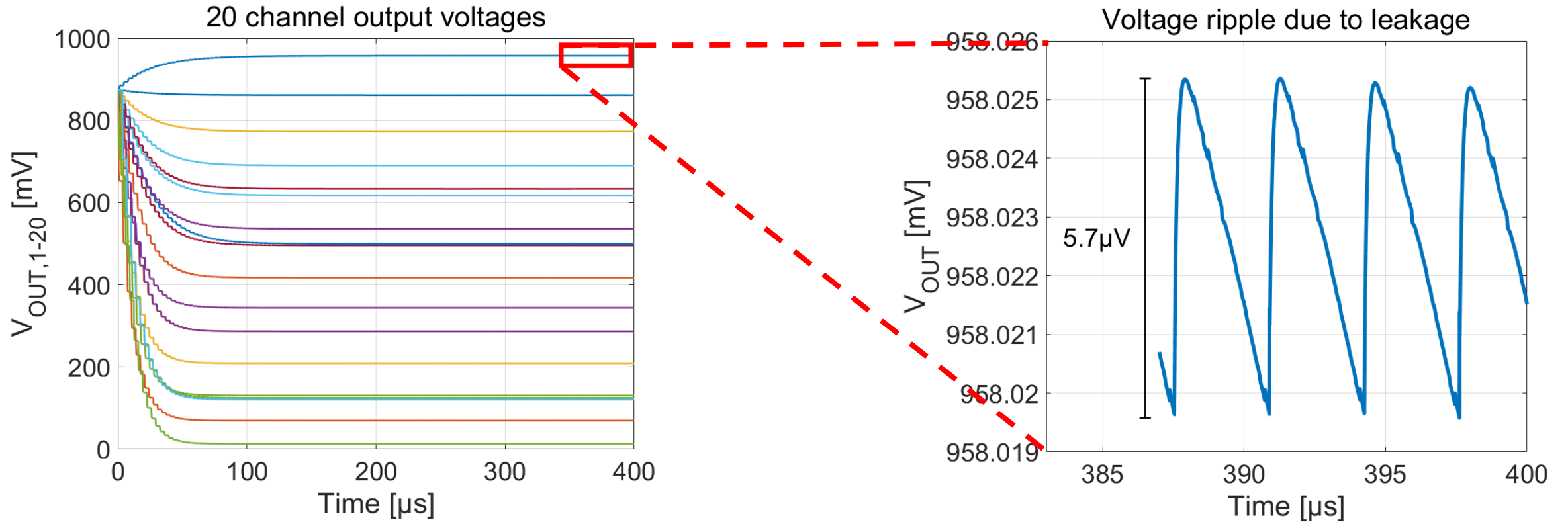
Charge-Redistribution Topology

- No static power dissipation
- Low thermal noise: $\bar{V}_N^2 = \frac{K_B \cdot T}{C}$
- Multiple output channel per DAC
- Loaded voltage divider:
 - Iterative charging to compensate voltage drop, no output buffer needed
- Coarse setting reference voltage, reduce power and bits in charge redistribution part



BIAS VOLTAGE DAC

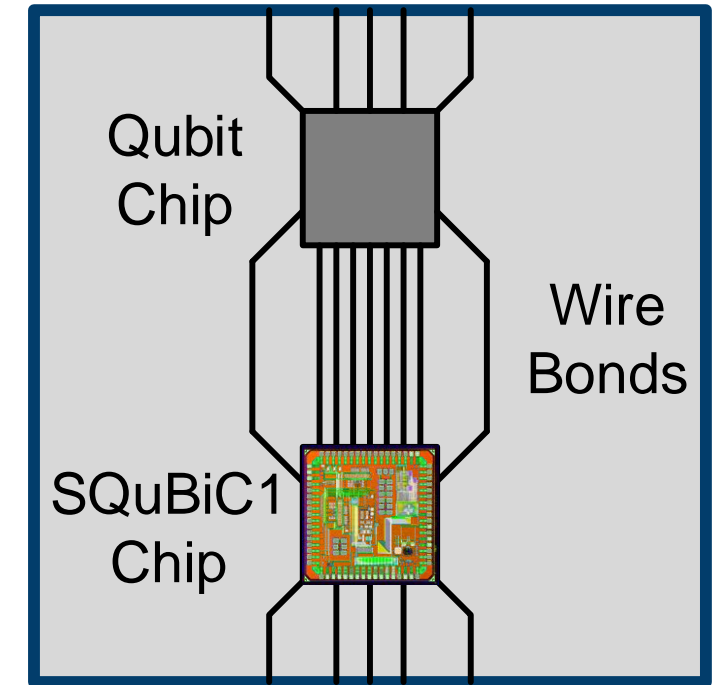
Refresh of Output Voltages



- Periodically refreshing of output voltages due to leakage (mainly into switch transistor bulk) \rightarrow expected to decrease due to bulk freeze-out!

NEXT STEPS

- Measure SQUBIC1...
...room temp. and cryogenic temp.
- Proof of principle
→ Qubit operation by cryogenic integrated chip
- Outlook:
→ Road to full scalability



QUESTIONS ?

