







Exploiting the switching dynamics of HfO_2 -based ReRAM devices for reliable analog memristive behavior

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ABSTRACT

The utilization of bipolar-type memristive devices for the realization of synaptic connectivity in neural networks strongly depends on the ability of the devices for analog conductance modulation under application of electrical stimuli in the form of identical voltage pulses. Typically, filamentary valence change mechanism (VCM)-type devices show an abrupt SET and a gradual RESET switching behavior. Thus, it is challenging to achieve an analog conductance modulation during SET and RESET. Here, we show that analog as well as binary conductance modulation can be achieved in a Pt/HfO₂/TiO_x/Ti VCM cell by varying the operation conditions. By analyzing the switching dynamics over many orders of magnitude and comparing to a fully dynamic switching model, the origin of the two different switching modes is revealed. SET and RESET transition show a two-step switching process: a fast conductance change succeeds a slow conductance change. While the time for the fast conductance change, the transition time, turns out to be state-independent for a specific voltage, the time for the slow conductance change, the delay time, is highly state-dependent. Analog switching can be achieved if the pulse time is a fraction of the transition time. If the pulse time is larger than the transition time, the switching becomes probabilistic and binary. Considering the effect of the device state on the delay time in addition, a procedure is proposed to find the ideal operation conditions for analog switching.

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I. INTRODUCTION

Nowadays, the speed limit of computing architectures is determined by the so-called von Neumann-bottleneck, which describes the data transfer rate between the processing unit and the data storage unit. For the processing of big amounts of unstructured data occurring in future artificial intelligence (AI) applications, significant interest arises in the research on Artificial Neural Network (ANN) architectures. Here, large numbers of synaptic weights have to be accessed and updated frequently.^{1,2} If these values are stored offline, the data transfer to the storage memory reduces the overall speed of data processing and contributes significantly to the energy consumption. Therefore, various technologies are emerging that are

capable of storing information close to the processing unit. Some concepts additionally allow computation in the memory (CIM) enabling further energy saving and speed enhancement. A highly promising candidate for the storage elements in these networks is the two-terminal nonvolatile redox-based Resistive Random Access Memory (ReRAM) device, which comprises ultrahigh scaling properties, fast read/write operation, and easy fabrication.^{3–5} The bipolar resistance switching operation in filamentary-type transition metal oxide based ReRAM devices follows the valence change mechanism (VCM). In this widely accepted model, a drift-/diffusion process of oxygen vacancies under the applied electrical field controls the memristive behavior of the cells based on insulating metal oxide layers, which are sandwiched between two metal electrodes.⁶ The

resulting change in the atomic configuration leads to a conductance change. The dynamics of the conductance change of a typical VCM device is asymmetric in nature: The transition from a Low Conductive State (LCS) to a High Conductive State (HCS), termed the SET process, is quite abrupt due to a positive feedback between the current increase and Joule heating.^{7,8} In contrast, the opposite process, termed RESET, is gradual in nature due to a negative thermal feedback and, eventually, the counteracting forces of drift and diffusion of oxygen vacancies approaching equilibrium concentration.⁹ Based on these properties, programming of multiple conductance states is achieved either by limiting the current during SET, e.g., by using a transistor in series to the ReRAM,¹⁰ or by changing the RESET voltage amplitude exploiting the gradual RESET transition.^{11,12}

When used as analog synapse, however, this asymmetric SET/RESET behavior is unfavorable as a gradual conductance change for both SET and RESET is desired. Different strategies have been proposed in the literature to achieve a gradual tuning. A layer stack modification to the typical VCM ReRAM device can change the switching properties.^{13,14} The introduction of an inherent conduction limiter (ICL) has a positive impact on reducing SET variability and has opened up the possibility of a gradual transition on either side, increasing single device and network performance.^{15–17}

Two operation possibilities arise from the inherent properties of the so-designed VCM devices: In the first approach, the intrinsic SET and RESET voltage variability inherent to HfO₂-based VCM devices¹⁸ and the subsequent switching probability at a given voltage amplitude can be exploited for realization of synapse functionality in ANNs.¹⁹ Application of a train of identical pulses yields an abrupt change between two well distinguishable binary-type LCSs and HCSs. The second approach is the optimization toward analog conductance change upon a series of identical pulses.²⁰ This enables efficient weight update routines in backpropagation ANNs.^{21,22} Despite these empirical approaches, an understanding of the physical mechanism controlling analog vs binary switching is still lacking.

II. EXPERIMENTAL

In this paper, the operation conditions leading to analog and binary conductance modulation of the VCM-type system Pt/HfO₂/TiO_x/Ti are investigated. Gradual and abrupt device operation is characterized by means of transient current analysis upon voltage stimuli varied over amplitude and several orders of magnitude in switching time. Using the acquired knowledge about the switching characteristics, pulses with constant voltage amplitude and duration are employed to modulate the device conductance in an analog manner. In the context of an ANN application, the analog SET process is termed potentiation, whereas the analog RESET is termed depression. If the programmed conductance states are stable, the terms Long Term Potentiation (LTP) and Long Term Depression (LTD) apply. The LTP/LTD cycles presented in this study follow a behavior, which is described well by a softbound synaptic model.²³ The experimental study is complemented by simulation using a fully dynamic physical compact model, called “JART VCM 1”. The model is used to identify the operation conditions for analog and binary stochastic switching.

In the VCM-type system Pt/HfO₂/TiO_x/Ti, the TiO_x layer acts as the aforementioned ICL. The reader is referred to Ref. 15 for a

detailed investigation on the impact of the introduction of an artificial interface titanium oxide layer on resistive switching in voltage sweep mode. HfO₂ itself is among the most researched VCM materials.^{24,25} Beside its Complementary Metal Oxide Semiconductor (CMOS) fabrication process compatibility, it has the benefit of reproducible switching at voltages acceptable in CMOS integrated circuits.²⁶ The 100 nm × 100 nm Pt/HfO₂/TiO_x/Ti/Pt devices under testing were structured by nanoimprint and electron beam lithography for the 30 nm thick Pt bottom (BE) and the 10 nm Ti and 20 nm Pt thick top electrodes (TE), respectively, combined with reactive ion beam etching. The 3 nm HfO₂ and 3 nm TiO_x layers were deposited by plasma enhanced and thermal atomic layer deposition (ALD), respectively. Metals were deposited using electron beam evaporation. Process details can be found in Ref. 27. For the electrical characterization, all signals were applied to the Pt BE of the device. The as-prepared devices require an initial electroforming step before stable resistive switching is observed. The forming process was carried out by a negative voltage sweep, using an Agilent B1500A semiconductor analyzer with an active compliance current of 50 μ A.

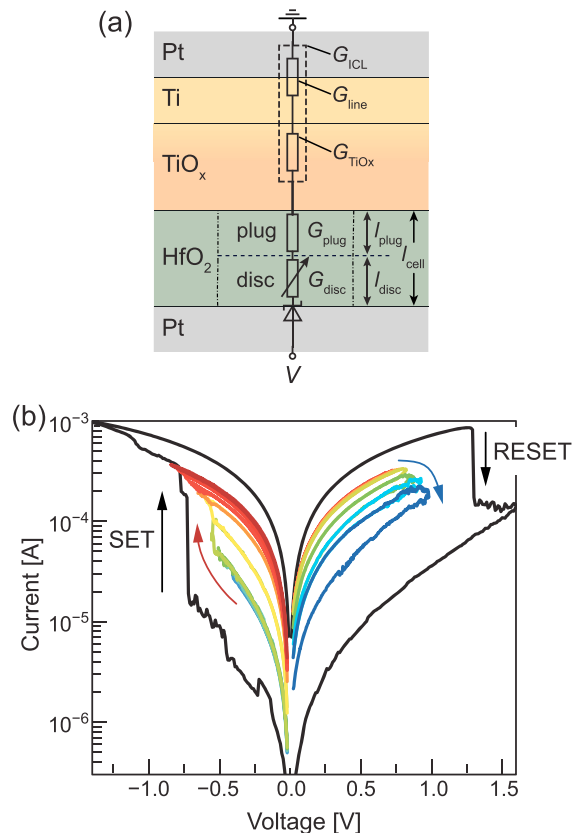


FIG. 1. (a) Stack design of the nanosized 30 nm Pt/3 nm HfO₂/3 nm TiO_x/10 nm Ti/20 nm Pt devices and equivalent circuit including the conductance-limiting element G_{ICL} composed of contributions from the lines, G_{line} , and from the inherent TiO_x layer, G_{TiOx} . The HfO₂-based memristive element is characterized by the conductive filament which is divided into a conductive plug, G_{plug} , and the resistive disc regime, G_{disc} ; dimensions not to scale. (b) Current-voltage sweeps measured for the device in (a) visualizing the two switching operations of the BRS SET and RESET, which are the abrupt mode (black line) and gradual mode (colored lines).

Typical forming voltages are found at (-2.9 ± 0.1) V, which makes the devices compatible to the voltage range offered by CMOS integrated circuits. Subsequently, 30 voltage sweeps are performed to ensure proper device functionality. Here, the voltage is ramped from 0.0 V, then to 1.3 V, and back to 0.0 V, using a sweep rate of 0.67 V/s and a measurement setup sided current compliance of 100 μ A. Pulse analysis of the SET operation was performed with a custom-built pulse measurement setup comprising an Agilent B1110A pulse-/pattern generator and a Tektronix TDS6804B digital storage oscilloscope. For the exact measurement setup, the reader is referred to Ref. 9. For RESET transient current analysis as well as “pulse and read”-operation, a Keithley 4200-SCS, equipped with a pulse measure unit (4225-PMU) with two channels and two remote amplifiers (4225-RPM), was employed. An ArC ONE platform of ArC Instruments Ltd. was used for analog switching characterization.

The complete stack design is illustrated in Fig. 1(a). The equivalent circuit shows the different components that are combined in the device under testing (DUT). The conductance of the metal connections (G_{line}) and the titanium oxide interface layer (G_{TiO_x}) can be combined into a conductance G_{ICL} , which represents the ICL. For simulation purposes, the HfO_2 layer is split into a plug and disc region, where the plug is conductive and represents an infinite reservoir of oxygen vacancies.⁷

III. SWITCHING BEHAVIOR

In Fig. 1(b), two sweep measurements of bipolar resistive switching (BRS) of a single device are shown. The slow rate of the voltage ramps was set constant at 1.0 V/s. In the first case (solid black line), the initial starting LCS is low. Negative bias to the Pt BE leads to an abrupt increase in the current at a voltage of -0.75 V. The current through the device after the SET process is initially limited by the ICL. At a voltage below -1.3 V, a measurement system sided current compliance of 900 μ A is active. The conductance is close to the maximal achievable HCS. At positive bias applied to the Pt BE, the device switches back to the LCS at a voltage of 1.3 V. As the voltage is stopped at 1.6 V, the device is in a low LCS again, which promotes another SET process with abrupt characteristic in the subsequent BRS cycle. The second operation mode, drawn in solid colored lines each representing an individual conductance state, stands in contrast to the first operation mode. Here, the initial LCS is more conductive. The first switching loop is taken for a voltage sequence from 0.0 V to -0.5 V to 0.0 V. The stop voltage of the SET sweep is consecutively decreased from -0.5 V to -0.85 V in steps of 10 mV. Every negative sweep results in a new, separable conductance state, indicated by the different colors. In this operation mode, no measurement sided current compliance is necessary. Analogously, upon applying triangular voltage signals (0.0 V to RESET stop voltage to 0.0 V) with increasing positive amplitude to the Pt BE, a gradual decrease in the conductance is achieved for RESET stop voltages between 0.75 V and 1.0 V. Starting the switching hysteresis with the device in a low LCS leads to an abrupt SET and abrupt RESET characteristic, which is due to the thermoelectric coupling during the SET event and the voltage divider effect during RESET. In contrast, switching loops recorded in the defined limits of moderate LCS and HCS level enable gradual bipolar BRS for the SET and the RESET process. This shows that the initial conductance states play a decisive role for achieving the desired switching properties.

IV. ANALYSIS OF THE SET PROCESS

This state-dependence of the switching mode is further investigated by analyzing the current transients for constant voltage pulses. For this measurement procedure, the device is initialized with a defined LCS. Then, a negative SET voltage pulse of variable duration and amplitude is applied. Figure 2(a) shows the read conductance states obtained by 0.2 V read signals after the application of a pulse with 1 μ s width and variable amplitude. A clear dependence of the read conductances from the voltage pulse amplitude and from the initial LCS (indicated by colors) is obtained. For the lowest initial LCS of about 2 μ S to 10 μ S (pink triangles), two regimes appear. At low amplitudes below $|V_{\text{pulse}}| = 0.75$ V, only minor deviations from the initial LCS are measured. At higher voltage amplitudes, a mixture of successful and unsuccessful SET events is observed. While, in general, a higher amplitude leads to a higher HCS, intermediate conductive states appear as well, indicating an incomplete switching event. In contrast to the low initial LCS, the highest initial LCS conductance state (closed black circles) shows an almost linear relation of the conductance increase with $|V_{\text{pulse}}|$ starting at about 0.625 V. Intermediate conductance levels, which are inaccessible from the lowest LCS, are reproducibly addressable. For intermediate initial states of 16–20 μ S (open blue triangles), only a slight deviation from a linear behavior at voltages between 0.65 V and 0.7 V is observable. Some events, however, are delayed in their conductance change, while others follow the linear increase in conductance. It is interesting to note that the final HCS is independent of the initial state; it is only a matter of the applied voltage amplitude as indicated by the data overlap in Fig. 2(a) at voltages above 0.7 V. This effect can be related to the voltage divider effect due to the ICL.¹⁵ The state-dependence of the programming behavior shown in Fig. 2(a) is correlated with a different current response during the application of the voltage pulse. Figure 2(b) shows a typical SET current transient from a high initial LCS of about 40 μ S at a pulse amplitude of 0.72 V. In contrast, Fig. 2(c) shows the effect of a low initial LCS value, in detail 5 μ S, on the transient current for a SET voltage pulse of 0.85 V and 1 μ s. Typically, the current transients starting from a moderately low LCS [Fig. 2(c)] show a slow current increase in the beginning, followed by the fast current increase. This two-step SET process is related to a positive feedback between the conductance increase and increasing Joule heating, which finally leads to a thermal runaway.^{8,28} The delay time of the SET process t_{delay} describes the initial low current increase and is often assumed to be equal to the SET time, t_{SET} , because it marks the onset of the fast current increase, consistent with the literature.⁸ However, a more precise definition of t_{SET} should include the time for the fast, abrupt current increase, which we term transition time $t_{\text{trans,SET}}$; see zoom-in below Fig. 2(c). Therefore, t_{SET} is the sum of $t_{\text{delay,SET}}$ and $t_{\text{trans,SET}}$. Statistics on the relation between t_{trans} and the pulse amplitude starting from low initial LCS can be found in Figure S1 in the [supplementary material](#). Exemplarily, two effects on the SET transition behavior can be determined from Figs. 2(b) and (c). An increase in the SET voltage by 0.13 V leads to a significant reduction in the SET transition time to the point, where the entire transition event is undergone within the pulse duration. This demonstrates a strong nonlinearity of the transition time from the applied voltage consistent with results on SrTiO_3 -based devices reported in the literature.⁸ In contrast, SET events from high initial LCS [Fig. 2(b)] show a different dependence.

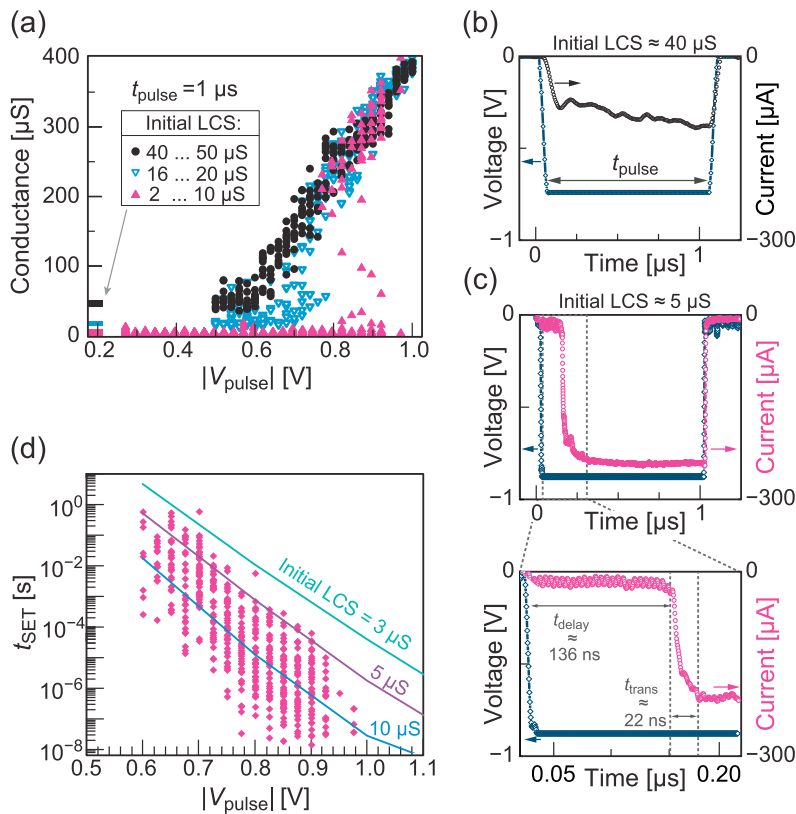


FIG. 2. (a) Observed conductance values after 1 μs SET pulse with varying amplitude for low (closed triangles), intermediate (open triangles), and high (filled circles) initial LCS level. (b) Analog transient current response during SET obtained for a high initial LCS and a SET voltage of 0.72 V. (c) Abrupt transient current response during the SET pulse obtained for a low LCS level and a SET voltage of 0.85 V. (d) SET switching kinetics study revealing the variability of the experimental delay time at given SET voltage amplitudes. The simulation results (solid colored lines) show that the differences in the delay time can largely be explained through a variation of the initial LCS values.

The high LCS strongly reduces the delay time up to where it is not observable any more. The analysis of the current transients from low LCS during the SET event in 1 μs pulses lead to a better understanding of the SET switching kinetics plot given in Fig. 2(d), which was recorded using pulse lengths between 100 ns and 1 s. Here, the variability in the SET time, which scatters over about four orders of magnitude at a specific voltage, originates from different low initial states. The lower the LCS is, the longer is the SET time, consistent with previous studies^{29–31} and with the simulation results presented in this study as shown above. However, the more careful analysis revealed that this variation in the experimentally derived SET time is, in detail, due to an increase in the delay time leaving the transition time almost unaffected. Further control of the SET behavior of defined VCM-type devices requires the determination of the transition time vs voltage dependence in separation from the effect of the experimental conditions on the delay time.

The study in Fig. 2(a) for 1 μs SET pulses was extended to cover pulse lengths from 100 ns up to 1 s, resulting in the graphs given in Figs. 3(a)–3(c) for high initial LCS of 40–50 μS , intermediate initial LCS of ~ 16 –20 μS , and low initial LCS of ~ 2 –10 μS , respectively. The median conductance averaged over ten SET pulses is given for the high and intermediate LCS in (a) and (b). Since the median value of conductance would misrepresent the reality of the mix of successful and unsuccessful SET events for the low LCS case, a different depiction method is chosen for Fig. 2(c). Combinations of pulse duration and amplitude which leave the device conductance unaffected are drawn as LCS values (dark blue color). In cases where the device

undergoes a SET event or remains in the LCS, which is defined as probabilistic switching, a mixture of LCS and HCS values is drawn, with the density of HCSs representing the probability of a SET event. When the pulse voltage-time-combination always leads to a SET event, the respective reached HCS is drawn (orange to red color). The shown diagrams can be understood in several ways. First, the voltage dependence on the achieved HCS at a read voltage of 0.2 V, which was already shown in Fig. 2(a), is evident. By application of increased voltage, a higher HCS is achieved. This holds true for all three initial states. This means that the reached HCS level is independent of the initial LCS state. However, depending on the initial state, the voltage threshold for conductance modulation is influenced. High initial LCS levels require lower voltages for state modulation than low LCS start conditions. Yet, in the experiments presented in this study, all initial conditions lead to almost the same slope in the voltage-time-plot, indicating identical physical processes. This observation supports the thermally activated switching model. Alternatively, the diagrams can be understood from the viewpoint of constant voltage operation. Using extended pulse durations instead of increasing the amplitude also yields a gradual transition between LCS and HCS in the case of high initial LCS conditions. At low initial LCS, longer pulse times additionally make the switching event more likely.

Apparently, the two kinds of switching characteristics observed for high/intermediate LCS and low LCS are related to the different behavior during the current transients. To access intermediate conduction values, the length of the pulse time t_{pulse} must be comparable with the transition time t_{trans} . For very low initial LCS, $t_{\text{pulse}} \gg t_{\text{trans}}$

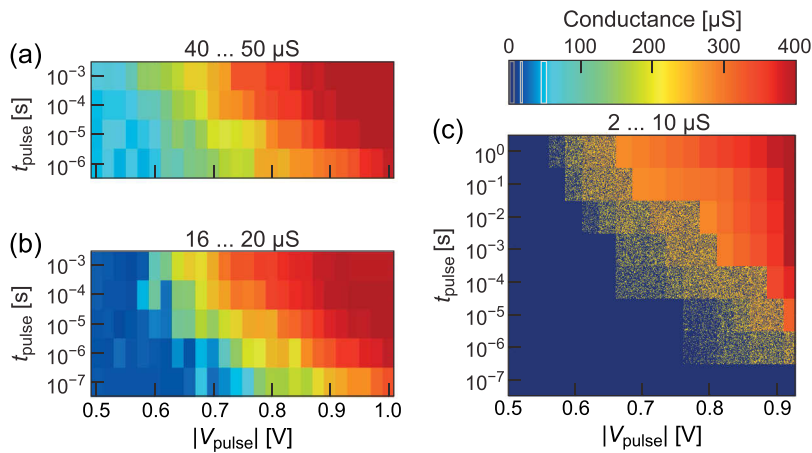


FIG. 3. Median conductance values after SET pulses (at $V_{\text{read}} = 0.2$ V) with varied amplitude and duration, starting from (a) high LCS and (b) intermediate LCS. (c) Conductance values after SET pulses starting from low initial LCS level. A mixture of successful and unsuccessful SET events is observed. In the HCS, the values coincide independent of LCS.

holds, and thus, the pulse time for switching is a lot longer than the transition time. In consequence, the switching appears binary. Only when the switching transition happens at the end of the applied pulse, intermediate states might be accessible, but these are rare events.

V. ANALYSIS OF THE RESET PROCESS

To study the state- and voltage-dependence of the RESET process, the devices were programmed to different HCSs by applying different pulses of -0.9 V up to -1.6 V for a duration of 10 μs in a preceding SET process. The respective HCSs, read at 0.3 V, are plotted in Fig. 4(a). The obvious nonlinearity of HCS and SET voltage arises from the ICL element of the device [see Fig. 1(a)]. This interplay arises only at SET voltages below -1 V and was therefore not

visible in Fig. 2(a). Subsequently, RESET experiments at constant voltage are performed for various HCSs. Representatively, Fig. 4(b) shows the transient currents recorded for a RESET voltage of 1.0 V. The device shows strongly delayed RESET behavior depending on the initial HCS level. Equivalent to the analysis of the SET processes, the RESET process is experimentally defined by the RESET time t_{RESET} , which is determined when the current drops below 300 μA . In the more specific analysis, the transient RESET behavior reveals two regimes. The time addressed to the regime of low current reduction is named the delay time, $t_{\text{delay, RESET}}$, and the one related to the strong current reduction is identified as the transition time, $t_{\text{trans, RESET}}$. The addition of both yields the RESET time t_{RESET} . In the case of low initial HCS, about 500 μS , drawn in dark blue, the RESET occurs within the first few microseconds after pulse application. In the case of high initial HCS, about 700 μS , drawn as orange lines, several hundred

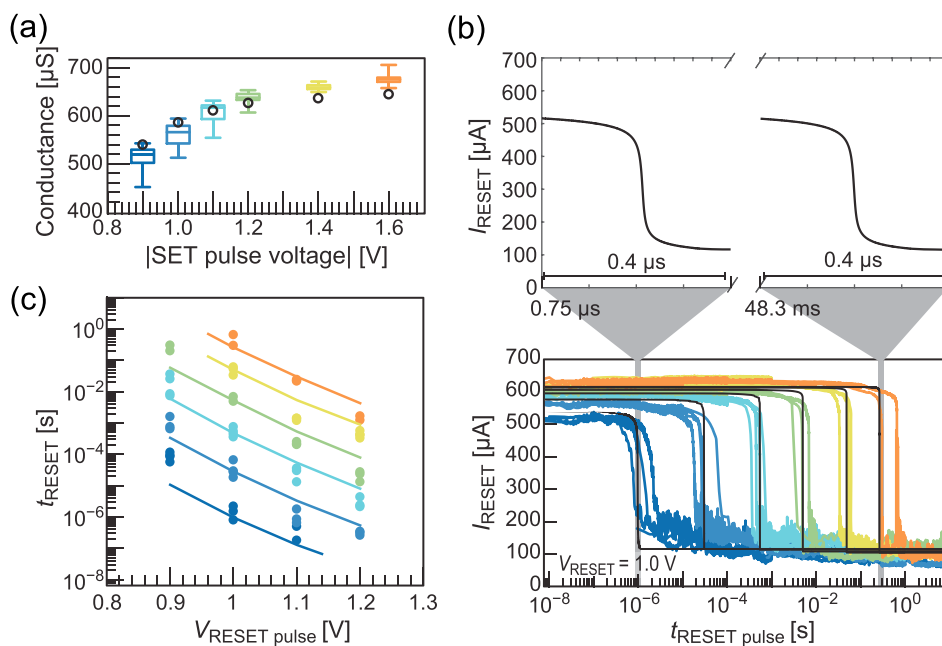


FIG. 4. (a) HCS of the devices programmed by application of a SET pulse of 10 μs and the given voltage amplitude. The nonlinearity originates from the influence of the ICL. The black circles show the initial states of the corresponding simulations in (b). (b) RESET current transients at a constant RESET voltage of 1.0 V for different initial HCSs. High HCS values lead to pronounced delays during the RESET operation. The simulated transients (black solid lines) are able to fit the variation of the delay by assuming different initial states. The zoom of the simulated transients illustrates that the transition time is state-independent. (c) RESET switching kinetics for various HCSs characterized by the SET pulse amplitude. A delay of up to six orders of magnitude in switching time is observed. The simulations (solid lines) predict the voltage-time-dependence well.

milliseconds up to 1 s are needed for obtaining the RESET. Here, the RESET time is controlled by the delay time, which turns out highly state-dependent. In contrast, the duration of the sharp transition between HCS and LCS, i.e., the RESET transition time $t_{\text{trans, RESET}}$, stays constant. Zooming into the transition regime reveals a transition time of about 65 ns for all initial HCS. From this, the RESET process can be viewed as consisting of three distinct phases. During the first phase, the state stays almost constant and little switching occurs because during this phase, most of the applied voltage drops over the ICL. This delay phase increases significantly for higher HCS and thereby leads to the state dependent delay time. The second phase is the abrupt RESET transition. It has a constant duration at a specific voltage independent of the initial state. The third phase is the slow “phasing out” after the abrupt transition that appears due to the strong temperature decrease with increasing resistance, which slows down the switching into lower LCS states.⁹ The strong state dependence of the experimentally accessible RESET time was further analyzed at different voltages. A pattern of increasing RESET time with increasing HCS level, highlighted by the colors of the data points, is visible in Fig. 4(c). In the extreme case tested, the RESET is delayed by about six orders of magnitude in time while changing the voltage amplitude of the preceding SET process by 0.7 V. The simulation results, drawn as solid lines, closely match the experimental findings. The strong nonlinearity of the switching time dependence on the applied pulse voltage underlines the importance of controlling the conductance window since unfavorable delay times arise when the conductance leaves the moderate regime.

VI. POTENTIATION/DEPRESSION OPERATION

Based on the systematic experimental analyses combined with the simulations by means of the fully physical switching model (see below), a detailed description of the SET and RESET dynamics and their state-dependence is developed. Utilizing this understanding, two alternative types of synapses can be realized with the same device. Bivalent switching between distinctive high HCS and low LCS levels is possible by pulse operation with increased voltage. In this case, the SET/RESET delay time will become significantly longer

than the transition time and intermediated states are not accessible. Figure 5(a) depicts a suggested pulse scheme of alternating pulse packages for LTP and LTD operation. Shown in Fig. 5(b) is an exemplary extract of three alternating LTP/LTD cycles. In this specific case, the voltages were chosen high enough to obtain reproducible switching with the first two pulses. As shown in Fig. 5(c), the change in normalized conductance over the pulse number, which is essentially the weight update function, is highly nonlinear as the first pulse already traverses the entire dynamic range of conductance. In the case of linear weight update, this function would follow the straight diagonal line between 0 and 1. A significant step toward a more linear weight update function is taken by (i) choosing a pulse length that is smaller than the transition time at a specific voltage and (ii) reducing the HCS level and increasing the LCS value. During operation, this is effectively achieved by reducing voltage amplitudes as given in Fig. 5(d). The LTP/LTD cycles depicted in Fig. 5(e) show conductance levels inaccessible by the method shown in (a). The normalized conductance change function over pulse repetition is therefore shaped more toward the straight diagonal line, as can be seen in Fig. 5(f). The major difference between the two modes seems to be the transition time from LCS to HCS. Low initial LCS levels require a high SET voltage, which, in turn, results in very short transition time (e.g. 22 ns), and is just above the resolution limit of the measurement setup. Hence, intermediate conductance steps are highly infrequent as the transition from LCS to HCS is orders of magnitude shorter than the pulse duration. Once triggered, it is likely to begin and finish within a single pulse. Additionally, a delay time of high variance is inherent. This makes the accessibility of intermediate conductance states very complicated to achieve even if accordingly short pulse durations were available in the employed measurement setup. In contrast to this, the transition times corresponding to lower SET/RESET voltages in Figs. 5(e) and 5(f) approach toward the range of the pulse length of 1 μ s for this experiment. Furthermore, in our experiments, no delay time for the SET transition was observable as the initial LCS is quite high. This makes intermediate conductance states accessible by single pulse application since the SET process has not been finished by the end of the pulse and is subject to further changes in the subsequent pulse

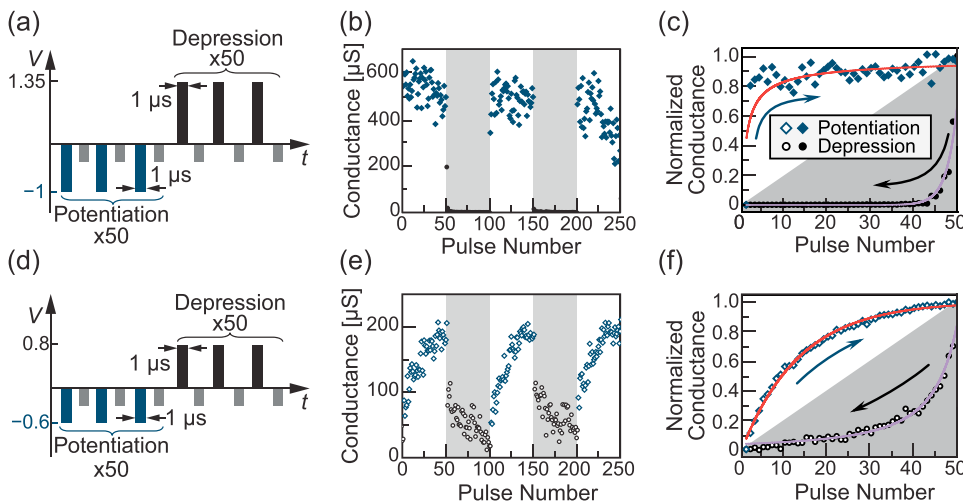


FIG. 5. LTD and LTP operation with parameters resulting in abrupt and gradual switching behavior. (a) and (d) Operation method and parameters. (b) and (e) Resulting alternating LTP and LTD cycles. (c) and (f) Normalized conductance evolution revealing the high abruptness of the SET/RESET operation parameters in (a) and the more gradual behavior for parameters of (d). The diagonal line marks linear behavior. The fits in (c) and (f) are performed according to the model of Fusi and Abbott.²³

with the same amplitude. Comparable studies on TiN/HfO₂/Ti/TiN devices have been reported by Frascaroli *et al.*²⁰ Interestingly, the voltage regimes defining analog-type behavior in the different HfO₂-based memristive devices are quite comparable. This might prove the universal applicability of the transition-time concept suggested here.

VII. PHYSICAL SIMULATION

Based on the shown experimental results, we conclude that analog switching is possible if the pulse length is of the order of the transition time. Furthermore, the state-dependence of the SET/RESET transition should be eliminated. To this end, a proper conductance window needs to be chosen. To validate and generalize this conclusion, a simulation study is performed using the compact model for filamentary switching based on the valence mechanism called JART VCM v1, which is part of the Juelich-Aachen Resistive Switching Tool Box (JART). The model varies slightly from the original description.¹⁵ The ion conduction mechanism, which was previously modeled according to the Mott and Gurney law,³² is now modeled as suggested by Genreith-Schriever.³³ This provides a more accurate description for very high electric fields. To achieve a consistent description of the SET and RESET dynamics, a polarity-dependent effective thermal resistance R_{th} is used. The switching parameters have been fitted within physically reasonable limits to match the experimental data. The used parameters are listed in Table I, and the equivalent circuit diagram is shown in Fig. 1(a). The model reproduces the state- and voltage-dependence of the experimental data over many orders of magnitude in time. The solid colored lines in Fig. 2(e) show the simulated SET delay times for three different initial resistance values. In the simulations, a constant voltage pulse with a rise time of 1 ns is applied. The SET delay is defined at the point in time with the steepest current increase. The spread of the experimental data is well reproduced by assuming different initial resistances (2 μ S–10 μ S) in the simulation, which agrees well with the initial resistance states in the experimental data. In the simulations, the SET delay time is orders of magnitudes higher than the transition time, consistent with the experimental data shown in Fig. 2(c) and our previous simulation studies.⁸

TABLE I. Simulation parameters (for the explanation of the symbols, see the work of Hardtdegen *et al.*¹⁵).

Symbol	Value	Symbol	Value
l_{cell}	3 nm	A^*	$6.01 \cdot 10^5 \text{ A}/(\text{m}^2 \text{K}^2)$
l_{disc}	0.4 nm	$e\Phi_{Bn0}$	0.18 eV
r_{fil}	45 nm	$e\Phi_n$	0.1 eV
z_{vo}	2	μ_n	$4 \cdot 10^{-6} \text{ m}^2/(\text{Vs})$
a	0.25 nm	N_{plug}	$20 \cdot 10^{26} \text{ m}^{-3}$
ν_0	$2 \cdot 10^{13} \text{ Hz}$	$N_{disc,max}$	$20 \cdot 10^{26} \text{ m}^{-3}$
ΔW_A	1.35 eV	$N_{disc,min}$	$0.008 \cdot 10^{26} \text{ m}^{-3}$
ε	$17 \varepsilon_0$	$R_{th,eff,SET}$	$15.72 \cdot 10^6 \text{ K/W}$
$\varepsilon_{\Phi B}$	$5.5 \varepsilon_0$	$R_{th,eff,RESET}$	$4.2444 \cdot 10^6 \text{ K/W}$
T_0	293 K	G_{TiOx}	1538 μ S
$G_{line} (I = 0 \mu\text{A})$	1391 μ S	$G_{line} (I = 700 \mu\text{A})$	1234 μ S

The simulated RESET current transients are shown in black in Fig. 4(b). The initial oxygen vacancy concentrations are chosen to match the initial experimental states at 0.2 V. In the simulations, the RESET pulse of 1.00 V is applied as a constant voltage signal with a rise time of 1.0 ns. As in the experiment, the RESET transition is strongly delayed for higher HCS. This delay results from the voltage-divider effect of the ICL. In the beginning, most of the voltage drops over the ICL rather than the active switching part. As soon as the conductance decreases, the voltage drop over the device increases, and in turn, the switching speed increases. This leads to the fast RESET transition. Due to the reduced power dissipation, the conductance change slows down finally. This “phasing out” origins from the decrease in the local temperature in combination with ionic drift, and the diffusion approaching equilibrium defines the behavior in this region during RESET.⁹ In contrast, the plateau region at the final stages of the SET transition is due to the current limitation by the ICL.

To achieve a stable analog switching, the time frame of the input signals should be of the order of the transition time. Thus, we extracted the transition time from SET and RESET pulse simulations. It turns out that the SET/RESET transition time is state-independent [cf. zoom in Fig. 4(b)], which is consistent with the presented experimental findings. Figure 6(a) shows the simulated SET/RESET transition time as a function of the applied voltage. Consistent with data of Ta₂O₅- and SrTiO₃-based filamentary VCM cells, the transition time is a highly nonlinear function of the applied voltage⁸ but almost independent of the initial state. The graph also shows that the transition times required for the RESET are longer than for the SET. Thus, asymmetric voltages need to be chosen to achieve a transition in comparable times. The desired order of time depends on the application. For the simulation, transition times of 1 ms and 1 μ s were chosen. According to Fig. 6(a), the corresponding SET/RESET voltage pairs are (−0.33 V/0.68 V) and (−0.44 V/0.91 V) for 1 ms and 1 μ s transition time, respectively. To access intermediate values between the HCS and the LCS, the pulse width needs to be smaller than the transition time. In addition, too high HCS and too low LCS should be avoided as this would lead to long delay times. To achieve an optimum tunability, the conductance values within the transition regime need to be chosen as illustrated in Figs. 6(b) and 6(c) for the 1 ms and 1 μ s case, respectively. The marked maximum and minimum conduction states allow for an almost linear tuning of the conductance with consecutive pulses of identical voltage amplitudes and duration. The length of the pulses is adjusted to achieve 10 different conductance levels. To this end, the elapsed time between the beginning [see t_0 and t_1 in Figs. 6(b) and 6(c)] and the end [$(t_0 \text{ resp. } t_1) + \Delta t$] of the conductance transition is divided by 10. Using the voltage amplitudes and the pulse widths determined as described before, pulse train simulations with 10 consecutive SETs followed by 10 consecutive RESETs are performed. The simulation results are shown as crosses in Figs. 6(d) and 6(e) for the 1 ms and 1 μ s case, respectively. In both cases, an almost linear conductance tuning can be achieved. Furthermore, the tuning turns out to be very symmetric.

Following the above-described procedure, conductance tuning for analog memristive behavior can be achieved on every time scale. However, any deviation from the procedure unavoidably leads to undesired results. This is demonstrated in Fig. 6(d), where the diamonds are the results of a tuning starting from the same initial

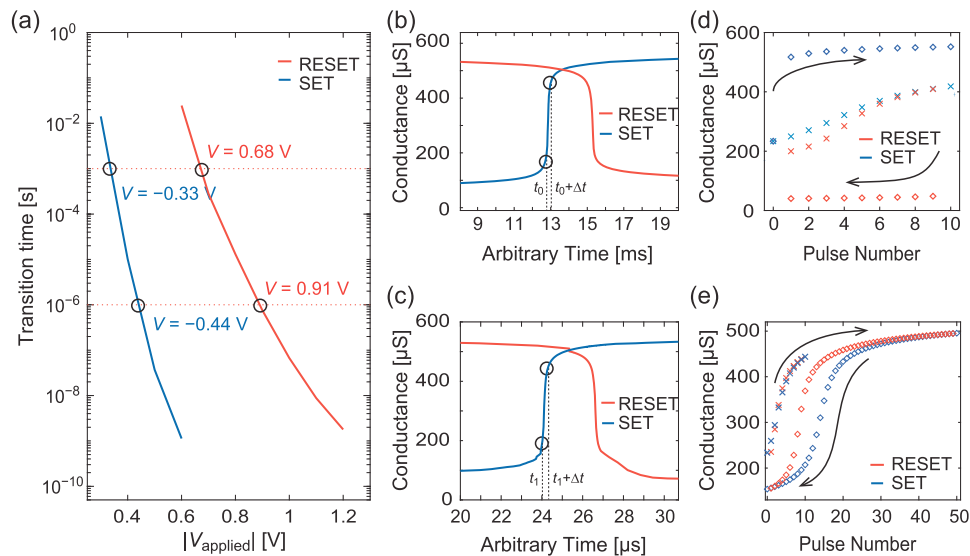


FIG. 6. (a) Simulated transition times for SET and RESET showing the SET and RESET voltages to achieve transition times of 1 ms and 1 μ s. The corresponding SET and RESET transients for 1 ms and 1 μ s transition time are shown in (b) and (c), respectively. The times t_0 and t_1 are arbitrary reference times at the beginning of the transition. Δt represents the time range in which linear conductance modulation is achieved. In (d), the cross symbols show the conductance evolution for consecutive SET pulses (blue) and RESET pulses (red) in the conductance regime defined by the black circles in (b). The diamonds in (d) show the conductance modulation for too high voltage amplitudes (-0.4 V/ 0.8 V). In (e), the cross symbols show the conductance evolution for consecutive SET and RESET pulses in the conductance regime defined by the black circles in (c). The diamonds in (e) show the simulated conductance modulation using the same pulse length and amplitudes as for the crosses, but starting from a lower initial conductance.

conductance and with the same pulse widths as before, but using higher voltage amplitudes (-0.4 V/ 0.8 V). The transition times for these amplitudes are smaller than the chosen pulse width [see Fig. 6(a)]. Thus, intermediate states are hardly accessible and the switching becomes binary reaching high HCS and low LCS. The accompanying increase in stochasticity is due to the state-dependence of the delay times in these conductance regimes. The simulation results correspond well with the experimental data shown in Figs. 5(a)–5(c). If a lower initial conductance value is chosen while keeping the pulse width and height the same as for the linear case, the resulting conductance modulation follows an S-shape [diamonds in Fig. 6(e)]. In this case, the pulse voltages and the pulse width are chosen according to the procedure described before, but higher HCS and lower LCS values are used. Thus, there is a trade-off between nonlinearity of the conductance tuning and the accessible conductance window.

VIII. CONCLUSIONS

This work showed that the same Pt/HfO₂/TiO_x/Ti stack could be exploited for analog or binary, stochastic conductance modulation. The controlling parameters are the voltage amplitude and the pulse length. The most important issue is that a proper conductance window must be chosen. In general, SET and RESET in the VCM-type memristive devices are a two-step process: A sharp conductance change within a transition time succeeds a slow conductance change described by a delay time. Both times highly depend on the applied voltage. While the delay time turns out to be highly state-dependent for a specific voltage, the transition time is relatively independent of

the state of the device. Based on these findings, we deduced two conditions for achieving analog conductance behavior in filamentary VCM cells. First, the applied pulse length must be shorter than the transition time. Otherwise, the switching will become binary. Second, the conductance window must be chosen in a way that delay times are significantly reduced below several percent of the transition time. This can be effectively done by increasing the initial LCS and by decreasing the HCS, prior to SET operation (potentiation) and to RESET operation (depression), respectively. Using the JART VCM v1 model, we could generalize this result and deduce an experimental procedure to find the optimum working condition. First, the transition time needs to be determined as a function of the applied voltages. Based on this result, the SET and RESET voltage amplitudes can be chosen according to the operation time of the targeted application. From the recorded SET and RESET transients, a proper conductance window needs to be defined. It is important to note that, in principle, every time scale allows for proper operation conditions. The voltages, however, may not be compatible to the application. The present study points a new direction for further research. As the transition time is identified as the most important parameter, future research should strive for the elucidation of the physical parameters influencing the transition time and the size of the addressable conductance window.

SUPPLEMENTARY MATERIAL

See [supplementary material](#) for additional experimental data showing the voltage dependence of the transition time and an additional SET transient.

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