Selective area growth and stencil lithography for in situ fabricated quantum devices

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The interplay of Dirac physics and induced superconductivity at the interface of a 3D topological insulator (TI) with an s-wave superconductor (S) provides a new platform for topologically protected quantum computation based on elusive Majorana modes. To employ such S–TI hybrid devices in future topological quantum computation architectures, a process is required that allows for device fabrication under ultrahigh vacuum conditions. Here, we report on the selective area growth of $(Bi,Sb)_2Te_3$ TI thin films and stencil lithography of superconductive Nb for a full in situ fabrication of S–TI hybrid devices via molecular-beam epitaxy. A dielectric capping layer was deposited as a final step to protect the delicate surfaces of the S–TI hybrids at ambient conditions. Transport experiments in as-prepared Josephson junctions show highly transparent S–TI interfaces and a missing first Shapiro step, which indicates the presence of Majorana bound states. To move from single junctions towards complex circuitry for future topological quantum computation architectures, we monolithically integrated two aligned hardmasks to the substrate prior to growth. The presented process provides new possibilities to deliberately combine delicate quantum materials in situ at the nanoscale.

With their experimental verification in 2007, topological insulators (TIs) render a new and fascinating class of materials[1]. A band inversion in the bulk of three-dimensional (3D) TIs creates a 2D metallic subspace at the physical surface of these 3D crystals. The charge carriers of the 2D metal (Dirac electrons) have their spin locked to the momentum, which leads to a topological protection of the subspace[2–4]. This intrinsic quantum-spin texture enables the realization of novel technologies, which range from spintronics to quantum computing. Particularly in combination with superconductors (S), TIs promise new quantum devices. Networks of TI nanostructures in proximity to superconductive islands have been predicted to host non-Abelian Majorana modes at the ends and at the crossing points of the networks[5–8]. Braiding of these elusive modes, that is, exchanging the position of Majorana modes in a 2D plane (Supplementary Fig. 2), resembles topologically protected quantum operations in the Majorana platform. Topological quantum bits (qubits), which use Majorana modes[9,10] to store and process quantum information, are expected to compute fault tolerantly with minimal need for error correction[11–14].

Topological qubits require high-quality (multi-terminal) Josephson junctions (JJs)[12,15,16]. The simplest type of such a JJ is a two-terminal S–TI–S device (Fig. 1). The Josephson effect[17] allows for an electrical current to conduct dissipationlessly across a lateral junction of two close-by superconductive electrodes separated by a weak link of non-superconductive material. In conventional lateral

JJs, the supercurrent is mediated by Andreev bound states (ABS), which effectively transport Cooper pairs across the weak link[18]. In S–TI–S junctions the Dirac system forms a weak link. The quantum spin texture of the Dirac system causes an additional transport channel, known as Majorana bound states (MBS), which adds to conventional ABS[19]. In contrast to ABS, MBS facilitate single-electron transport across the weak link[20]. The contribution of MBS to a supercurrent can be detected via Shapiro response measurements[19,21–24]. MBS manifest themselves by a suppression of odd Shapiro steps in low-temperature transport experiments under radio frequency (RF) radiation, due to their 4π-periodic energy-phase dependency[25].

To create and preserve MBS in S–TI–S junctions, the Dirac system in between the superconductive electrodes needs to be conserved (Fig. 1b). Surface oxidation[26,27] and reactions with water molecules at ambient conditions[28] can lead to additional non-topological states at the surface of (Bi,Sb)-based TIs. These superimpose locally with the Dirac system, and thus allow for additional scattering events that could destroy the MBS. To avoid surface degradation in (Bi,Sb)-based TIs, an in situ deposited protective AlO_x capping layer on top of the topological surface is often employed[29,30]. Although such capping layers protect the topological surface states for ex situ fabrication steps, they also prevent the realization of high-quality S–TI interfaces, as their removal deteriorates the TI surface and makes highly transparent S–TI interfaces hard to achieve[31]. Here, the fabrication of high-quality S–TI–S junctions with pristine
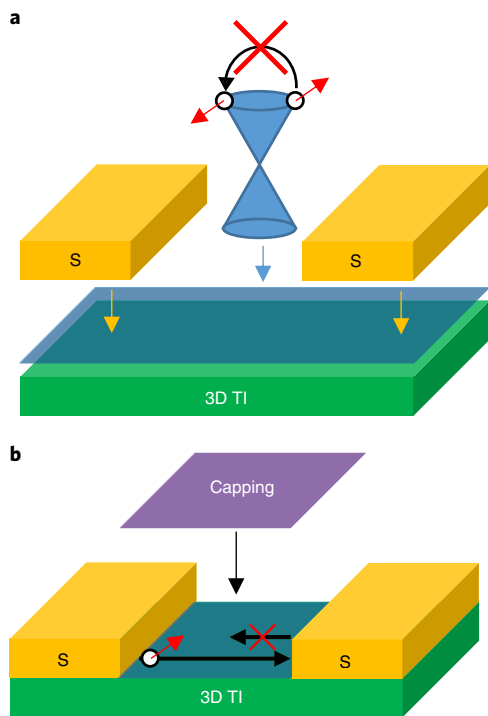
Fig. 1 | Schematic of an S–TI–S junction. a, Two close-by superconductive leads (yellow) in contact with the upper Dirac system (blue) of a 3D TI (green) define a lateral topological Josephson device. The TI surface inherits a Dirac-like dispersion relation, represented by a Dirac cone. Owing to the helical spin texture of the surface states, direct back scattering into the state with opposite momentum is fundamentally forbidden by quantum mechanics. **b**, An in situ capping layer (purple) in the weak link area is required to preserve the topological surface states and the forbidden backscattering after exposure to ambient conditions.

S–TI interfaces and fully capped weak link areas is demonstrated by employing suspended Si_3N_4 masks for on-chip stencil lithography. The monolithic integration of a second mask for selective area growth (SAG) allows for the in situ fabrication of complex S–TI networks in a highly scalable manner (Supplementary Fig. 3). This is important because the computational power, as well as the fidelity of the proposed topological quantum processors, scale with the size and complexity of the S–TI networks[13,15].

In situ fabricated Josephson devices

The topological and superconductive thin films were deposited in ultrahigh vacuum molecular-beam epitaxy chambers. As stencil lithography in such an environment and at high temperature requires resistless mask-fabrication techniques, a Si_3N_4 stencil mask was monolithically integrated to the Si(111) substrate prior to the deposition of the topological and superconductive thin films (Fig. 2a). Degassing the prepatterned substrate at 700 °C inside the molecular-beam epitaxy chamber restored a pristine Si(111) surface in areas that were not covered by the stencil. Through this process, the TI film selectively nucleated only on this pristine Si(111) surface[32,33]. The diffusion of adatoms deposited under a tilted angle (Methods) during substrate rotation made the $(Bi_{0.06}Sb_{0.94})_2Te_3$ thin film grow homogeneously underneath the freestanding stencil bridges. During the subsequent deposition of 50 nm of superconductive Nb, the substrate rotation was stopped in a well-defined orientation to the stencil bridge with respect to the Nb source. In this way, the TI thin film was covered completely by Nb, except for the narrow strip shaded by the free-standing bridge, which posed the

weak link between the two superconductive electrodes (Fig. 2b). For the capping of the TI weak link, the substrate rotation was restarted again for a global deposition of 5 nm of Al_2O_3 (Fig. 2c) to finish the device fabrication. In this way, the S–TI–S junction could be characterized without any further ex situ fabrication processes.

Pseudo four-terminal measurements (Fig. 2d) of five as-prepared devices (device details are given in Supplementary Table 1) at 12 mK yielded high switching supercurrents (I_C) of up to 14.1 μA and ballistic superconducting coherence lengths up to $\xi_{ball} = 110$ nm (Supplementary Section C). The product of I_C with the normal resistance (R_N) yielded high $I_C R_N$ values of up to 310 μV. The $I_C R_N$ product provided a lower bound on the induced superconducting gap $I_C R_N \leq \Delta_{ind}/e$, where e is the charge of an electron. The high $I_C R_N$ product is in line with the measured junction T_c of 4 K (Fig. 2e), which indicates a large induced gap of about 0.6 meV beneath the Nb electrodes. Besides the high S–TI interface quality, we found an excellent in-plane transparency of $D = 0.95$ (with $D = 1$ being a perfectly transparent interface) between the proximitized TI and the non-proximitized TI (Supplementary Fig. 5). The transparency was determined by analysing the ballistic contributions to the transport of the junction (Supplementary Section C). In Fig. 2e, the temperature dependency of the switching current $I_C(T)$ of device 2 is shown. The total supercurrent comprises ballistic surface modes and diffusive bulk contributions. Strikingly, above 2 K, we found that the supercurrent is solely carried by Dirac states (Supplementary Section C), which is in stark contrast to the normal transport in $(Bi_{0.06}Sb_{0.94})_2Te_3$ TI thin films in which the dominating contributions come from the bulk states. For normal transport in an in situ capped $(Bi_{0.06}Sb_{0.94})_2Te_3$ TI thin film, we found a high 2D sheet carrier density of $n_{2D} = 9.5 \times 10^{14}$ cm^{-2} and a low bulk mobility of $\mu = 62$ cm^2 V^{-1} s^{-1} (Supplementary Fig. 4). The low bulk mobility translates into a low diffusion constant. This allowed us to fully suppress the bulk contributions in the superconducting regime at elevated temperatures. Owing to the high interface transparency, we observed a supercurrent that was solely carried by surface states across a wide temperature range that spanned from 2 K to 4 K.

Shapiro response of single JJs

Shapiro response measurements were carried out to gain further insights into the quality of the hybrid devices and to investigate the presence of MBS in in situ fabricated Nb–$(Bi_{0.06}Sb_{0.94})_2Te_3$–Nb JJs. The transport of single electrons across the weak link via pure MBS manifests itself as a sequence of only even Shapiro steps at well-defined voltages under RF exposure:

$$V = 2nV_0 \quad (1)$$

with

$$V_0 = \frac{hf_{RF}}{2e} \quad (2)$$

being the characteristic Shapiro voltage[25]. Here, e is the charge of an electron, h is the Planck constant, n is an integer number and f_{RF} is the frequency of the RF signal. In 1D topological edge channels, missing odd steps up to the ninth have been reported[22]. For S–TI–S junctions with a 3D TI as a weak link, conventional ABS also contribute. These differ from MBS by manifesting as an integer sequence of Shapiro steps:

$$V = nV_0 \quad (3)$$

as they effectively transfer Cooper pairs (that is, two electrons). In JJs with a 3D TI as a weak link, ABS and MBS contribute to the total supercurrent[19]:

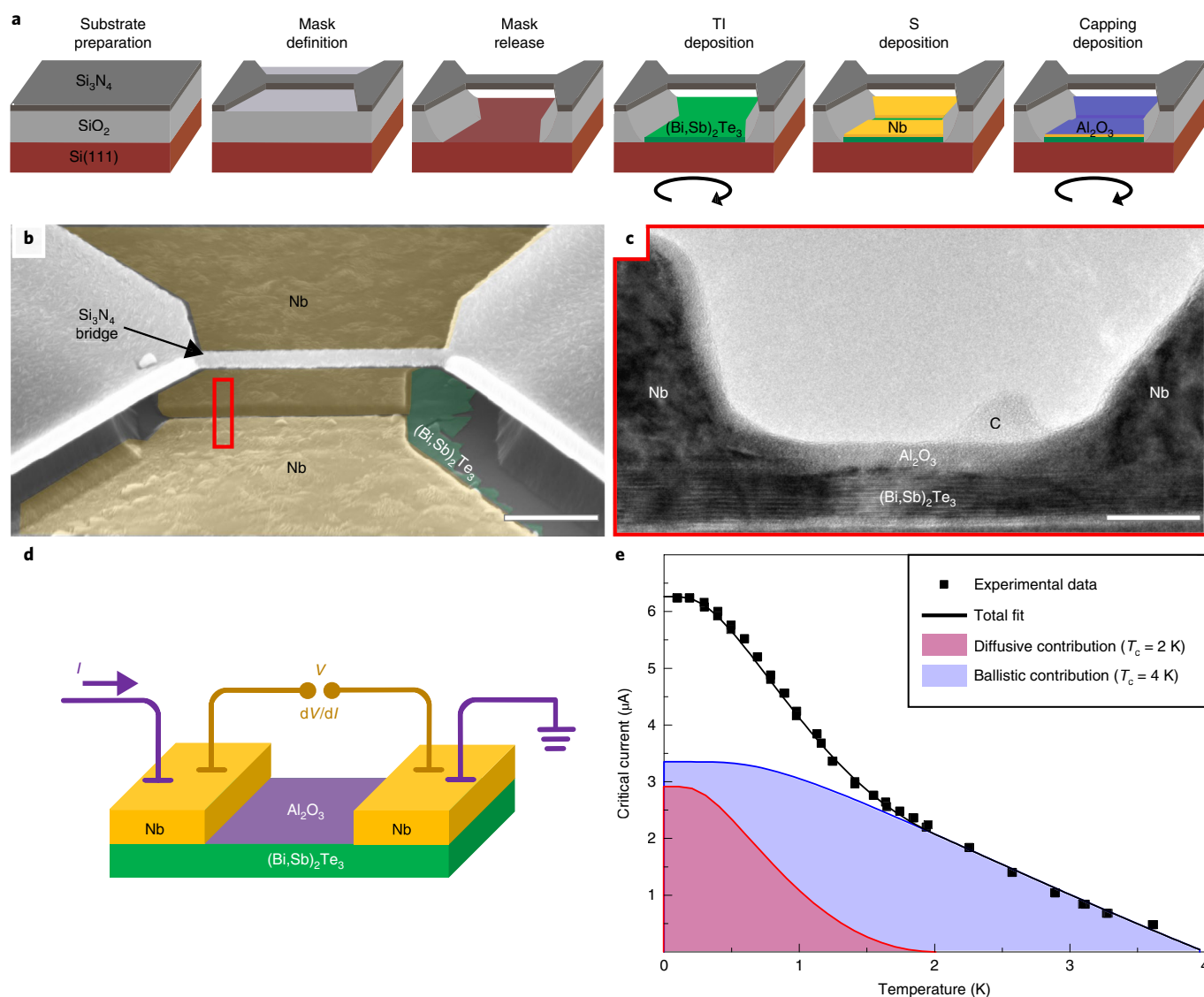$$I_C = I_{MBS} + I_{ABS} \quad (4)$$

Fig. 2 | In situ fabricated JJs. a, A stack of 500 μm Si (red), 300 nm SiO$_2$ (light grey) and 100 nm Si$_3$N$_4$ (grey) was utilized. A bridge structure was defined into the top Si$_3$N$_4$ layer via reactive ion etching. The bridge was then released by selectively etching the 300 nm SiO$_2$ layer in hydrofluoric acid. The TI layer (green) was deposited under substrate rotation via molecular-beam epitaxy. The superconductor (yellow) was deposited without substrate rotation, such that the free-standing Si$_3$N$_4$ bridge acts as a stencil. As a final step the capping layer Al$_2$O$_3$ (blue) was deposited under substrate rotation. Note that superconductive and dielectric thin films are also deposited on top of the mask, but they are not shown in the scheme for clarity. **b**, False colour scanning electron micrograph of an in situ fabricated junction. The stencil bridge casts a shadow that divides the Nb thin film into two electrodes, which are solely interconnected by the (Bi$_{0.06}$Sb$_{0.94}$)$_2$Te$_3$ weak link. Scale bar, 500 nm. **c**, Transmission electron micrograph of the cross-section of a single S–TI–S junction. Scale bar, 20 nm. The lamella was taken from the area indicated by the red frame in **b**. The layered structure of the rhombohedral (Bi,Sb)$_2$Te$_3$ crystal and a fully capped weak link are clearly visible. The carbon (C) mount is an artefact from specimen fabrication via focused ion beam. **d**, Schematic layout of the measured pseudo four-terminal topological Josephson devices. **e**, Temperature dependence of the diffusive bulk and the ballistic surface contributions to the supercurrent as calculated from the Usadel and Eilenberger fit (Supplementary Section C). At base temperature, the bulk and surface modes contribute similarly. Above 2 K, the supercurrent is solely carried by the ballistic surface modes.

Thereby, each contribution, I_{MBS} and I_{ABS}, has a characteristic Josephson frequency:

$$f_{MBS} = I_{MBS} R_N \frac{e}{h} \text{ and } f_{ABS} = I_{ABS} R_N \frac{2e}{h} \quad (5)$$

The suppression of odd Shapiro steps becomes observable only when f_{RF} is smaller than f_{MBS} (ref. [23]). Owing to the rather small contribution of MBS to the total current in JJs having a 3D TI as a weak link, odd steps usually start to disappear at rather low

frequencies[23,24]. Additionally, the large contribution from ABS[19] and the associated Joule heating[21] only makes the first step disappear in JJs with a 3D TI as a weak link.

We performed Shapiro measurements on two out of five in situ fabricated Nb–(Bi$_{0.06}$Sb$_{0.94}$)$_2$Te$_3$–Nb junctions. The measurements on device 1 were conducted at 1.5 K (Fig. 3) to rule out the possibility of missing steps due to hysteresis (Supplementary Fig. 6). For device 2, an increase in temperature to 3.2 K was needed to suppress the more pronounced hysteresis in this JJ (Supplementary Fig. 7). Furthermore, as thermal broadening smears out signal, the
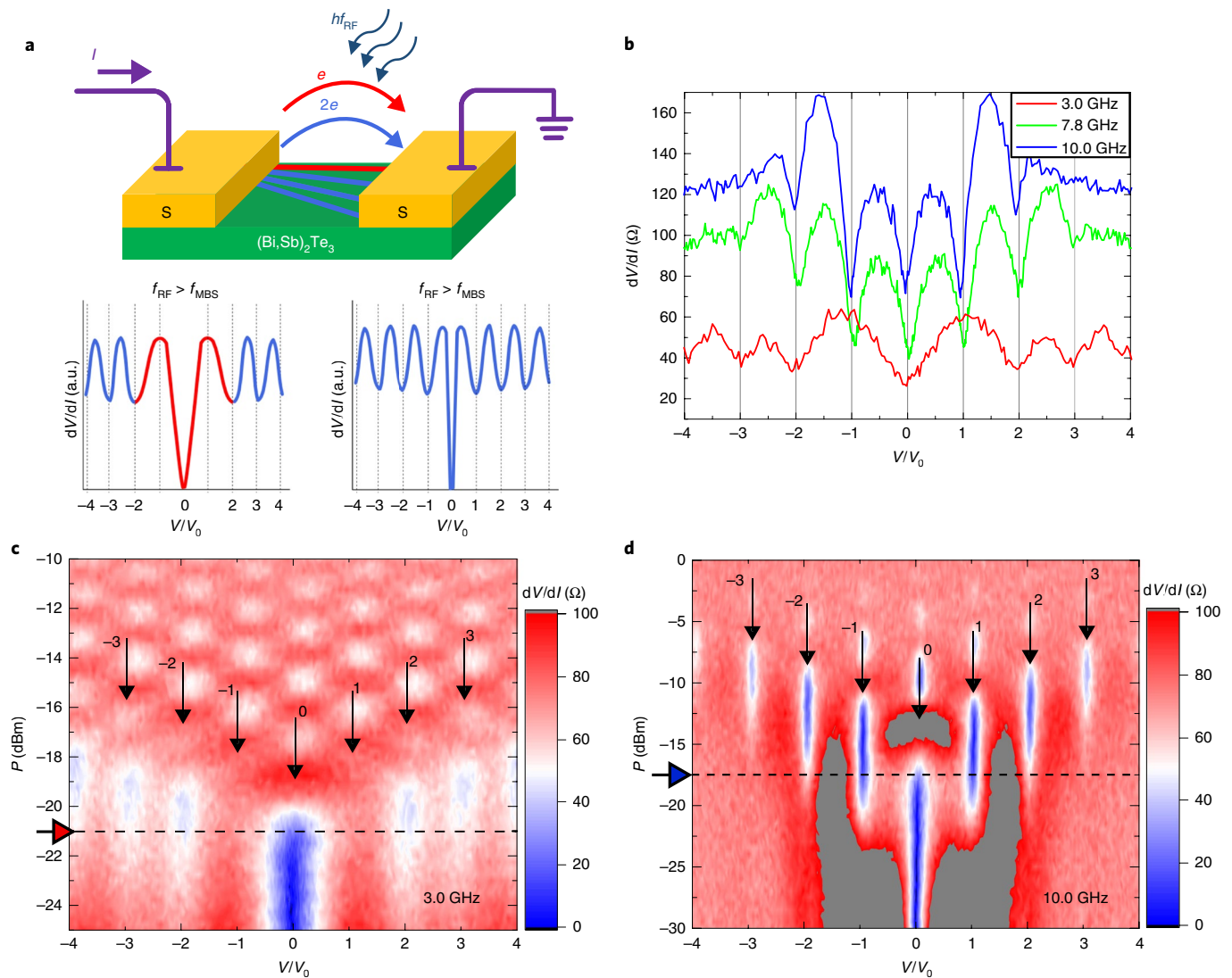
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Fig. 3 | Frequency dependency of Shapiro response of device 1 at $T = 1.5$ K. a, Schematic experimental set up with a Shapiro response at f_{RF} below and above the characteristic Majorana frequency (f_{MBS}). For $f_{RF} < f_{MBS}$ (bottom left), the first Shapiro dip ($n = \pm1$) is suppressed. For high excitation frequencies ($f_{RF} > f_{MBS}$ (bottom right)), the first dip should reappear. **b**, dV/dI–V/V_0 for 3.0, 7.8 and 10.0 GHz. The first minimum in dV/dI evolves as a function of frequency. For the sake of clarity, the line scans are shifted. **c**, dV/dI–V/V_0–P for $f_{RF} = 3.0$ GHz. The first step is fully suppressed for all the available power levels. **d**, dV/dI–V/V_0–P for $f_{RF} = 10.0$ GHz. The first step is fully resolved for the range -21 dBm $< P < -11$ dBm. Note that the blue and red line scans in **b** are extracted from **c** and **d** at the indicated power levels (dashed lines).

differential resistance dV/dI–V/V_0 was measured (Fig. 3b). Shapiro dips appear in dV/dI measurements at the energy of Shapiro steps. However, Shapiro dips have a higher sensitivity at this temperature range compared to Shapiro steps.

Pseudo four-terminal measurements were again performed as shown in Fig. 2d. Both d.c. voltage and differential resistance were measured as a function of bias current. Additionally, an RF antenna was mounted above the chip to irradiate the JJs (Fig. 3a). For $f_{RF} = 10.0$ GHz, Shapiro dips evolve at integer multiples of the characteristic voltage $V_0 = h \times 10.0$ GHz$/2e$. In the blue line scan in Fig. 3b, which was extracted from the P–dV/dI map (Fig. 3d) at $P = -17.5$ dBm, the first two Shapiro dips are clearly visible as local minima in the dV/dI curve. Note that the RF source was not calibrated and signals could only be attenuated relatively to the unattenuated signal. For 10 GHz and 7.8 GHz, the first Shapiro dip is clearly visible. For 3.0 GHz, however, we observed a fully suppressed first Shapiro dip (red line scan in Fig. 3b), as is expected for low excitation frequencies (Fig. 3a). The suppression of the first Shapiro dip

persists for the whole power spectrum, as indicated by the P–dV/dI maps (Fig. 3c). This observation is consistent with measurements on device 2 (Supplementary Fig. 8).

In both JJs, a fully suppressed first Shapiro dip at low frequencies was measured, whereas for higher frequencies all the Shapiro dips were observed. The full suppression of the first Shapiro dip as a function of frequency provides some evidence for MBS. The presented findings are in accordance with theoretical predictions[19,21] and reports on other topological JJs[21,23,24]. Following the analysis of Wiedenmann et al.[23], for a crossover frequency of 4 GHz, and an $I_C R_N$ value of about 0.3 meV, one can deduce the potential Majorana contribution to the supercurrent in device 2, which amounts to ~320 nA. In device 1, the potential Majorana contribution only amounts to ~160 nA due to a smaller induced gap, a slightly higher normal resistance and a lower crossover frequency. To further investigate elusive Majorana modes and to demonstrate their non-Abelian exchange statistics, more elaborate devices are required[6,7,12,13,15].
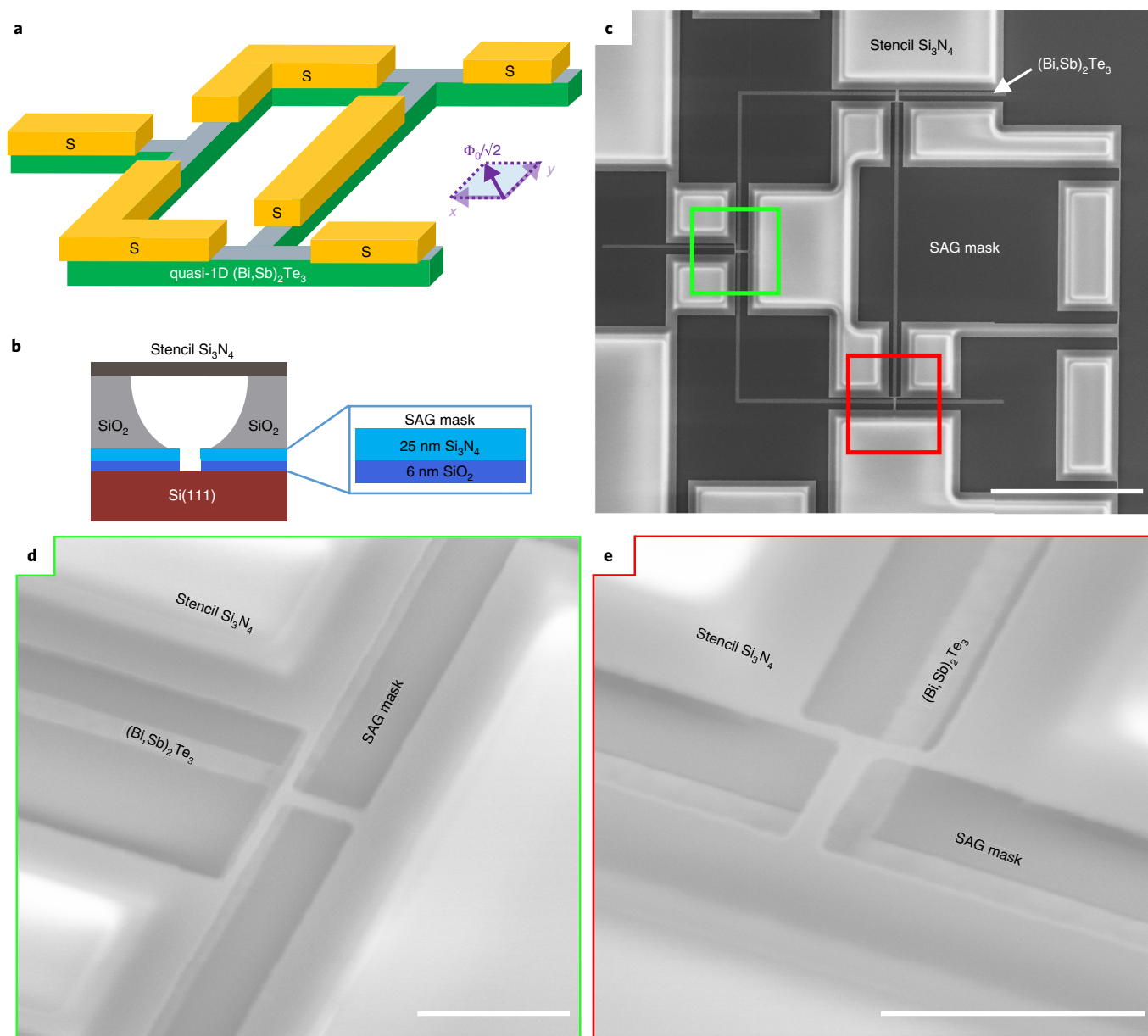
Fig. 4 | To employ the stencil technology to networks of nanostructures, the growth of TI has to be restricted to selected areas only. a, Schematic of a proposed S–TI hybrid network for topological quantum computation[15]. The purple arrows define the superposition of the x and y directions, in which a magnetic flux of $_0/\sqrt{2}$ needs to be applied to turn the quasi-1D TI network (green) into the topological regime[7]. **b**, SAG can be achieved by inserting a second SiO_2/Si_3N_4 mask underneath the stencil mask (blue colours). By patterning the SAG mask via reactive ion etching, it is possible to restrict the TI growth on top of the Si(111) surface to well-defined nanostructures. **c**, Scanning electron microscopy image of the TI network demonstrated in **a** after TI deposition. The micrometre-long trenches are continuously and homogenously filled. Scale bar, 10 μm. **d**, Close-up of the green frame in **c**. Underneath the T-shaped stencil bridge the thin films homogeneously coalesce (60° tilted view). **e**, Close-up of the red frame in **c** (60° tilted view). Scale bars (**d** and **e**), 1 μm.

Networks of hybrid nanostructures

To apply the stencil lithography to more complex layouts, it was useful to define the dimensions of the TI films independently from the shape of the stencil mask for subsequent electrode deposition. As the electrodes and capping layer needed to be defined in situ, the structuring of the TI thin film had to be performed under ultrahigh vacuum conditions as well. In Fig. 2b, the TI film only nucleated on the Si(111) surface, and not on top of the Si_3N_4 stencil mask. By inserting a second mask, which comprised an additional SiO_2 (6 nm) + Si_3N_4 (25 nm) layer stack (blue in Fig. 4b) between the Si(111) and the sacrificial SiO_2 layer of the stencil mask, it was possible to restrict the TI

growth to well-defined nanostructures. Importantly, the top layer of the mask for SAG was Si_3N_4 to preserve the shape of the nanostructures during the release of the stencil mask in hydrofluoric acid. The lower SiO_2 layer was intended to reduce possible strain defects in the silicon induced by the tensile stress in the SAG Si_3N_4 (ref. [34]). On the as-prepared substrates, TI only nucleated on the exposed Si(111) surface. This allows for the in situ fabrication of precisely defined TI networks. In a second in situ fabrication step, the stencil mask made it possible to deposit superconductive islands to selected parts of the network. Finally, all the devices on the chip were conserved with a global dielectric capping layer.
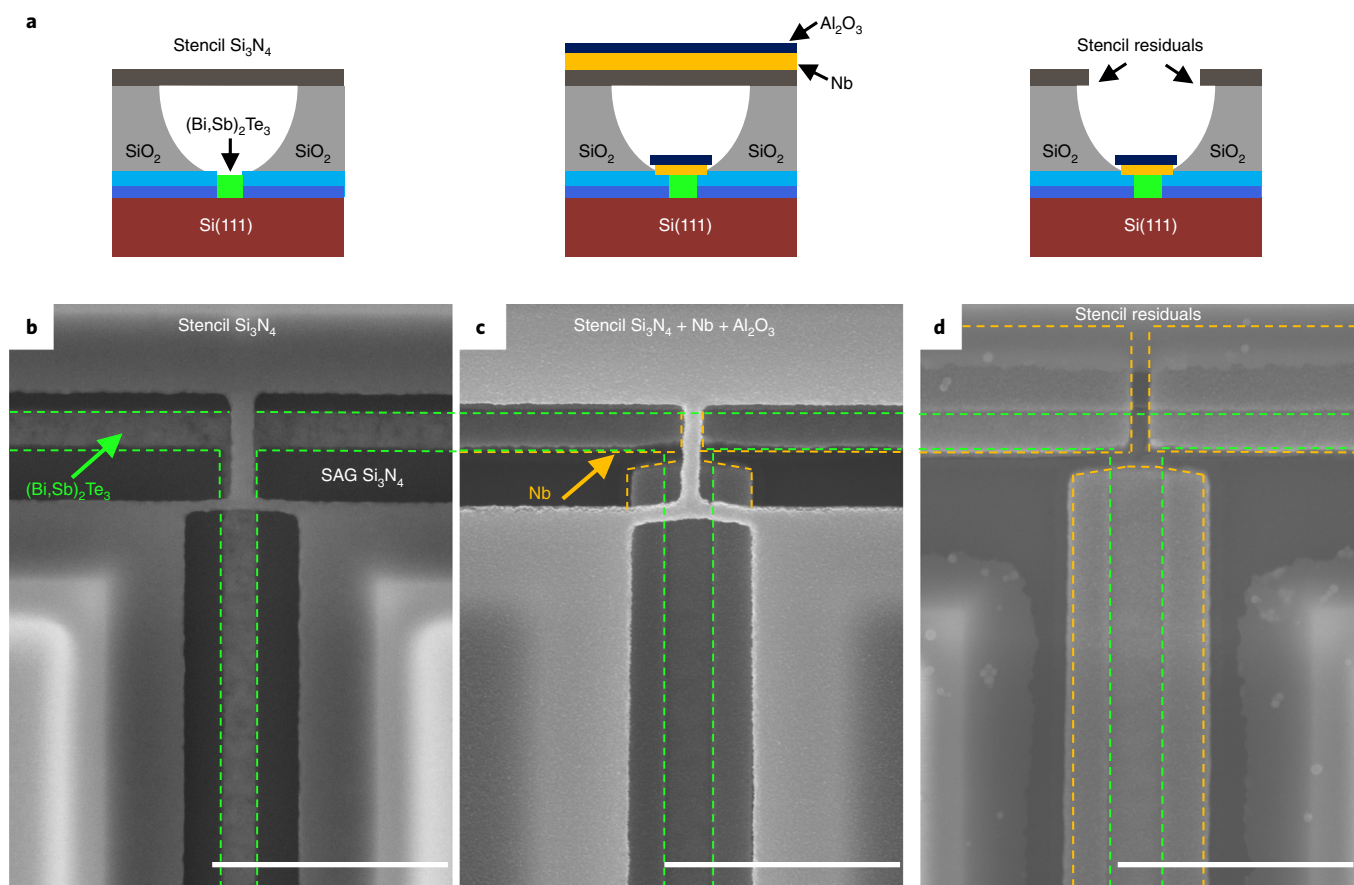
Fig. 5 | Combined in situ process. a, Schematic of the process flow. **b**, SAG of a confined TI T-junction (green dashed area). **c**, Stencil lithography of the superconductive electrodes (yellow dashed areas) and passivation by a global Al_2O_3 capping layer. **d**, Removal of Nb and Al_2O_3 on top of the stencil mask to make the as-prepared chips accessible for external magnetic fields. Scale bars, 1 μm.

To demonstrate the working principle of the combined process as well as its scalability and flexibility, we fabricated a theoretically proposed mock device of an S–TI network for topological qubits (Fig. 4a). However, for an operational device one needs to adjust the layout and materials. At this stage, the residual bulk contributions in $(Bi_{0.06}Sb_{0.94})_2Te_3$ and quasiparticle poisoning in Nb are detrimental to the as-proposed devices. Here, the S–TI hybrid layout was chosen to demonstrate the high potential of SAG and stencil lithography for future topological quantum computing architectures. In Fig. 4c, we show that the TI grew selectively in wire-like structures. The predefined, micrometre-long nanotrenches were filled homogeneously, but nucleation took place neither on top of the exposed SAG mask nor on the stencil mask. Underneath the free-standing bridges, the TI coalesces and forms T-junctions, as can be seen in the scanning electron microscopy images (Fig. 4d,e). The orthogonal alignment of the nanostructures and their well-defined cross-section should allow for turning all the arms into a topological regime by applying a global in-plane magnetic field to the chip[35], which is mandatory to create localized Majorana zero modes at the ends of quasi-1D hybrid devices[7].

After the SAG of TI thin films under substrate rotation (Fig. 5b), Nb was deposited via molecular-beam epitaxy without rotation to yield precisely defined superconductive islands well-aligned to the $(Bi_{0.06}Sb_{0.94})_2Te_3$ network (Fig. 5c). As Nb and the final Al_2O_3 capping do not grow selectively, the stencil mask was completely covered with these materials. Nb shows a diamagnetic behaviour at low temperatures and should therefore be removed from the

stencil mask via mechanical polishing (Fig. 5d). Owing to the global capping layer, further ex situ fabrication (such as the implementation of a gate or flux control) can be performed without risking any exposure of the TI to ambient conditions (Supplementary Fig. 1).

Conclusion

Here, we present a new platform for the scalable in situ fabrication of S–TI hybrid devices. The combination of molecular-beam epitaxy, SAG and stencil lithography allows for a full device fabrication under ultrahigh vacuum conditions. Attaching a stencil mask at a well-defined distance from the substrate surface enabled us to fabricate superconducting Nb electrodes with nanometre precision on top of $(Bi_{0.06}Sb_{0.94})_2Te_3$. In the as-prepared JJs, we observed a missing first Shapiro step, which indicates the presence of MBS. The key towards achieving the Majorana regime in (Bi,Sb)-based TIs is highly transparent interfaces and an in situ capped weak link. By implementing an additional mask between the Si substrate and stencil mask, it was possible to restrict the TI growth to selected areas with dimensions and alignment accuracy at the nanoscale, which makes it possible to transfer pristine interface quality and in situ capping layers to complex quantum devices. To employ this technology for topological qubits, it is mandatory to replace $(Bi_{0.06}Sb_{0.94})_2Te_3$ by a bulk insulating $Bi_{2-x}Sb_xTe_{3-y}Se_y$ compound[36] and to implement a parity-conserving superconductor, such as NbTiN (ref. [37]) that does not create an interdiffusion barrier at the interface to (Bi,Sb)-based TIs, as observed for Al (ref. [38]). In general, the presented in situ technology can be applied to any quantum material

that can be grown selectively, such as InSb (ref. [39]) or InAs (refs [40,41]), and to any electrode material that can be deposited directionally (for example, via molecular-beam epitaxy).

Online content

Any methods, additional references, Nature Research reporting summaries, source data, statements of code and data availability and associated accession codes are available at https://doi.org/10.1038/s41565-019-0506-y.

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Author contributions

P.S., D.R., T.W.S., M.S. and E.B. fabricated the substrates in the clean room. S.T. performed electron-beam lithography. P.S., M.S., A.R.J., S.S., M.W. and G.M. grew the TI thin films via MBE. B.B. grew the superconducting Nb. U.P. capped the sample with stoichiometric Al_2O_3. P.S., D.R., C.L. and T.W.S. performed the electrical transport measurements on Josephson devices. D.R. and J.K. investigated the magnetotransport on Hall bars. T.G. removed the stencil mask via mechanical polishing. L.K., D.M. and M.L. prepared the focused ion-beam lamellae and performed high-resolution scanning transmission electron microscopy measurements. A.B. and A.A.G. carried out the Eilenberger and Usadel fitting. P.S., D.R. and A.B. wrote the paper with contributions from all the co-authors. P.S. initiated the project, which was supervised by N.T., A.A.G., A.B., T.S. and D.G.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information is available for this paper at https://doi.org/10.1038/s41565-019-0506-y.

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Peer review information: *Nature Nanotechnology* thanks Torsten Karzig and other, anonymous, reviewer(s) for their contribution to the peer review of this work.

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Methods

A 4″ n-type Si(111) substrate (>2,000 Ω cm) was wet chemically cleaned by an RCA HF-last procedure[42] before deposition of 300 nm of SiO_2 and 100 nm of Si_3N_4 in a Centrotherm LPCVD System E1200 R&D furnace for stencil mask fabrication. In the next step, the top Si_3N_4 layer was patterned via electron-beam lithography and removed via reactive ion etching. In this manner, the electrode pattern was defined in the Si_3N_4 layer. Dipping the chip for 15 min in 1% hydrofluoric acid removed the exposed SiO_2 isotropically, which released the freestanding Si_3N_4 bridges at a height of 300 nm above the substrate.

Additionally, the dip in 1% hydrofluoric acid passivated the surface dangling bonds of the Si(111) substrate during the handling prior to loading it in the molecular-beam epitaxy (MBE) growth chamber[42]. The hydrogen passivation was removed from inside the MBE chamber by keeping the substrate at $T_{sub} = 700\,°C$ for 20 min under ultrahigh vacuum conditions, which restored a pristine Si(111) surface. A $(Bi_{0.06}Sb_{0.94})_2Te_3$ thin film was grown in a Te-overpressure regime, following the recipe of Kellner et al.[43]. At $T_{sub} = 280\,°C$, the TI nucleates on the pristine Si(111) surface, but not on the amorphous Si_3N_4 mask. The molecular flux impinges at the substrate under a polar angle of 32.5°. The diffusion of adatoms and the steady substrate rotation ($10\,min^{-1}$) makes the TI grow homogeneously underneath the freestanding bridges.

For the deposition of the superconductive electrodes, the chip was transferred via a portable vacuum chamber to a MBE cluster with the maximum pressure kept below $10^{-8}\,mbar$. Superconducting Nb was deposited in a metal MBE chamber by using an electron-beam evaporator (MBE-Komponenten EBVM 250-4×8-S) under a polar angle of 32.5°, but without substrate rotation. For the deposition of the Al_2O_3 capping layer the chip was transferred under ultrahigh vacuum conditions to the metal oxide MBE chamber. Al_2O_3 was deposited under substrate rotation by electron-beam evaporation (MBE-Komponenten EBVM 250-6×8-S) from a stoichiometric target. The growth rates for the Al_2O_3 and Nb were set to $1\,Å\,s^{-1}$, respectively. The metal chamber and metal oxide chamber are part of one multichamber MBE cluster tool.

Low-temperature transport experiments were carried out in an Oxford Triton 500 system with a base temperature of 12 mK.

Structural investigations on the atomic scale were performed with an aberration-corrected high-resolution STEM (FEI Titan 80–300[44]). Specimens were prepared by focused ion-beam etching using, first, 30 keV Ga ions followed by a 5 keV final treatment. Ar ion milling with the NanoMill operated at 900 V and subsequently at 500 V was employed to reduce the surface damage introduced by the focused ion beam.

For the SAG mask fabrication, 6 nm of SiO_2 were thermally generated in a Tempress oxidation furnace and the SAG Si_3N_4 was deposited in the Centrotherm LPCVD System E1200 R&D furnace. Depth markers were subsequently defined via reactive ion etching to make it possible to align the stencil mask with an accuracy of ±2.5 nm with respect to the layout of the underlying SAG mask during further fabrication processes. To assure a smooth top stencil nitride layer, 500 nm of sacrificial SiO_2 instead of 300 nm were deposited. In a subsequent chemical mechanical polishing step, the 500 nm of SiO_2 were thinned down to 300 nm of SiO_2 to assure a smooth oxide topography above the buried nanostructures in the SAG mask. Finally, 100 nm of Si_3N_4 were globally deposited on top and structured, as described above.

To remove the Nb on top of the stencil mask after the deposition of topological, superconductive and dielectric thin films, the chip was polished. To avoid any etching effects, the slurry used during the polishing did not contain any chemically active components. Furthermore, a thin resist layer was applied to the chip beforehand to protect the S–TI devices from the polishing slurry.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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