Experimental Demonstration of Memristor-Aided Logic (MAGIC) Using Valence Change Memory (VCM)

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***Abstract*— Memristor-aided logic (MAGIC) is a technique for performing in-memory computing using memristive devices. The design of a MAGIC NOR gate has been described in detail, and it serves as the basic building block for several processing-in-memory architectures. However, the input stability of the MAGIC NOR gate forces a limitation on the threshold voltages: the magnitude of the set voltage must be higher than the magnitude of the reset voltage. Unfortunately, many of the current leading resistive switching technologies, particularly, valence change memory (VCM), have the opposite ratio between the threshold voltages. In this article, we experimentally demonstrate the undesirable effects of input instability. Furthermore, we introduce three new MAGIC gates for devices with low set-to-reset voltage ratios and experimentally demonstrate their robust operation using Pt/Ta_2O_5/W/Pt devices. The three gates, combined with constant values, are functionally complete and are demonstrated as building blocks for in-memory logic on VCM devices.**

***Index Terms*— Logic-in-memory, memristor, memristor-aided logic (MAGIC), processing-in-memory (PIM), valence change memory (VCM).**

I. Introduction

MEMRISTIVE devices have attracted much attention, in the context of both future nonvolatile memories, as well as computation-in-memory [1]–[4]. For binary storage and computing using memristive devices, the logical states are represented by two resistive states. Generally, the high resistive state R_{OFF} is considered as logical '0' ("OFF") and the low resistive state R_{ON} as logical '1' ("ON"). To switch between the states, a voltage pulse is applied across the device; V_{SET} is used to switch from OFF to ON and V_{RESET} from ON to OFF. In bipolar devices, the polarity of these voltages is opposite. In this article, we refer to V_{SET} as a negative voltage and V_{RESET} as a positive one.

Stateful logic [4] is a computation-in-memory technique, in which the data stored in the memristors, represented by their logical state, is used as input and the result is written to an output memristor as a logical state. Examples of such logic families include material implication (IMPLY) [5] and memristor-aided logic (MAGIC) [6], [7]. In the MAGIC family, unlike IMPLY logic, memristors for the input and output are separated, the output is written to a dedicated memristor, and there are no additional devices in the periphery. The MAGIC architecture is therefore, preferable over IMPLY logic in terms of area, latency, and energy [8]. Furthermore, the crossbar-compatible MAGIC NOR gate is considered a promising building block for processing-in-memory (PIM) architectures [9]–[12].

To the best of our knowledge, the MAGIC NOR gate, as opposed to the IMPLY logic gate [13]–[15], has only been experimentally demonstrated on exotic polymer-resistive devices [16]–[18]. Yet, these devices are not compatible with complementary metal–oxide–semiconductor (CMOS) processes.

Valence change memory (VCM) [19] is a category of CMOS-compatible bipolar-resistive switching devices, which use transition metal oxides as the insulating material, e.g., TiO_2 [20], HfO_2 [21], [22], or Ta_2O_5 [23]–[26], combined with asymmetric electrodes. Specifically, Ta_2O_5-based devices are considered as a promising resistive technology because of their fast switching speed [23], relatively high endurance [24], and long retention properties [25]. However, to prevent overwrite of inputs in the MAGIC NOR gate, the magnitude of the set voltage should be at least twice the magnitude of the reset voltage. Yet, many VCM devices exhibit low set-to-reset voltage ratios.ł

In this article, we describe and experimentally demonstrate the obstacles in executing MAGIC NOR using VCM. Then, we propose adding three new logic gates to the MAGIC family. We describe the design methodology, and explain how these gates ensure input stability for devices with low set-to-reset

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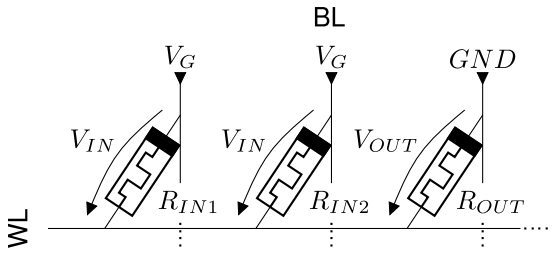


Fig. 1. Schematic of a two-input MAGIC gate within a crossbar. According to the passive sign convention, V_{OUT} has the same sign as V_G, while V_{IN} has the opposite sign.

voltage ratios. Finally, we experimentally demonstrate, using Ta_2O_5-based memristive devices, that the new gates produce correct and reproducible results. Additionally, we demonstrate more complex logic operations, such as half adders, using the proposed gates as building blocks.

II. Memristor-Aided Logic

MAGIC [6] is a family of stateful memristive logic gates. A two-input MAGIC gate consists of two input memristors (IN1, IN2), connected in parallel, and an additional memristor (OUT) for the output. A schematic of a two-input gate is shown in Fig. 1. The operation of a MAGIC gate consists of two sequential steps. The first step initializes the output memristor to a known logical state. In the second step, a voltage V_G is applied across the logic gate. While applying V_G, the voltage across the output memristor depends on the logical states of the input and output memristors (i.e., a voltage divider). For specific input combinations, the voltage across the output memristor is sufficiently high to change its logical state, whereas, for other input combinations, the voltage across the output is relatively low and its logical state remains at the initialized state.

A. MAGIC NOR

Since NOR is functionally complete and MAGIC NOR can be easily mapped to a crossbar array, the MAGIC NOR gate was originally proposed as the basic building block for implementing in-memory logic in memristive memory processing units (mMPU) [27]. The initial execution step includes setting the output memristor to R_{ON}. Then, evaluation is achieved by grounding the OUT bitline and applying a voltage pulse V_G at the bitlines of the input memristors (for simplicity, the wire resistance is neglected in the following calculations).

In the evaluation step, the voltage on the output cell is the result of a voltage divider between the input cells and the output cell

$$V_{OUT}(\text{IN1,IN2}) = V_G \cdot \frac{R_{ON}}{R_{IN1}||R_{IN2} + R_{ON}}. \quad (1)$$

Assume $R_{OFF} \gg R_{ON}$ (at least one order of magnitude), to switch the output in all cases, except for the (IN1=IN2='0') case, V_G must be greater or equal to $2|V_{RESET}|$. Table I lists the voltages across the output for each input combination, when selecting $V_G = 2|V_{RESET}|$. This dictates the functionality of a NOR gate.

B. Input Stability

Another constraint of the gate is input stability. Table I lists the voltages across the input and output memristors for each input combination. It demonstrates that the voltage across the input memristors is not negligible and may unintentionally change their logical state during the logical operation. Since the voltage polarity of the inputs is opposite to the voltage polarity of the output, when a reset event is targeted on the output, we risk triggering a set event on the inputs. This leads to the following device parameters condition to ensure input stability:

$$\left|\frac{V_{SET}}{V_{RESET}}\right| > 2. \quad (2)$$

While this condition can be extended for an n-input MAGIC NOR gate:

$$\left|\frac{V_{SET}}{V_{RESET}}\right| > \frac{1 + \frac{1}{1+\frac{R_{ON}}{R_{OFF}}\cdot(n-1)}}{1 + \frac{R_{ON}}{R_{OFF}} \cdot n} \quad (3)$$

correct logic implementation requires that $R_{ON} \ll (R_{OFF}/n)$, which reduces (3) to approximately (2). It is noted that other gates based on the same principle of conditional reset switching, e.g., NOT [6], NAND [7], and minority logic function (MIN) [28], have a more relaxed condition on the set-to-reset voltage ratio, but still require $|V_{RESET}| < |V_{SET}|$.

Originally, this condition was described to prevent destructive input operation and not for the functionality of the gate operation itself [6], [7]. Table II lists different popular VCM memristive devices and demonstrates that they do not sustain the MAGIC NOR condition for input stability. A recent study simulated MAGIC NOR with set/reset voltage pairs that do

TABLE I
Input and Output Voltages for the MAGIC NOR Gate

State		Voltage	
R_{IN1}	R_{IN2}	V_{IN}	V_{OUT}
R_{OFF} ('0')	R_{OFF} ('0')	$-2\|V_{RESET}\|$	$0V$
R_{OFF} ('0')	R_{ON} ('1')	$-\|V_{RESET}\|$	$\|V_{RESET}\|$
R_{ON} ('1')	R_{OFF} ('0')	$-\|V_{RESET}\|$	$\|V_{RESET}\|$
R_{ON} ('1')	R_{ON} ('1')	$-\frac{2}{3}\|V_{RESET}\|$	$\frac{4}{3}\|V_{RESET}\|$

TABLE II
VCM Devices Comparison

Device	$\left\|\frac{V_{SET}}{V_{RESET}}\right\|$	$\frac{R_{OFF}}{R_{ON}}$	Reference
Pt/Ti/TiO_2/TiN	0.6	10	[20]
TiN/HfO_2/Ti/TiN	0.25-1	-	[21]
Pt/HfO_2/TiN	1-1.3	10^2	[22]
Pt/Ta_2O_{5-x}/TaO_{2-x}/Pt	0.5	10	[24]
Pt/Ta_2O_5/Ta/Pt	0.3-0.6	10-10^2	[26]
Pt/Ta_2O_5/W/Pt	0.4-0.6	10-10^3	[26]

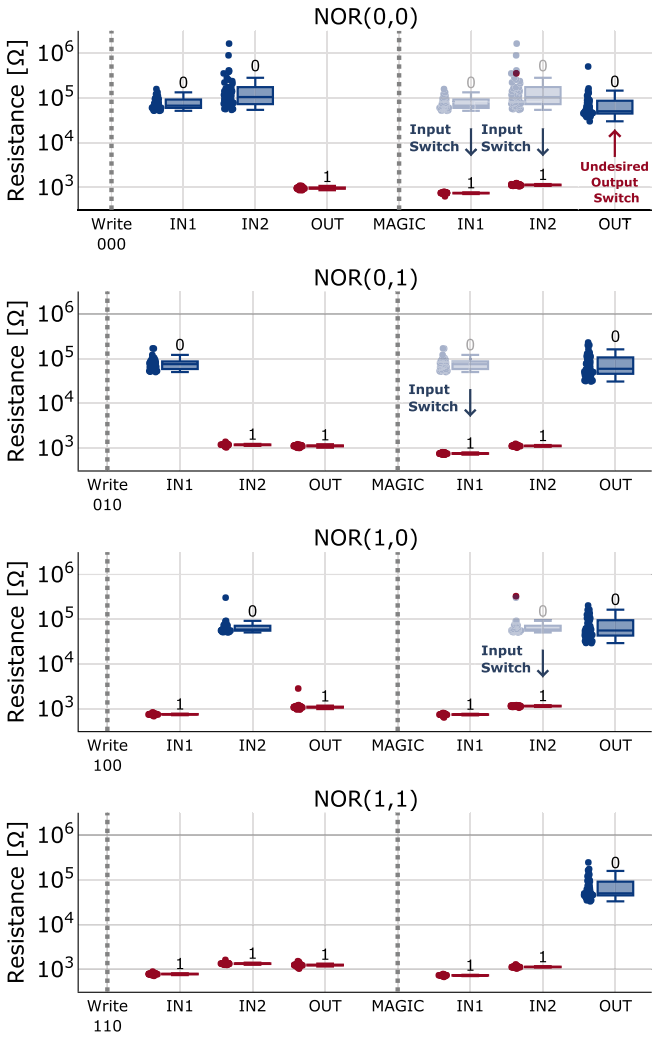


Fig. 2. Results of 50 cycles of MAGIC NOR attempts measured on the fabricated VCM devices. For the NOR(0, 0) case, due to input instability, the inputs switch, resulting an undesired output switch.

not fulfill the condition for input stability [29]. It discussed the fact that input stability is critical, since changing the inputs means that, eventually, the output will also change. The authors suggested solving this issue by finding a pulse length that is sufficiently long to switch the output for the desired cases, but short enough to prevent unintended switching for the (IN1=IN2='0') case. While they succeeded in simulating this for a single gate, they eventually concluded that to execute MAGIC NOR in a crossbar array, a device with $|V_{\mathrm{RESET}}| \ll |V_{\mathrm{SET}}|$ is needed. Furthermore, in our view, basing the functionality of the gate on fine-timing of the pulse length is impractical for real devices because of cycle-to-cycle variations in the switching time between states.

We conducted several experiments with fabricated VCM devices, and concluded that input stability is critical for proper logic operation. For successful logic operation of the MAGIC NOR gate, we were interested in switching the output in all input states, except the (IN1=IN2='0') case. Unfortunately, as can be seen from the results in Fig. 2, the output switched for all possible states of the inputs, including the (IN1=IN2='0') case, resulting in logical failure. The complete experimental setup is detailed in Section IV.

The instability of the inputs was dominant when the two inputs are initially in the R_{OFF} state. Furthermore, for almost all the cycles, if an input was in the R_{OFF} state, it switched to R_{ON}. These results can be explained by the voltage across the input cells, which was above the set threshold. This instability of the input cells can further explain the logical failure of the MAGIC NOR gate. For the (IN1=IN2='0') state, the voltage across the output cell is lower than the reset threshold, but the voltage across the inputs is higher than the set threshold. This causes a switching event on the inputs. After the input is switched, the state of the gate is effectively in a different input combination. Then, the voltage across the output cell is greater than the reset threshold, causing an undesired switching of the output. Logically, we can think about it as if we moved from one row of the truth table to another.

Considering these experimental results, we conclude that to support computation using VCM memristive devices, new MAGIC gates that support the set-to-reset ratio of VCM devices are required. In Section III, we propose three gates that fit the VCM properties and are compatible within a memristive crossbar array.

III. New MAGIC Gates

A. MAGIC OR

The same structure of a two-input MAGIC, as shown in Fig. 1, can be used to implement different logic gates [7]. Herein, we propose a MAGIC OR gate. First, the output memristor is initialized to R_{OFF} (rather than R_{ON} in NOR). Hence, a set event on the output is targeted, as opposed to a reset event in MAGIC NOR. To support this, a negative V_{G} is used. In the evaluation step, the voltage across the output is

$$V_{\mathrm{OUT}}(\mathrm{IN1},\mathrm{IN2}) = V_{\mathrm{G}} \cdot \frac{R_{\mathrm{OFF}}}{R_{\mathrm{IN1}} || R_{\mathrm{IN2}} + R_{\mathrm{OFF}}}. \tag{4}$$

Assume $R_{\mathrm{OFF}} \gg R_{\mathrm{ON}}$, by setting $V_{\mathrm{G}} \approx -|V_{\mathrm{SET}}|$, we maintain the output in R_{OFF} for the (IN1=IN2='0') case, and switch it to R_{ON} for any other input combination. This gives the desired functionality of an OR gate.

The voltages across inputs and output for the MAGIC OR gate are listed in Table III. The voltage across the inputs is always approximately 0 V, except for the (IN1=IN2='0') case, where the inputs are already in the R_{OFF} state. Hence, input stability is guaranteed and, in terms of functionality, the MAGIC OR gate can be performed without any limitation on the set-to-reset voltage ratio of the device.

Nevertheless, for the cases where the output switches to R_{ON}, the amplitude of the voltage across the inputs increases during the operation. Therefore, if we want to guarantee a nondestructive operation and keep the inputs unchanged even after the output switched to R_{ON}, the threshold voltages should fulfill the following condition:

$$\left| \frac{V_{\mathrm{SET}}}{V_{\mathrm{RESET}}} \right| < 2 \tag{5}$$

since once the output has completed the switch to R_{ON}, the maximum voltage across the inputs is half of the applied voltage. It is noted that all the devices listed in Table II fulfill this condition.

If we extend these results for an n-input MAGIC OR gate, we get similar results. Before the output is switched,

TABLE III
INPUT AND OUTPUT VOLTAGES FOR THE MAGIC OR GATE

State		Voltage	
R_{IN1}	R_{IN2}	V_{IN}	V_{OUT}
R_{OFF} ('0')	R_{OFF} ('0')	$\frac{1}{3}\|V_{SET}\|$	$-\frac{2}{3}\|V_{SET}\|$
R_{OFF} ('0')	R_{ON} ('1')	$0V$	$-\|V_{SET}\|$
R_{ON} ('1')	R_{OFF} ('0')	$0V$	$-\|V_{SET}\|$
R_{ON} ('1')	R_{ON} ('1')	$0V$	$-\|V_{SET}\|$

the voltage across the inputs is always approximately 0 V, except for the case where all the inputs are in the R_{OFF} state. After switching, the maximum voltage across the inputs is half of the applied voltage.

B. MAGIC NIMP

Enabling MAGIC OR is still insufficient for in-memory logic, since it is not functionally complete. To support (partially) complete logic, we introduce another MAGIC gate by breaking the symmetry between the two inputs, as shown in Fig. 3.

The output cell is initialized to R_{OFF}, and in the evaluation step, V_{G} is applied to the bitline of one of the inputs, while αV_{G} $(0 < \alpha < 1)$ is applied to the bitline of the other input. The voltage across the output during the evaluation step is

$$V_{\text{OUT}}(\text{IN1,IN2}) = V_{\text{G}} \cdot \frac{R_{\text{IN2}}||R_{\text{OFF}}}{R_{\text{IN2}}||R_{\text{OFF}} + R_{\text{IN1}}} + \alpha V_{\text{G}} \cdot \frac{R_{\text{IN1}}||R_{\text{OFF}}}{R_{\text{IN1}}||R_{\text{OFF}} + R_{\text{IN2}}}. \quad (6)$$

Assume $R_{\text{OFF}} \gg R_{\text{ON}}$, by setting $V_G \approx -|V_{\text{SET}}|$, switching is achieved only in the (IN1='1', IN2='0') case, resulting in the not implication (NIMP) operation.

The NIMP logic operation has previously been suggested for memristive crossbars, using a crossbar structure with a resistor in the periphery. Chen *et al.* [30] proposed a two-memristor version, where the output overwrites one of the inputs. It was simulated and used sequentially to implement more complex logic operations [31]. Kim and Williams [32] demonstrated a three-memristor, nondestructive version. The peripheral resistor was left floating, so, essentially, the gate functionality is similar to ours.

The factored voltage, αV_{G}, gives some degree of freedom for gate implementation. To minimize errors, the voltage on the output should be minimal for all non-switching cases. At the same time, to ensure input stability, the voltage across the inputs should be minimal, for all input combinations. The maximum voltage across the output, for all non-switching cases, is given by the (IN1=IN2='1') case. The maximum voltage across the inputs, that can cause input switching, is the voltage across IN2 for the (IN1='1,' IN2='0') case. Since α has an opposite effect on the magnitude of these voltages, we select $\alpha = \frac{1}{3}$, their equality point.

The voltages across inputs and output for the MAGIC NIMP gate are listed in Table IV. The (IN1=IN2='1') input case

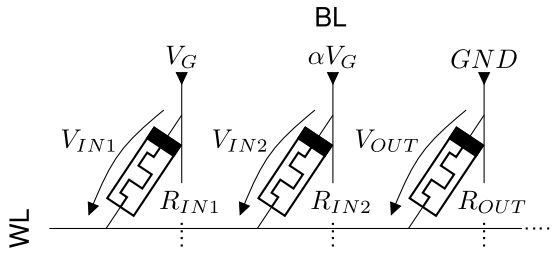


Fig. 3. Schematic of a MAGIC NIMP gate within a crossbar.

TABLE IV
INPUT AND OUTPUT VOLTAGES FOR THE MAGIC NIMP GATE

State		Voltage		
R_{IN1}	R_{IN2}	V_{IN1}	V_{IN2}	V_{OUT}
R_{OFF} ('0')	R_{OFF} ('0')	$\frac{5}{9}\|V_{SET}\|$	$-\frac{1}{9}\|V_{SET}\|$	$-\frac{4}{9}\|V_{SET}\|$
R_{OFF} ('0')	R_{ON} ('1')	$\frac{2}{3}\|V_{SET}\|$	$0V$	$-\frac{1}{3}\|V_{SET}\|$
R_{ON} ('1')	R_{OFF} ('0')	$0V$	$-\frac{2}{3}\|V_{SET}\|$	$-\|V_{SET}\|$
R_{ON} ('1')	R_{ON} ('1')	$\frac{1}{3}\|V_{SET}\|$	$-\frac{1}{3}\|V_{SET}\|$	$-\frac{2}{3}\|V_{SET}\|$

forces the following condition on the threshold voltages:

$$\left|\frac{V_{\text{SET}}}{V_{\text{RESET}}}\right| < 3. \quad (7)$$

Therefore, the MAGIC NIMP gate can be implemented on devices with low set-to-reset voltage ratios. For the (IN1='1', IN2='0') input case, since the output is being switched, the voltage across the inputs changes during the operation. To guarantee a nondestructive operation, and keep the inputs unchanged, even after the output switched to R_{ON}, the threshold voltages should fulfill the same condition in (5).

C. Two-Cycle MAGIC XOR

In the MAGIC NIMP gate design, we initialized the output to R_{OFF}, and targeted a set event. If the output is not initialized, and is already in R_{ON}, a MAGIC NIMP operation will not affect its state. Namely, if we apply subsequent operations on the same output, without an initialization cycle between them, we gain an OR operation between these operations. Thus, we can create a two-cycle XOR logic gate, by running the NIMP operation twice, according to the following steps.

1) Initialize the output memristor to R_{OFF}.
2) Apply $-|V_{\text{SET}}|$ on IN1 bitline, $-\frac{1}{3}|V_{\text{SET}}|$ on IN2 bitline, and ground OUT bitline.
3) Apply $-\frac{1}{3}|V_{\text{SET}}|$ on IN1 bitline, $-|V_{\text{SET}}|$ on IN2 bitline, and ground OUT bitline.

The results of these steps are presented for each input case in Table V, which corresponds to the truth table of a XOR gate.

D. Crossbar Compatibility

The structure of the proposed MAGIC gates is compatible with the standard memristive memory crossbar array. To reliably perform computation within the crossbar array, a voltage isolation scheme is required to lower the sneak-path current and the write-disturb phenomena [8]. For MAGIC operations,

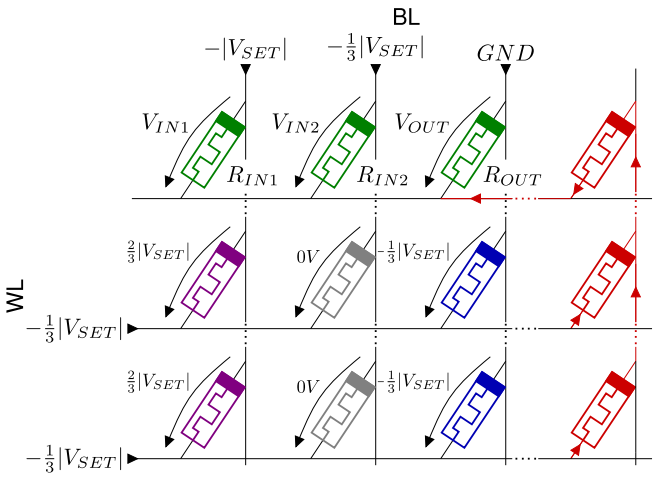


Fig. 4. MAGIC NIMP within a crossbar array. Cells participating in the logic operation are marked in green. Unselected cells with a constant voltage drop of $-\frac{1}{3}|V_{SET}|$, $\frac{2}{3}|V_{SET}|$ and 0 V are marked in blue, purple and gray, respectively. Floating cells and the possible sneak-path current passing through them are marked in red.

TABLE V
MAGIC XOR GATE STEPS

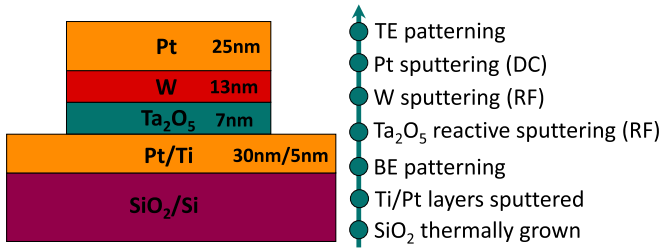
Input		Output		
IN1	IN2	Step (1) Initialize	Step (2) NIMP(IN1,IN2)	Step (3) OR(OUT, NIMP(IN2,IN1))
'0'	'0'	'0'	'0'	'0'
'0'	'1'	'0'	'0'	'1'
'1'	'0'	'0'	'1'	'1'
'1'	'1'	'0'	'0'	'0'

we set unselected rows to a third of the set voltage, and keep unused bitlines floating, as shown in Fig. 4 for the MAGIC NIMP gate. This maintains the voltage across the unselected cells below the switching threshold. Nevertheless, the sneak-path currents from unselected columns still affect the output of the gate, as demonstrated in the red mark in Fig. 4, where current flows from the unselected cells to the output. Given the resistance of cells and wires, this effect is low and can be mitigated by minor adjustments to the input voltages. MAGIC operations can be also implemented in selector-based crossbar arrays, e.g., 1T1R [33] 1S1R [18], and will likely suffer less from sneak-path and write-disturb phenomena. We are planning to examine the use of such structures in future work. The distribution of voltages between the operating cells, as described in the proposed gates, remains valid as long as the wire resistance is negligible when compared with the memristor resistance. In large crossbar arrays, this assumption might not hold [8]. We leave the exploration of this constraint in large arrays for future work.

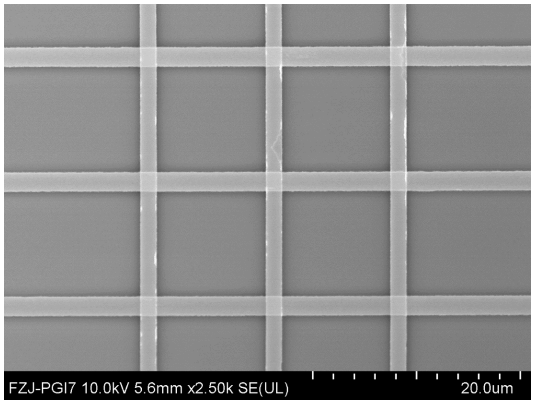
IV. EXPERIMENTS

A. Fabrication

To experimentally demonstrate the proposed MAGIC gates, a thoroughly studied VCM device [26], [34] was fabricated.



(a)



(b)

Fig. 5. Pt/Ta_2O_5/W/Pt VCM device fabrication details. (a) Schematic cross-sectional diagram of experimental split conditions. (b) SEM image of the 2 μm $\times$ 2 μm VCM device in passive crossbar configuration.

TABLE VI
DEVICE MEASUREMENT PARAMETERS

Parameter	Value
V_{SET}	-1.0 $[V]$
V_{RESET}	2.0 $[V]$
V_{READ}	0.1 $[V]$
R_{ON}	$2-5$ $[k\Omega]$
R_{OFF}	$50-500$ $[k\Omega]$
t_{SET}	0.5 $[\mu s]$
t_{RESET}	1 $[\mu s]$
t_{MAGIC}	2 $[\mu s]$
t_{RISE}/t_{FALL}	30 $[ns]$

About 5-nm-thick titanium (Ti) and 30-nm-thick platinum (Pt) layers were deposited by sputtering on a thermally grown 450-nm-thick SiO_2 layer on a Si substrate. Next, photolithography and dry-etching processes were used to pattern the Pt layer as a bottom electrode. Thereafter, 7-nm-thick Ta_2O_5 was deposited by reactive sputtering under a process gas mixture of argon (77%) and oxygen (23%) with an RF power of 116 W, and at a chamber pressure of 2.3×10^{-2} mbar. Without breaking the vacuum, a 13-nm-thick tungsten (W) and a 25-nm-thick Pt layer were deposited by RF and dc sputtering, respectively. All deposition processes were performed at room temperature. To pattern the top electrode, photo-lithography with positive photoresist was applied. After the photoresist

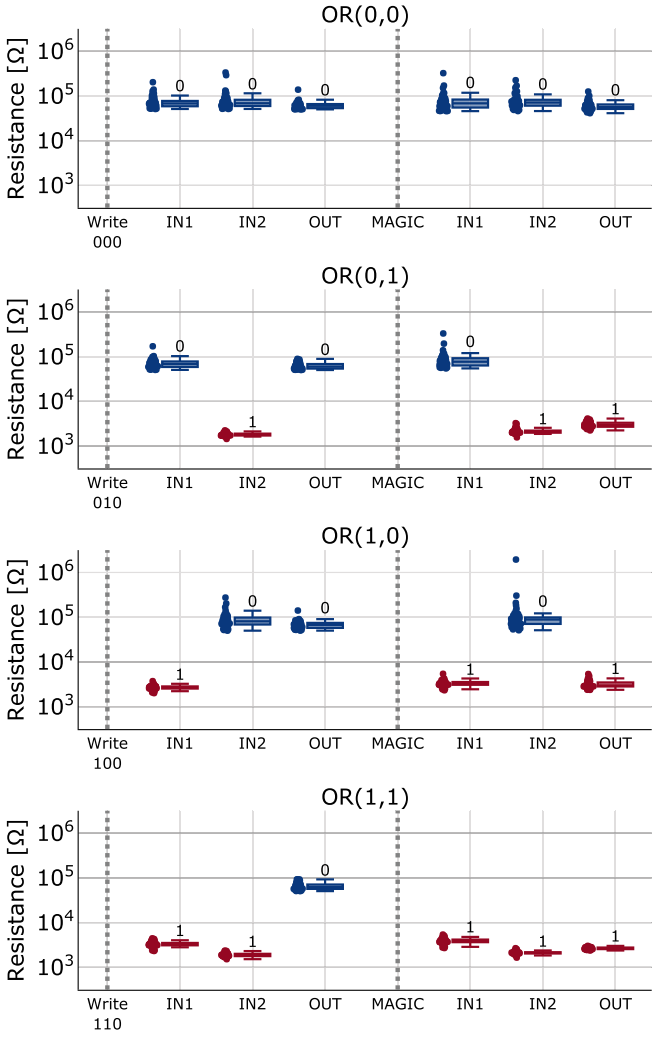


Fig. 6. Results of 50 cycles of MAGIC OR measured on the fabricated VCM device. The results show correct logic operation and exhibit input stability.

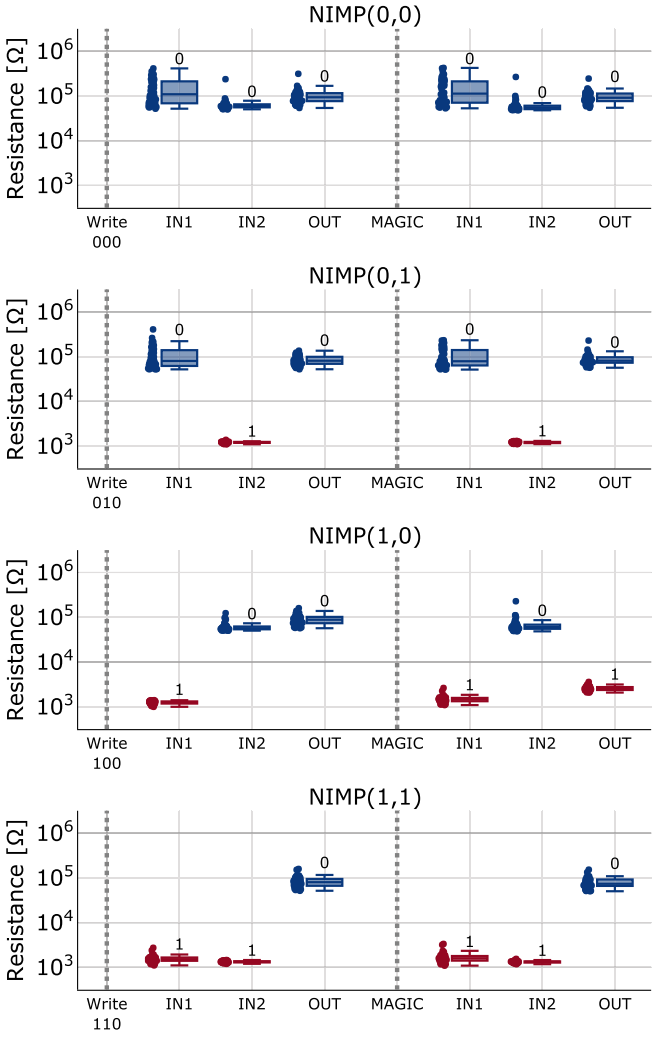


Fig. 7. Results of 50 cycles of MAGIC NIMP measured on the fabricated VCM device. The results show correct logic operation and exhibit input stability.

development, the top electrode was etched down with reactive ion beam etching (RIBE), forming the Pt/Ta_2O_5/W/Pt VCM device sketched in Fig. 5(a). A scanning electron microscope (SEM) image of the patterned passive crossbar structure, with a 2 μm $\times$ 2 μm cell size, is shown in Fig. 5(b).

B. Functionality and Robustness

The experiments were managed using Keysight's B1530 WGFMU for voltage pulse control, a probe station, and an automated script to perform write, read, and MAGIC operations on the cells. The measured device parameters and selected timing conditions are listed in Table VI. To program a cell to R_{ON}, we use a voltage pulse with an amplitude of V_{SET} and width of t_{SET}. To program it to R_{OFF}, we use a voltage pulse with an amplitude of V_{RESET} and width of t_{RESET}. For each gate (NOR, OR, NIMP), we tested the four input combinations and measured the output. For each input pattern, the test protocol was as follows.

1) Apply write pulses to program the inputs to their desired logical state and the output to an initial state (R_{OFF} or R_{ON}, according to the desired logic gate).
2) Read the resistance of the inputs and output by grounding the bitlines, applying V_{READ} to the wordline (WL) and reading the resulting current in each bitline. If the resistance is not in the desired state, go back to step (1).
3) Apply the MAGIC pulse.
4) Read the resistance of the output and the input memristors.

Each gate was tested for 50 cycles. Figs. 2, 6, and 7 present the results of the test protocol for the NOR, OR, and NIMP MAGIC gates, respectively. The x-axis represents the cell state or an operation (initialization or gate evaluation) and the y-axis represents the measured resistance in logarithmic scale. Each read cycle is plotted as a scatter and a median box is marked. By comparing the resistance of the output cell before and after the MAGIC pulse, the switching event can be identified, if it occurs.

The results for the MAGIC OR (Fig. 6) and MAGIC NIMP (Fig. 7) show correct logic operation and exhibit input stability. Although there was some resistance variation, which is common for these devices [26], the general logic value was correct and there was always a distinguishable margin (at least

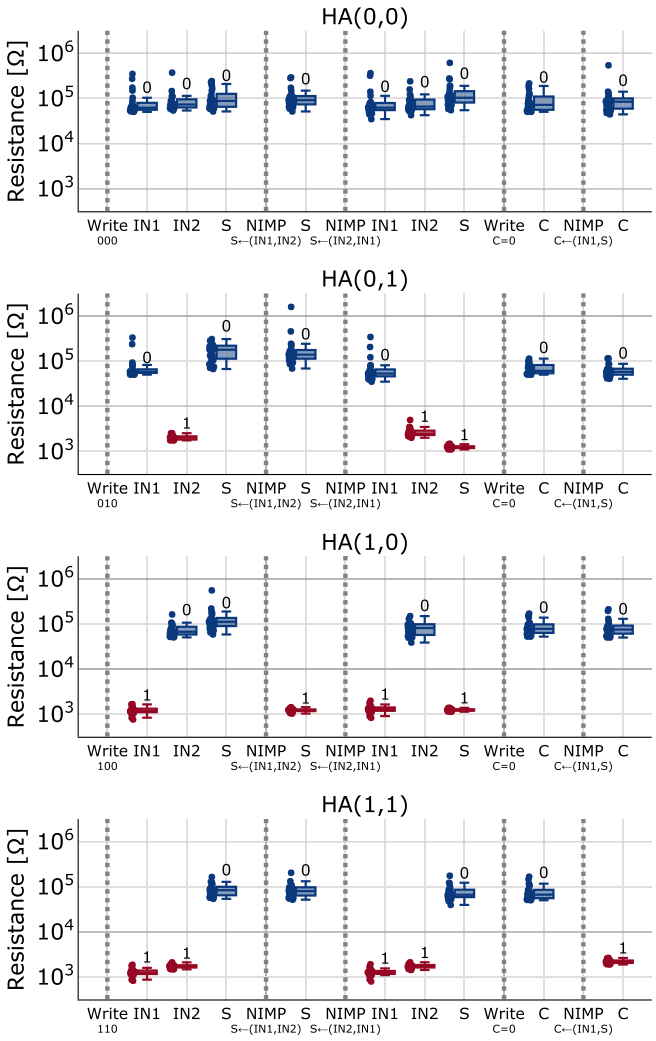


Fig. 8. Results of 25 cycles of the 1-bit half adder implementation using MAGIC gates.

one order of magnitude) in the resistance between the two logical states.

C. Timing

To find the minimal pulse duration for performing the logic operation, we selected the input case (among those that switch the output), with the lowest voltage across the output, and increased the pulse length until a switching event occurred. Successful results were obtained with a minimal pulse width of 2 μs. Since this is an experimental setup, we speculate that for a complete integrated design, with an optimized cell and lower capacitance, even substantially shorter pulses will work. The relatively long pulse length is dominated by the equipment's capacitance, mostly the probes' capacitance. Additionally, the capacitance driven by the gate is higher than a single cell because of the floating WL. To explore how variations of the pulse length affect the results, we increased the length of the pulse to as long as 100 μs, while still getting correct results and stable inputs. This suggests robustness of the gates to pulse width and switching time variations.

TABLE VII
COMPARISON OF STATEFUL FULL ADDER IMPLEMENTATIONS

Logic Operations	Computation Cycles	Additional Cells	Additional Resistor
IMPLY [5]	29/23	2/5	Yes
NIMP, AND, OR, XOR [32]	8	2	Yes
IMPLY, COPY, ORNOR [35]	16	1	Yes
NOR, NOT [8]	15/13	5/10	No
NOR, NOT, NAND, MIN, XOR [28]	6	2	No
NIMP, OR, XOR (This Work)	6	1	No

D. Half Adder Demonstration

To show the performance of the proposed gates as a building block for more complex operations, we present a 1-bit half adder. Using the previously described XOR implementation, we get the sum output:

$$S_{\mathrm{HA}} = \mathrm{IN1} \oplus \mathrm{IN2}. \tag{8}$$

This sum can be further used to obtain the carry output:

$$C_{\mathrm{HA}} = \mathrm{IN1} \cdot \mathrm{IN2} = \mathrm{NIMP}(\mathrm{IN1}, S_{\mathrm{HA}}). \tag{9}$$

Fig. 8 shows correct logic operation of the proposed 1-bit half adder for 25 cycles. This demonstrates how the output of one MAGIC gate can serve as the input for another MAGIC gate. This concept can be extended to perform any desired function.

The half adder operation can be combined in consecutive cycles to create a full adder

$$\begin{aligned} S_{\mathrm{FA}} &= S_{\mathrm{HA}} \oplus C_{\mathrm{IN}} \\ C_{\mathrm{FA}} &= C_{\mathrm{HA}} + \mathrm{NIMP}(C_{\mathrm{IN}}, S_{\mathrm{FA}}). \end{aligned} \tag{10}$$

Table VII compares different stateful logic full adder designs in terms of computation cycles, additional memristive cells, and whether an additional peripheral resistor is required. For some implementations, there is a tradeoff between the number of cycles and required cells. This comparison highlights that the full adder design using the proposed gates is attractive, since it is compact when compared with other stateful logic techniques, in terms of both computation time and area. Energy dissipation is not included in this comparison since it is highly dependent on device parameters, which are different for each study. Additionally, most of these studies are based on simulations and not experimental measurements. Nevertheless, generally, reset switching energy is higher than set energy in VCM devices [23], so the proposed logic gates may also reduce the energy dissipation compared to some of the implementations mentioned.

V. CONCLUSION

In this article, we demonstrated the limitations of executing the popular MAGIC NOR gate in VCM memristive devices

arising from input instability. To overcome this problem and perform computation within a memristive memory, three new logic gates based on the stateful MAGIC technique were proposed. These gates ensure input stability for devices such as VCM memristors, where the set voltage is lower than the reset voltage.

The design and usage of these gates in VCM devices were successfully demonstrated on fabricated Pt/Ta_2O_5/W/Pt VCM devices. Additionally, we demonstrated how more complex logic operations can be implemented, by consecutive operations of the proposed gates. This work enables stateful logic based on MAGIC for popular memristive technologies and is an important milestone toward real processing-in-memory.

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