

Boosting the Performance of Liquid-Gated Nanotransistor Biosensors Using Single-Trap Phenomena

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In small-area transistors, the trapping/detrapping of charge carriers to/ from a single trap located in the gate oxide near the Si/SiO2 interface leads to the discrete switching of the transistor drain current, known as singletrap phenomena (STP), resulting in random telegraph signals. Utilizing the STP-approach, liquid-gated (LG) nanowire (NW) field-effect transistor biosensors have recently been proposed for ultimate biosensing with enhanced sensitivity. In this study, the impact of channel doping concentration on the capture process of charge carriers by a single trap in LG silicon NW structures is investigated. A significant effect of the channel doping concentration on the single-trap dynamic is revealed. To understand the mechanism behind unusual capture time behavior compared to that predicted by the classical Shockley-Read-Hall theory, an analytical model based on the rigorous description of the additional energy barrier that charge carriers have to overcome to be captured by the trap at different gate voltages is developed. The enhancement of the sensitivity for single-trap phenomena biosensing with an increase of the channel doping concentration is explained within the framework of the proposed analytical model. The results open prospects for the development of advanced single trap-based devices.

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1. Introduction

Over the last few decades, nanoscience has made huge strides toward implementing theoretical abstractions and predictions in cheap and reliable devices with a wide range of applications.[1-3] Although a variety of structures have found applications in different branches of technology and everyday life, there remains a strong demand for applications that utilize novel effects obtained through ongoing research.[4-8] Among these applications, sensors play a crucial role, for instance, in quality control, safety management, health, and environmental monitoring. Application-oriented research is becoming increasingly progressive due to recent advances on the nanoscale.[9-11] In particular, the continuous downscaling of device dimensions has led to the introduction of new generations of sensors based on nanoscale field-effect transistor (FET) structures.^[12–16] Such nanoscale sensor devices, which are very similar to massproduction state-of-the-art semiconductor

transistors, enable faster, more compact, more accurate, and more cost-effective biological[11,17,18] and chemical[12,14,19] detection. However, along with these advantages, minimizing the dimensions of the biosensor to the nanoscale also facilitates new challenges in terms of determining the conditions for improved performance and sensitivity of the sensors. In particular, the latter is still limited by the intrinsic electrical noise of the transducer element.[20-24] Typically, a main physical source of noise in such transistor-based structures is attributed to the interactions of charge carriers with traps in a gate oxide layer. [25-29] However, as the device size shrinks, the number of electrically active traps decreases. To this end, when the number of active traps is reduced to a single trap, a strong modulation of nanotransistor conductance appears as single-trap phenomena, resulting in two-level characteristic switching known as random telegraph signal (RTS) noise.[25-30] In general, RTS noise has become one of the most important issues for electronic nanoscale devices in terms of affecting their performance and reliability.^[30] Therefore, charge traps were often treated as undesirable objects, and all technological processes were intended to improve the fabrication steps in order to minimize the impact of traps on device performance.

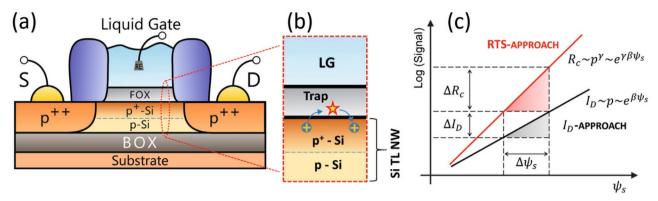


Figure 1. a) Schematic illustration of a two-layer silicon nanowire structure configured as a liquid-gated accumulation-mode FET biosensor. Note that the change of doping concentration of the p⁺-Si layer is analyzed in this work with respect to obtaining enhanced sensitivity in biosensors. b) Cross section of the device, showing a single trap in the gate oxide that is responsible for the RTS noise. The dashed blue line schematically represents the boundary between a low-doped and a highly doped layer of the two-layer silicon nanowire. c) Schematic demonstration of the response of a sensor to the change in the surface potential for different sensing approaches. The slope of the response curve defines the sensitivity of the detection approach. The RTS approach demonstrates considerably enhanced sensitivity.

On the other hand, RTS can be considered as a singleatom phenomenon, which makes it a promising diagnostic tool to study interface properties and the quality of the gate oxide at the atomistic level in small electronic devices such as metal-oxide-semiconductor field-effect transistors (MOS-FETs).[27,28,30] Furthermore, due to its discrete nature and specific properties, the use of single-trap phenomena has been suggested for many useful and important applications.^[29,31] For instance, it has been demonstrated that a single electron captured in a single-trap state responsible for an RTS behaves quantum mechanically, and such a trap can thus be considered a promising candidate for use in quantum information computing.[32,33] Moreover, an important role of single traps has been shown for digital processing systems and memory devices. [34] These opportunities offered by an electrically active single trap in nanoscale devices attract the increasing interest of the scientific community. In addition to the aforementioned advantages, the use of a single trap in liquid-gated (LG) nanobiosensors (see Figure 1a,b) was recently proposed and demonstrated for ultimate scaling, noise suppression, [16] and enhanced sensitivity in comparison to conventional LG FETbased sensors.[35-37]

The sensitivity of typical LG FET-based sensor monitoring a change in drain current, ΔI_D caused by the change in surface potential, $\Delta \psi_S$ is usually defined as^[38,39]

$$S_{(I_{\rm D})} = \frac{\Delta I_{\rm D}}{\Delta \psi_{\rm S}} \tag{1}$$

In the case of the single-trap phenomena approach, the capture rate, $R_{\rm c}$ is used as the sensing parameter. Therefore, the sensitivity can be defined as

$$S_{(R_c)} = \frac{\Delta R_c}{\Delta \psi_s} \tag{2}$$

In the bulk semiconductor material under equilibrium conditions, the RTS capture rate typically exhibits a linear dependence on the carrier concentration and can be described within

the framework of the standard Shockley–Reed–Hall (SRH) $model^{[40,41]}$

$$R_{c}^{(SRH)} = \sigma_{p} \vartheta_{th} p \tag{3}$$

where σ_p is the capture cross section, ϑ_{th} is the average thermal velocity, and p is the concentration of free holes (in the case of hole capture) at the Si/SiO₂ interface. According to Equation (3) and assuming that the drain current is proportional to the concentration of free holes ($I_D \sim p$) in the transistor channel located near the Si/SiO₂ interface, a linear dependence of capture rate on I_D is expected. However, according to the experimental results, RTS fluctuations in various devices including liquid-gated nanowire structures demonstrate enhanced capture dynamic behavior, indicating a strong dependence of the RTS capture rate on carrier concentration [³⁶]

$$R_c \sim p^{\gamma}$$
 (4)

where γ is an exponent of the power function ($\gamma \ge 1$).

In the case of the SRH theory, $\gamma=1$ reflects the linear dependence of $R_{\rm c}$ on concentration p (see Equation (3)). It should be noted that the larger exponent γ in Equation (4) corresponds to the stronger dependence of the capture rate on the concentration of the major charge carriers, which is determined by surface potential (see Figure 1c). In the case of MOSFETs, the surface potential is controlled by the metal gate, and the enhanced dependence of the capture dynamic on the carrier concentration is explained within the Coulomb blockade model, taking into account the Coulomb interaction of the major carriers with image charges induced on the metal gate electrode. [27,28] At the same time, energy quantization effects should also be considered in cases of charge-carrier confinement in the conductive channel in order to explain superlinear RTS capture rate behavior. [42–44]

For the LG nanosensors, [12,35-37] the surface potential is a function of physical and chemical changes caused by specific reactions of the target charged biomolecules with the surface of a sensor. As a strong function of surface potential,

the enhanced RTS capture rate can be used as a sensing parameter to improve the sensitivity of LG FET-based biosensors. In this respect, we also recently discovered that nanotransistor channel comprising an additional single layer with definite doping concentration is effective for the design of advanced biosensors with enhanced sensitivity. [36,37] It should be noted that the RTS dynamic behavior in LG nanosensors with different doping concentrations has not yet been considered in the literature.

In this study, we explore the impact of channel doping concentration on the single-trap dynamic in LG NWs configured as accumulation-mode FETs. To this end, we fabricated unique two-layer (TL) silicon nanowire structures with different doping concentrations (see Figure 1a,b). The significant effect of doping on RTS time constants in fabricated devices was revealed during experiments and, to the best of the authors' knowledge, the effect is demonstrated, for the first time, in LG NW structures. The results are essential for improving single-trap-based nanobiosensor performance. To understand the mechanism behind the enhanced capture rate behavior in highly doped structures, we developed an analytical model based on the rigorous description of the additional energy barrier (AEB) that charge carriers must overcome to be captured by the trap at different values of surface potential controlled by a liquid-gate voltage. Experimental results of the enhanced

RTS capture dynamic processes registered in fabricated LG NW structures are explained within the framework of the proposed model

2. Experimental Results and Analysis

2.1. Electrical Performance of Si TL NW FETs

Fabricated TL NW structures configured as liquid-gated accumulation-mode FETs were first investigated from the perspective of electrical performance. Figure 2a shows a typical set of transfer characteristics measured for a 90 nm wide and 100 nm long LG Si TL NW FET with a channel doping concentration of 10¹⁶ cm⁻³ for different drain-source voltages. The corresponding curves obtained for the Si TL NW FET with the same channel dimensions but with a higher doping concentration (10¹⁷ cm⁻³) are shown in Figure 2b. Both devices were liquidgated using a commercially purchased Ag/AgCl reference electrode that was immersed in the phosphate-buffered saline (PBS) solution with pH = 7.4. The leakage current through the 8 nm thin front-gate SiO2 layer remained negligibly small (below 10 pA) during measurements in a liquid environment. In general, the LG NW devices exhibited good working stability and reproducibility of I-V characteristics, demonstrating

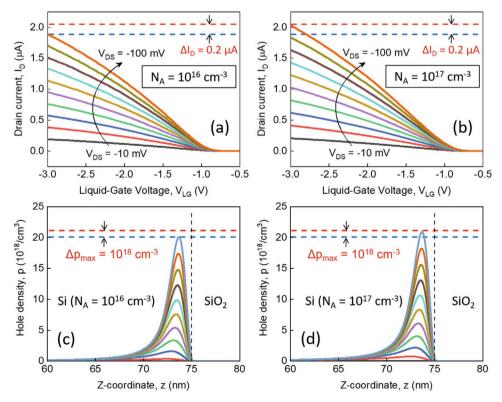


Figure 2. a,b) Transfer characteristics of 90 nm wide and 100 nm long liquid-gated TL NW FETs measured at different drain—source voltages, V_{DS} for devices with doping concentrations in the channel of 10^{16} and 10^{17} cm⁻³, respectively. c,d) Simulated densities of holes as major charge carriers in two-layer accumulated silicon with doping levels of 10^{16} and 10^{17} cm⁻³, respectively. The distribution of holes was calculated and plotted for the gate voltages varied in the range from (0 V) down to (–3 V) with a voltage step size of (–0.3 V). The calculations were performed using the NEXTNANO++ software. The Z-coordinate corresponds to the direction that is normal to the Si/SiO₂ interface (vertical dashed line). The horizontal blue and red dashed lines are guides to the eye reflecting the difference between drain currents (panels (a) and (b)) and maximum densities of holes (panels (c) and (d)) obtained for TL NW FET structures with 10^{16} and 10^{17} cm⁻³ concentrations of dopants in the channel at $V_{LG} = -3$ V.

a high-level performance for the fabricated two-layer nanostructures. It should be noted that under the same operating conditions, higher values of drain currents were measured for nanostructures with higher channel doping concentrations. Configured as accumulation-mode FETs (p+-p-p+), devices with a higher concentration of dopants in the channel exhibit lower channel resistance due to the higher concentration of holes as majority carriers, which in turn results in higher drain currents, as this follows from data shown in Figure 2a,b. The experimental results are in good agreement with calculated hole density profiles presented in Figure 2c,d for TL nanowires with doping concentrations of 10¹⁶ and 10¹⁷ cm⁻³, respectively. As can be seen in Figure 2c,d, a slightly higher concentration of holes was observed for the two-layer devices with a higher concentration of acceptors, which determine the conductivity of p-type semiconductor material. The distributions of holes, as the majority carriers in p-type silicon structures, in the direction that is normal to the Si/SiO2 interface were calculated at different gate voltages using the NEXT-NANO simulation software for semiconductor nanodevices.^[45] The modeled structures consist of two silicon layers with different concentrations of dopants. The first silicon layer with a thickness of 50 nm has a 10^{15} cm⁻³ concentration of boron (B)dopants, while the second layer with a thickness of 25 nm is highly doped silicon with a concentration of acceptors at either 10¹⁶ or 10¹⁷ cm⁻³ to match the doping profiles of the first type and the second type of fabricated structures, respectively. The simulation results (Figure 2c,d) demonstrate that the greatest amount of accumulated positive charges (holes) are located in the highly doped region of two-layer silicon structures, where they form the accumulation layer with a thickness of several nanometers in the vicinity of the Si/SiO2 interface. This indicates that the highly doped top silicon layer with advanced properties also plays a dominant role in terms of the singletrap phenomena that will be analyzed below.

Moreover, by monitoring the characteristic capture rate as a signal,[35-37] the analyte interacting with the surface of an LG NW sensor can be detected with enhanced sensitivity compared to the conventional approach based on the monitoring of drain current (see Figure 1c). In this case, the single trap can be considered to be the smallest ever atomic-size highly sensitive nanosensor. The enhancement of sensitivity by a factor of γ can be expected for the single-trap phenomena approach, as follows from the expression

$$\frac{S_{(R_c)}}{S_{(I_D)}} = \frac{\Delta R_c}{\Delta \psi_s} : \frac{\Delta I_D}{\Delta \psi_s} = \gamma \tag{5}$$

It should be noted that such a statement has been proven experimentally for one definite doping concentration.[35] According to Equation (5), the efficiency of such a new biosensing approach critically depends on the exponent γ reflecting the single-trap dynamic. The latter is determined by the intrinsic properties of the trap as well as the characteristics of the device (e.g., material properties, geometry, and operation mode). Therefore, relevant parameters including channel doping, which are required to optimize the performance of nanobiosensors utilizing single-trap phenomena, have to be carefully defined and investigated.

2.2. RTS Noise Features in Fabricated LG NW FET Structures

In this study, we focus on the effect of channel doping concentration on the single-trap dynamic in liquid-gated FET nanostructures. Figure 3a shows a typical RTS time trace measured for an LG NW structure at room temperature. The recorded time trace clearly indicates the charge trapping/detrapping process originating from a single trap in the gate oxide. As a fully stochastic process, the two-level RTS is usually characterized by the mean characteristic times that the system spends in the state when the trap is empty (emission state) or in which it is occupied by a charge carrier (capture state). It is commonly considered that the mean capture time, τ_c reveals the average time before a charge carrier is captured by a single trap, while mean emission time, τ_e reflects the average time during which the trap is occupied by a charge carrier. The probability rate for a charge carrier to be captured/emitted by/from the trap is governed by the emission rate $R_e = 1/\tau_e$ and capture rate $R_c = 1/\tau_e$, respectively.

The amplitude histogram of the recorded two-level drain current fluctuations is shown in Figure 3b. As can be seen, the histogram curve is composed of two peaks, which also reflect the two-state RTS switching kinetic. Each peak corresponds to a certain RTS state and can be fitted by a Gaussian distribution due to the presence of other noise sources in the system (e.g., flicker noise and thermal noise). The height of each peak reflects the probability of finding the system at a certain corresponding state, while the distance between the two maxima reveals the RTS amplitude.

Figure 3c presents the power spectral density (PSD) of current noise obtained from the measured time trace by performing a fast Fourier transform. A dashed red line shows a Lorentzian-shaped PSD of a single two-level RTS given by [21,46]

$$S_{I}(f) = \frac{4(\Delta I)^{2}}{(\tau_{c} + \tau_{e}) \left[\left(\frac{1}{\tau_{c}} + \frac{1}{\tau_{e}} \right)^{2} + (2\pi f)^{2} \right]}$$
(6)

where ΔI is the amplitude of RTS, f is the frequency, τ_c and τ_e are the capture and emission times, respectively. Both characteristic times characterize a specific trap level at a given bias condition.

The distribution of dwell times in capture and emission states is shown in Figure 3d. As can be seen in Figure 3d, both capture and emission times follow a Poisson distribution $P(t) \sim \exp(-t/\langle t \rangle)$, where $\langle t \rangle$ denotes a capture or emission time constant averaged over all states of an ensemble for a given time t. Therefore, the results shown in Figure 3d confirm, as expected, that the measured RTS noise is a Poisson process.^[25,26] If the RTS amplitude is large enough compared to the background noise and the measured time trace contains a relatively large number of transition events between capture and emission states (at least 200), [25,26,47] a dwell time histogram (Figure 3d) fitted to the Poisson distribution can be used to accurately extract RTS time constants. Otherwise, RTS analysis should be performed using a statistical method^[36,47,48] that requires both frequency and time domain data. In the case of two-level RTS noise, the distribution of the RTS signal (i.e.,

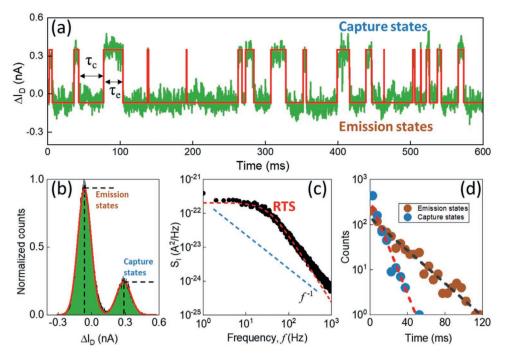


Figure 3. a) Time dependence of drain current change measured for the 100 nm wide and 200 nm long LG TL NW FET with a 10¹⁷ cm⁻³ concentration of B-dopants in the epitaxially grown Si layer. The time trace reflects typical two-level RTS behavior in the fabricated LG nanostructures. b) The corresponding amplitude histogram showing two peaks fitted with a Gaussian distribution. c) Noise current spectral density of the recorded time trace shown in panel (a). A dashed red curve shows the Lorentzian-shaped component that corresponds to the RTS, while a dashed blue line provides a visual guide for 1/f noise behavior typical for the flicker noise. d) Distribution of the RTS emission and capture states. The data are fitted with a Poisson distribution.

the amplitude histogram) is composed of two Gaussian peaks (see Figure 3b), which confirms two-level switching kinetic. Therefore, by calculating the ratio between the heights of two peaks as well as knowing the corner frequency of the RTS noise that can be obtained from the fitting of the frequency domain data (see Figure 3c), one can evaluate RTS characteristic capture and emission time constants.^[36] To minimize errors and exclude the effect of different extraction procedures on the accuracy and quality of the data extraction, the analysis of all measured RTS data shown below was performed using the statistical method.

2.3. Impact of Doping Level on a Single-Trap Capture Dynamic: Experimental Results

Dynamic processes in liquid-gated NW FETs were studied at different gate voltages applied using an Ag/AgCl reference electrode immersed in 10×10^{-3} M physiological PBS solution with pH = 7.4 at low constant drain–source voltages ($V_{\rm DS} \leq 100$ mV). Experimental dependences of RTS capture times ($\tau_{\rm c} = 1/R_{\rm c}$) on drain current for the fabricated devices with channel doping concentrations of 10^{15} , 10^{16} , and 10^{17} cm⁻³ are shown in Figure 4a, Figure 4b, and Figure 4c, respectively. As can be seen, RTS capture times exponentially decrease with increasing drain current that is controlled by the liquid gate. Such a behavior is typical for acceptor-type traps. [27,28] It should be noted that the majority of registered RTSs observed in the experiments exhibit non-SRH behavior with a considerably stronger dependence of

capture time on drain current (exponent γ > 1; see Equation (4)) compared to the SRH model (Equation (3)).

The distribution of RTS capture rate slopes, γ is presented in Figure 4d for the 100 nm wide and 200 nm long LG NW transistors with different doping concentrations in the channel. We reveal that the exponent γ increases with an increasing concentration of acceptor dopants in the p-type devices. It is worthy to note that the slope γ even reaches the value of 10 in Si TL NW structures with a doping level of 10¹⁷ cm⁻³. These results indicate the significant effect of doping on trapping/detrapping dynamics in LG nanoscale transistors. An approximately linear dependence of the exponent γ on the concentration of dopants in the channel was experimentally observed for the fabricated devices. In the following sections, we derive an analytical model to understand and highlight the mechanism behind enhanced capture dynamics in accumulation-mode LG nanostructures and describe the origin of the reveled effect of doping on RTS dynamics in LG Si NW FETs.

3. Proposed Analytical Model for LG NW FETs with Different Doping Concentrations and Discussion

To understand the impact of doping concentration on the superlinear capture rate behavior observed in the fabricated LG NW FET-based sensor structures, we derived the model based on the rigorous description of AEB, ΔE , that charge carriers must



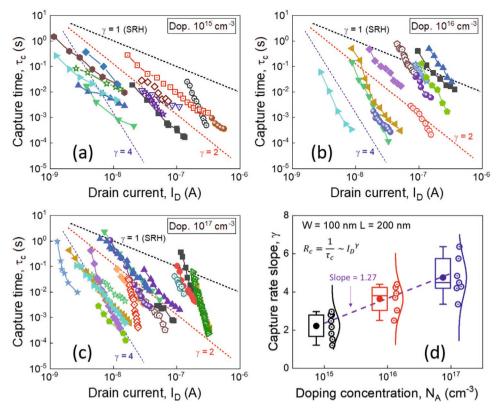


Figure 4. a–c) Comparison of dynamic processes in LG NW FETs with different concentrations of dopants in the channel. RTS characteristic capture time is shown as a function of drain current recorded for the different LG Si NW structures with doping concentrations in the channel of 10^{15} , 10^{16} , and 10^{17} cm⁻³, respectively. The dashed colored lines with indicated slopes represent a visual guide. The line with slope γ = 1 corresponds to the SRH model. d) The statistics of the capture rate slopes recorded for the 100 nm wide and 200 nm long LG NW FETs. The whiskers are determined by the 5th and 95th percentiles. The solid dots shown inside the boxes denote the mean values of the γ slopes obtained for different doping concentrations. The dashed violet line with a slope of 1.27 shows the increase of the mean value of registered exponents γ with increasing channel doping concentration.

overcome to be captured by a trap at different values of surface potential controlled by the gate voltage. The model was developed for the acceptor-type traps^[27,28] according to the experimental results (see Figure 4–c). For the acceptor trap, which is neutral when empty and charged after capturing a charge carrier, the RTS capture time constant is given by

$$R_{\rm c} = \frac{1}{\tau_{\rm c}} = C_{\rm p} N_{\rm V} e^{-(E_{\rm F} - E_{\rm V} - q\psi_{\rm s})/kT} \cdot e^{-\Delta E/kT} = R_{\rm SRH} \cdot e^{-\Delta E/kT}$$
(7)

where $R_{\rm SRH}=C_{\rm p}N_{\rm V}{\rm e}^{-(E_{\rm r}-E_{\rm V}-q\psi_{\rm s})/kT}$ is the conventional SRH capture rate into the trap in the homogeneous bulk semiconductor in the case of holes being captured as major carriers, $C_{\rm p}$ is the capture constant, $N_{\rm V}=2\left(\frac{2\pi\cdot m_{\rm p}^*kT}{h}\right)^{3/2}$ is the effective density of states, $E_{\rm V}$ is the top of the valence band, $E_{\rm F}$ is the Fermi energy, $\psi_{\rm s}$ is the surface potential defined by the applied gate voltage, and ΔE is AEB due to the interaction of a charge carrier with its image charge in LG NW FET structures. In the case of LG NW FETs (see Figure 1a), the surface potential is a complex parameter that also depends on the dynamic interactions occurring on the surface of the sensors (e.g., antibody–antigen recognition events, DNA hybridization processes, and protonation/deprotonation processes). The image charge appears on a liquid gate as the carrier approaches the interface between

media with different permittivities (e.g., Si/SiO₂ interface). As a result, the image force potential emerges, inducing the energy barrier for charge carriers near the Si/SiO₂ interface.

To understand the nature of the potential barrier for a carrier to be captured by the trap, it is important to obtain the total potential profile $\Psi(x)$ for the holes in the vicinity of the Si/SiO₂ interface in LG NW FETs taking into account the interface processes including the interaction of a charge carrier with its image charge. The total potential $\Psi(x)$ near the SiO₂ dielectric at the point of capture consists of two components: the band bending potential $\psi(x)$ and the additional potential created by the mirror image charge $\phi(x)$. This can be described as

$$\Psi(x) = \psi(x) + \varphi(x) \tag{8}$$

The $\psi(x)$ can be obtained by solving the Poisson equation^[25]

$$\frac{\partial^{2} \psi(x)}{\partial x^{2}} = -\frac{q}{\varepsilon_{s} \varepsilon_{0}} \left(p_{p0} e^{-\frac{q \psi}{kT}} - N_{A} - n_{p0} e^{\frac{q \psi}{kT}} \right)$$
(9)

where $\psi(x)$ is the electrostatic potential (band bending) controlled by liquid-gate voltage and charged molecules in the case of LG NW FETs, q is the unit charge, k is the Boltzmann constant, T is the temperature, ε_0 is the dielectric constant, ε_s is the relative dielectric permittivity of the semiconductor, N_A is the

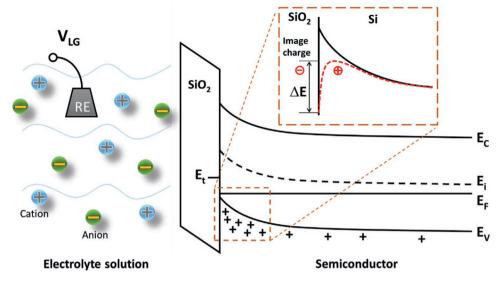


Figure 5. Schematic illustration of the energy profile for LG NW FETs with a trap at the Si/SiO_2 interface. The electrolyte solution is used as the liquid gate. The interaction processes on the liquid–solid interface determine the surface potential change influencing the charge-exchange processes between the single trap and the conductive channel of the LG FET. The inset shows an additional energy barrier, ΔE for a hole in a p-type semiconductor before capturing by a trap. In the figure, E_C is the conductance band, E_V is the valence band, E_V is the trap energy level, E_V is the intrinsic Fermi level, and E_V is the Fermi level position in the p-doped semiconductor under a negative bias voltage (accumulation mode P^+) FET).

concentration of the ionized acceptor atoms (dopants) in the semiconductor, p_{p0} is the equilibrium concentration of holes, and n_{p0} is the equilibrium concentration of electrons.

Note that the concentration of dopants, N_A , in Equation (9) is an important parameter influencing the potential distribution and thus transport phenomena in LG NW FET-based devices. The distribution of the electrostatic potential $\psi(x)$ in the low-doped p-type Si layer under a negative bias voltage on the gate (i.e., FET in accumulation mode) is schematically shown in **Figure 5**. The potential energy formed as a result of the image force can be described as follows^[25]

$$\varphi(x) = \frac{q}{16\pi\varepsilon_0\varepsilon_{\text{Si}}} \left(\frac{\varepsilon_{\text{Sio2}} - \varepsilon_{\text{Si}}}{\varepsilon_{\text{Sio2}} + \varepsilon_{\text{Si}}}\right) \frac{1}{x}$$
(10)

where ε_0 , ε_{Si} , and ε_{SiO_2} are the vacuum permittivity and the relative permittivities of Si and SiO₂, respectively, q is the elementary charge, and x is the position of the mirror image charge related to the Si/SiO₂ interface.

It should be noted that the dielectric permittivity of SiO_2 ($\varepsilon_{SiO2}=3.9$) is smaller than the dielectric permittivity of undoped Si ($\varepsilon_{Si}=11.7$). As a result, $\phi(x)$ changes sign at the Si/SiO_2 interface, repelling the holes from the interface. This results in the AEB formation for charge carriers being captured by the trap. The competitive contribution and superposition of $\psi(x)$ and $\phi(x)$ are schematically illustrated in the inset of Figure 5. As can be seen, the valence-band profile changes near the interface and becomes nonmonotonous with induced AEB for the holes. The height of the barrier, ΔE , can be defined as the difference between the maximum energy of the lowered valence band and the effective energy attained by a hole when the latter is approaching a critical distance to the point of capture, which is less than 1 nm to the interface trap. The barrier changes with a change in surface potential

and doping concentration as will be shown in the following sections.

Figure 6a,b shows the band diagrams calculated for different values of surface potential (which is the function of analyte concentration in the case of LG nanotransistor biosensors) with and without considering the image force effect. As can be seen in Figure 6a,b, the height of the barrier is a strong function of the surface potential controlled by the gate voltage. As surface potential increases, the height of the barrier decreases. This can be explained by the increase in the electrostatic screening of the image charge, resulting from the increased concentration of charge carriers accumulated at the Si/SiO2 interface with increasing gate voltage. [21] The band diagrams calculated for different concentrations of dopants in the channel while the surface potential remains constant are shown in Figure 6a,c,d. It is evident that at higher channel doping concentrations and the same surface potential values, ΔE is smaller. These results indicate that the height of the barrier diminishes faster for devices with a high concentration of dopants in the channel. The dependence of AEB height on the surface potential for transistors with different doping concentrations in the channel is shown in Figure 7. As can be seen, the barrier indeed reduces faster as the doping concentration increases. This can be explained by the increase of the vertical electric field at the Si/ SiO₂ interface with the increasing channel doping concentration. Therefore, the enhanced interaction of a single trap with charge carriers in the channel reveals a significant impact of dopants on charge-carrier dynamics in nanoscale devices.

In **Figure 8**a, the dependence of the capture rate on surface potential calculated for transistors with different concentrations of dopants in the channel is shown. Two regimes can be resolved in the behavior of the capture rate. At low surface potential values that correspond to the subthreshold regime of a transistor device, the capture rate behaves as a complex function

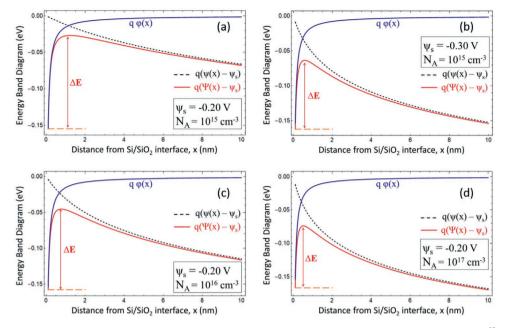


Figure 6. a,b) Energy band diagrams calculated for LG NW FETs under investigation with a doping concentration of $N_A = 10^{15}$ cm⁻³ at a gate bias corresponding to an accumulated silicon surface potential of $\psi_s = -0.2$ V and $\psi_s = -0.3$ V, respectively. c,d) The energy band profiles calculated at $\psi_s = -0.2$ V for NWs with $N_A = 10^{16}$ cm⁻³ and $N_A = 10^{17}$ cm⁻³, respectively. The black dashed lines show the potential distributions without considering the image force effect, while solid red lines denote the band diagrams with consideration of the image force potential, $\phi(x)$. Note that the height of the additional potential barrier, ΔE, decreases with increasing doping concentration in the NW channel of an LG FET under the same operating conditions.

of surface potential, reflecting non-SRH behavior (γ > 1). In the first approximation, the dependence is superlinear on a semi-logarithmic scale and can be fitted with a polynomial function $R_c \sim \psi_s^{\ \gamma}$ in which γ is used as a fitting parameter. At the same time, at higher values of ψ_s , the AEB diminishes (see Figure 7) and, therefore, the capture rate starts to behave as a linear function of surface potential, as predicted by the conventional SRH theory. For devices with a higher doping concentration, the barrier diminishes faster, which results in higher values of γ , i.e., increased sensitivity.

Figure 8b shows the normalized values of the exponent γ , i.e., capture rate slope as a function of the doping concentration.

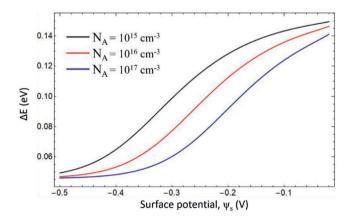
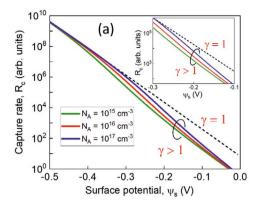


Figure 7. Dependence of the AEB height, ΔE , on the surface potential calculated for three different concentrations of dopants in the channel of LG NW FETs—black curve: $N_{\rm A}=10^{15}~{\rm cm^{-3}}$, red curve: $N_{\rm A}=10^{16}~{\rm cm^{-3}}$, and blue curve: $N_{\rm A}=10^{17}~{\rm cm^{-3}}$.

As can be seen in Figure 8b, γ increases with the concentration of dopants in the channel, which is in good agreement with experimental results shown in Figure 4d. It should be noted that higher values of capture rate slopes result in higher sensitivity of single-trap-based biosensors as demonstrated in ref. [36]. At the same time, as is evident in Figure 8b, the experimental results show a stronger dependence of γ on the doping concentration than the one predicted by the proposed model. This can be explained by the fact that our calculations were performed for a trap located at the Si/SiO2 interface and only over-barrier transport was considered within the model. For the traps located in the gate oxide, the factors which influence the probability of carriers' tunneling to/from the trap have also be taken into account. The trap distance to the Si/SiO2 interface is an important parameter in this regard. The position of the trap determines the local changes in potential distribution, inducing a variation in the trap energy level and additional energy ΔE . Another possible origin of the observed superlinear RTS capture rate behavior could be related to quantum and strain effects, [49] which might impact the RTS dynamic on the nanoscale. Steeper capture rate slopes for the traps in the gate oxide are thus revealed experimentally in the present study for LG NW FETs with different doping concentrations in the channel, operated in the accumulation regime. In this regime, more strong correlation effects between a trap and channel charge carriers are expected compared to the case of the inversion mode regime. At the same time, the phenomena considered in this work in LG nanostructures with increasing doping concentration in the channel should be taken into account for the development of ultrasensitive LG nanoscale FET-based biosensors and molecular devices for quantum information technology.



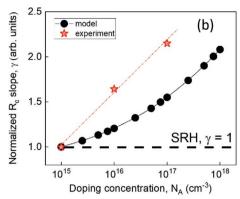


Figure 8. a) Capture rate as a function of surface potential calculated for devices with different concentrations of dopants in the conductive channel of LG NW FETs—green curve: $N_A = 10^{15}$ cm⁻³, red curve: $N_A = 10^{16}$ cm⁻³, and blue curve: $N_A = 10^{17}$ cm⁻³. The inset emphasizes a non-SRH behavior of capture rate (i.e., $\gamma > 1$) versus surface potential (ψ_s) varied in the range from (– 0.1 V) down to (– 0.3 V). b) Dependence of normalized logarithmic slope of the capture rate on the doping concentration in the transistor channel: black points and red points show the calculated and experimental data, respectively. The data on R_c slopes with $\gamma > 1$ reflect sensitivity amplification for the single-trap phenomena biosensing approach compared to SRH behavior with $\gamma = 1$ (shown by the dashed horizontal line).

4. Conclusion

Sensitivity enhancement is an important aspect in the development of ultrasensitive biosensors. In this study, we showed that single-trap phenomena observed in liquid-gated nanostructures provide a unique opportunity to enhance the sensitivity of nanoscale biosensors, helping to enhance knowledge of biological processes even at the molecular level. We revealed the impact of channel doping concentration on single-trap dynamics in liquid-gated nanowire biosensors and demonstrated how single-trap phenomena observed in the fabricated devices exhibit enhanced capture dynamics with increasing channel doping concentration compared to the SRH theory. The accurate model of the potential profile description for the holes in the accumulated p-Si has been proposed to explain the revealed doping effect. The calculations were performed while considering the additional energy barrier to capture a carrier by a trap. The obtained results give a clear description of the mechanism behind a carrier capture process and explain the RTS capture dynamic in fabricated LG NW FET structures. These results should be taken into account for the development of single-trap-based nanobiosensors with enhanced sensitivity.

5. Experimental Section

To investigate the impact of channel doping concentration on the dynamics of charge-exchange processes between a single trap and a nanowire channel, nanowires consisting of two silicon layers with different dopant concentrations were fabricated. The fabrication technology of Si TL NW FETs was similar to that of low-doped single-layer Si NW FETs, as described in the following sections.

Fabrication of Single-Layer Si NW FETs with 10^{15} cm⁻³ Doping Level: Single-layer low-doped Si NW FET structures were fabricated using silicon-on-insulator (SOI) wafers with a 50 nm thin, $\langle 100 \rangle$ -oriented Si layer, and a 145 nm thick buried oxide layer (BOX). Prior to NW patterning, the SOI wafers were covered with a 20 nm thick SiO₂ layer using plasma-enhanced chemical vapor deposition (PECVD), which served as a layer for the formation of a hard mask employing reactive

ion etching. The NW pattern was defined using e-beam lithography, and mesa structures were defined utilizing photolithography. Structures were then transferred to the active silicon layer of the SOI wafers using wet chemical etching in a 5% tetramethylammonium hydroxide (TMAH) solution at 80 °C. Ion implantation with B-dopants (energy = 6 keV, dose = 1×10^{15} cm⁻²) was subsequently performed to create accumulation-mode FET (p⁺-p-p⁺) transistor structures. An 8 nm thin SiO₂ layer was then thermally grown on the NW structures to serve as the gate dielectric and to protect the conductive channel of transistorbased biosensors from the liquid environment. The metallization process was then performed by sputtering a metal stack consisting of 5 nm of TiN and 200 nm of Al followed by the lift-off patterning and annealing process. In order to protect metal leads against the liquid environment, the structures were passivated with a polyimide layer. Access to Si NWs was ensured for the liquid solution by patterning the passivation layer with photolithography. After the fabrication process, wafers were cut into separate chips, each containing 32 transistors. The chips were then wire-bonded, encapsulated, and measured. All fabrication steps were performed at the Helmholz Nano Facility (HNF) of Forschungszentrum Jülich.

Fabrication of LG Si TL NW FETs: To fabricate two-layer silicon nanowire FET structures with different doping concentrations, an additional 25 nm thin p-type Si layer was epitaxially overgrown on top of the active 50 nm thin low-doped SOI layer with a B-dopants' concentration of 10¹⁵ cm⁻³. As a result, two SOI wafers with 10¹⁶ and 10¹⁷ cm⁻³ concentrations of B-dopants in the grown layer were used to fabricate Si TL NW FETs. Transistor structures were then patterned and fabricated further using the fabrication flow described above. A 2D schematic view of the LG Si TL NW FET device is shown in Figure 1a. The central idea was to introduce a highly doped top silicon layer with advanced properties from the perspective of the single-trap phenomena (see Figure 1a,b).

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

Keywords

nanowire biosensors, random telegraph signals, single-carrier dynamics, single-trap phenomena

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