SCALABLE QUANTUM BIT CONTROL (SQUBIC1)

Cryogenic CMOS IC for Spin Qubit Control

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QUANTUM COMPUTERS

General Introduction

- Possible **exponential speed up** for certain tasks:
  - Shor's algorithm for **factoring integers**
  - Grover's algorithm for **search in unordered databases**
  - **Quantum chemistry**: Simulate new molecules and catalysts
  - Quantum(-enhanced) machine learning

- Requirements for a universal quantum computer:
  - **Large number (10^6-10^8) of physical qubits**[1] (operated at T $\lesssim$ 1K)
  - Room temperature electronics to communicate with the qubits
  - **Scalable control and read-out electronics**

[1] Vandersypen, L.M.K., Bluhm, H., Clarke, J.S. *et al.* Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent. *npj Quantum Inf* **3,** 34 (2017). https://doi.org/10.1038/s41534-017-0038-y

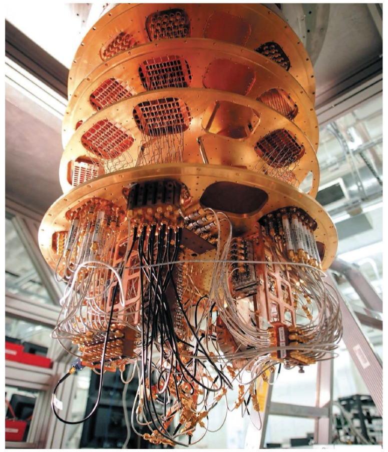
QUANTUM COMPUTERS

Current Approaches

- ‘Brute force’ scaling to operate up to 50-100 qubits
- Further scaling very difficult
- The ‚Tyranny of numbers‘ (Jack Morton, Bell Labs, 1958) is back
- **Let‘s solve it (again) with integrated circuits**

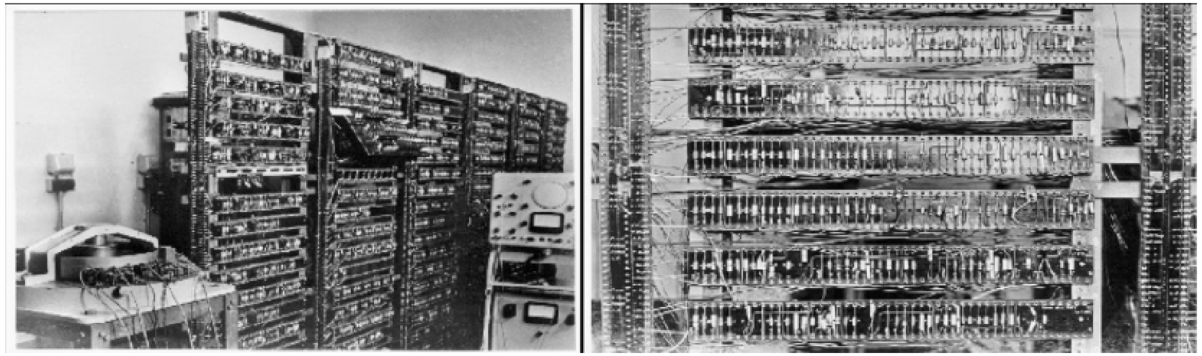
Today

Source: IBM



Source: Google, Mohseni et al., Nature 543 (2017)

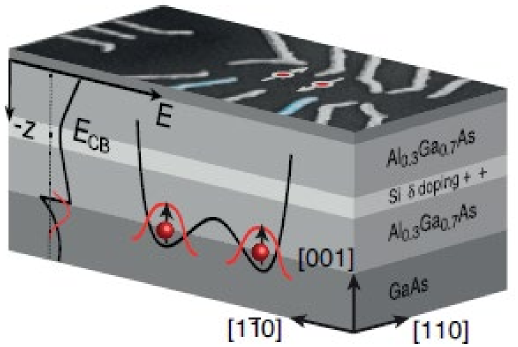
1950s



Source: IBM

QUANTUM COMPUTERS

Requirements GaAs Spin Qubits



Tim Botzem, "Coherence and high fidelity control of two-electron spin qubits in GaAs quantum dots," PhD Thesis, p. 7, Fig: 2.2.: Device Layout. Online: http://publications.rwth-aachen.de/record/689507, 2017, DOI: 10.18154/RWTH-2017-04410

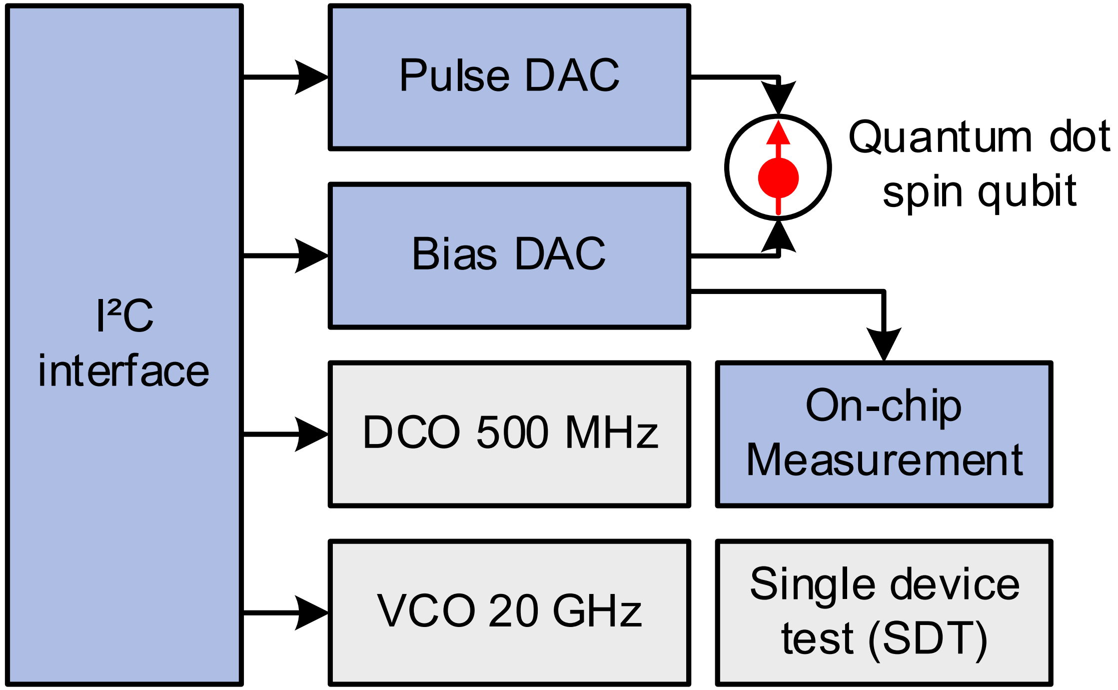
- Up to 8 uncorrelated bias voltages per qubit, forming potential wells
- 2 pulse electrodes for qubit operation
- Key performance indicator: fidelity of qubit gate

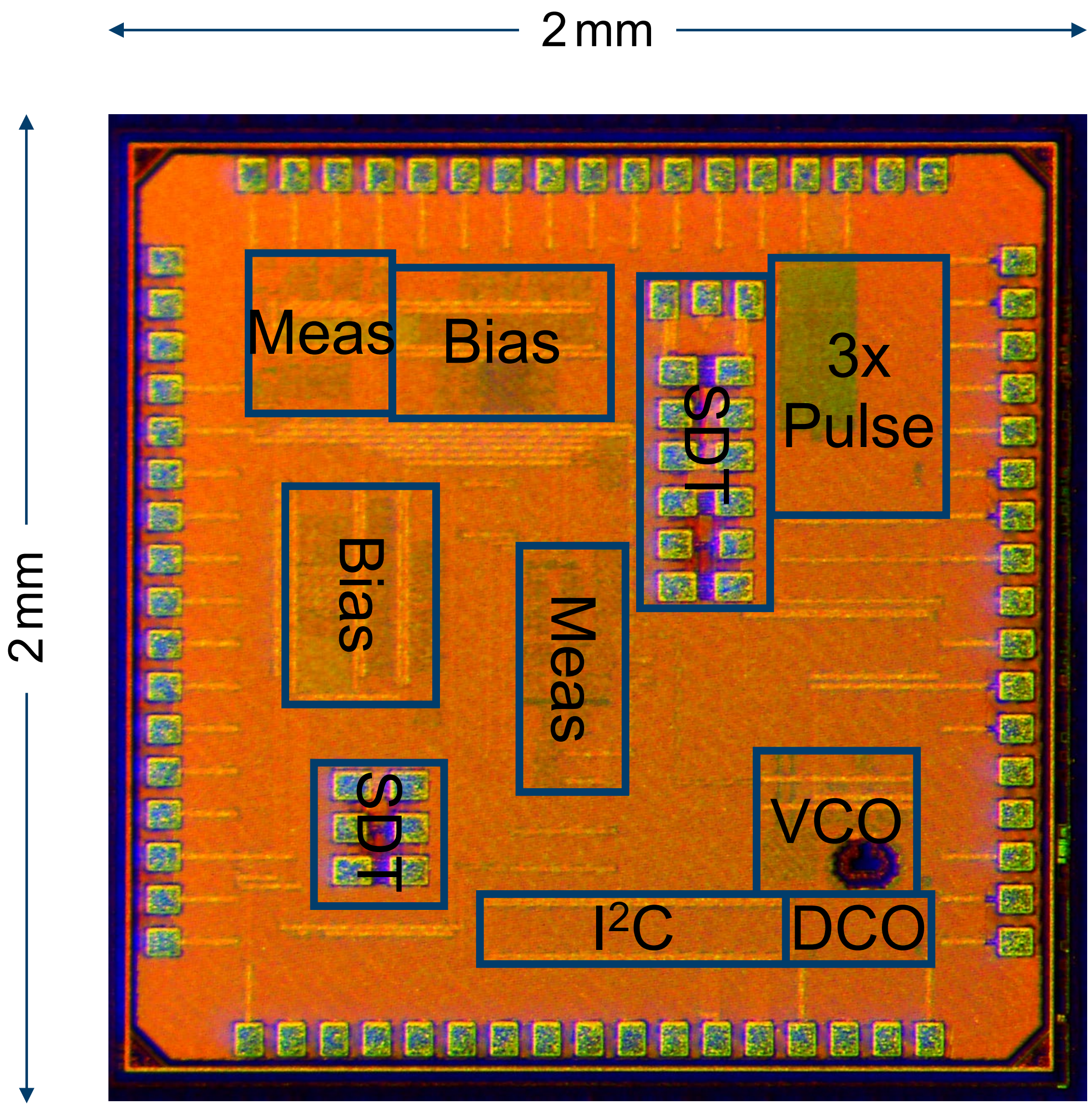
Characteristic	Specification
Bias voltage range	−1 V to 0 V
Bias voltage noise v_{RMS}	≲ 20 µV
Bias voltage step size	250 µV (≙12 bit)
Pulse dynamic range	± 4 mV
Pulse sampling rate	250 MHz
Pulse resolution (8 mV range)	30 µV (≙ 8 bit)
Cooling power budget @ 100 mK	<1 mW

SQUBIC1

Scalable Quantum Bit Control

- TSMC 65nm CMOS technology
- Biasing and pulse control of GaAs qubit

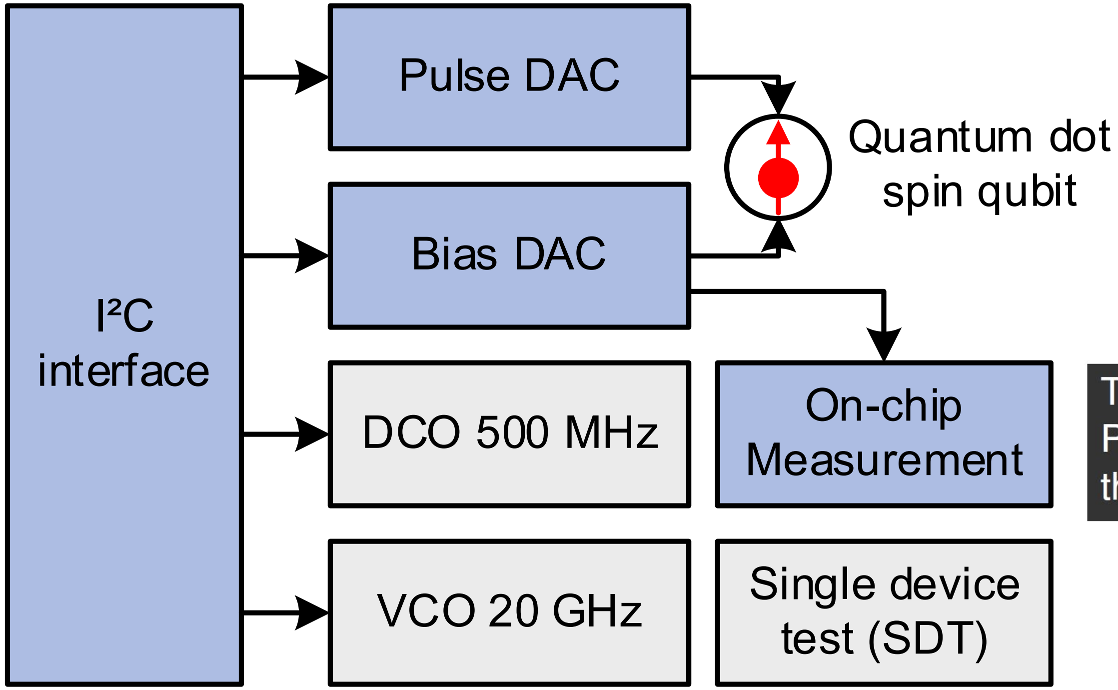


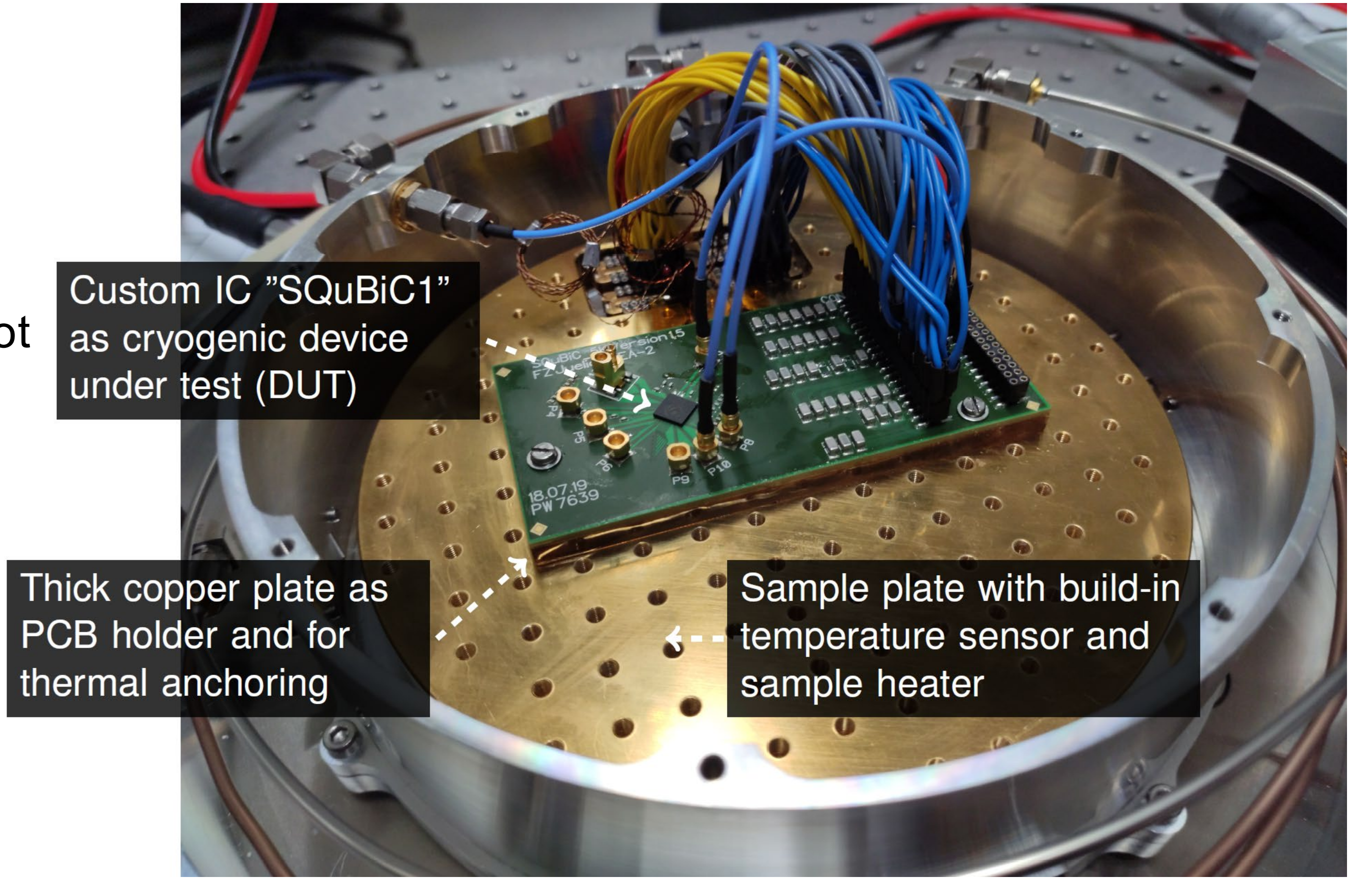


SQUBIC1

Measurement Setup

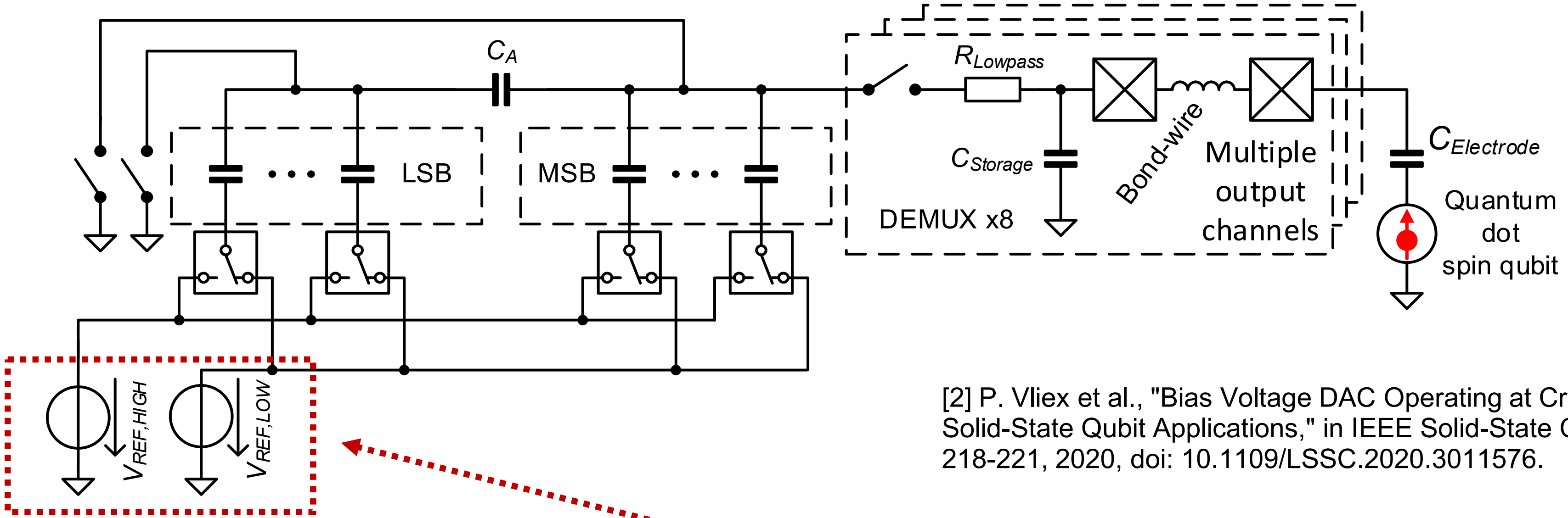
- Packaged sample inside cryostat
- Cryostat base temperature approx. 6 K





BIAS DAC

Charge-Redistribution Topology



[2] P. Vliex et al., "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications," in IEEE Solid-State Circuits Letters, vol. 3, pp. 218-221, 2020, doi: 10.1109/LSSC.2020.3011576.

- Negligible static power dissipation
- Low thermal noise at cryo. T : $\bar{v}_N^2 = \frac{k_B \cdot T}{C}$
- No output buffer needed
  → Reduce power and noise

- Coarse tuning by on-chip MUX[2]
  → Reduce power and increase resolution
  → But: need for calibration
- Multiple output channels per DAC

BIAS DAC

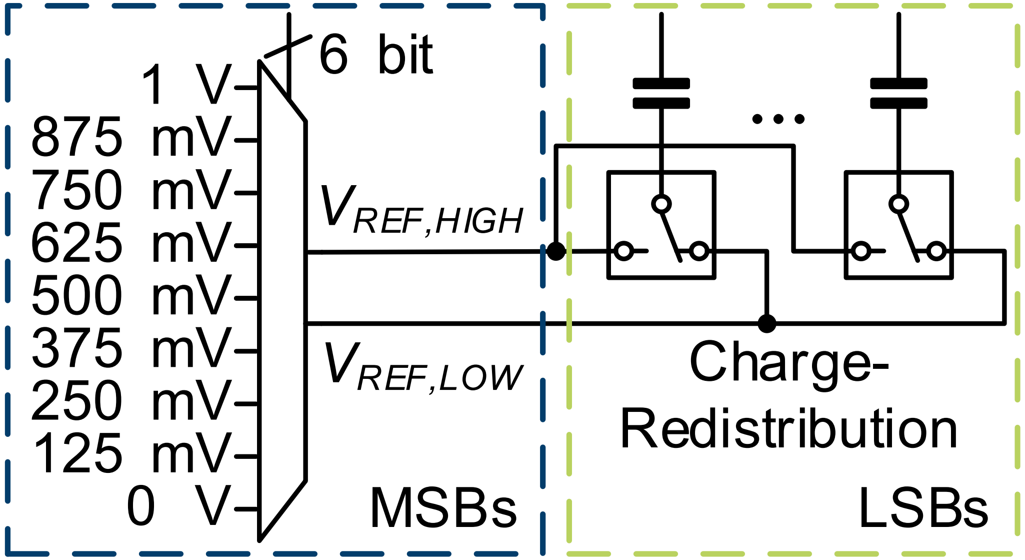
Coarse Tuning Reference Voltages

- Coarse tuning by on-chip MUX[2]
  - Reduce dynamic analog power P_{AD}

$$\Delta V_{REF} = V_{REF,HIGH} - V_{REF,LOW}$$

$$P_{AD} \propto C_{Total,DAC} \cdot (\Delta V_{REF})^2 \cdot f$$

    - $P_{AD}\downarrow$ by a factor $(125\,\text{mV} / 1\,\text{V})^2 = 1/64$
  - Resolution increased
    - 3 bit added for $V_{REF,HIGH}$ and $V_{REF,LOW}$ each
    - DAC resolution ↑ by 3 bit



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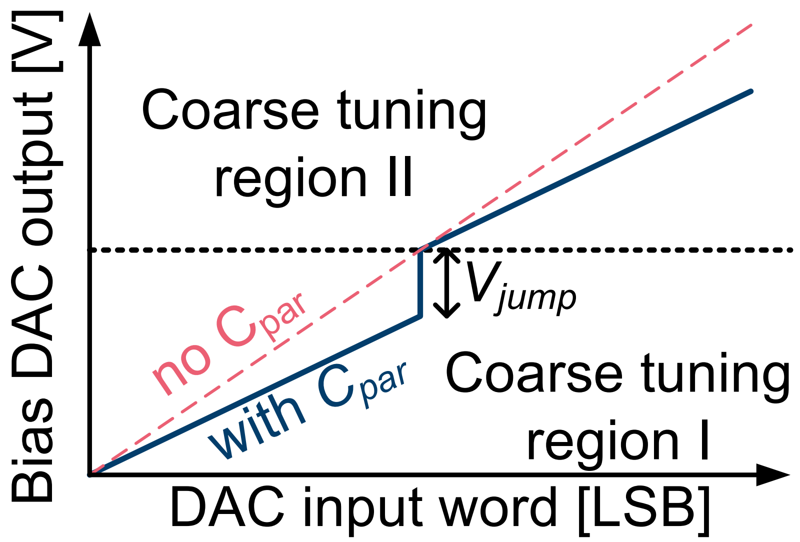
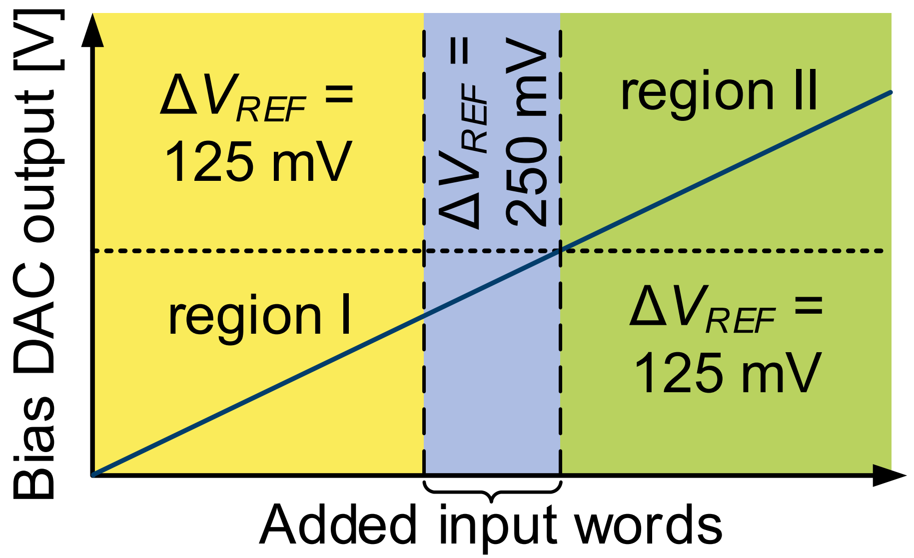
Coarse Tuning Reference Voltages

- Coarse tuning by on-chip MUX[2]
  - Parasitic C_{par} leads to DAC gain < 1
    - Voltage jump V_{jump} at coarse tuning crossings



- Introduce *intermediate steps*
  - Filling the missing codes range
  - Operated with ΔV_{REF} = 250 mV
  - Add input words
    - Saved in off-chip memory



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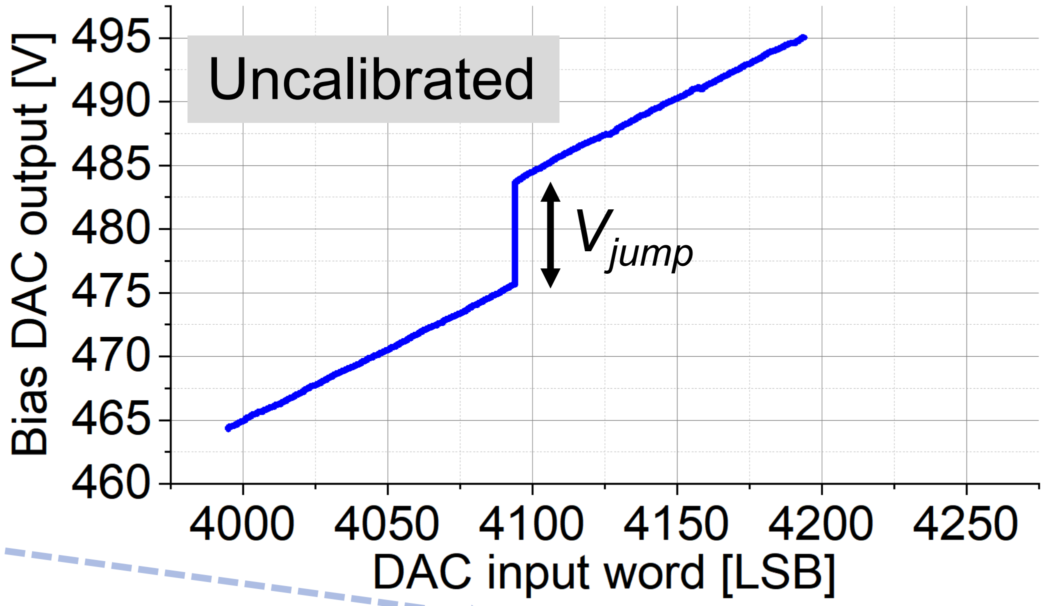
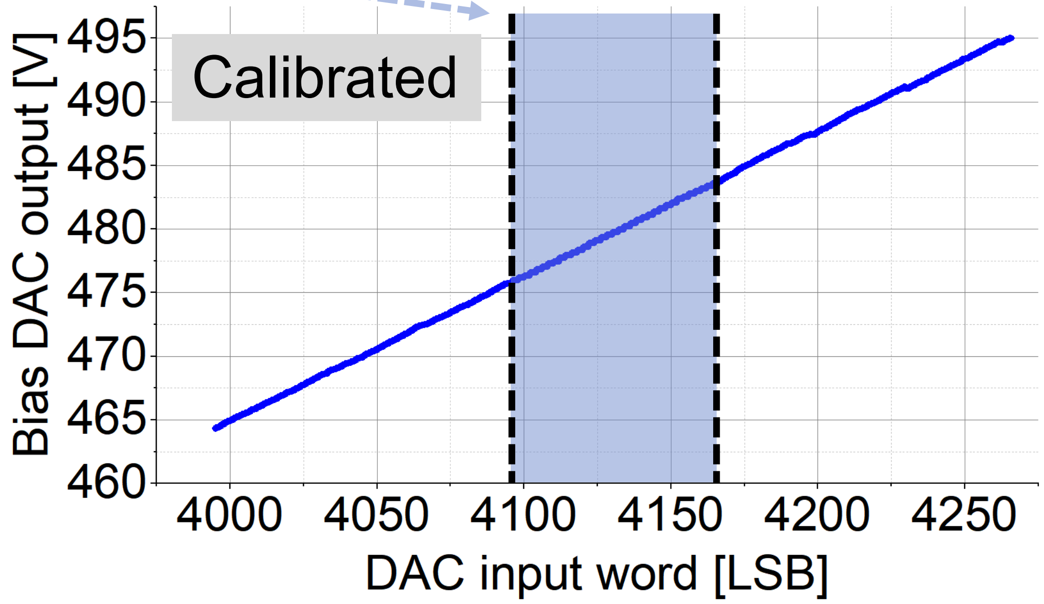
Coarse Tuning Reference Voltages

- Calibration verified at 6 K
  - *Intermediate steps*
  - Steps doubled

  → Correcting Bias DAC gain





Intermediate steps range (4096 – 4155)

$V_{REF,HIGH}$ 3 bit	3 (500 mV)		4 (625 mV)				• • •	4 (625 mV)					
$V_{REF,LOW}$ 3 bit	3 (375 mV)						• • •	3 (375 mV)				4 (500 mV)	
Charge-redistribution 10 bit	1022	1023	502	502	503	503	• • •	530	530	531	531	0	1
Z_{IN}	4094	4095	4096	4097	4098	4099	• • •	4152	4153	4154	4155	4156	4157

[2] P. Vliex et al., "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications," in IEEE Solid-State Circuits Letters, vol. 3, pp. 218-221, 2020, doi: 10.1109/LSSC.2020.3011576.

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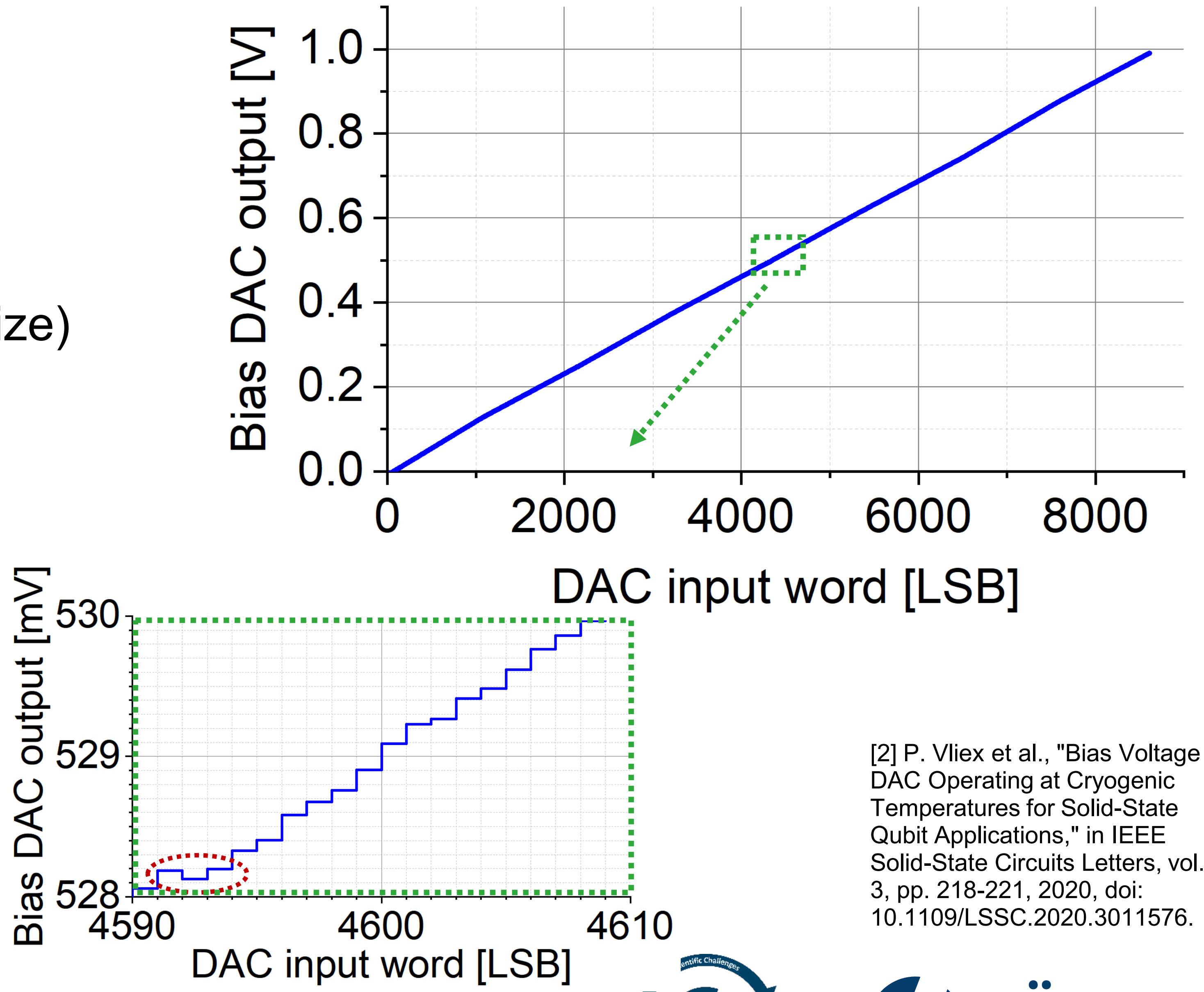
Measurement

- Fully functional at 6 K[2]
  - 13 bit resolution (≈ 120 µV step size)
  - 1 V output range
  - Channel refresh rate of 3.9 kHz
  - Calibrated reference voltage coarse tuning

- Singular non-monotonic steps
  - No issue for qubit biasing



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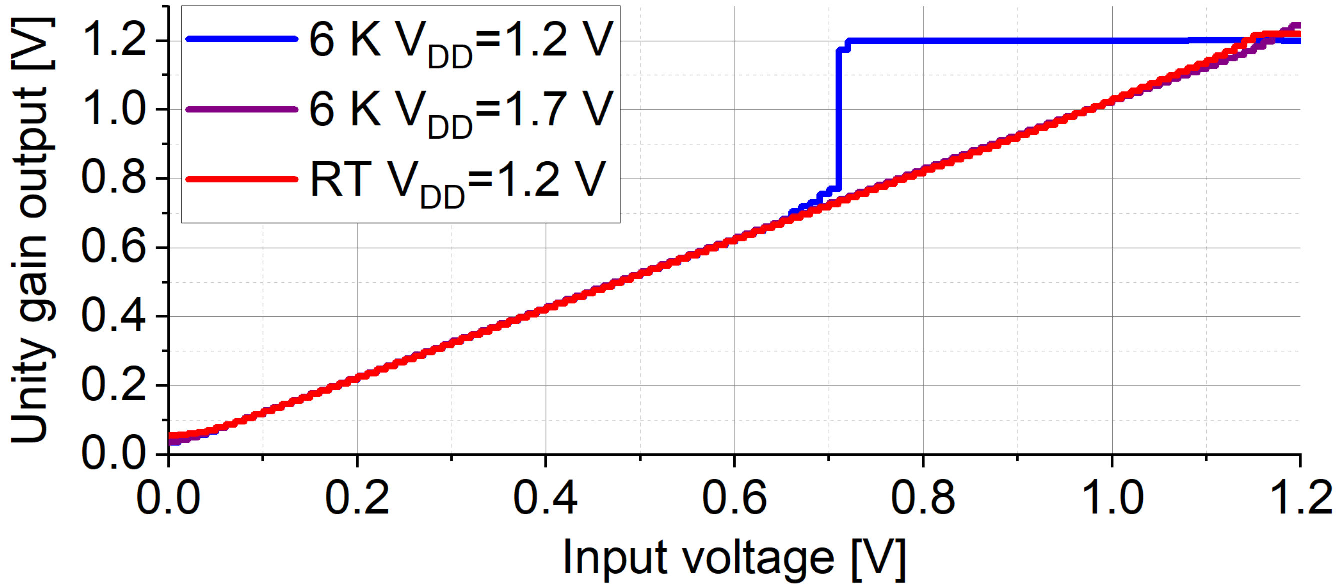
OPAMP

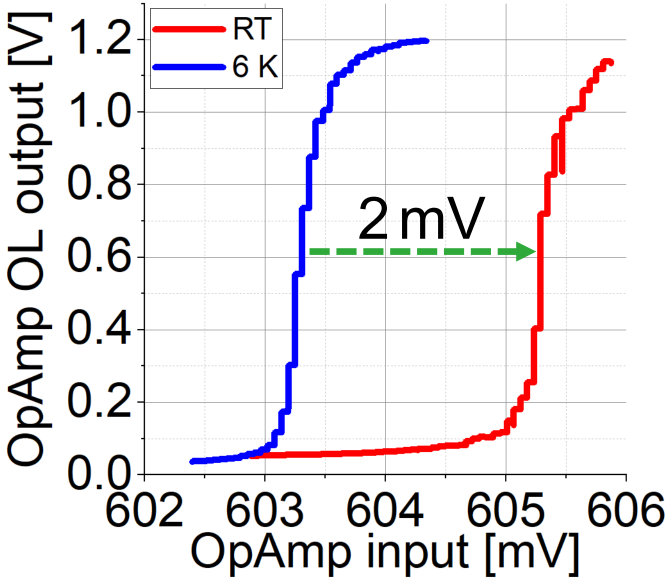
On-chip Measurement Circuitry

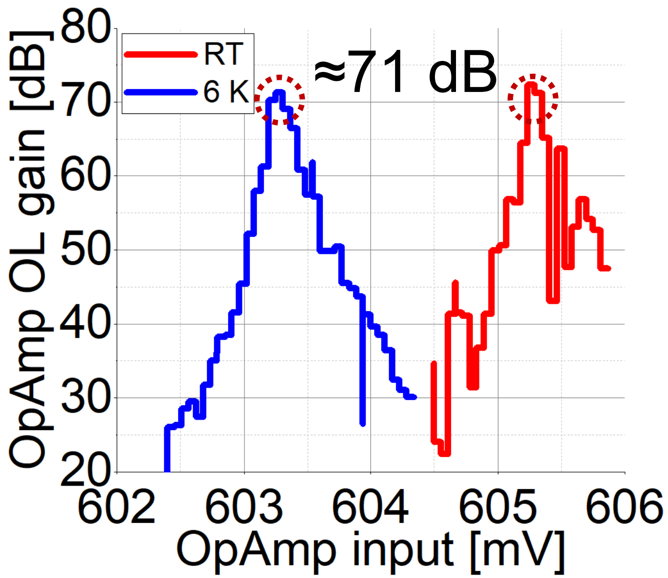
- Unity gain configuration

- Enable Bias DAC noise measurement
- Supply increase: 1.2 V to 1.7 V at 6 K

- Small offset voltage shift of ≈2 mV
- Comparable open-loop (OL) gain of ≈ 71 dB







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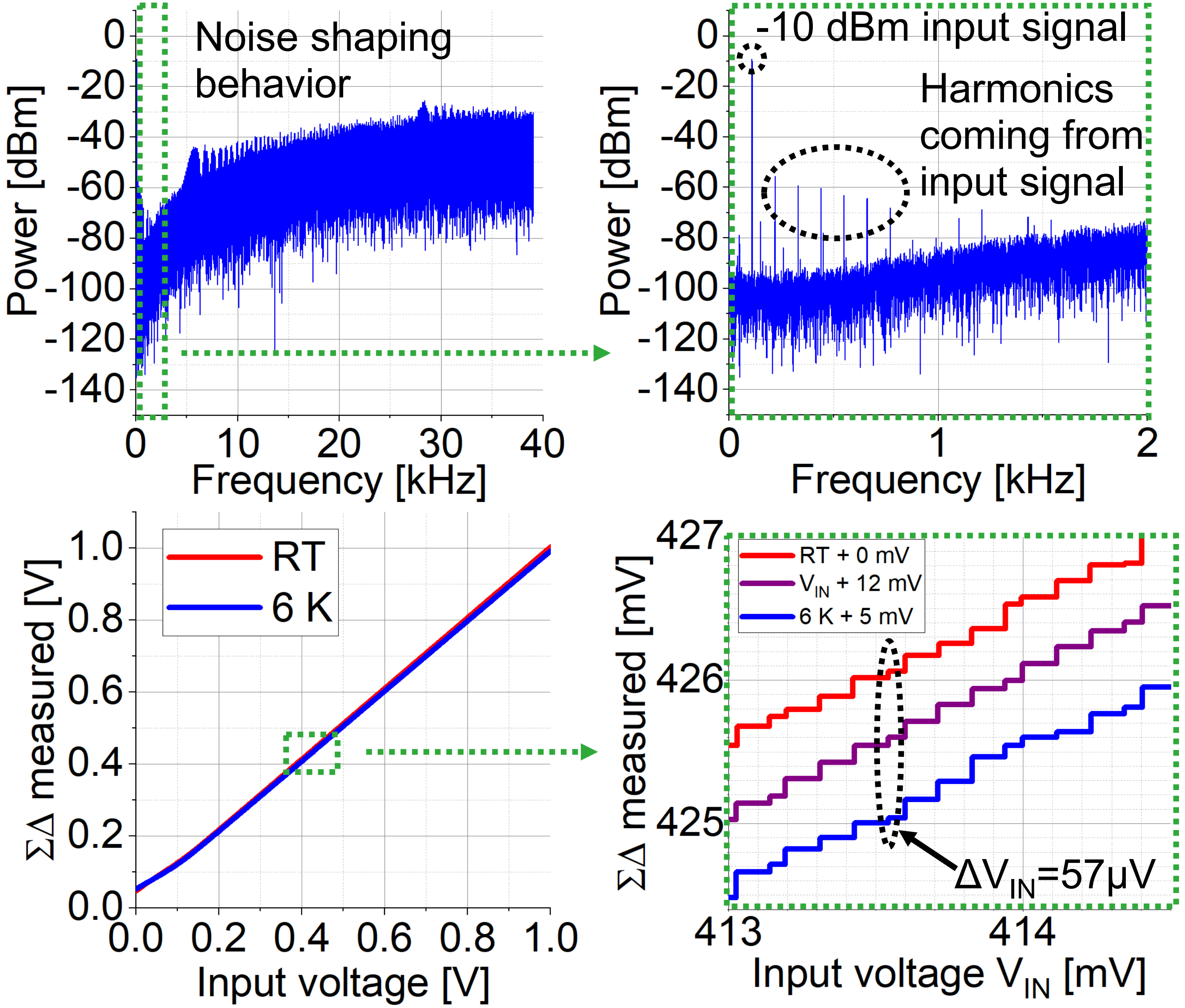
ΣΔ MODULATOR

On-chip Measurement Circuitry

- Measurement at 6 K
- On-chip analog-to-digital conversion
- 3^{rd} order 2-1 MASH modulator
- Noise floor (≈ -110 dBm) limited by input signal
- Off-chip bit-stream filtering
- Building block for future on-chip Bias DAC calibration



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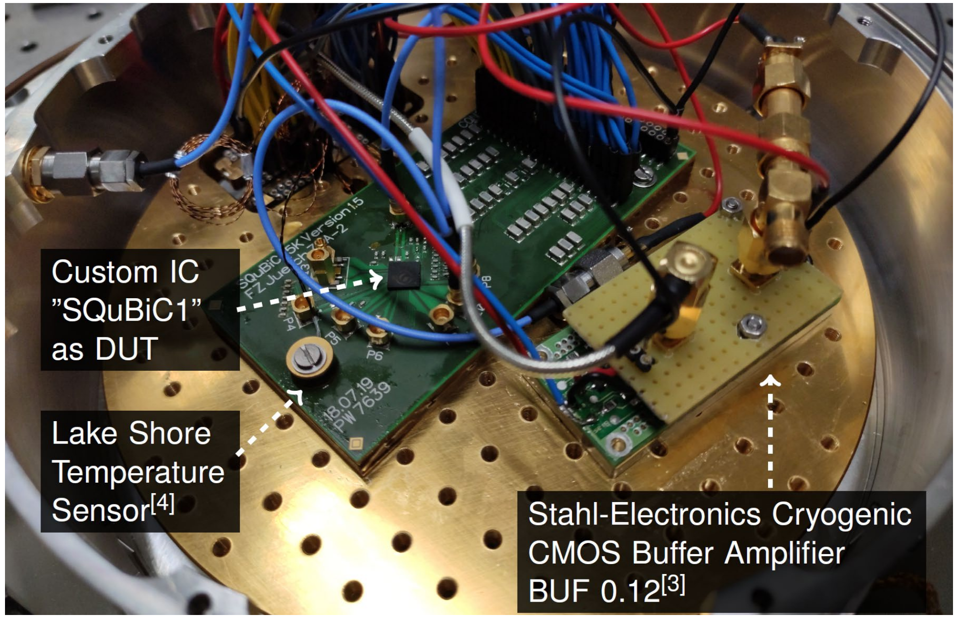
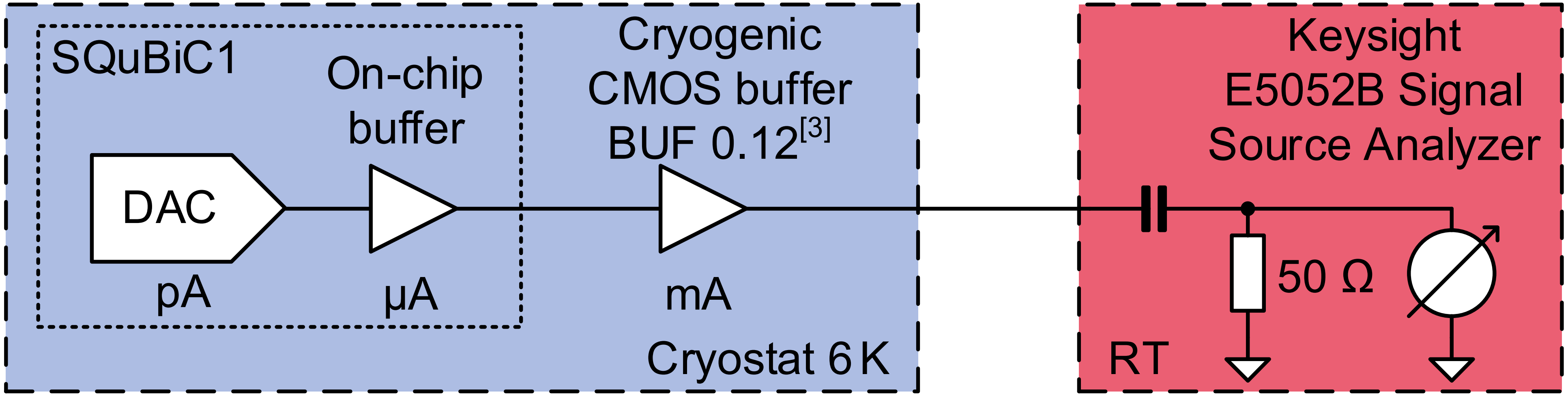
BIAS DAC

Noise Measurement Setup

[4] Lake Shore, DT-670 Silicon Diode, CU package, https://www.lakeshore.com/products/categories/overview/temperature-products/cryogenic-temperature-sensors/dt-670-silicon-diodes



- Noise measurement buffer chain (BC)
  - Impedance conversion: high-ohmic → 50 Ω
  - Gradually increasing driving capability
  - Commercial cryogenic buffer BUF 0.12[3]



[3] Stahl-Electronics, BUF 0.12 Cryogenic CMOS Buffer Amplifier, Datasheet, https://www.stahl-electronics.com/bilder/Datasheet_CryoAmp_BUF_V2-1.pdf

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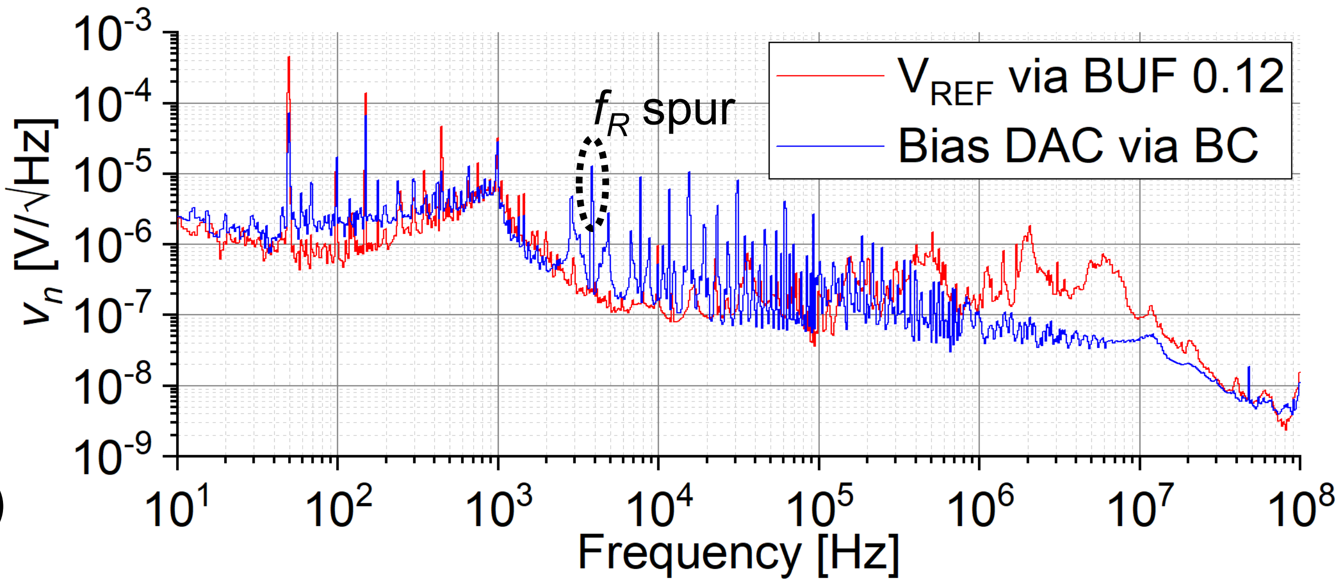
Noise Measurement Results

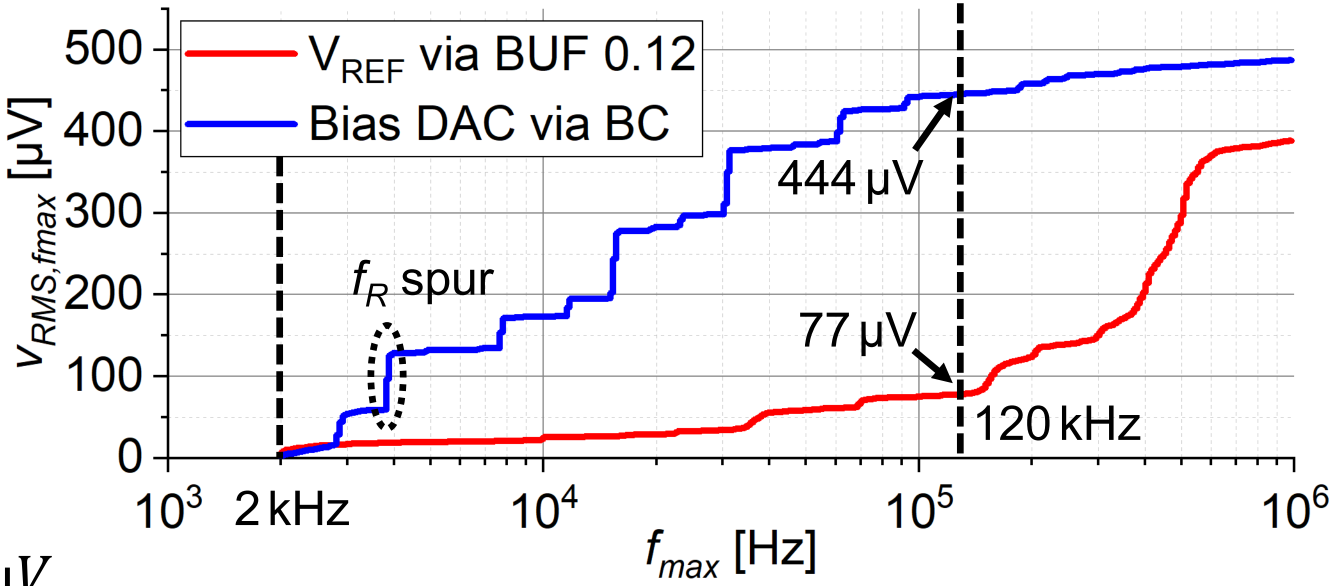
- Noise integrated from 2 kHz to 120 kHz
  - Exclude 50 Hz (spur from power grid)
  - Exclude 1 kHz (spur from power source)
  - BUF 0.12 → DC to 120 kHz
  - Bias DAC refresh rate f_R = 3.9 kHz

$$v_{RMS,fmax} = \sqrt{\int_{2\,\mathrm{kHz}}^{f_{max}} v_n^2(f)\,\mathrm{d}f}$$

- Noise added by Bias DAC

$$v_{RMS,DAC} = \sqrt{(444\ \mu V)^2 - (77\ \mu V)^2} = 437\ \mu V$$





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Power

[2]

Bias DAC component	Power Consumption
Analog DAC core (slide 7)	77 nW
Analog DAC reference voltages	3 nW
DAC digital (memory & logic)	21 µW
DAC total	21.1 µW (2.63 µW per channel)
Clock buffer	4.3 µW
Total	25.4 µW (3.18 µW per channel)

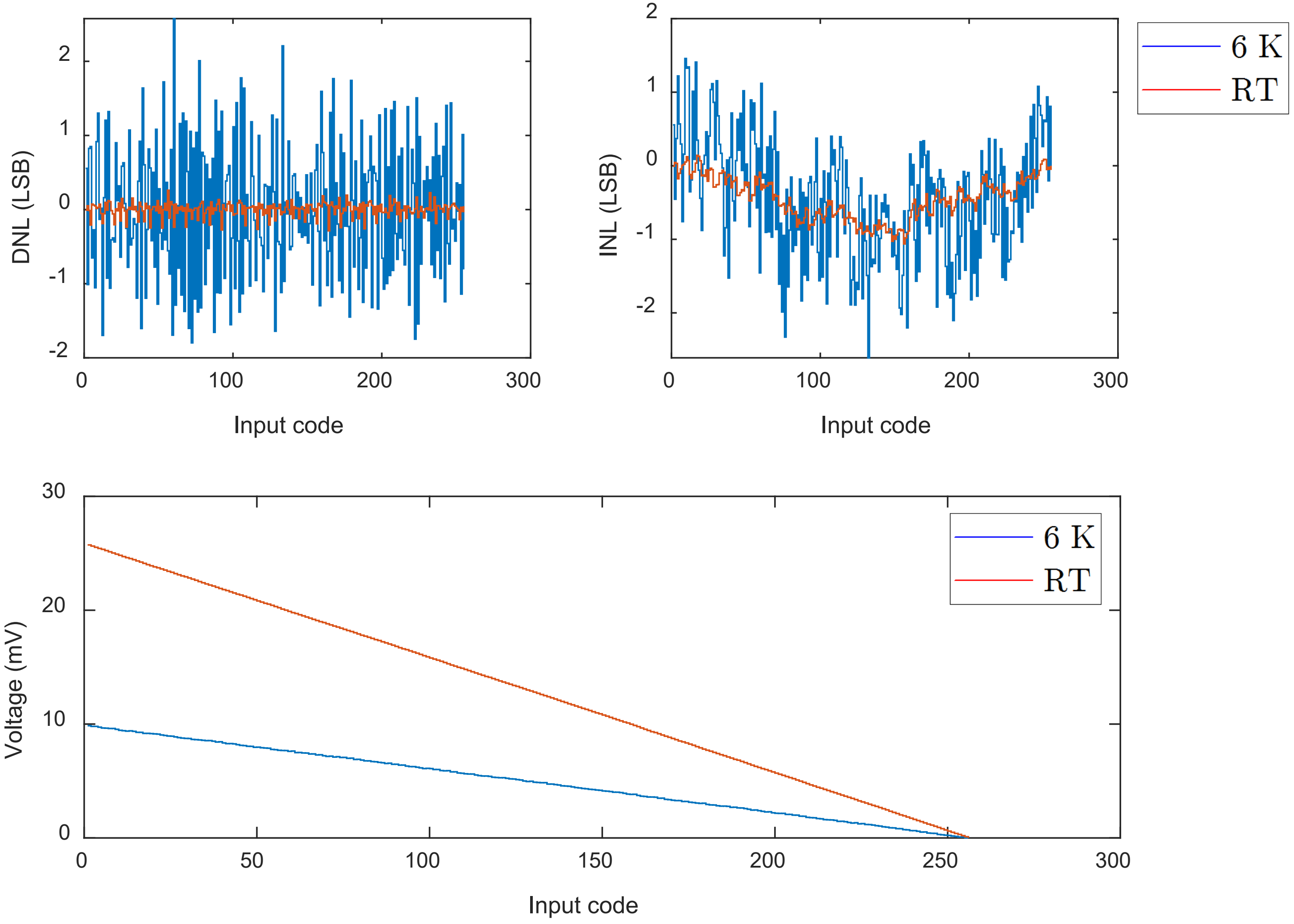
- 8 Bias DAC channel running and f_R = 3.9 kHz
- Ultra-low power consumption ≈ 3 µW per channel
  - Digital part > 99% → Scales well with CMOS technology

[2] P. Vliex et al., "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications," in IEEE Solid-State Circuits Letters, vol. 3, pp. 218-221, 2020, doi: 10.1109/LSSC.2020.3011576.

PULSE DAC

Measurement

- Current steering DAC
- At cryogenic temperatures INL and DNL worse due to increased mismatch
- Can be improved by calibration



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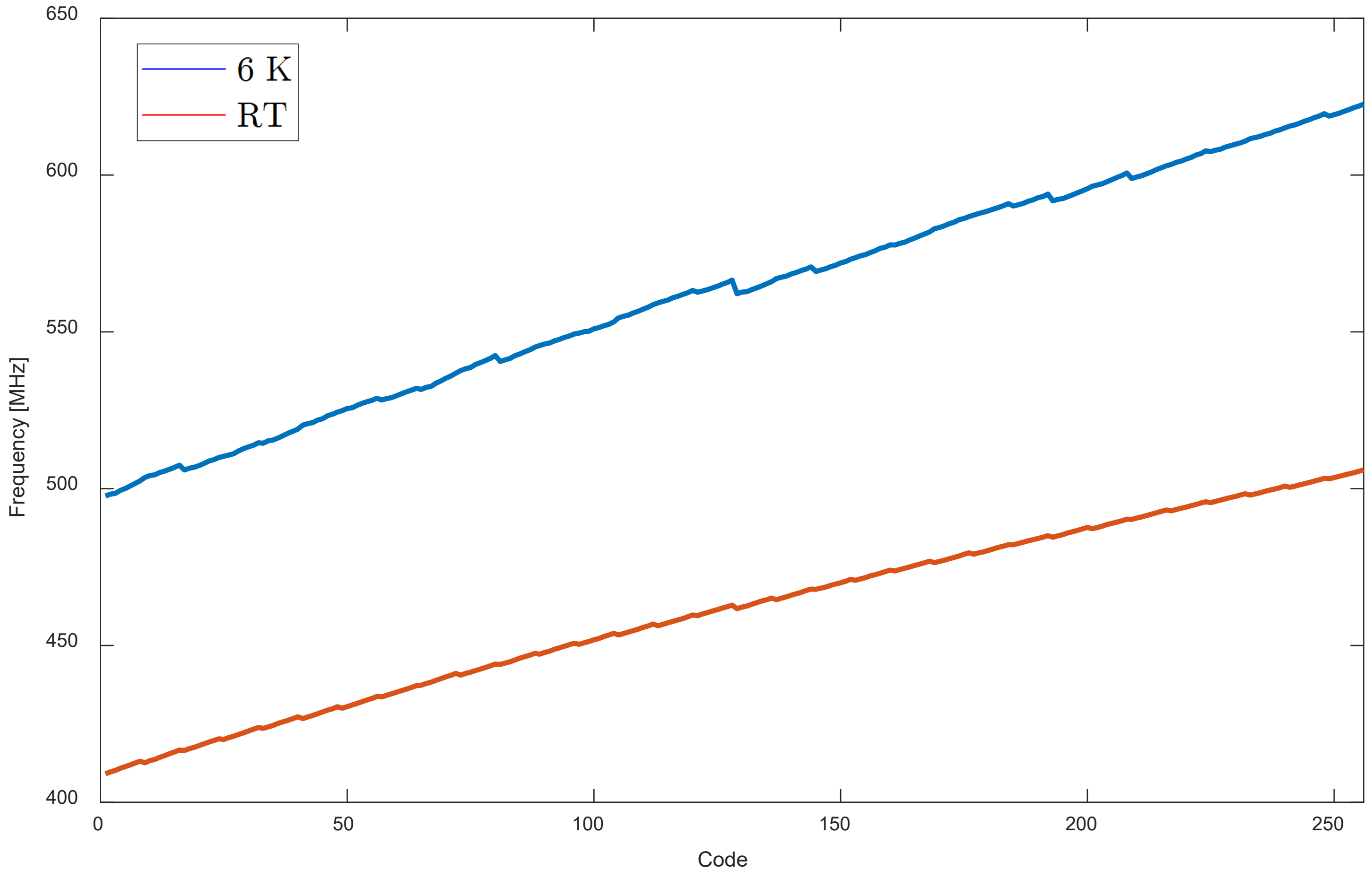
DCO

Digital controlled oscillator

- Current starved ring oscillator
- Frequency shifts to higher frequency at 6 K
- Non monotonic behavior due to mismatch (increased at 6 K)

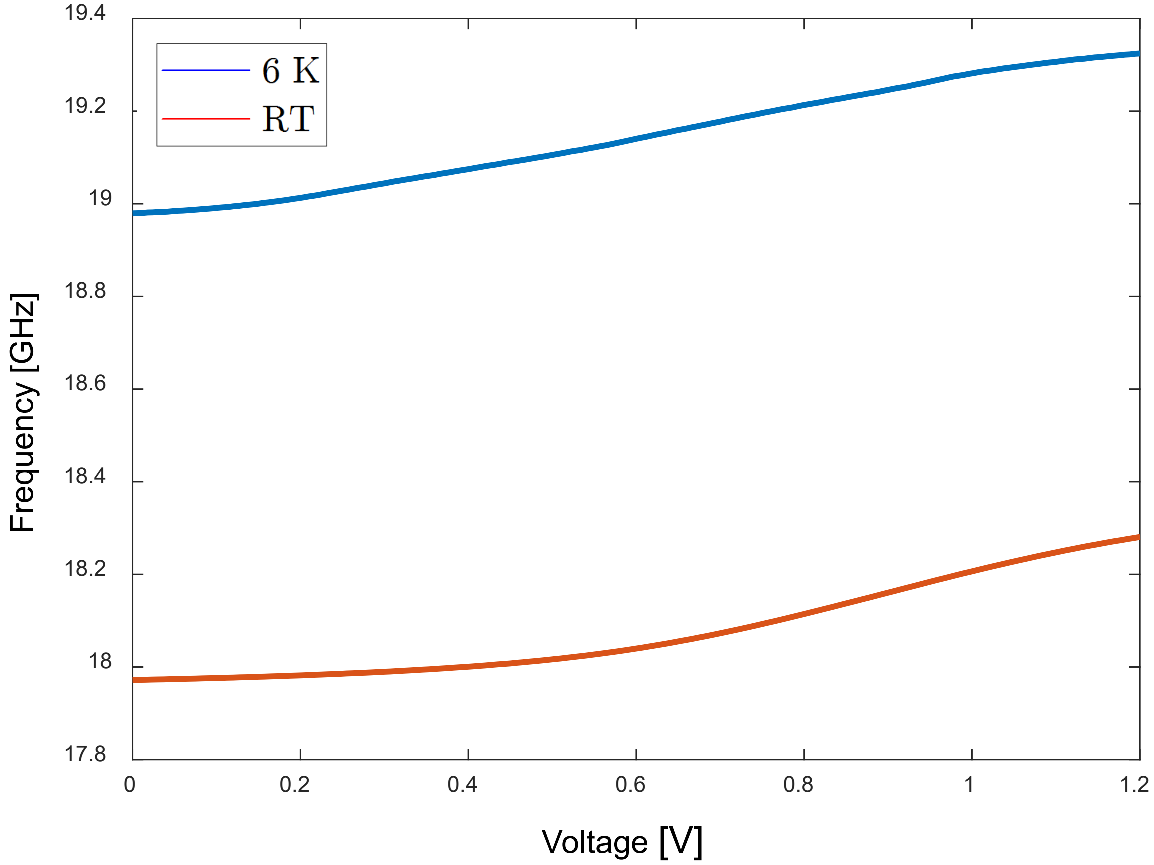


VCO

Voltage controlled oscillator

- LC oscillator
- Center frequency increased by ~5%
- Smaller gain but increased linear region

Temperature	300 K	6 K
KVCO	425 MHz/V	375 MHz/V
Frequency-span	310 MHz	324 MHz
Center-frequency	18.12 GHz	19.15 GHz



SUMMARY

Outlook

- SQuBiC1: IC for local qubit biasing and control
  - Incl. additional measurement and support circuitry

- Promising performance results at 6 K
  - All circuits are tuned operational

- Next steps:
  - Ongoing effort to test with a qubit sample (Prof. Bluhm's group at RWTH Aachen)
  - SQuBiC1 on 100 mK interposer