# Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications

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# Outline

- Motivation: quantum computers & cryogenic electronics
  - Requirements for GaAs spin qubit biasing
- Prototype IC for local cryogenic qubit biasing (Bias DAC)
  - Topology
  - Coarse tuning reference voltages
    - Benefits and calibration method
  - Bias DAC results
  - Auxiliary circuits results
    - OpAmp buffer
    - ∑Δ modulator
- Summary & Outlook

# Quantum Computers

- Possible **exponential speed up** for certain tasks:
  - Shor's algorithm for **factoring integers**
  - Grover's algorithm for **search in unordered databases**
  - **Quantum chemistry**: Simulate new molecules and catalysts
  - Quantum(-enhanced) machine learning

- Requirements for a universal quantum computer:
  - **Large number ($10^6$-$10^8$) of physical qubits[1]** (operated at T $\lesssim$ 1K)
  - Room temperature electronics to communicate with the qubits
  - **Scalable control and read-out electronics**

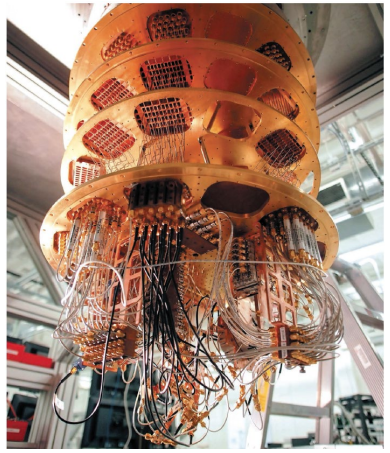
[1] Vandersypen, L.M.K., Bluhm, H., Clarke, J.S. *et al.* Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent. *npj Quantum Inf* **3,** 34 (2017). https://doi.org/10.1038/s41534-017-0038-y

# Quantum Computers

- ‘Brute force’ scaling to operate up to 50-100 qubits
- Further scaling very difficult
- The ‚Tyranny of numbers‘ (Jack Morton, Bell Labs, 1958) is back
- **Let‘s solve it (again) with integrated circuits**

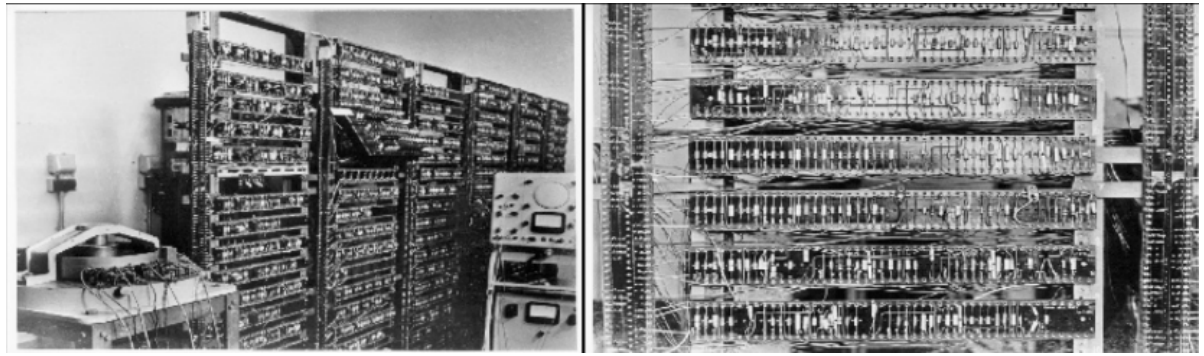
Today

Source: IBM



Source: Google, Mohseni et al., Nature 543 (2017)

1950s



Source: IBM

# Requirements GaAs Spin Qubit

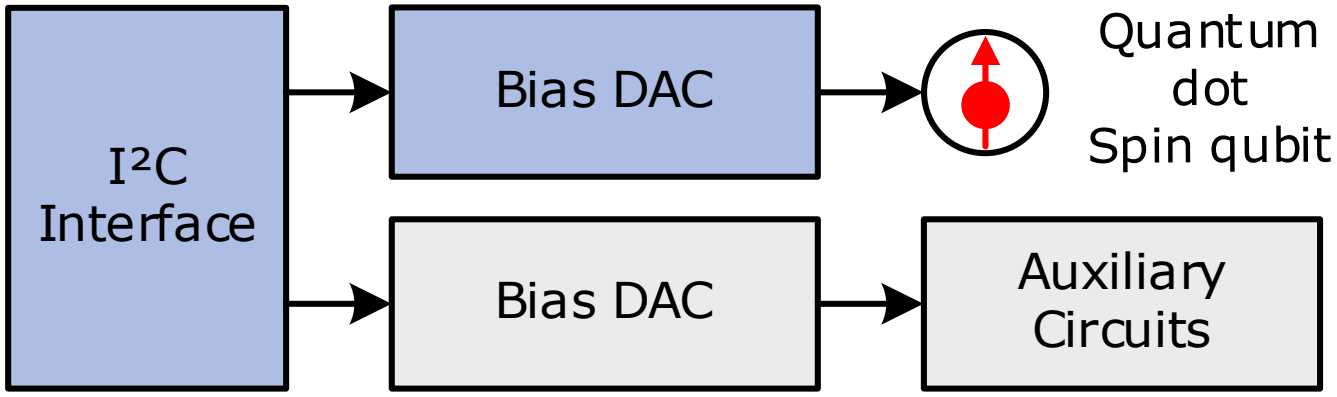
| Characteristic | Specification |
|---|---|
| Bias voltage range | −1 V to 0 V |
| Bias voltage noise $v_{RMS}$ | ≲ 20 µV |
| Bias voltage step size | 250 µV (≙12 bit) |
| Operating temperature | 100 mK |
| Cooling power budget @ 100 mK | <1 mW |

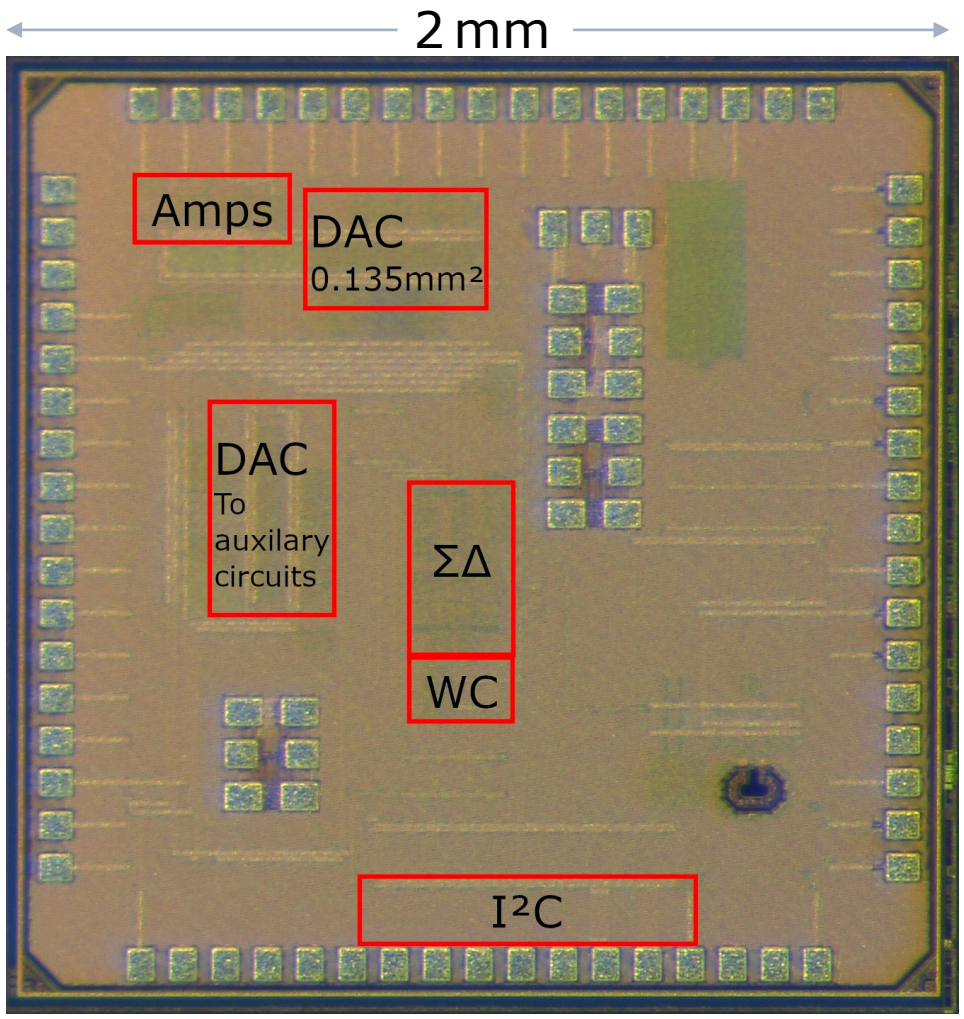
- Up to 8 uncorrelated bias voltages per qubit
  - Forming potential wells

- Key performance indicator: fidelity of qubit gate

# Prototype IC

- TSMC 65nm CMOS technology
- Bias DAC duplicate for measurement purposes
  - Auxiliary circuits
    - OpAmp buffer/amplifier
    - ∑Δ modulator

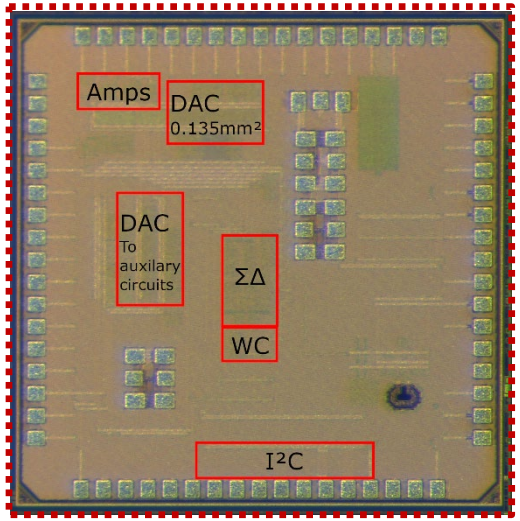


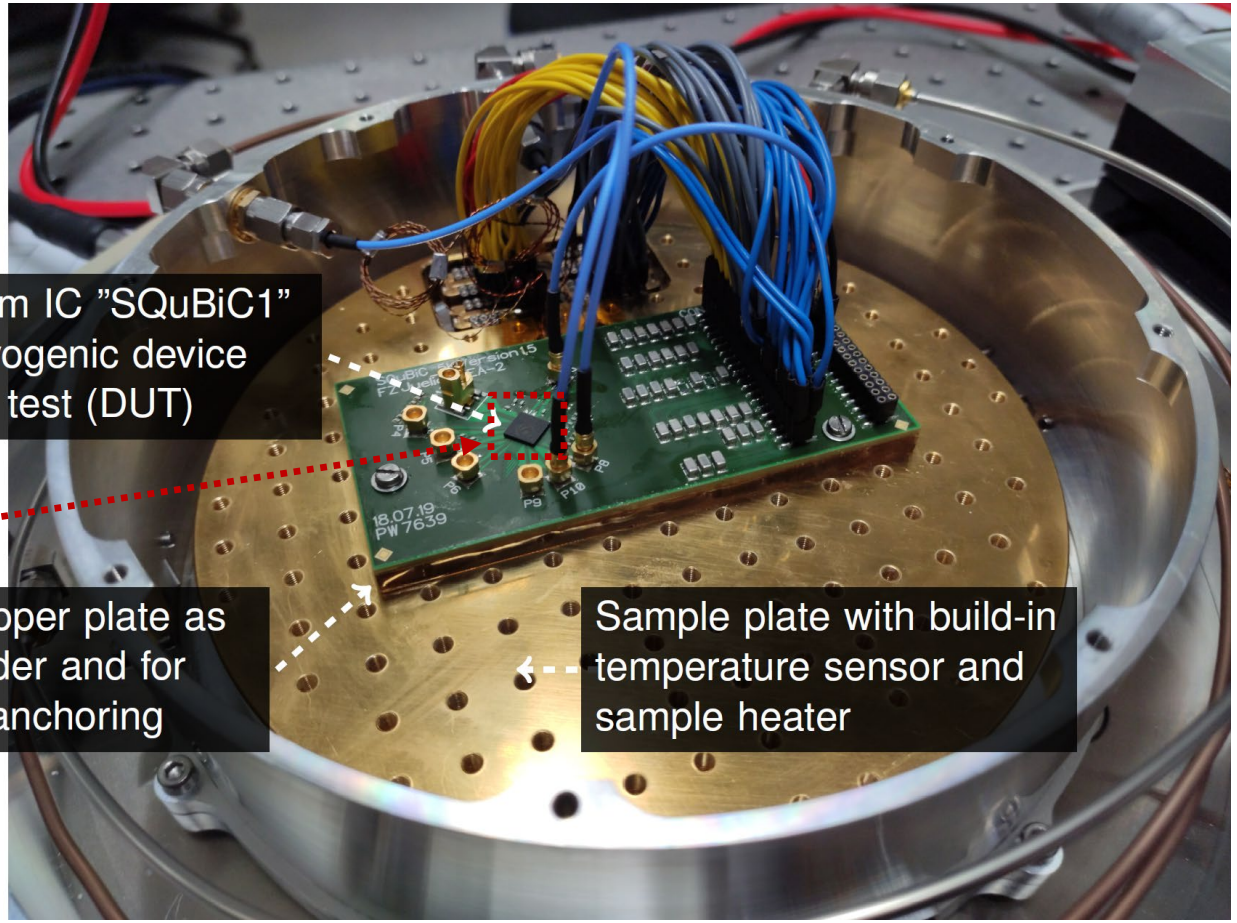




Source: Forschungszentrum Jülich GmbH

# Measurement Setup

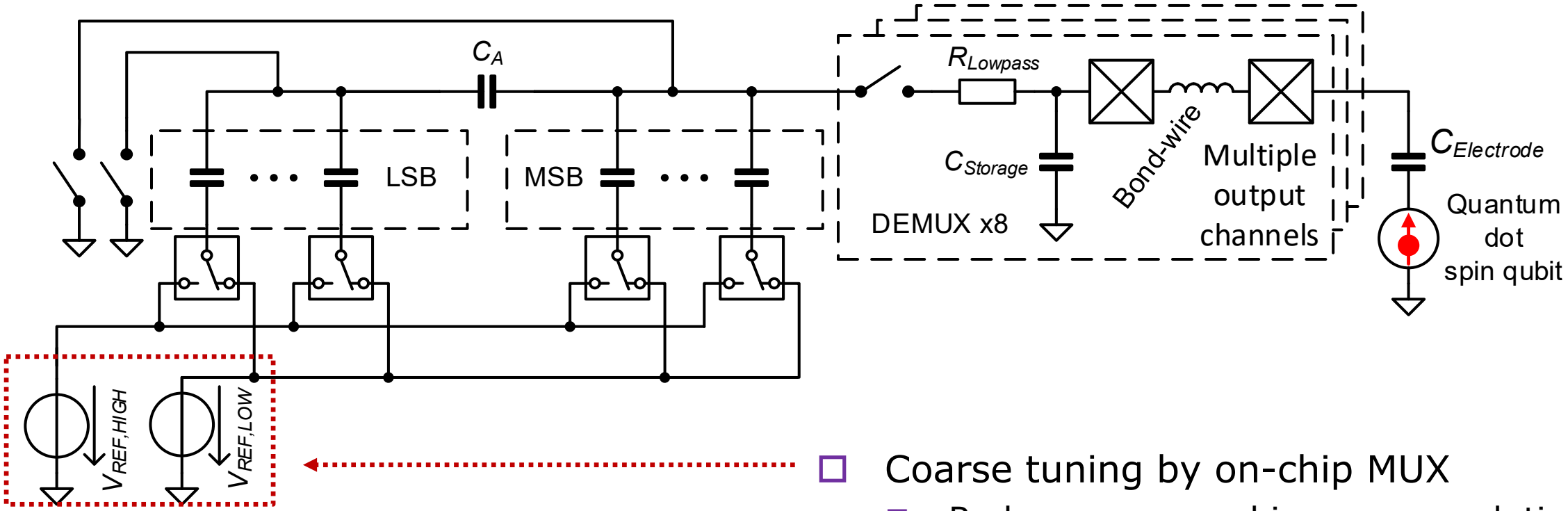
- Packaged IC sample inside cryostat
- Cryostat base temperature approx. 6 K




Source: Forschungszentrum Jülich GmbH

# Charge-Redistribution Topology




- Negligible static power
- Low thermal noise at cryo. temp.

$$\bar{v}_N^2 = \frac{k_B T}{C}$$

- Coarse tuning by on-chip MUX
  - Reduce power and increase resolution
  - But: need for calibration
- Multiple output channels per DAC
- No output buffer needed
  - Reduce power and noise

# Coarse Tuning Reference Voltages

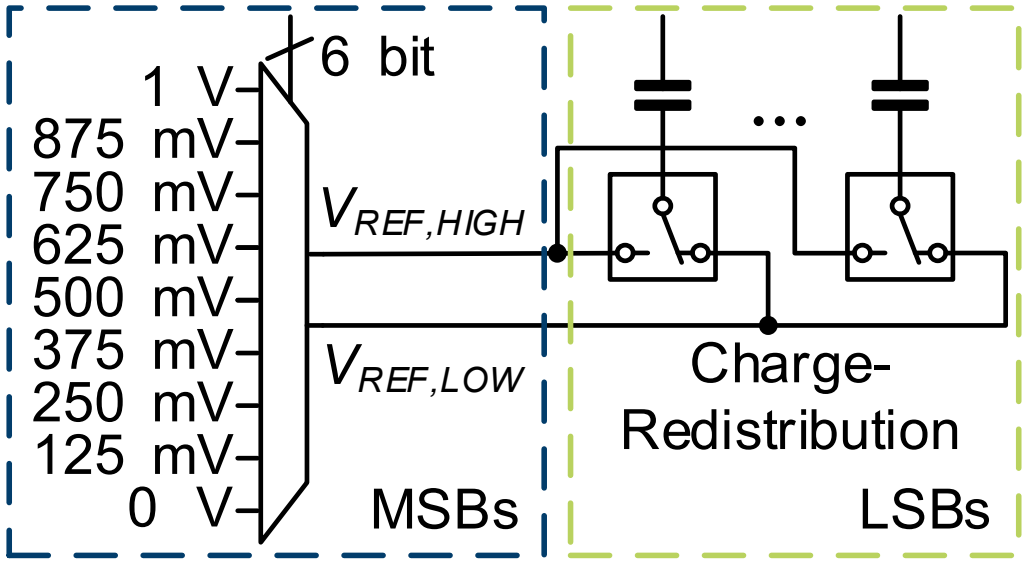
- Coarse tuning by on-chip MUX
  - Reduce dynamic analog power $P_{AD}$

$$\Delta V_{REF} = V_{REF,HIGH} - V_{REF,LOW}$$

$$P_{AD} \propto C_{Total,DAC} \cdot (\Delta V_{REF})^2 \cdot f$$

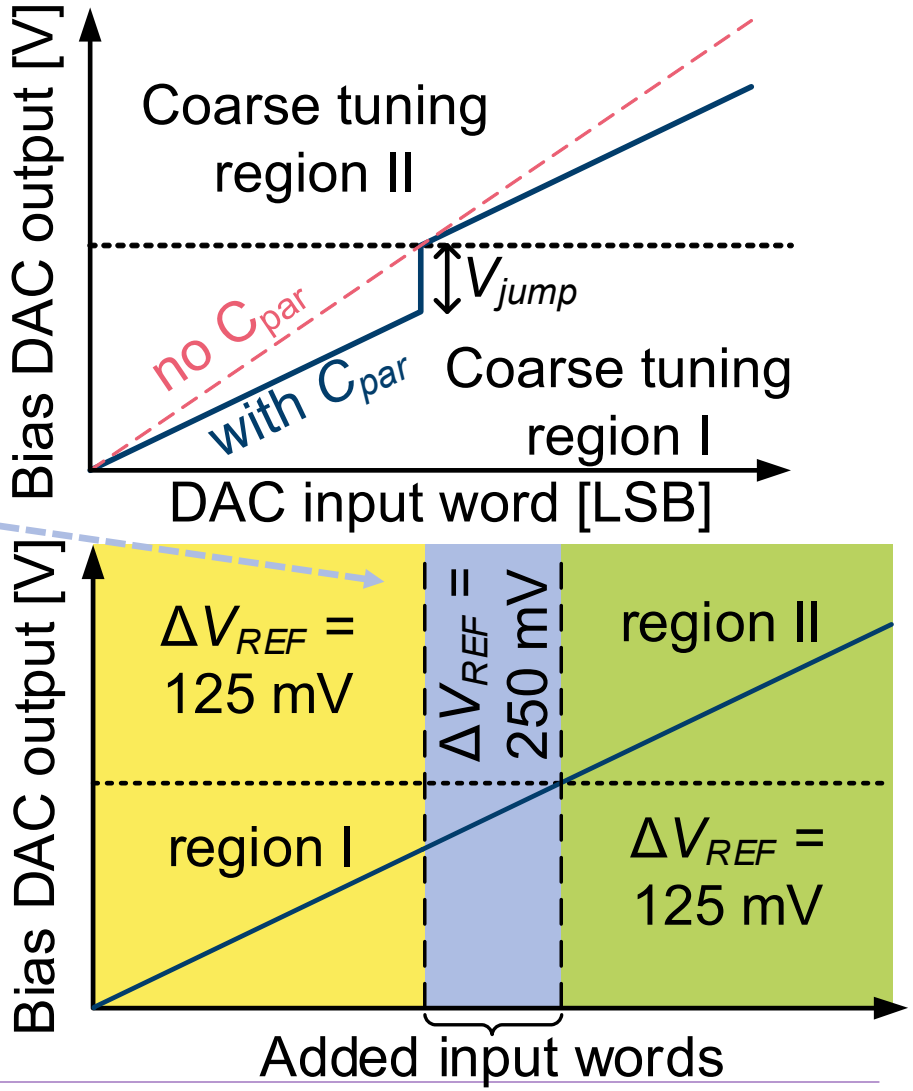
  - $P_{AD}\downarrow$ by (125 mV / 1 V)² = 1/64

- Resolution increased
  - 3 bit added for VREF,HIGH and VREF,LOW each
  - DAC resolution ↑ by 3 bit



# Coarse Tuning Reference Voltages

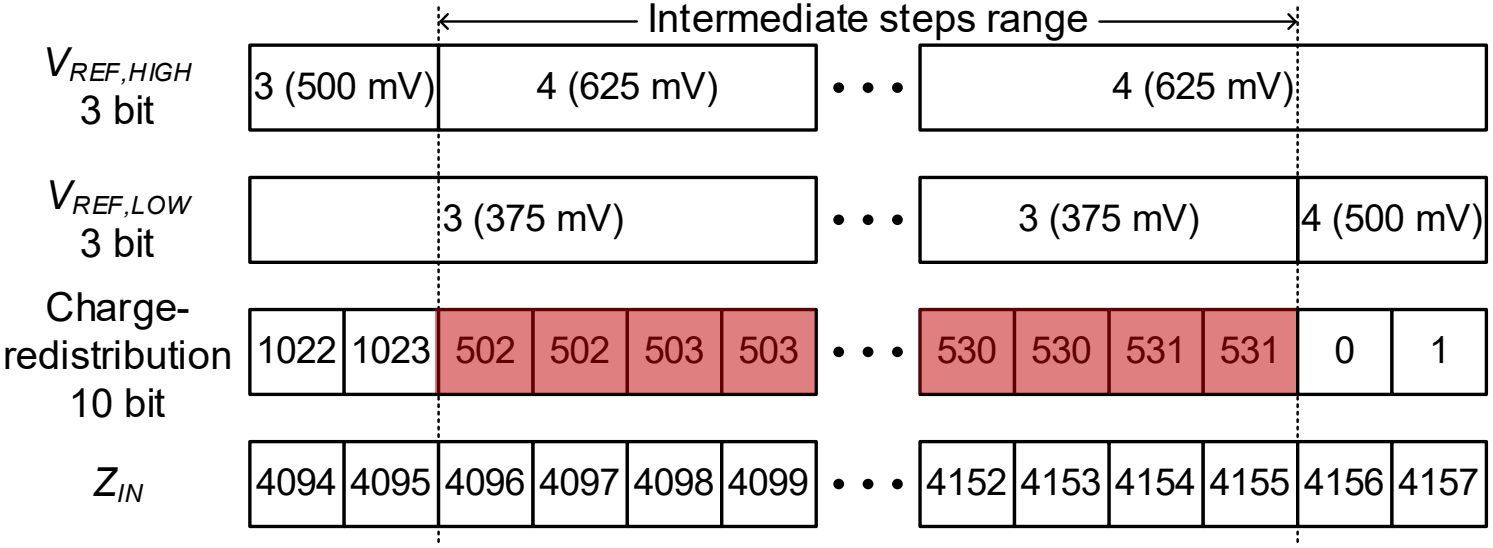
- Coarse tuning by on-chip MUX
  - Parasitic $C_{par}$ leads to DAC gain < 1
    → Voltage jump $V_{jump}$ at coarse tuning crossings
  - Introduce *intermediate steps*
    - Filling the missing codes range
    - Operated with $\Delta V_{REF}$ = 250 mV
    - Add input words
      → Saved in off-chip memory

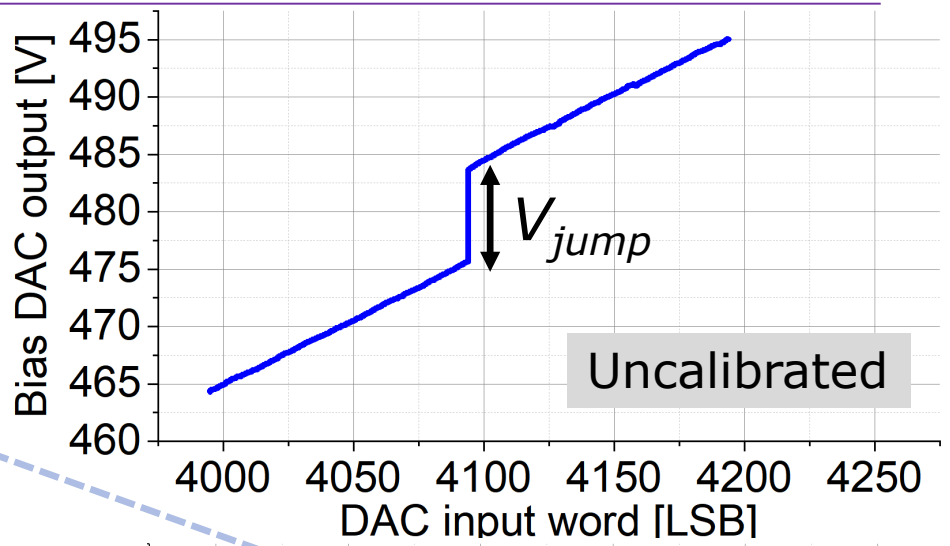


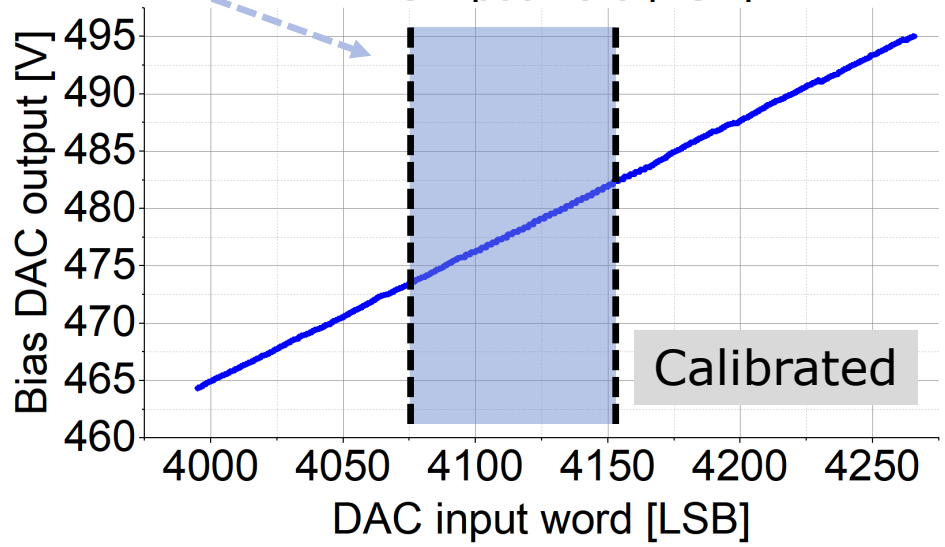
# Coarse Tuning Reference Voltages

- Calibration verified at 6 K
  - *Intermediate steps*
  - Steps doubled

→ Correcting Bias DAC gain

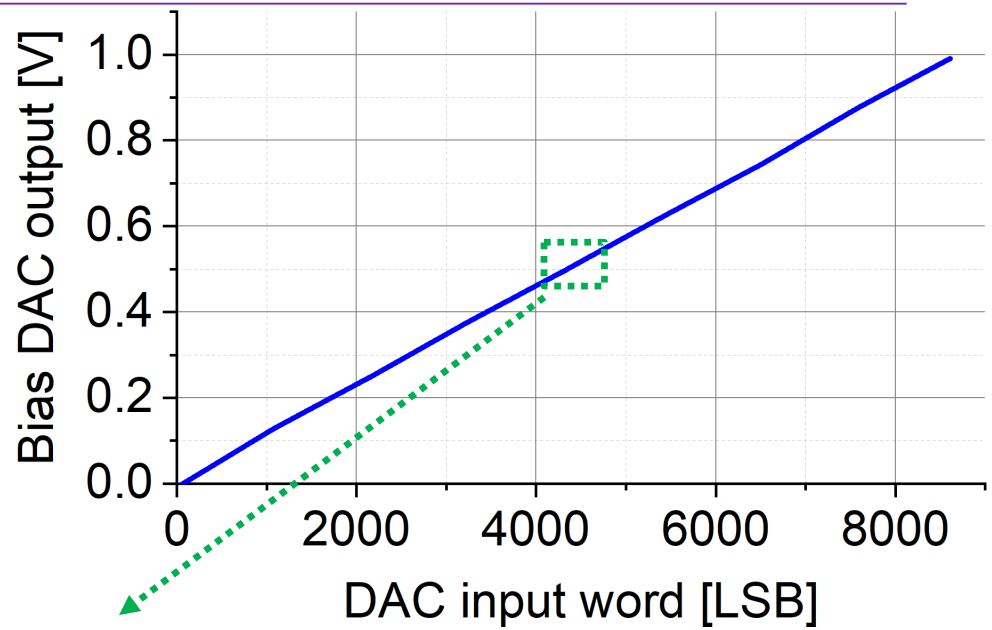


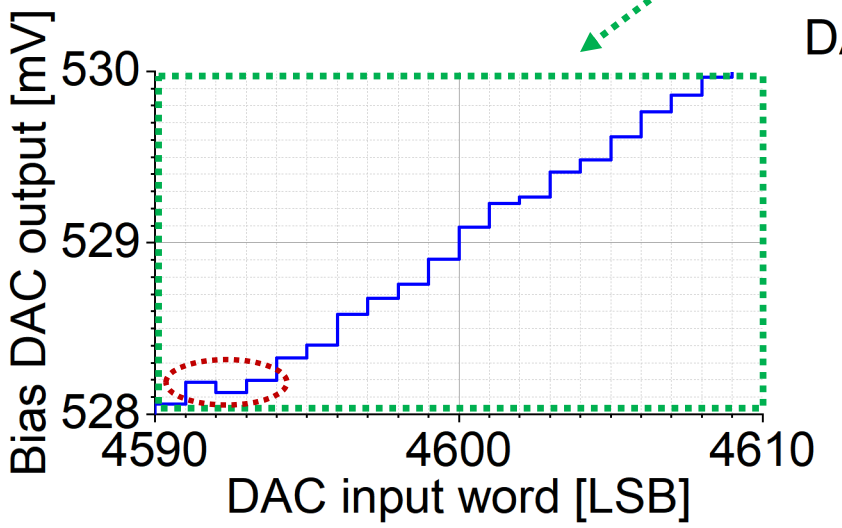



# Bias DAC Results

- Fully functional at 6 K
  - 13 bit resolution (≈ 120 µV step size)
  - 1 V output range
  - Channel refresh rate $f_R$ of 3.9 kHz
  - Calibrated reference voltage coarse tuning
- Singular non-monotonic steps
  - No issue for qubit biasing



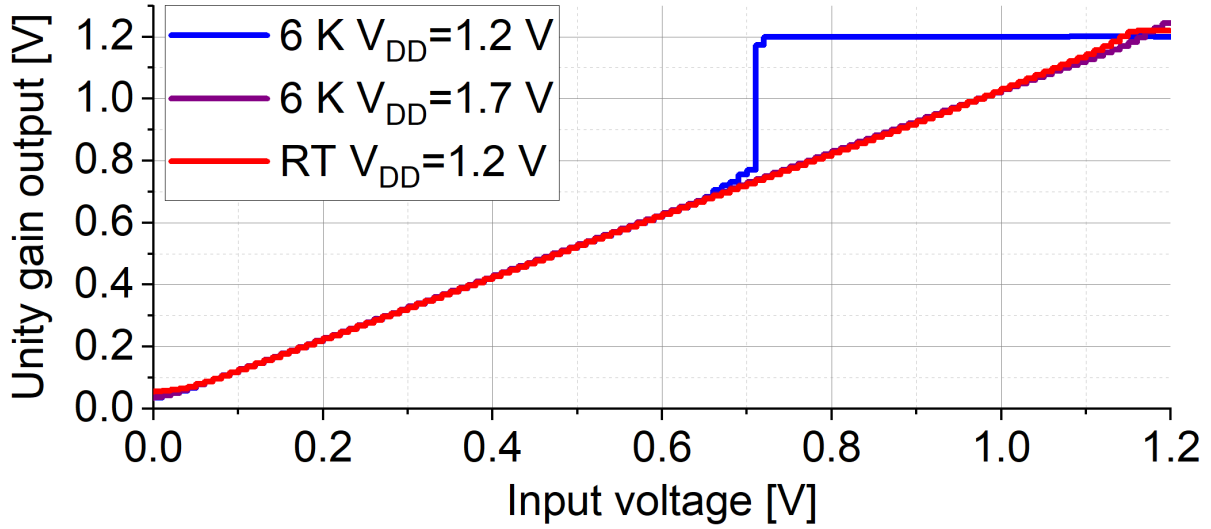
# Bias DAC Power Consumption

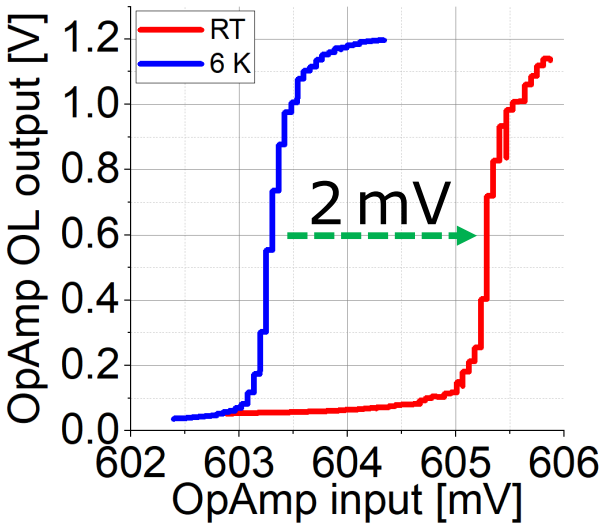
| Bias DAC component | Power Consumption |
|---|---|
| Analog DAC core (slide 7) | 77 nW |
| Analog DAC reference voltages | 3 nW |
| DAC digital (memory & logic) | 21 µW |
| DAC total | 21.1 µW (2.63 µW per channel) |
| Clock buffer | 4.3 µW |
| Total | 25.4 µW (3.18 µW per channel) |

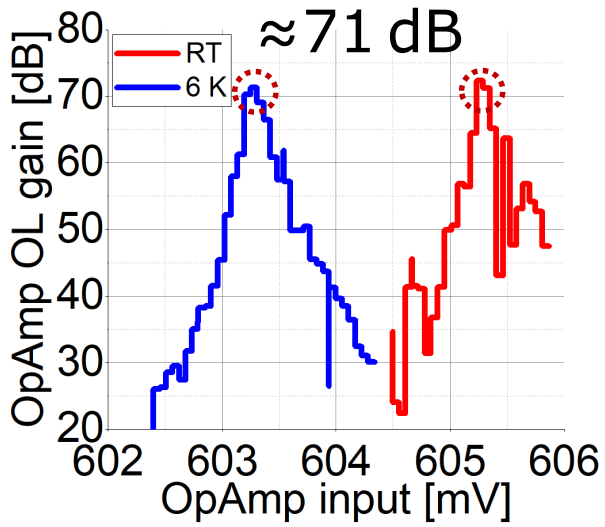
- 8 Bias DAC channel running and $f_R$ = 3.9 kHz
- Ultra-low power consumption ≈ 3 µW per channel
  - Digital part > 99% → Scales well with CMOS technology

# OpAmp Results

- Unity gain configuration
- Enable Bias DAC noise measurement
- Supply increase: 1.2 V to 1.7 V at 6 K
- Small offset voltage shift of ≈ 2 mV
- Comparable open-loop (OL) gain of ≈ 71 dB

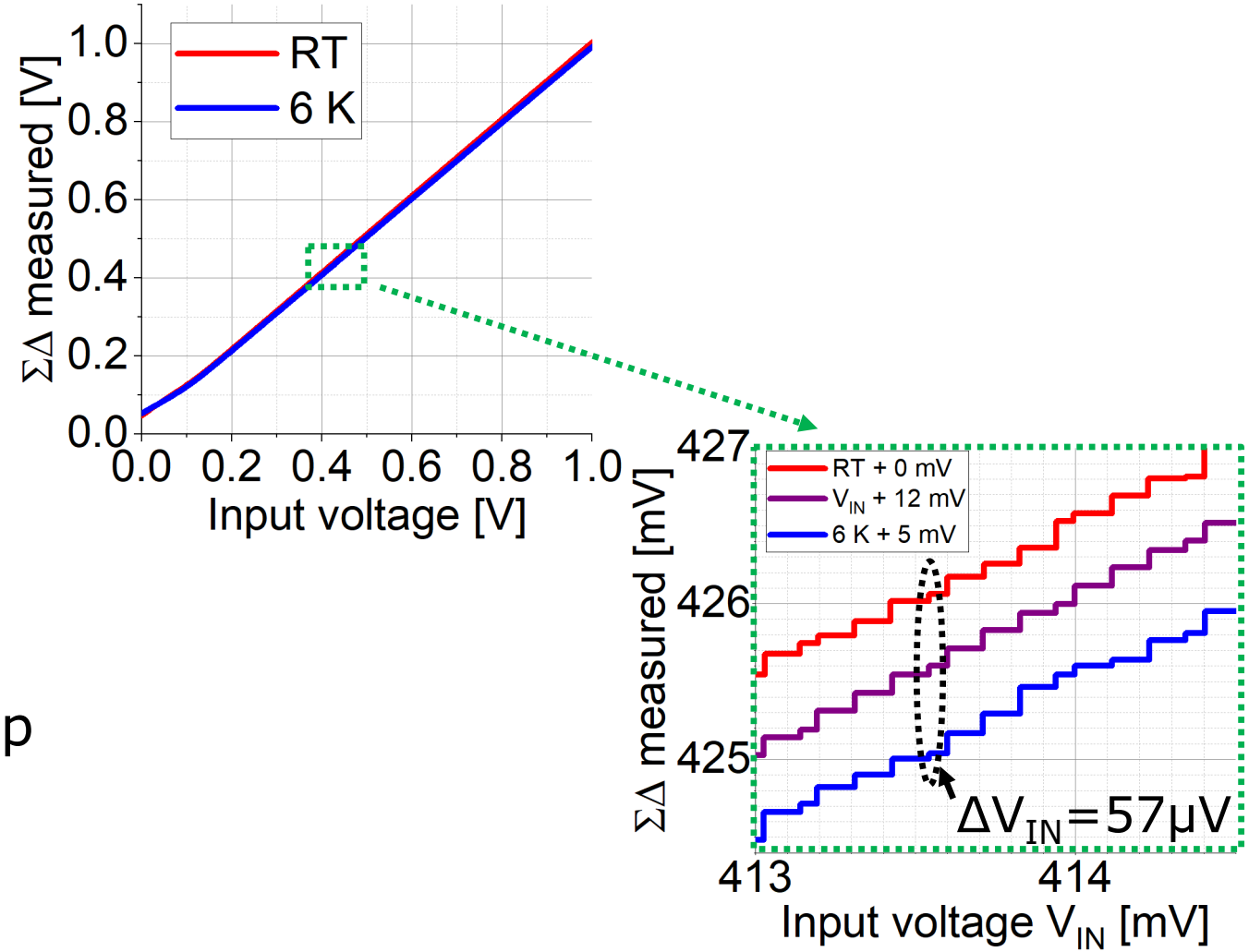


# ∑Δ Modulator Results

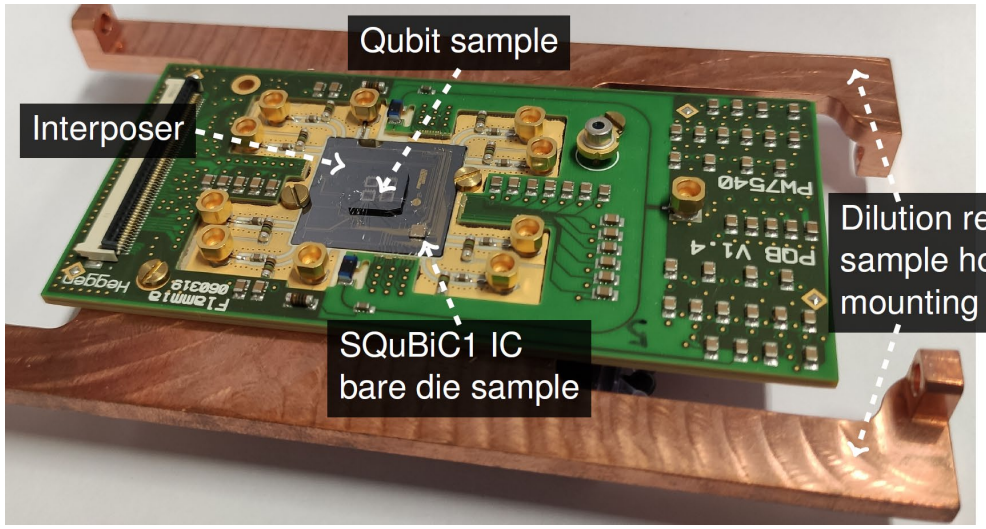
- Measurement at 6 K
- On-chip analog-to-digital conversion
  - 3rd order 2-1 MASH modulator
- Off-chip bit-stream filtering
- Building block for future on-chip Bias DAC calibration



# Summary & Outlook

- Prototype IC for local qubit biasing
  - Incl. additional measurement and support circuitry
  - All circuits are tuned operational at 6 K
  - Bias DAC power ≈ 3 µW per channel

- Next steps:
  - Ongoing effort to test with a qubit sample
    - (Prof. Bluhm‘s group at RWTH Aachen)
  - IC sample on 100 mK interposer




Source: Forschungszentrum Jülich GmbH

- [1] Vandersypen, L.M.K., Bluhm, H., Clarke, J.S. *et al.* Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent. *npj Quantum Inf* **3,** 34 (2017). https://doi.org/10.1038/s41534-017-0038-y
- P. Vliex et al., "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications," in IEEE Solid-State Circuits Letters, vol. 3, pp. 218-221, 2020, doi: 10.1109/LSSC.2020.3011576.