Current-limiting amplifier for high speed measurement of resistive switching data

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(Dated: 12 February 2021)

Resistive switching devices, important for emerging memory and neuromorphic applications, face significant challenges related to control of delicate filamentary states in the oxide material. As a device switches, its rapid conductivity change is involved in a positive feedback process that would lead to runaway destruction of the cell without current, voltage, or energy limitation. Typically, cells are directly patterned on MOS transistors to limit the current, but this approach is very restrictive as the necessary integration limits the materials available as well as the fabrication cycle time. In this article we propose an external circuit to cycle resistive memory cells, capturing the full transfer curves while driving the cells in such a way to suppress runaway transitions. Using this circuit, we demonstrate the acquisition of 10^5 I,V loops per second without the use of on-wafer current limiting transistors. This setup brings voltage sweeping measurements to a relevant timescale for applications, and enables many new experimental possibilities for device evaluation in a statistical context.

I. INTRODUCTION

Today, much effort is focused on employing emerging materials and physical mechanisms for the purpose of data storage and computation[1–5]. Several schemes make use of Resistive Switching (RS), which refers to a large class of related phenomena wherein the resistance of a two-terminal device can be controlled via electrical stimuli[6]. These effects can be used, as in Resistive Random Access Memory (RRAM), to store bits as non-volatile resistance states. Resistive switches can be fabricated using wide variety of CMOS-compatible materials, and are highly attractive due to their simple device structure, high speed, scalability, and potential for 3D integration as required by next generation memory and computing architectures.

A central challenge for RRAM is the intrinsically stochastic nature of the RS process, which leads to large variability in the programmed resistance states and switching parameters[7,8]. Achieving an acceptable level of control over the switching process will require an in-depth understanding of the statistical processes at play, as well as an optimization of active material together with the control circuitry. For this purpose, it is necessary to drive memory cells through a statistically significant number switching cycles, and to rapidly test different materials and modes of operation on a wafer probing system.

RRAM is commonly benchmarked by direct application of square voltage pulse sequences, but one of the shortcomings of this approach is that only the resulting resistance states are typically recorded, while the dynamics of the conductance changes in the material are very often left unmeasured. Quasistatic I,V loops are an alternative measurement where switching is induced by an applied voltage that is continuously ramped at low speed ($\sim$1 V/s) between positive and negative values. The current resulting from these sweeps is sampled and plotted against the applied voltage as shown in Fig. 1. Such I,V loops are relatively rich in information, and important parameters such as the resistance non-linearity, voltage/current switching thresholds, and details of the transition behavior can be extracted. However, the low speed of the measurement puts excessive electrical stress on the device and makes experiments involving more than a few hundred switching cycles impractical.

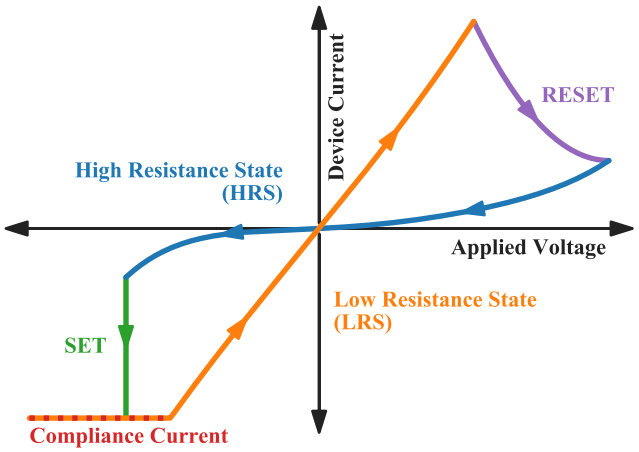

FIG. 1. Schematic diagram of a single cycle I,V loop measurement. Such loops show statistical variation device-to-device and cycle-to-cycle, and important switching parameters may be extracted from their measurement.

While negative resistance transitions in RS materials can occur on timescales below 1 ns[9–11], the nanoscale material volumes involved cannot normally survive prolonged exposure to the voltage required to initiate the transition, as the current density quickly reaches levels that cause irreversible thermal damage[12]. Thus, I,V loop measurements are only possible in the context of a feedback mechanism to prevent runaway destruction of the RS device. Externally implemented current limiting such as the current compliance function of commercial Source Measure Units (SMUs) and Semiconductor Paramater Analyzers (SPAs) are known to cause large overshoots that can lead to catastrophic damage to cells[13,14] (Fig. 2) and can otherwise strongly influence the measurements[15,16]. Patterning RS devices directly on MOS transistors provides superior current limiting, but the required

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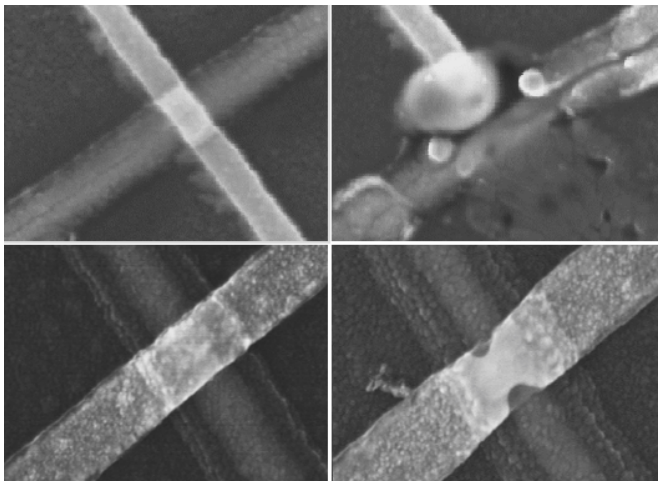

FIG. 2. Crossbar structures (100 nm) before (left) and after (right) being subjected to a current overshoot induced by an SMU with current compliance (top), and capacitive discharge of a 20 cm coaxial cable placed after a current limiting series resistance (bottom). Although the cells are visibly destroyed, both nevertheless continued to show measurable RS behavior, as a conducting path still existed through what remained of the oxide material.

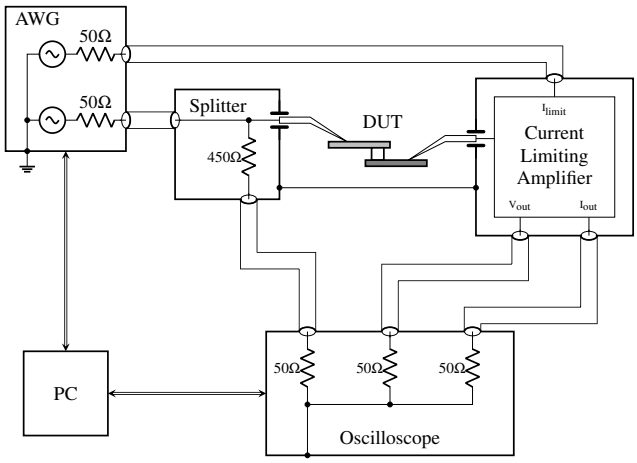

FIG. 3. Schematic of a measurement setup using the current limiting amplifier circuit. A two channel arbitrary waveform generator (AWG) applies a driving signal to the DUT as well as a signal to control the value of the forward current limit. An oscilloscope measures simultaneous samples of the voltage at both electrodes, as well as the device current. A jumper connects the ground planes of the left and right probes to reduce interference and inductance in the signal path.

integration limits the materials available and necessitates long fabrication cycle times[15,17,18]. A simpler approach from the point of view of fabrication is to integrate fixed resistors in series with the devices[19,20]. However, the large linear feedback introduced by this relatively inflexible method significantly affects the switching behavior[21,22], and can push the operating voltage outside of the practical range.

The circuit design reported in this work represents a new way to characterize RS devices. It can be used to suppress current overshoots and collect very large volumes of I,V sweeping characteristics without the requirement of CMOS integration. We demonstrate collection of 10^5 switching cycles per second, which is highly useful for studying the stochastic nature of switching processes.

II. EXTERNAL CURRENT LIMITING AMPLIFIER

A. Design principles

For the purpose of rapidly testing devices with minimal nano-fabrication overhead, compatibility with isolated two-terminal structures is necessary and should be provided by an external Current Limiting Amplifier (CLA) circuit placed in series with the Device Under Test (DUT) in a setup similar to that shown in Fig. 3. When the series combination is driven by a voltage waveform, the circuit should provide a variable current limit in the approximate range 10 μA$-$1 mA in the forward polarity (SET direction). Because of the self-limiting nature of the RESET process under voltage control, current should flow through the circuit unimpeded in the reverse polarity (RESET direction).

To avoid any influence of the circuit on the switching process before the current limit is reached, the circuit should present a negligible impedance for all currents below the limit. Only once the DUT current reaches the limit, the circuit should rapidly transition into a current source behavior to terminate the runaway switching process. In other words, the circuit should ideally present a frequency independent I,V characteristic as shown in Fig. 4(a) in series with the device. The circuit should be highly stable for a variety of loads, and its design should be as simple as possible in order to easily distinguish the role of the DUT in measurements of the overall electrical response.

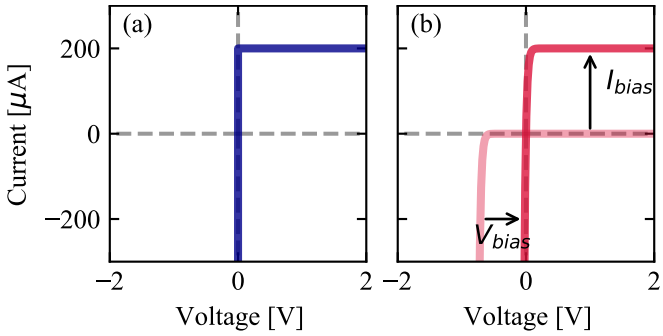

FIG. 4. The current limiting I,V characteristic intended to be placed in series with the DUT. In the ideal case (a), the differential resistance is zero below the adjustable current limit (here 200 μA), and infinite above. An approximation (b) can be realized using a common-base amplifier with voltage and current bias.

Crucially, any overshoot above the current limit following a SET transition should be suppressed as much as possible. Because such overshoots are caused by the stray capacitance at the terminal of the current limiting circuit, this capacitance is considered a critical design parameter to be minimized. It is therefore not an option to connect the CLA to the DUT over a length of coaxial cable, as this would present an effective capacitance of 100 pF/m. To reduce this capacitance, the probing circuit needs to be mounted as close as possible to the DUT, and a short unshielded probe needle should be mounted directly to its circuit board.

The measurement setup should allow application of voltage signals of at least 1 MHz to the device, and a low-noise current output should have a resolution below 1 μA and should be able to register fast rise times of switching events below 100 ns. The bandwidth of signal application and current measurement should not depend strongly on the resistance state of the DUT, nor on the current limit used. External commercial equipment should be used to generate and sample voltage waveforms, where an important requirement is a large enough memory capacity to capture hundreds to thousands of I,V datapoints each switching cycle for $10^5 - 10^6$ cycles per measurement shot.

B. Implementation

The basic idea behind the presented circuit design is to use a single bipolar junction transistor (BJT) I,V characteristic to implement the desired current limiting response while also providing transimpedance amplification of the DUT current. Packaged discrete BJTs for radio frequency applications are available with very low parasitic capacitance, making them highly suitable here for use in the input stage. The common-base (CB) amplifier configuration is of particular interest as a high-bandwidth current buffer, featuring a low input impedance and small feedback capacitance that does not suffer from the Miller effect. With voltage and current biasing, a CB amplifier can closely approximate the targetted current limiting I,V characteristic shown in Fig. 4. A simplified schematic of the input stage used to accomplish this is shown in Fig. 5.

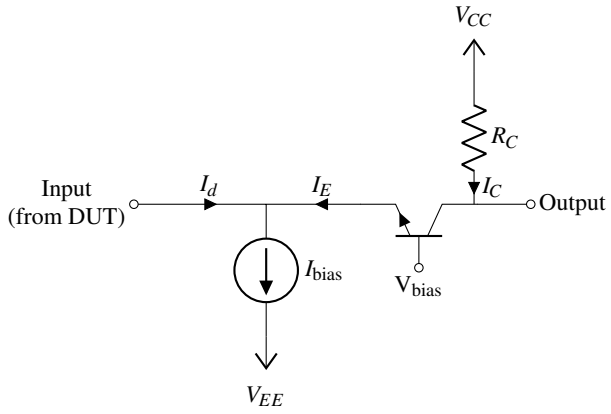

FIG. 5. A simplified diagram of a circuit implementing unipolar current limiting and transimpedance amplification. The value of the forward current limit is set by I_{bias}, and the input voltage is approximately 0 V for input currents below this limit.

The basic operation of this input stage is straightforward to analyze. Applying Kirchhoff's current law at the input node, it can be seen that whenever the DUT current I_d is less than the bias current I_{bias}, the BJT emitter current I_E is positive and transistor will be in forward-active mode. In this mode, with an appropriate setting of $V_{\text{bias}} \approx 0.7$ V, the input voltage V_{in} will be held close to 0 V due to the high forward transconductance of the BJT. Thus, for either positive or negative voltages applied to the DUT, the input stage effectively presents a low impedance to ground as long as $I_d < I_{\text{bias}}$. As I_d approaches I_{bias}, the BJT enters cut-off mode, where its effect in the circuit can be ignored and the input behaves as a current source with $I_d = I_{\text{bias}}$.

Ideally, the voltage bias V_{bias} should be chosen so that the input current is zero for an input voltage of zero (such that the curve of Fig. 4 intersects the origin). Considering an approximated Ebers-Moll model of the BJT, it follows that

$$V_{\text{bias}} = -nV_T \log\left(\frac{I_{\text{bias}}}{I_s} + 1\right), \tag{1}$$

where I_s is the saturation current of the base-emitter junction, $V_T \approx 26$ mV is the thermal voltage, and n is the diode ideality factor. The output of this stage then gives an amplified voltage signal V_{out} that is linearly related to the input current

$$I_d = I_{\text{bias}} - \left(\frac{1+\beta}{\beta}\right)\left(\frac{V_{CC} - V_{\text{out}}}{R_C}\right), \tag{2}$$

where β is the forward common-emitter current gain of the NPN transistor.

A full circuit diagram expanding on this concept is given in Fig. 6, with a prototype PCB layout also pictured in Fig. 7. Here, Q_1 is the CB amplifier corresponding to that depicted in Fig. 5, and a nearly ideal voltage controlled current source is realized by the emitter degenerated cascode amplifier formed by Q_2, Q_3, and R_2. The dependence of the current limit I_{bias} on the control voltage V_c, which is approximately linear for $I_{\text{bias}} > 100$ μA, is calibrated for V_c values between -10 V and -1 V by an SMU measurement. The V_c signal is then generated according to interpolation of the calibration table at the desired I_{bias} values.

Further circuitry in Fig. 6 is included to null voltage offsets and condition the output signals for transmission to 50 Ω oscilloscope inputs. From Eq. 1, it is seen that the ideal value of V_{bias} depends slightly on the value of I_{bias}. Therefore, simply using a constant value of V_{bias} would create offset voltages at the input terminal on the order of $10 - 100$ mV as I_{bias} is varied. To automatically compensate this effect, a reference path R_3, Q_4, Q_5, Q_6, R_4 mirrors the components R_1, Q_1, Q_2, Q_3, R_2, and is used to actively zero the input offset for all values of I_{bias} via OPA277. This same structure also generates a reference voltage for a differential measurement performed by AD8130, producing a low-offset output signal I_{out} proportional to the input current. A voltage follower (THS3091) with very low input capacitance (0.1 pF) is also placed directly at the input node, providing a simultaneous measurement of the DUT voltage drop.

III. MEASUREMENT RESULTS

Current overshoots accompanying sudden negative resistance transitions are suppressed in our measurement scheme by minimizing the capacitance at the input node of the CLA. This is done by careful selection of the input transistors and by avoiding proximity of input traces to the ground plane. However, the parasitic capacitance cannot be fully eliminated and the potential to create overshoots inevitably remains. Since overshoot transients tend to play a critical role in switching behavior in practice, it is important to characterize and model them.

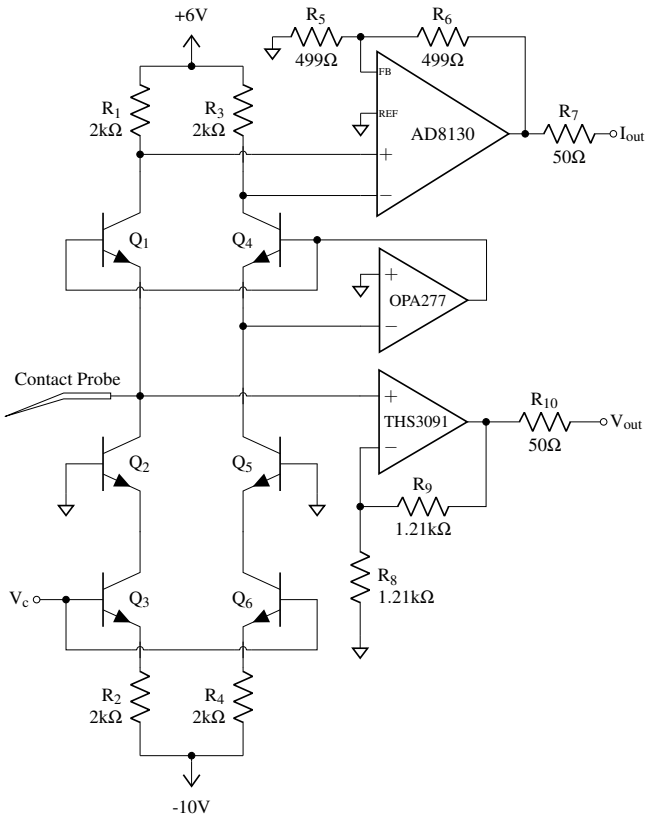

FIG. 6. Full schematic for the current limiting probing circuit. All BJT devices are ON Semiconductor part no. NSVF5501SKT3G. Transistors Q1-Q3 perform the current limiting function, with the current limit controlled by the input signal V_c. Regulated power supplies providing ± 10 V and +6 V are not shown.

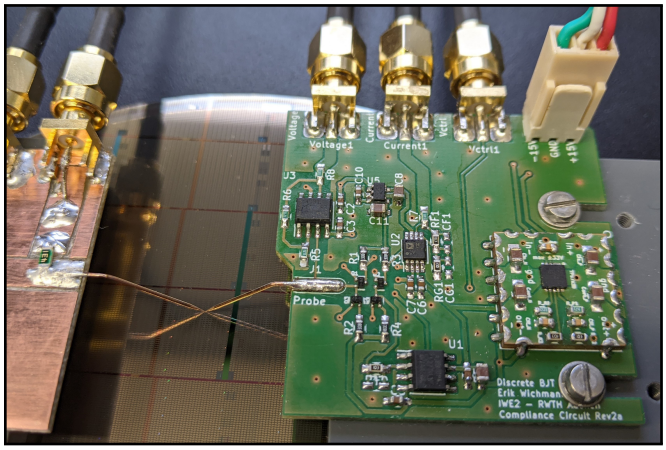

FIG. 7. Photograph of the probing circuit board contacting a prototype RRAM device. Left and right probes are mounted on independent micropositioners.

In general, the time-dependent I,V trajectory of a current overshoot is not solely a characteristic of the measurement setup, but is determined by the coupled dynamics of the DUT conductance and the driving circuitry. The duration and amplitude of the overshoot therefore depends on the type and history of the RS cell being measured, and is not easily reproducible. To measure the overshoot characteristic in a standardized way, a test sample designed to imitate the resistive switching action was constructed using surface mount components. A mechanical reed relay in series with a 1.2 kΩ and in parallel with 100 kΩ was found to be well suited for this purpose, providing a controllable sub-nanosecond transition between two discrete resistance levels with negligible parasitic effects.

With the reed switch connected in the position of the DUT and biased by 1 V, the current transient following a resistance transition was measured with 350 MHz bandwidth (Fig. 8). Close agreement of the transient was found with the solution of a differential equation describing the charging of the CLA input node,

$$C_p \frac{dV_d}{dt} = I_{\text{bias}} \left[1 - \exp\left(\frac{V_d - V_a}{V_T} \right) \right] - \frac{V_d}{R_d}, \qquad (3)$$

where $C_p = 5.7$ pF is the parasitic capacitance at the input, V_d is the DUT voltage drop, V_a is the applied voltage, and R_d is the DUT resistance (here assumed a step function in time). Note that C_p includes the self-capacitance of the measured cell, which is approximately 0.5 pF for the reed relay circuit. This should be taken into consideration in the memory cell design itself, where thin dielectric layers and large contact pads or device areas can contribute significantly to the total C_p, which intrinsically degrades the overshoot performance. Given the single parameter C_p, the simple model of Eq. 3 is expected to accurately characterize the transient response of the CLA circuit, and should be incorporated with a physical device model to properly understand the complete picture of the coupled system during a measurement.

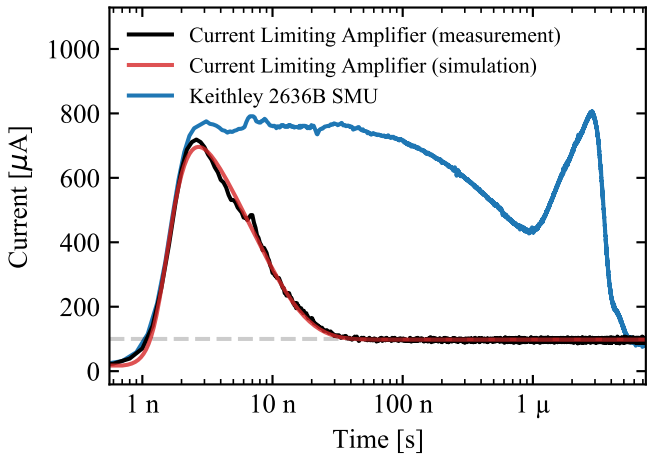

FIG. 8. Current overshoot characterization using a reed relay to abruptly switch from 100 kΩ to 1.2 kΩ at time 1 ns with 1 V applied and with a current limit of 100 μA. Under these conditions, the CLA returned to the current limit in ∼20 ns, whereas a commercial SMU produced a more complex overshoot response lasting several microseconds.

For comparison, the current overshoot transient induced using a modern SMU was measured under identical conditions. For the first 1 μs after the resistance transition, the transient begins with the discharge of a 1 m coaxial cable which must be used to connect the instrument. Between $1-10$ μs, a proprietary feedback circuit is engaged and produces a long unpredictable current excursion before undershooting and eventually settling to the programmed current compliance level.

Relative to this, the overshoot duration is reduced in the CLA measurement by over two orders of magnitude.

To demonstrate the RS cycling operation using the external CLA circuit, we tested a TaOx-based nano-scaled (100 nm) RRAM device of a design which was known not to survive repeated switching using a commercial SMU. With the CLA input connected to the DUT top electrode, the current limit was set to 300 μA and a triangular voltage signal with period 10 μs and amplitude 1.5 V was applied to the DUT bottom electrode using a Rigol DG5102 AWG. The applied voltage and device current were sampled at 1.25 GS/s using a Picoscope 6404D deep-storage oscilloscope. In a single measurement lasting only one second, 10^5 full I,V loops were successfully collected, each containing 1,564 8-bit I,V samples (Fig. 9). It is furthermore possible to collect millions of such cycles in a practical amount of time by collating multiple measurement shots, creating powerful datasets for statistical evaluation of RS devices.

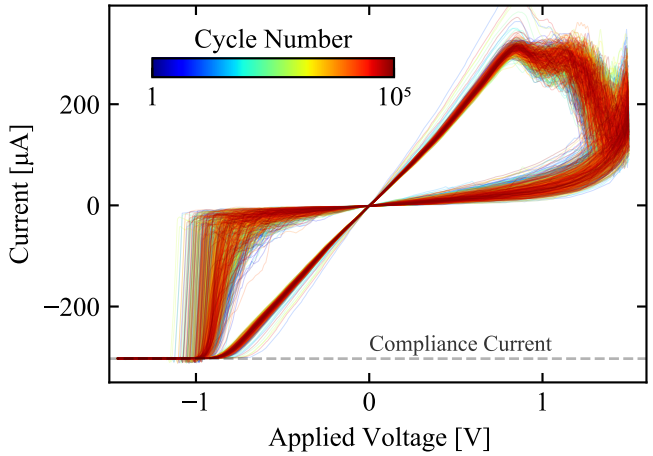

FIG. 9. A measurement of 10^5 consecutive I,V loops collected in one second with the CLA circuit using a triangular voltage excitation and 300 μA current limit. Data is smoothed by a 15 sample moving average, and every 100th cycle is plotted. To conform to plotting convention, the applied voltage is defined as the negative of the AWG voltage.

IV. CONCLUSION

Resistive switching devices are promising building blocks for future memory and neuromorphic architectures, with the salient property of large cycle-to-cycle variability. Conventional lab measurements of these cells commonly represent very different conditions from integrated systems, and often have unclear implications for device applications. In particular, current overshoots during runaway resistance transitions hinder the ability to control and characterize the switching process. In this work, an external current limiting amplifier was developed to reduce the overshoot effect and allow for measurements of full I,V loops at $\sim 10^6$ times faster rates than commercial SMUs. The minimal design with low transistor count is relatively robust against load-induced instability and has the important advantage that its response is accurately predictable using a few idealized component models.

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