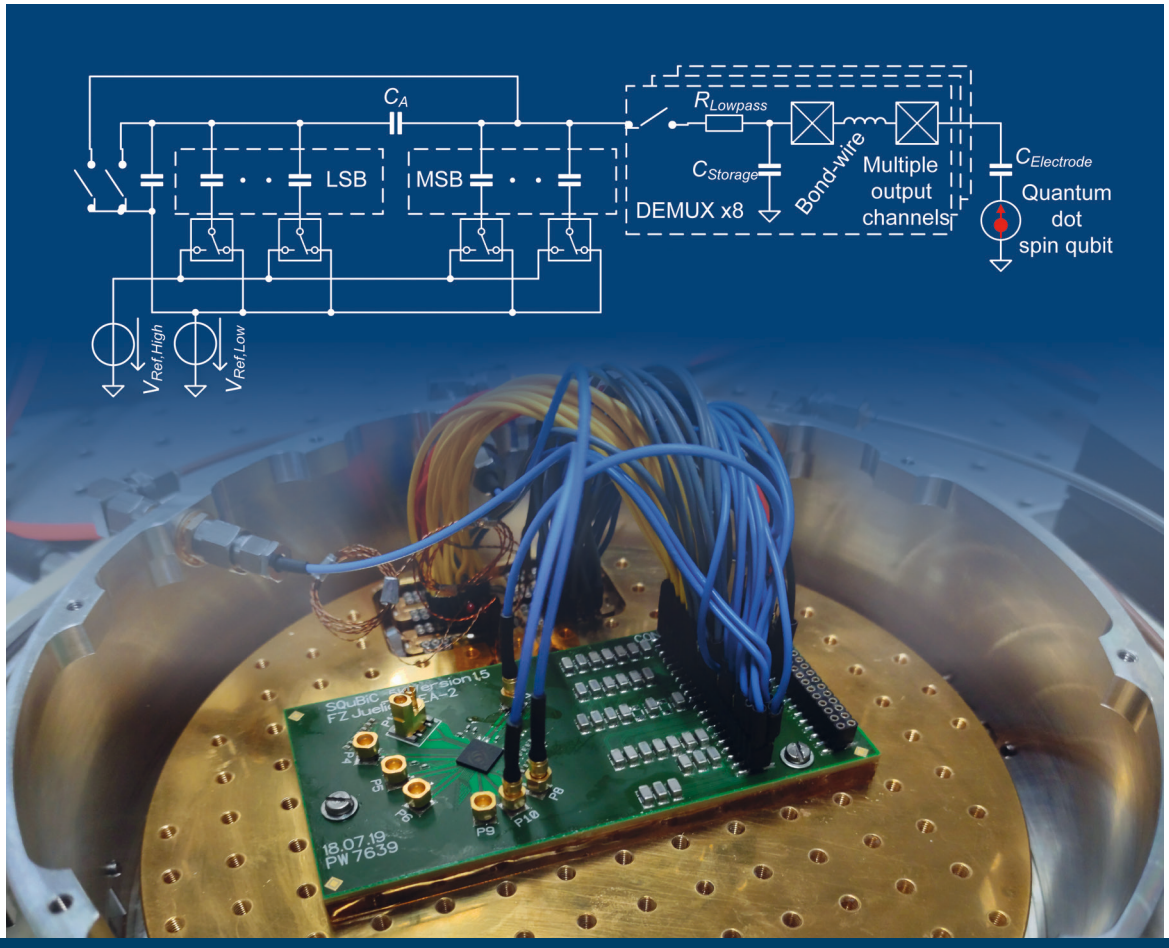


Modelling, implementation and characterization of a Bias-DAC in CMOS as a building block for scalable cryogenic control electronics for future quantum computers

Patrick Norbert Vliex

Information
Band / Volume 74
ISBN 978-3-95806-588-8

Mitglied der Helmholtz-Gemeinschaft

JÜLICH
Forschungszentrum

Schriften des Forschungszentrums Jülich
Reihe Information / Information Band / Volume 74

Forschungszentrum Jülich GmbH
Zentralinstitut für Engineering, Elektronik und Analytik (ZEA)
Systeme der Elektronik (ZEA-2)

Modelling, implementation and characterization of a Bias-DAC in CMOS as a building block for scalable cryogenic control electronics for future quantum computers

Patrick Norbert Vliex

Schriften des Forschungszentrums Jülich
Reihe Information / Information Band / Volume 74

ISSN 1866-1777 ISBN 978-3-95806-588-8

Bibliografische Information der Deutschen Nationalbibliothek.
Die Deutsche Nationalbibliothek verzeichnet diese Publikation in der
Deutschen Nationalbibliografie; detaillierte Bibliografische Daten
sind im Internet über http://dnb.d-nb.de abrufbar.

Herausgeber und Vertrieb:	Forschungszentrum Jülich GmbH Zentralbibliothek, Verlag 52425 Jülich Tel.: +49 2461 61-5368 Fax: +49 2461 61-6103 zb-publikation@fz-juelich.de www.fz-juelich.de/zb
Umschlaggestaltung:	Grafische Medien, Forschungszentrum Jülich GmbH
Druck:	Grafische Medien, Forschungszentrum Jülich GmbH
Copyright:	Forschungszentrum Jülich 2021

Schriften des Forschungszentrums Jülich
Reihe Information / Information, Band / Volume 74

D 82 (Diss. RWTH Aachen University, 2021)

ISSN 1866-1777
ISBN 978-3-95806-588-8

Vollständig frei verfügbar über das Publikationsportal des Forschungszentrums Jülich (JuSER)
unter www.fz-juelich.de/zb/openaccess.

Acknowledgement

First and foremost, I would like to start by thanking my examiners Prof. Stefan Heinen for supervision of my thesis work and Prof. Stefan van Waasen for giving me the opportunity to work on this truly interesting and motivating project at the Forschungzentrum Jülich. I want to express my deepest gratitude for all of your guidance during the work of this thesis.

Special thanks goes to my day-to-day supervisor Dr. Andre Kruth for offering a lot of his time and help with the thesis and the project, including all the support with the top level design, layout and the setup of design flow.

My deepest gratitude also goes towards my colleague and personal friend Dennis Nielinger. I thank you for suffering with me through long days and late evenings during the tape out. Your input in design, layout and verification as well as your commitment and hard work helped us to get the chip into production before the deadline. I also remember all the stressful, but thanks to you still enjoyable, evenings in the lab.

I would like to express the deepest appreciation to Dr. Carsten Degenhardt who helped me a lot during the course of the project. Your support with the handling of all the peripheral tasks surrounding the project helped me a lot in achieving this thesis.

In addition, I want to thank Anton Artanov and Christian Roth for all the help offered in measurement, verification and testing of the chips. I also thank Dr. Andre Zambanini, Dr. Pavithra Muralidharan and Daniel Liebau for the support on the digital side of things.

I would like to thank all my colleagues, at the Central Institute of Engineering, Electronics and Analytics - Electronic Systems (ZEA-2) who I have worked with, for their kindness and company.

Finally, I want to express a particular personal thank you to my parents, my brother and Jeanette. I could not imagine my life without your unconditional support and never-ending motivation.

Abstract

Quantum computing is a research field of increasing attention and popularity, which has steadily gained momentum in the recent years. The promises made for universal QC are vast in terms of their predicted impact to science, economy and society. A universal quantum computer will be able to solve specific tasks up to exponentially faster than any modern supercomputer. Applications range from quantum chemistry in catalyst research and protein folding simulations to search algorithms for unordered databases and cryptography.

Quantum bits are typically operated inside a dilution refrigerator at temperatures close to absolute zero, i.e. $< 1\,\mathrm{K}$. The majority of the QC scientific research community agrees that an estimated number of $\gtrapprox 10^6$ quantum bits are required to build an universal quantum computer. This number leads to foreseeable connectivity bottlenecks to fed all the required biasing, control and read-out signals into the cryostat.

This work is using a TSMC 65 nm CMOS technology to integrate classical control electronics closer with the quantum bits and thus pave a way for scalability. Other publications showed the feasibility of operating CMOS technologies at deep cryogenic temperatures. Whereas various papers presented implementations of cryogenic electronics for quantum bit control, a scalable solution for quantum bit biasing is missing and is the focus of this work.

A capacitive digital-to-analog converter (DAC) for biasing of quantum bits is modeled, implemented and characterized at cryogenic temperatures. Special emphasis is placed upon achieving a systematically scalable and ultra-low power DAC design. The DAC design includes a reference voltage coarse tuning scheme in order to lower power consumption and increase resolution. Two calibration procedures to mitigate gain error induced output voltage jumps are described and the most promising approach is verified at cryogenic temperatures. Auxiliary circuitry is added to enable DAC characterization, i.e. operational amplifiers and a $\Sigma\Delta$ modulator. System level considerations as well as implementation details and measurement results for of all these circuit blocks are presented.

The design and implementation of a bandgap reference and a linear regulator, which are investigated as building blocks for cryogenic supply and reference voltage regulation, are also described. Measurement results of these circuit blocks at cryogenic temperatures are also part of this work.

All circuit designs are aimed at optimum robustness and high configurability in order to cope with cryogenic CMOS effects and the lack of valid device models in the temperature regime of interest.

Contents

List of Figures

List of Tables

Acronyms

2DEG	two-dimensional electron gas
ADC	analog-to-digital converter
BG	bandgap reference
CB	conduction band
CM	common-mode
CMFB	common-mode feedback
DAC	digital-to-analog converter
DNL	differential non-linearity
DNP	dynamic nuclear polarization
DUT	device under test
ESDR	electron dipole spin resonance
ESR	electron spin resonance
FF	flip-flop
GM	Gifford-McMahon
IC	integrated circuit
ILD	inter-layer dielectric
INL	integral non-linearity
LDO	low drop-out
LR	linear regulator
LS	level shifter
LVT	low-threshold voltage
MASH	multistage noise shaping
NISQ	noisy intermediate scale quantum
OpAmp	operational amplifier
OSR	oversampling ratio
PDK	process design kit
PM	phase margin
PSRR	power supply rejection-ratio
PVT	process, voltage and temperature
PWM	pulse width modulation
QC	quantum computing
QPC	quantum point contact
qubit	quantum bit
RT	room temperature
s.i.	strong inversion
SET	single-electron transistor
SSA	signal source analyzer
T&L	track & latch
TG	transmission gate
TSV	through-silicon-via

UGB unity gain bandwidth
w.i. weak inversion
WC window comparator

Chapter 1

Introduction

1.1 Motivation

Quantum computing (QC) is a research field of increasing attention and popularity, which is steadily gaining momentum in the recent years. The promises made for universal QC are vast in terms of their predicted impact on science, economy and society. The term *universal* refers to no constrains to the computational task a quantum computer should be able to solve. Multiple use cases for a universal quantum computer are already known today and one can expect more applications to be opened up in the coming years, as research on quantum algorithms is a prominent topic in this field. Most of these promises are based on a predicted speed-up compared to its classical computing equivalent. A universal quantum computer will be able to solve specific tasks up to exponentially faster than any modern supercomputer. Quantum supremacy to its classical counterpart has been published based on experimental results by F. Arute et al. [1]. 53 quantum bits completed a task in about 200 s, which would take ≈10.000 years on a modern supercomputer.

Typical examples of applications benefiting of this performance gain are: quantum chemistry in catalyst research and protein folding simulations, search algorithms for unordered databases and cryptography, e.g. prime factorization [2]. For the industrial production of ammonia, which is used as fertilizer, about 1 % of the world's energy consumption is spent, because high pressure and temperature are required in the process. QC could provide insights in process improvements by enabling quantum simulations and unveil how a biological catalyst is able to produce ammonia at ambient temperatures. [3]

However, considerable challenges have to be overcome before the first universal quantum computer can be build. Among these challenges is the sheer number of required quantum bits, that will be needed for universal QC. A publication by L.M.K. Vandersypen et al. [2] predicts about 10^6 to 10^8 required quantum bits. Quantum bits are typically operated at deep cryogenic temperatures < 100 mK inside of a dilution refrigerator. Feeding all biasing, control and read-out signals from external into the cryostat appears unpractical at best. A proposed solution is local cryogenic classical electronics, bringing control and read-out closer to the quantum bits themselves. However, an implementation for local qubit biasing is still missing.

This work is taking up the idea of using modern CMOS technologies for this task, due to their low area footprint, low power consumption and natural synergy with semiconductor quantum bits. The focus is the implementation of an integrated digital-to-analog converter (DAC) for the generation of static biasing voltages in a 65 nm CMOS technology, which is named *Bias-DAC* in this work. The biasing voltages are used to tune quantum dots for semiconductor spin-based quantum bits and are generated in close proximity at deep cryogenic temperatures of 100 mK. Taking the required number of qubits and the low cooling power budget of a dilution refrigerator, i.e. $\approx$ 1 mW [2], into account, the Bias-DAC design must be ultra-low power, highly scalable and able to cope with the extreme environmental conditions, e.g. an ambient temperature of 100 mK.

1.2 Structure of this work

Following this introduction chapter, chapter 2 introduces QC and describes the underlying physical properties of quantum bits. Furthermore, often used terms in QC research like quantum gate fidelity and the Bloch sphere are explained. Alongside an overview to the various qubit implementation types, cryogenic CMOS effects are explained and a record of current state of the art (integrated) cryogenic electronics is presented. In chapter 3, system level considerations for power and noise are discussed and special emphasis is placed upon systematic scalable approaches in order to scale the number of Bias-DACs most efficiently. Chapter 4 presents the design of an implemented bandgap reference and linear regulator, which are investigated as building blocks for cryogenic supply and reference voltage regulation. Chapter 5 discusses the Bias-DAC design in detail and shows some additional circuitry in order to enable measurement of the Bias-DAC. Measurement results of all these circuit blocks down to cryogenic temperatures of 6 K to 7 K are presented in chapter 6. An outlook to future research activities is given in chapter 7. Chapter 8 concludes this work with a summary of the achieved results.

Chapter 2

Application and Qubit Fundamentals

2.1 Quantum Bits

Quantum bits (qubits) are the quantum mechanical equivalent of a classical bit, which describes information in a binary numeral system. As its classical counterpart, the qubit is the basic unit of information with two distinct states. The major difference between a qubit and a classical bit is that the qubit can be in a superposition state of both basis states at the same time, i.e. "1" and "0", due to its quantum mechanical nature, which is graphically elucidated in Fig. 2.1.

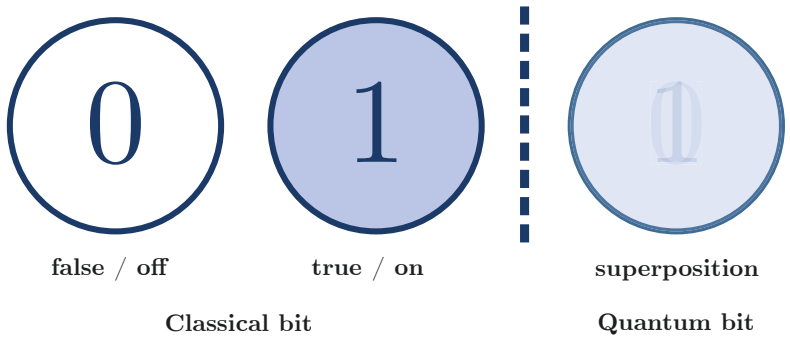


Figure 2.1: Quantum bit enables a superposition of the two distinct classical states of a conventional bit

In classical computer systems, a bit is represented by a voltage level. A logical "1" is a high voltage level, and consequently a logical "0" is a low voltage level. These two logical states are normally represented by a large span of physical states, i.e. the signal voltage level, which are grouped together as one of the states. As described in [4, pp. 235-236] and shown in Fig. 2.2 the available signal range, which is $0V$ to $1.2V$ for the 65 nm CMOS technology used in this work, can be divided into 3 regions: logical high "1" state, logical low "0" state and a region of uncertainty. Every physical state grouped together in one of these regions holds the same logical level and information. This is done in order to minimize the effects of noise and distortion in the system and to maximize the noise margin of the signals [4, pp. 236-237]. This is to some extent inapplicable when encoding

a continuous superposition state in a qubit and leads to a definition of operation fidelity as a figure of merit (see section 2.2.1).

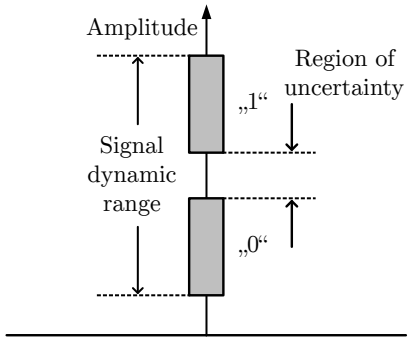


Figure 2.2: Amplitude region for a classical logical bit [4, p. 236 Bild 4.1.a]

As described above, in most cases of classical computing a bit is propagated, processed and stored by a voltage level. However, other physical representations are also realized for example a bit value can also be stored by the presence or absence of charge (on a capacitor). This storing method of a bit is employed in almost every modern computer in a DRAM. Furthermore, also magnetic flux can be used to store bits, e.g. in hard disk drives. This shows that the bit itself is just a unit of information and not bound to a fixed physical quantity. Likewise, a qubit as “an abstract, information-theoretic concept, which is best not equated with any particular physical object which may embody it” [5, p. 578], can be utilized in many quite drastically different implementation typologies (see section 2.3).

2.1.1 Dirac Notation

For the mathematical descriptions of quantum states, the so-called *Dirac notation* is commonly used in quantum physics, also referred to as “bra-ket” notation. This work will give only a brief introduction and takes no aim for completeness. The following explanation is based on [6, pp. 10-12]. The notation describes vectors in a complex vector space, more precisely a complex Hilbert space. A “ket” denotes a vector in the vector space and is written as follows:

$$|V\rangle \rightarrow \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \end{bmatrix} \tag{2.1}$$

This ket vector can also be written as a column vector [6, p. 10], allowing for the definition of the inner product of two quantum states $|V\rangle$ and $|W\rangle$ as $\langle V|W\rangle$ and this “is given by the matrix product of the transpose conjugate of the column vector representing $|V\rangle$

with the column vector representing $|W\rangle$"[6, p. 11]:

$$\langle V|W\rangle = \begin{bmatrix} v_1^* & v_2^* & \cdots & v_n^* \end{bmatrix} \begin{bmatrix} w_1 \\ w_2 \\ \vdots \\ w_n \end{bmatrix} \tag{2.2}$$

This conversion from row to column vector is mathematically achieved by the definition of two vector spaces, the "space of kets" and the "dual space of bras". A "bra" vector $\langle V|$ is the adjoint of the associated ket vector $\langle V| \leftrightarrow |V\rangle^\dagger$, which is then used to calculate the matrix product. This can be summarized as [6, p.12]:

$$|V\rangle \leftrightarrow \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \end{bmatrix} \leftrightarrow \begin{bmatrix} v_1^* & v_2^* & \cdots & v_n^* \end{bmatrix} \leftrightarrow \langle V| \tag{2.3}$$

A quantum mechanical particle is described by the corresponding wavefunction $\psi(\vec{r}, t)$ in space $\vec{r}$ and time t which can be determined by the Schrödinger equation [5, p. 67]:

$$j\hbar \frac{\partial}{\partial t}\psi(\vec{r}, t) = \left[-\frac{\hbar^2}{2m}\Delta + V(\vec{r}) \right] \psi(\vec{r}, t) \tag{2.4}$$

Now the wavefunction $|\psi\rangle$ of a qubit with its two orthogonal basis vectors $|0\rangle$ and $|1\rangle$ (also named micro-states [5]) can be described in Dirac notation as [5, p. 578]:

$$|\psi\rangle = c_0 |0\rangle + c_1 | |1\rangle \tag{2.5}$$

With c_0 and c_1 being any complex coefficients, which satisfy the condition $|c_0|^2 + |c_1|^2 = 1$. As described further by [5, p. 578], the squared coefficients can be interpreted as probability of the qubit being projected into one of the corresponding micro-states $|0\rangle$ or $|1\rangle$ when measured [5, p. 578]. The complex coefficients c_0 and c_1 are also referred to as "probability amplitude" [6, pp. 111, 121].

2.1.2 Bloch Sphere

A common way to visualize the physical state of a single qubit is the so-called "Bloch sphere". The Bloch sphere can be derived by rewriting (2.5) under the condition that $|c_0|^2 + |c_1|^2 = 1$, which is leading to [7, p. 15]:

$$|\psi\rangle = e^{j\gamma}(\cos\frac{\theta}{2}|0\rangle + e^{j\phi}\sin\frac{\theta}{2}|1\rangle) \tag{2.6}$$

with θ, ϕ and γ being real numbers. However, as [7] points out, $e^{j\gamma}$ has no observable effects and is neglected. [5, p. 578] further adds to this point that "the common phase of c_0 and c_1 does not have physical significance, and can be chosen accordingly to an

arbitrary convention". Therefore, it is:

$$|\psi\rangle = \cos\frac{\theta}{2}|0\rangle + e^{j\phi}\sin\frac{\theta}{2}|1\rangle \tag{2.7}$$

It is then shown in [7] that the real numbers θ and ϕ define a point on the unit three-dimensional sphere, see Fig. 2.3. Thus, a physical state of an ideal single qubit is somewhere on the surface of the Bloch sphere. However, there are some limitations to this geometric representation: First there is no straightforward generalization for a multiple qubit system [7], secondly the two micro-states are orthogonal basis states but are not represented as those in the Bloch sphere. Nevertheless, the Bloch sphere provides an useful way for understanding and visualization of single qubit operation.

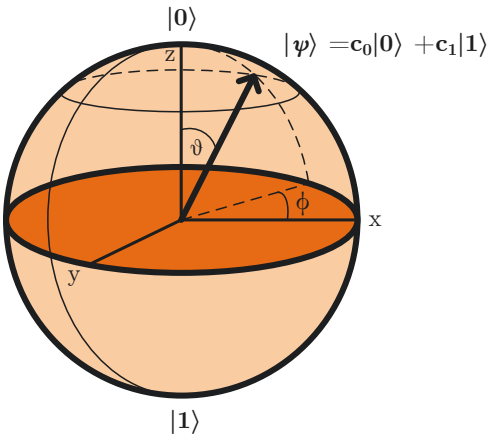


Figure 2.3: Bloch sphere [7, p. 15 Fig. 1.3.]

2.1.3 Quantum Computation

Quantum computation promises an up to exponential speedup calculation for certain tasks when compared to classical computation. This is due to two quantum mechanical effects. First, the superposition of states, which was already described in this chapter and secondly the entanglement of wavefunctions. Entanglement is required for generating one wavefunction consisting of multiple qubits and is described as: "[...] a state that cannot be written as a product of individual qubit wavefunctions. In fact, the states of individual qubits are highly correlated, possessing the type of correlation that is special to quantum systems and is referred to as 'entanglement'. Entanglement is actually a form of statistical correlation that is stronger than is possible, even in principle, in classical systems." [5, p. 579]

A classical two-bit sized word can be in 4 states: 00, 01, 10 and 11. The wavefunction of two entangled qubits can be written as [5, p. 578]:

$$|\psi\rangle = c_{00}|00\rangle + c_{01}|01\rangle + c_{10}|10\rangle + c_{11}|11\rangle \tag{2.8}$$

The squared complex coefficients c_{ik} can still be understood as the probability for the system to be projected into the corresponding micro-state (orthogonal basis vector). Thus, the sum of the squared coefficients has to be one [5, p. 578]:

$$\sum_{i=0}^{1}\sum_{k=0}^{1}|c_{ik}|^2 = 1 \tag{2.9}$$

This can now be analogously expanded to an arbitrary word size of entangled qubits. The same number of qubits as classical bits are required to construct a certain word size. However, the difference between quantum mechanical and classical nature is visible when performing a mathematical operation on a qubit register. The following example is based on [5, p. 579]. Assuming a three-qubit register with $|x\rangle$ that describes the equivalent decimal value $x \in [0;7]$ saved in a qubit register, e.g. $|101\rangle \leftrightarrow |5\rangle$. Thus, the wavefunction of the state "equal superposition of all odd values" can be written as:

$$|\psi_{odd}\rangle = \frac{1}{\sqrt{4}}(|1\rangle + |3\rangle + |5\rangle + |7\rangle) \tag{2.10}$$

Now the operation "add 3" is performed on the qubit register:

$$add3\,|\psi_{odd}\rangle \Rightarrow |\psi_{odd+3}\rangle = \frac{1}{\sqrt{4}}(|4\rangle + |6\rangle + |0\rangle + |2\rangle) \tag{2.11}$$

This example gives a first impression of the promising advantages quantum computation is offering. By performing one instruction on a single qubit register we calculated the result of what would require 4 classical operations and registers, i.e. $1 + 3 = 4$; $3 + 3 = 6$; $5 + 3 = 0$; $7 + 3 = 2$ (integer overflow in the last two). Thus, a maximum of 2^N, where N is the word size of the register, classical instructions can be conducted in parallel by a qubit register. Yet, when measuring/reading the qubit we will get only one result as the physical qubit state is projected onto the orthogonal basis vectors (each qubit can only be $|1\rangle$ or $|0\rangle$) and only one word is read from the qubit register. It is therefore required to develop "quantum algorithms" to utilize the possible gain one can achieve by the quantum mechanical superposition of states [5, p. 579]. However, detailed explanation to quantum algorithms is beyond the scope of this work and further information is available in [8].

2.2 Quantum Gates

Quantum gates can be thought of as an analogy to the logic gates of classical computing, used to perform computation on the qubits. In classical computing only the NAND (or NOR) gate and the logical inversion are required to enable construction of every logical function. A similar approach can be taken with qubits, referred to as a universal set of quantum gates, which is one of the five requirements for the implantation of quantum computing, the so-called "DiVincenzo Criteria" with two additional requirements for quantum communication [9]:

1. A scalable physical system with well characterized qubits
2. The ability to initialize the state of the qubits to a simple fiducial state, such as $|000\ldots\rangle$
3. Long relevant decoherence times, much longer than the gate operation time
4. A "universal" set of quantum gates
5. A qubit-specific measurement capability

6. The ability to interconvert stationary and flying qubits
7. The ability to faithfully transmit flying qubits between specified locations

Those criteria are commonly accepted as requirements for a quantum information processor or quantum communication [10].

Quantum algorithms are sequential sequences of quantum gates, which is again similar to classical logic operations. However, one major distinction of quantum gates from classical logic gates is the possibility to perform fractions of gates, e.g. when changing the phase of the qubit. Quantum gates are divided into groups representing the number of qubits involved, e.g. one-qubit gates, two-qubits gates, etc. One example for an one-qubit gate would be an inversion "NOT gate". Analogous to classical logic it should invert the physical state of the qubit. This leads to the definition of the evolution $U(t)$ for a NOT gate: [5, p. 580]

$$U_{NOT}(c_0 |0\rangle + c_1 |1\rangle) = c_1 |0\rangle + c_0 |1\rangle \tag{2.12}$$

Alternatively, written as vectors and matrices:

$$U_{NOT} \begin{pmatrix} c_0 \\ c_1 \end{pmatrix} = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \begin{pmatrix} c_0 \\ c_1 \end{pmatrix} = \begin{pmatrix} c_1 \\ c_0 \end{pmatrix} \tag{2.13}$$

A prominent example for a two-qubit gate is the "controlled NOT" or short "CNOT" which is inverting the state of qubit y depending on the state of qubit x, resulting in an logical equivalent XOR operation for qubit y and x. The notation for a CNOT gate is:

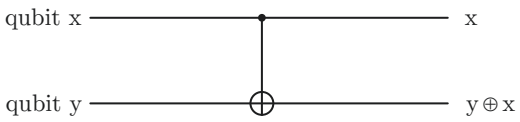


Figure 2.4: CNOT notation, qubit 1 "control", qubit 2 "target" [5, p. 581 Fig. 2]

With one and two-qubit gates, it is possible to generate a universal set of quantum gates. Furthermore, one additional characteristic of quantum computing can be noticed when looking at Fig. 2.4, i.e. qubit x is still saved after the CNOT gate was performed. This is due to the circumstance that "reversibility is required by quantum mechanics; quantum transformations are always invertible, so in a quantum computation, it must always be possible to recover the input from the knowledge of the output" [5, pp. 579-580]. This means by keeping the qubit x we can restore the input from the output by applying another CNOT on the output of qubit y: $(y \oplus x) \oplus x = y$.

2.2.1 Fidelity for Quantum States

One important measure of the quality of a qubit is the so-called *fidelity* of quantum states, defining a way to measure distance between two quantum states [7, pp. 399-401]. This enables a method to evaluate the distance of the wanted or ideal quantum state to the measured disturbed state with errors being induced by e.g. noise. The work "Fidelity for mixed quantum states" by Richard Jozsa [11] was the first to use this term for mixed quantum states, being based on a general quantum analog of Shannon's noiseless coding theorem [12], also being called "Schuhmacher's theorem".

First, to give a brief explanation on the following terms for quantum states: *pure state* and *mixed state*. A pure state is known exactly and can be described by a single ket vector $|\psi\rangle$. A mixed state is a statistical distribution of different pure states described by the density operator (density matrix) ρ, e.g. for entangled multi-qubit systems. ρ is defined in eq. 2.14, with index i, probabilities p_i and the ensemble of pure states $\{p_i, |\psi_i\rangle\}$. The density operator for a pure state is $\rho = |\psi\rangle \langle\psi|$. Hence, mixed states include pure states and are the more general case. For a single qubit a pure state is placed on the surface of the Bloch sphere, whereas a mixed state lies within the Bloch sphere with a so-called *Bloch vector* $||\vec{r}|| \leq 1$ for the state ρ. [7, pp. 98-105][8, p. 18]

$$\rho \equiv \sum_i p_i |\psi_i\rangle \langle\psi_i| \tag{2.14}$$

It was derived by [11] using the work of [13] starting from the fidelity F as a measure of distance of two pure states ψ_1 and ψ_2

$$F(|\psi_1\rangle \langle\psi_2|, |\psi_2\rangle \langle\psi_2|) = |\langle\psi_1|\psi_2\rangle|^2 \tag{2.15}$$

that the so-called *Uhlmann–Jozsa fidelity* F_1 of two mixed quantum states ρ_1 and ρ_2, with $tr()$ being the trace of the matrix, can be calculated as:

$$F_1(\rho_1, \rho_2) = \left[tr\left(\sqrt{\sqrt{\rho_1}\rho_2\sqrt{\rho_1}} \right) \right]^2 \tag{2.16}$$

An alternative way is to start from $|\langle\psi_1|\psi_2\rangle|$ as done in [7, p. 409], resulting in a fidelity F'.

$$F'(\rho_1, \rho_2) = tr\left(\sqrt{\sqrt{\rho_1}\rho_2\sqrt{\rho_1}} \right) \tag{2.17}$$

This already shows that multiple fidelity definitions are possible and a recent overview is given in a 2019 publication [14]. For 2.16 a metric, based on Bures metric, can be defined for the distance, the so-called *Bures distance* [11] based on the work of [15]:

$$d_B(\rho_1, \rho_2) = \sqrt{2 - 2\sqrt{F(\rho_1, \rho_2)}} \tag{2.18}$$

and from 2.17 for the *Bures angle* [7, pp. 412-413][14]:

$$d_A(\rho_1, \rho_2) = arccos\left(\sqrt{F'(\rho_1, \rho_2)}\right) \tag{2.19}$$

The fidelity of quantum gates, describing how precise the gate operations were performed and which magnitude of noise is present, is one important mean to compare different qubit implementations. The quantum threshold theorem or quantum fault-tolerance theorem as proven by [16] shows that with quantum error correction a universal quantum computer is feasible even in the presence of physical error rates. Current error-correction schemes require a fidelity of about $> 99.9\,\%$ which is generally considered as required to limit the number extra physical qubits to approx. 1000 to 10000 per logical qubit [17]. Fidelity is most of the time tested with *randomized benchmarking* proposed by [18].

The fidelity of quantum gates is described by Schreiber and Bluhm [19] as: "Roughly speaking, it [the fidelity of quantum gates] specifies the success probability of a single gate operation."

2.3 Overview of Qubit Topologies

As described in section 2.1 a qubit is an information-theoretic concept and thus every multi-level quantum mechanical system can be employed as a qubit, but typically only two-level systems are used. This leads to a great variety of dissimilar physical qubit implementations, ranging from trapped ions over superconducting circuits and solid-state implementations to topological qubits. Every implementation has its own distinct set of properties, advantages and disadvantages.

Whereas topological qubits could be referred to as the most exotic, due to them being *Anyons*, a quasiparticle whose statistics is neither fermionic nor bosonic [20] and exists only in two-dimensional space [21, 22]. No physically working topological qubit has been experimentally proven up to now to the best of the author's knowledge [23, 24]. Therefore, this work will not go into detailed explanation of topological qubits.

2.3.1 Trapped Ion Qubits

The following section about trapped ion qubits is based on a recent review paper on "Trapped-Ion Quantum Computing: Progress and Challenges" from the Massachusetts Institute of Technology published April 2019 [10]. One way to create trapped ion qubits is to utilize RF Paul traps, which have been used since 1980 [25], to confine single ions in a high vacuum, see Fig. 2.5. The ions are trapped by applying an RF voltage V_{RF} on a set of (parabolic) electrodes. Many more different geometries are possible but they are all based on the principle of an oscillating electric field confining charged particles. Trapped ion qubits promise "robust trap lifetimes, long internal-state coherence, strong ion-ion interactions, [...]" which makes them in general one of the most robust and long-living qubits summarized in this work [10]. One concern is the scalability to millions or billions

of qubits, as this challenge might be not as straightforward as for solid-state qubits which can rely on modern semiconductor industry processes.

Gate fidelities of trapped ion qubits are reported among the top of all qubit types. For single qubit gates T. P. Harty [26] shows a fidelity of 99.9999 %, which "surpass the performance of any other modality" [10], alongside long coherence times of 50 s. Two years later a paper including further research results of [27] was published, showing two-qubit logic gate operation and achieving a Bell state fidelity of 99.7 % and [28] reports on 99.9(1) % two qubit gate fidelity, being "significantly above the ≈ 99 % minimum threshold level required for fault-tolerant quantum computation".

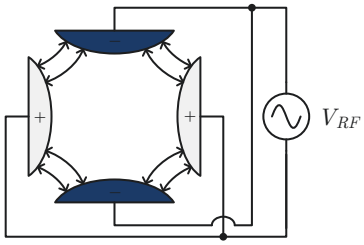


Figure 2.5: RF Paul trap [29, Fig. 2a]

RF Paul traps are the main focus for researchers in quantum computing using trapped ions and these traps are operated with RF voltage amplitudes of 10 V to 1000 V at 10 MHz to 100 MHz [10].

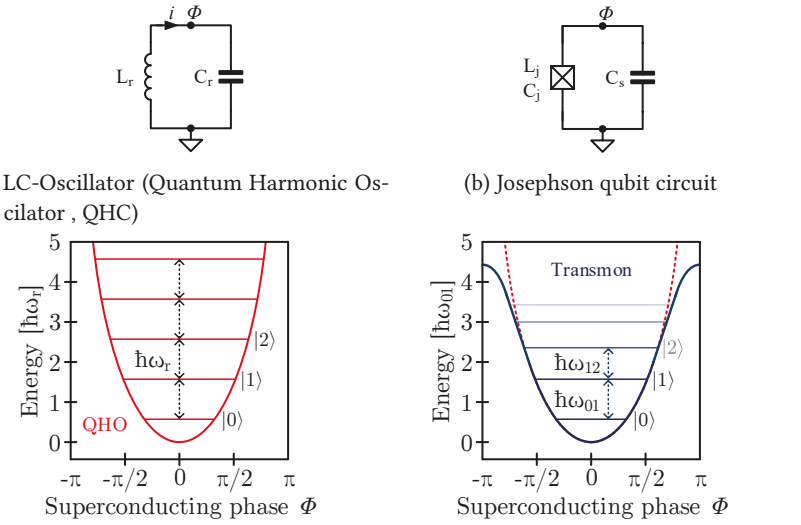
2.3.2 Superconducting Qubits

Another way to implement qubits is to utilize superconducting materials. Two prominent examples for superconducting qubits are the research work at IBM and Google both relying on this type of qubit, with Google recently showing the operation of 53 qubits [1]. Recent review papers for superconducting qubits are given by [30] and [31]. Superconducting qubits can be understood by looking at a basic LC-oscillator as shown in Fig. 2.6a, due to the nonexistent losses (superconducting materials) no damping is present. By using the time dependent magnetic flux present in the oscillator, [30] derived a quantum harmonic oscillator behavior for this setup with equidistant energy level spacing, i.e. $\hbar\omega_r$. However, this is not fitting to create a qubit as the same energy would be required for each energy level transition, rendering a distinct selection of only two specific energy levels impossible, i.e. a "leakage" to higher levels is possible.

A solution is to replace the inductance with a so-called *josephson junction* [7, 32, 33], which can be viewed as a non-linear inductance and consists of two superconducting materials separated by a thin isolating barrier, which allows for tunneling of Cooper pairs [31]. This non-linearity leads to non-equidistant energy level spacing and thus allows driving specific and distinct energy level transitions and finally selecting single energy levels for the ground $|0\rangle$ and the excited $|1\rangle$ state of the qubit. [30] Giaever1973

One of the challenges for this type of qubits may be scalability as superconducting qubits rely on the fact that a macroscopic structure exhibits quantum effect properties, which are normally taking effect in elementary particles and sub-nanometer sizes. Even though advantages in material properties could improve on this, today's superconducting qubits typically require a few hundred micrometer large superconducting wires, see Fig. 2.7.

Today superconducting qubits are regularly achieving single qubit gate fidelities $\gtrapprox 0.99$ and also two qubit gate fidelities > 0.99 have been demonstrated. Superconducting qubits are a promising candidate to use in *noisy intermediate scale quantum* (NISQ) technologies and subject to ongoing research for usage in universal quantum computers. [31]



(a) LC-Oscillator (Quantum Harmonic Oscilator , QHC)

(b) Josephson qubit circuit

(c) LC-Oscillator equidistant energy level spacing.

(d) Transmon noneuqidistant energy level spacing.

Figure 2.6: Superconducting charge qubit [30, Fig. 1]

According to Kjaergaard et al. [31] the predominant method to control single qubit operations is via microwave signals and the authors name an exemplary qubit level spacing of 5 GHz for the transmon, which is stated to be currently the most widely used type of superconducting qubit.

2.3.3 Spin Qubits

The last discussed type of qubits in this work are spin-based qubits, referring to the use of the quantum mechanical spin to create a qubit, e.g. nuclear or electron spin. This work will focus mostly on electron spins used to encode the state of qubits. One of the major selling points of this type of qubit is the similarity to structures used in the modern semiconductor industry, managing to implement billions of MOS transistors in integrated circuit chips, whose dimensions are in the centimeter range. Therefore,

semiconductor spin-based qubits are one of the promising qubit types when talking about implementation of long-term large-scale quantum circuits. [2]

Even though superconducting qubits are considered more mature today, the current trend of solid-state qubits catching up with superconducting qubits in terms of coherence time performance is shown in Fig. 2 of [34]. Whereas superconducting qubits' requirement for cryogenic temperatures is obvious due to their need to be operated below the critical temperature of their material, operating spin qubits requires a cryogenic temperature, too. Spin qubit implementations are placed in temperatures of below 100mK to reduce the thermal energy below the Zeeman energy splitting in reasonable magnetic fields. This enables an easy way to initialize qubits into the ground state by waiting for the thermal equilibrium state. Nuclear spins would require three orders of magnitude less temperature due to their about 100 times smaller magnetic momentum compared to electrons. [5, p. 591]

A comparison of semiconductor qubits alongside other types like ion traps and transmons is shown in Fig. 2.7. The size of a transmon is depicted greater than 100 µm and the size of ion traps bigger than 1 µm, both being considerably larger than silicon and GaAs quantum dots. FinFET based qubits are even another magnitude smaller in size. Showing the potential advantage in scaling the number of qubits in comparison. Moreover, the big relevance of semiconductor dots (Silicon, GaAs) and FinFET qubits to quantum computing is depicted below the size comparison. However, Fig. 2.7 is not evaluating the relevance of superconducting and ion qubits for these applications. In [35] the reasoning for each ranking in relevance is given. For FinFETs, silicon and GaAs dots, the major relevance in quantum computing applications, alongside superconducting qubits, is reasoned with the advanced development in "coherence, scalability and the ability to make small-scale quantum processors". The synergy of silicon based qubits and semiconductor process technologies is described as demonstration for the scalability of these qubits, being fabricated by modern semiconductor foundries.

Fidelities > 99.9 % have been reported for many types of semiconductor spin qubits, P-Donors [36], Si-MOS [37] and Si/SiGe [38]. Furthermore, also GaAs qubits are reported to show fidelities of 99.5 % [39]. Demonstrated two-qubit gates are achieving fidelities of 70 % to 90 %, which are below current state of the art two qubit fidelities of trapped ion and superconducting qubits. Increasing the fidelity to above error correction threshold is in the focus of ongoing research. The authors of [40] showed the values listed in Table 2.1 are achievable for GaAs and Si spin qubits.

	GaAs	Si
Single-qubit	$\geqslant$ 99.69 %	$\geqslant$ 99.95 %
Two-qubit	99.90 %	99.99 %

Table 2.1: Achievable spin qubit gate fidelities according to [40]

This work focuses on GaAs spin qubits as well as giving an outlook to integration for Si/SiGe ones. Thus, the following chapters give further details to both types of spin qubits.

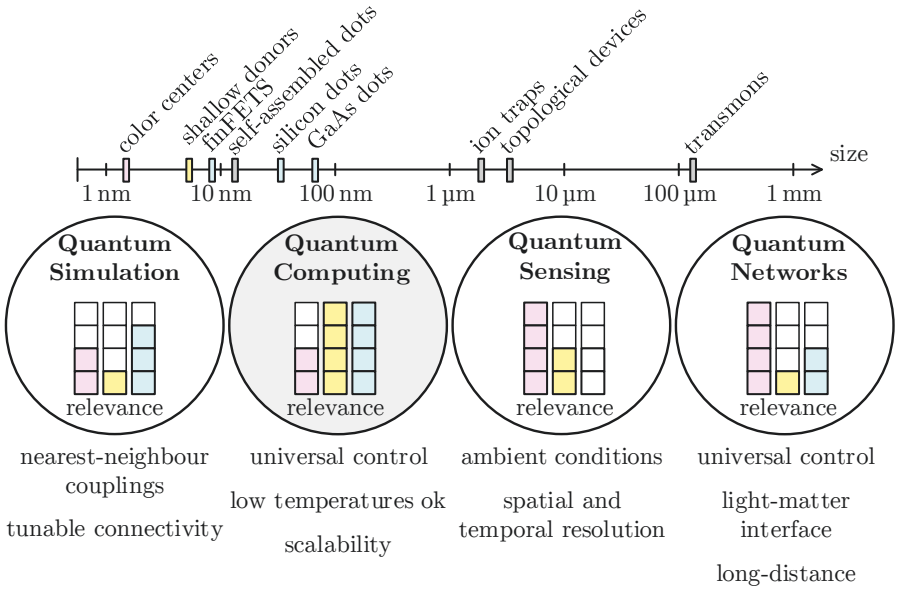


Figure 2.7: Comparison of semiconductor qubits adopted from [35, Fig. 1]

2.3.3.1 GaAs Qubits

Semiconductor spin qubits were first pioneered with (Al,Ga)As quantum dots [41–43], which are in the following referred to as GaAs qubits for ease of reading. This choice was made due to some specific advantages of using these materials, i.e. larger feature sizes of the devices compared with silicon due to a smaller effective electron mass enabling easier fabrication of first research samples in order to demonstrate all key requirements for QC [44]. Additional advantages are the ability to fabricate these with high crystal quality [19] and the capability for optical coupling due to its direct bandgap nature [44]. The general structure of a GaAs quantum dot is schematically shown in Fig 2.8. A single qubit composed of two electron spins trapped in a double-well potential alongside a sensor dot for read-out of the charge state is shown. The location of these dots is highlighted on the surface. In addition, the band structure is depicted to show the two-dimensional electron gas (2DEG) in the conduction band (CB) confining the dots in the z-axis. X and y-axis of the dots are confined by applying negative voltages (referenced to ground) on the metal electrodes placed on the surface, thus locally depleting the 2DEG. Confinement in all three dimensions allows for placement of single electrons in the quantum dots. Whereas differences may be present in the hetero-structure, the overlying working principle will be the same also for Si-based qubits. The gate voltage ϵ can be used to apply quantum gates to the qubit. An optional external magnetic field B_{ext} may be present depending on the experiment. [3, p. 7]

One not depicted effect in Fig. 2.8 is the hyperfine interaction of electron spins coupling to nuclear spins. Fluctuations in this hyperfine field are known as a possible source for decoherence [45, 46]. However, by utilizing the interaction Foletti et al. [47] showed

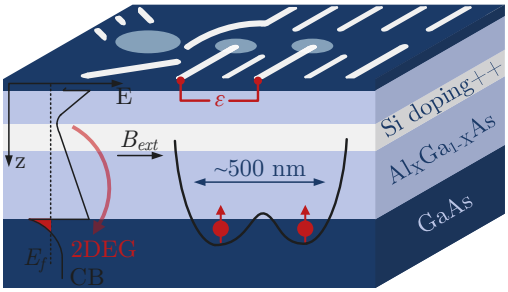


Figure 2.8: GaAs structure for single qubit and read-out. Fig. adopted from [3, Fig. 2.1].

a way to generate a required magnetic-field gradient between the two quantum dots through the usage of dynamic nuclear polarization (DNP). The created gradient was demonstrated for times longer than 30 min, considerably exceeding the fluctuation times. This technique was further enhanced by utilizing the qubit as feedback loop to polarize the nuclear spin bath and increased qubit dephasing times T_2^* nearly tenfold [48].

As one qubit is constructed out of two individual electron spins, various qubit encodings are possible. One method of encoding which is showing the best current gate-fidelity rates is the so-called *singlet-triplet qubit*, which also allows for sub-GHz baseband control [40]. This encoding scheme was also utilized in the work of Foletti et al. [47], which demonstrated dynamic nuclear polarization. The authors of [39, 47] denote the singlet state $|S\rangle$ and desired triplet state $|T_0\rangle$, with arrows representing the direction of the electron spin, as:

$$|S\rangle = \frac{|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle}{\sqrt{2}} \tag{2.20}$$

$$|T_0\rangle = \frac{|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle}{\sqrt{2}} \tag{2.21}$$

and the undesirable tripled states (leakage states) as $|T_+\rangle = |\uparrow\uparrow\rangle$ and $|T_-\rangle = |\downarrow\downarrow\rangle$, creating the so-called S-T_0 spin qubit [49].

Manipulation of the qubit is done via control of the exchange coupling $J(\epsilon)$ between the two quantum dots, as is shown in Fig. 2.9. One reason to operate this type of qubits in cryogenic temperatures is to ensure that the "exchange interaction is the dominating energy scale compared to the electron temperature $J(\epsilon) \gg T_e$" [50]. Voltage pulses changing the detuning ϵ and therefore $J(\epsilon)$ are used to drive rotations around one axis on the Bloch sphere, whereas the second rotation around the orthogonal axis is driven by the magnetic field gradient ΔB_z, which is generated by DNP, across the two quantum dots [39]. With these two degrees of freedom all points on the surface of the Bloch sphere can be reached.

Read-out can be realized by spin to charge conversion [42]. This read-out scheme relies on the Pauli spin blockade to enable measurement of electron spins. Fig. 2.10 shows the

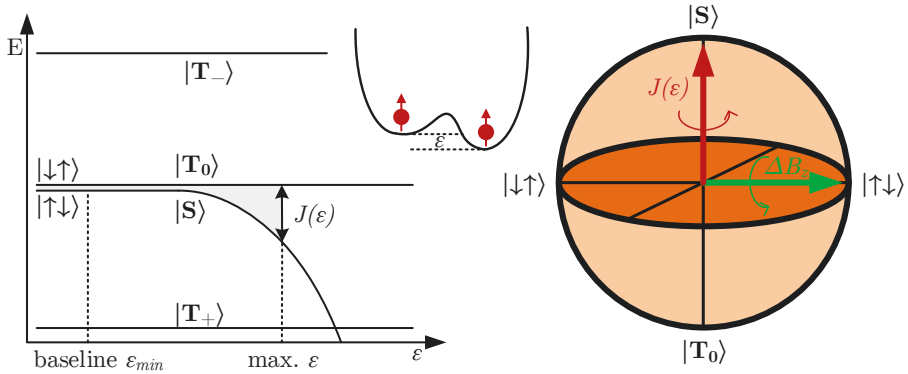


Figure 2.9: S-T_0 qubit energy diagram and states on the Bloch sphere. Fig. adopted from [39, Fig. 1] and [51, Fig. 1].

concept of changing the capacitance of the quantum point contact (QPC) C_{QPC} depending on the qubit states $|S\rangle$ and $|T_0\rangle$. The electric field of either one or two electrons in the left quantum dot is influencing C_{QPC}. These variations can then be measured by RF reflectometry like done in [50] and [3]. Details of how the qubit state either allows or disallows for both electrons to move to the left QPC is given in [50].

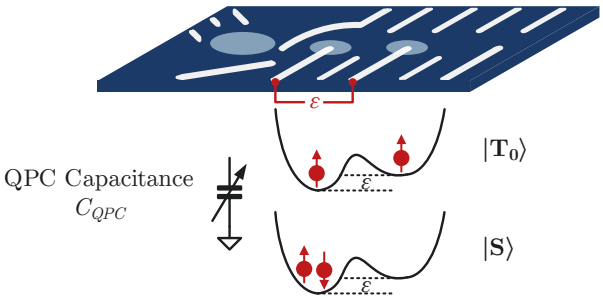


Figure 2.10: S-T_0 qubit read-out by spin to charge conversion.

Concerning the requirements for DC voltages to form the potential well and tune the qubit into operation following requirements were conducted from a research cooperation with Prof. Hendrik Bluhm, who holds – together with his research group – a long track-record of (GaAs) qubit research [2, 3, 19, 39, 40, 44, 48, 50–53]. For a single GaAs qubit consisting of two quantum dots up to eight independently controllable bias voltages with an output range of −1 V to 0 V and a step size of 250 µV are required. Meanwhile, noise should be minimized as much as possible down to around a root-mean-square value of $v_{RMS} \lesssim 20\,\mu V$. These design goals for the later discussed cryogenic integrated circuit (IC) are also summarized in Table 3.1.

2.3.3.2 Si/SiGe Qubits

Si and SiGe host materials for implementation of qubits have some advantages over GaAs, like the absence of nuclear spin in isotopically purified ^{28}Si, as well as a comparably weak spin-orbit interaction and thus promising long coherence times [19]. Fig. 2.11 shows the implantation in different materials like SiGe and isotopically purified ^{28}Si alongside a qubit created with a p-donor in contrast to electron spins caught in a quantum dot.

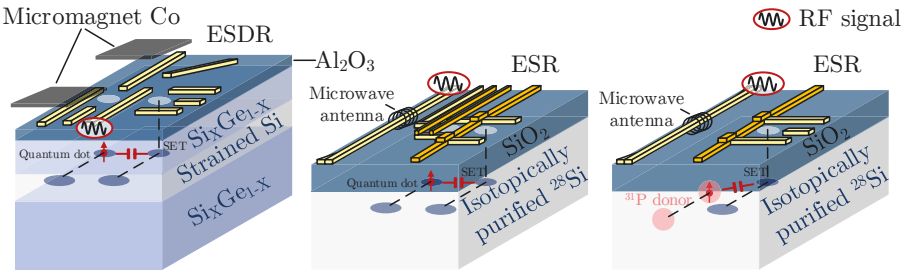


Figure 2.11: Si/SiGe qubit topologies. Fig. adopted from [19, Fig. 1]

Unlike GaAs qubits, Si/SiGe qubits are in most research groups made of a single quantum dot and electron spin [36–38, 54–56], also called Loss-DiVincenzo qubit [57]. Moreover, a scalable qubit gate architecture approach for single quantum dot SiGe qubits was proposed in 2016 [58]. Either electron spin resonance (ESR) pulses emitted by a microwave antenna or electron dipole spin resonance (ESDR) of RF signals is employed to achieve qubit manipulation. Thus, RF signals are required opposed to GaAs qubits control via baseband voltage pulses, e.g. Struck et al. [59] use a reference frequency of 19.9 GHz for qubit manipulation. An inhomogeneous magnetic field, like for GaAs qubits achieved via DNP, is required for ESDR control and can be generated by adding on-chip cobalt micromagnets. Qubit state read-out is achieved by using a single-electron transistor (SET). [19]

Quantum dot creation follows the same approach as for GaAs qubits, i.e. voltages being applied to metal electrodes to laterally confine potential wells. Discussions with Dr. Schreiber, who focuses on Si/SiGe qubit research in the group of Prof. Bluhm (see section 2.3.3.1), showed that Si/SiGe qubits have similar requirements to bias voltages as their GaAs counterpart, with one distinction being a wider output range of −1 V to +1 V. Furthermore, as only one quantum dot is required per qubit, only fewer bias voltages are needed per qubit.

2.4 Cryogenic Electronics

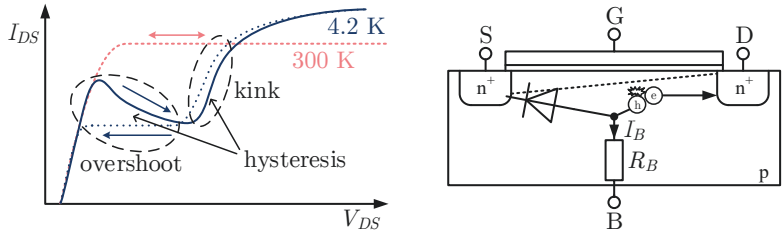
For a universal quantum computer, which fulfills the DiVincenzo Criteria (see section 2.2), millions or even billions of physical qubits are required, considering the nowadays often-named ratio of 1000 physical qubits per logical qubit for error correction schemes [2, 60]. This gives rise for the need of local classical cryogenic control electronics, to mitigate interfacing problems arising when scaling the number of qubits, e.g. feeding an

increasing amount of cables supplying DC voltages, pulses or RF signals into and out of the cryostat. One promising approach is using modern semiconductor industry CMOS technologies to design custom circuits operating inside the cryostat and in close vicinity of the qubits [2].

2.4.1 Cryogenic CMOS

When operating CMOS transistors at temperatures as low as 100 mK some cryogenic anomalies changing the behavior of transistors are appearing, which are not included in standard semiconductor process design kits (PDKs) caring typically covering temperature ranges of −40 °C to 120 °C. Modeling of various CMOS technology nodes and process flavors at cryogenic temperatures is a field of ongoing research and aims to provide IC designers with device models tailored to the cryogenic environment inside a dilution refrigerator, e.g. for 40 nm bulk CMOS [61] and 28 nm bulk CMOS [62].

Starting from older technology nodes Creten et al. [63] showed in 2009 the effects of kink, overshoot and hysteresis appearing in 0.7 µm CMOS at 4.2 K. Fig. 2.12a shows a kink, which is explained by self-polarization due to impact ionization by hot carriers. At room temperature (RT), this impact ionization is normally able to flow off via the bulk contact of the substrate. However, in cryogenic temperatures dopant freeze-out in the substrate is creating a high-ohmic substrate R_B, blocking the current flow I_B as depicted in Fig. 2.12b. Thus, leading to a shift in threshold voltage V_{TH}, because of the self-polarization induced bulk-source voltage V_{BS}. Incandela et al. [61] explain the flatting out in the current jump as effect of the bulk-source junction diverting most of the current flow and thus gradually saturating I_B. The overshoot in the transition of linear to saturation region at temperatures below 15 K is reasoned with slow ionization processes of the dopants and slow recharging of interface traps at the substrate to oxide transition border, thus delaying the formation of the depletion layer. [63, 64]



(a) Kink, overshoot and hysteresis anomalies in 0.7 µm CMOS. As reported in and adopted from [63, Fig. 1].

(b) Schematical cause of kink effekt. Adopted from [61, Fig. 11].

Figure 2.12: Cryogenic anomalies in CMOS MOSFETs.

Measurements of transistor characteristics in modern CMOS processes of 0.16 µm and 40 nm at 4 K and down to temperatures as low as 100 mK are shown by Incandela et al. [61]. They show that a kink behavior is absent for modern CMOS processes (thin-oxide FETs in 0.16 µm and all FETs in 40 nm) and only two thick-oxide NMOS transistors

exhibit a kink in the I-V curve, which the authors describe as: "This [thick-oxide short-channel 0.16 µm NMOS devices] type of transistors, in fact, closely resembles a 0.35 µm device [...]". The authors further support the statement of a kink being present only in older technologies, i.e. feature sizes larger than 0.35 µm and at temperatures below 100 mK. Hysteresis is also only present for thick-oxide FETs in 0.16 µm and the authors of [61] conclude an insignificance for nanometer nodes, as the presence of hysteresis is connected to a kink behavior leading to a difference in V_{TH} when turning the transistor on and when turning it off as V_{TH} was for the latter lowered by the kink effect. Thus, a kink and hysteresis effect are not to be expected for core devices in this work relying on 65 nm bulk CMOS, however thick-oxide devices are still possibly exhibiting one or both effects at cryogenic temperatures. All measurements of [61, 62] showed the absence of an overshoot and did not report on such a behavior for modern CMOS processes.

Another aspect of cryogenic CMOS, which also holds true for nanometer nodes, is the increase in mobility μ and V_{TH} as well as a significant steeper substhreshold slope SS for cryogenic temperatures compared to RT. Mobility is increasing due to reduced electron phonon scattering at lower temperatures [65], which is leading to a higher maximum transconductance g_m as well as an overall steeper g_m curve [66], plotted in [66, Fig. 2b]. The effect of V_{TH} increase is investigated in detail in [66], arguing against the usual thought of channel dopant freeze-out and according required ionization voltage/energy playing a major role [61]. Beckers et al. [66] see the reason for an increase and saturation of V_{TH} in the temperature dependence of the bulk Fermi potential as well as in the temperature dependent density of interface traps close to the band edge, whereas "dopant freeze-out is of minor importance to predict the qualitative behavior of V_T [named V_{TH} in this work] over temperature in enhancement-mode devices" [66]. An overview of cryogenic DC characteristics of modern bulk CMOS processes in cryogenic temperatures is given in Table 2.2, showing the according RT value in parentheses. Transconductance over drain current g_m/I_D is given for weak inversion (w.i.) and strong inversion (s.i.). Shift in threshold voltage is defined as the difference between RT $V_{TH,RT}$ and cryogenic $V_{TH,4K}$: $\Delta V_{TH} = V_{TH,4K} - V_{TH,RT}$. Some values for the 28 nm process required manual extraction from plots [67, Fig. 2] and are therefore subject to imprecision. Those are accordingly marked in Table 2.2.

Authors of a recent published paper in July 2020 Yang et al. [68] characterized commercial 40 nm bulk CMOS devices at deep cryogenic temperatures of 50 mK and showed classical MOSFET behavior with improved performance compared to RT as well as some quantum mechanical properties like Coulomb blockade oscillations for low V_{DS} and near V_{TH}. Comparisons of the MOSFET performance parameter at RT and 50 mK are summarized in Table 2.3, showing results for low $V_{DS} = 0.1$ V and high $V_{DS} = 1.0$ V biasing conditions. Measurement was performed on 18 similar DUTs, i.e. planar n-type low threshold FETs with a length 40 nm and width of 120 nm, and Table 2.3 includes statistical results for these. These results are further substantiating the usage of local classical commercial CMOS for co-integration with the qubits on the lowest temperature stage inside a dilution refrigerator.

Additionally, non-planar and non-bulk CMOS processes are being characterized at cryogenic temperatures, e.g. FinFET [69], 28 nm [70–72] and 22 nm [73] FDSOI, 14 nm SOI FinFET [74], and Gate-All-Around Nanowire MOSFETs [75]. Especially the opportunity

Characteristic		0.16 µm [61]	40 nm [61]	28 nm [67]	
W/L	[µm]	2.32 / 0.16	1.2 / 0.04	3 / 1	0.3 / 0.028
ΔV_{TH}	[V]	0.15	0.12	≈0.12	≈0.16
SS	[mV/dec]	22.8 (87.0)	27.7 (88.2)	11 (≈62)	≈18 (≈95)
n	[-]	28.7 (1.5)	34.9 (1.5)	≈13 (≈1.4)	20 (1.47)
$I_{on,4K}/I_{on,RT}$	[-]	1.33	1.13	≈1.28	≈0.9
I_{off}	[A]	$<3 \cdot 10^{-11}$ ($<1.6 \cdot 10^{-10}$)	$<1.5 \cdot 10^{-12}$ ($<1.4 \cdot 10^{-10}$)	—	—
λ	[V^{-1}]	3.3 (0.6)	4.0 (1.3)	—	—
μ_0	[cm^2/Vs]	—	—	≈820 (≈270)	≈280 (≈100)
g_m	[S]	—	—	$\approx 7 \cdot 10^{-4}$ ($\approx 4.2 \cdot 10^{-4}$)	$\approx 5.5 \cdot 10^{-4}$ ($\approx 4.5 \cdot 10^{-4}$)
g_m/I_D w.i.	[V^{-1}]	70 (27)	92 (27)	—	—
g_m/I_D s.i.	[V^{-1}]	6 (9)	9 (10)	—	—

Table 2.2: Comparison of cryogenic bulk CMOS characteristics at 4 K (RT).

Temperature		300 K		50 mK	
V_{DS}	[V]	0.1	1.0	0.1	1.0
V_{TH}	[V]	0.388±0.030	0.442±0.036	0.514±0.038	0.510±0.037
SS	[mV/dec]	86.41±2.43	86.88±1.69	9.93±4.32	15.79±6.27
g_m	[µS]	21.48±1.79	118.07±7.48	29.51±6.02	144.53±10.48
ΔV_{TH}	[V]	—	—	0.126±0.017	0.067±0.011
$DIBL$	[mV/V]	162.22±27.85		113.33±24.67	

Table 2.3: Comparison of 40 nm bulk CMOS characteristics at RT and 50 mK. As reported in [68, Table I].

to influence and possibly counteract the cryogenic V_{TH} increase in FDSOI processes could be a promising approach for future cryogenic circuitry [76].

Passive elements like capacitors and inductors are less prone to changes in cryogenic temperature regime compared to RT [77]. Resistor changes are depending on their implementation. Polysilicon (±10 %) and p-active (±20 %) resistors are mostly stable over temperature. However, n-well resistors are shown to exhibit a significant increase of multiple magnitudes in resistivity. [78]

One last aspect of operating CMOS technologies at cryogenic temperatures is transistor mismatch, which is reported to commonly deteriorate by a factor of 1.2 to 2 [79]. A recent paper by P. A. 'T Hart [80] showed extensive research on characterization and modeling of mismatch in 40 nm CMOS for cryogenic temperatures. Major conclusions are that the Pelgrom scaling law [81] holds valid also in cryogenic temperatures down to 4.2 K. Current-factor variability increases by 75 % and "threshold-voltage variability

remains substantially unaffected". Furthermore, the authors use a Croon model to reflect and predict this cryogenic drain current mismatch. However, reliable CMOS device models do not yet exist with important characteristics like AC, RF and noise behavior at cryogenic temperatures. Those are still subject to active research and not yet thoroughly investigated [82, 83].

2.4.2 State of the Art

This section aims to give an overview of the current state of the art cryogenic electronics with emphasis placed upon quantum computing applications. In the recent years, the focus on classical control electronics operated at cryogenic temperatures and in closer vicinity to qubits is clearly gaining more attention. Looking at prospects to overcome qubit scaling issues, requiring unpractical amount of room temperature interconnects at some point. Many of those cryogenic electronics are currently targeted for placement on the 4 K stage, which allows for magnitudes higher power dissipation, i.e. about 1 W, than on the lowest temperature stage of a dilution refrigerator with a power budget of <1 mW at $\approx$ 100 mK.

Cryogenic electronics for quantum computing applications range from discrete circuitry over off-the-shelf devices to commercial FPGAs and custom designed ICs. The downside of more complex off-the-shelf commercially available devices like FPGAs or VCOs is the operation far below the specified temperature range. As most off-the-shelf components will be above the <1 mW power limit, those are aimed and tested at the 4 K stage.

Homulle et al. [84] characterized Altera and Xilinx 28 nm FPGAs at cryogenic temperatures. The authors concluded an operation of the Altera Cyclone V down to 30 K, whereas the Xilinx Artix 7 is fully functional down to 4 K. Although, the authors present the prospect of utilizing cryogenic FPGAs in the future error-correction loop of quantum computers, some limitations with off-the-shelf FPGAs have to be overcome. The main limitation being an increase in auxiliary supply power consumption by a factor of 5× at 4 K, which is also concluded to be the reason for the Altera FPGA to stop operating below 30 K. Besides other limitations, such as operating problems with the Altera PLL and a slightly deteriorated maximum register clock speed, most of the cryogenic changes are positive with increased speed, higher driving strength, and overall lower jitter. Albeit FPGAs being a possible candidate for in the overall qubit control loop, recent focus shifted towards research and development of custom ICs aiming for highest efficiency and lowest possible power consumption.

Compared to discrete electronics, custom designed ICs can be tailored towards the application, trading flexibility for improved efficiency in energy and area. In addition to the characterization and modeling advances for cryogenic CMOS already discussed in section 2.4.1, multiple research groups are exploring and implementing cryogenic CMOS circuits, which are able to operate at cryogenic temperatures inside a dilution refrigerator [78, 85]. Most of the work up to this day focuses on implementing, testing and evaluating circuit building blocks for future complex cryogenic CMOS systems. A listing of such blocks is given in Table 2.4, without a claim for completeness. Table 2.4 shows the ongoing trend to design in more increasingly advanced technology nodes and

aim for modern semiconductor compatibility to achieve high integration density with best energy efficiency and thus scalability. Most of the circuitry either aims for on-chip reference voltage generation by bandgaps, qubit control (QC control) or read-out (QC read-out), however, to the best of the author's knowledge no other work focuses on qubit bias voltages (QC biasing) with respect to a local cryogenic scalable IC.

Block	Temp.	Technology	Year	Application	Ref.
FPGA	4 K	28 nm bulk CMOS	2017	QC	[84]
Bandgap	4 K	40 nm bulk CMOS	2018	QC	[86]
Bandgap	4 K	40 nm bulk CMOS	2019	QC	[87]
Bandgap	4 K	0.35 µm SiGe BiCMOS 28 nm FDSOI CMOS	2019	QC	[88]
TIA	4 K	0.5 µm SOS CMOS	2014	QC read-out	[89]
LNA	4 K	160 nm bulk CMOS	2018	QC read-out	[78]
DCO	4 K	40 nm bulk CMOS	2018	QC control	[78]
ADC	4 K	0.7 µm bulk CMOS	2009	Space/Sensor	[63]
ADC	4 K	0.35 µm bulk CMOS	2010	Space/Sensor	[90]
ADC	20 K	0.35 µm bulk CMOS	2013	Space/Sensor	[91]
ADC	77 K	180 nm bulk CMOS	2018	Space/Sensor	[92]
ΣΔ mod.	4 K	0.35 µm bulk CMOS	2012	Space/Sensor	[93]
DAC	93.15 K	0.5 µm SiGe BiCMOS	2008	Space/Sensor	[94]
DAC	93.15 K	0.5 µm SiGe BiCMOS	2011	Space/Sensor	[95]
DAC	4 K	0.5 µm SOS CMOS	2016	QC control	[96]
DAC	6 K	65 nm bulk CMOS	2020	QC biasing	[97]*

Table 2.4: Overview to state of the art of cryogenic IC blocks. *This work.

In 2019, an increasing number of complex systems for qubit control is emerging, see Table 2.5, taking the scalability aspect of qubit control to the next level. By showing complex systems capable of operating at cryogenic temperatures of 4 K [85, 98] and even 100 mK [99] to manipulate one or even multiple qubits, always taking future scaling and scalability into consideration, one can see the current momentum in cryogenic IC development for QC applications.

An overview of analog and mixed-signal cryogenic CMOS circuitry design challenges and advantages is given by van Dijk et al. [83]. The authors give detailed recommendations and hints to potential pitfalls when designing cryogenic IC blocks, like digital circuitry, voltage references, DACs and ADCs. Furthermore, the challenges in QC requirements are highlighted, naming the need of cryogenic CMOS electronics "on par or even exceeding their room-temperature counterparts". However, the deep cryogenic temperatures also hold opportunities for higher circuit performance, e.g. for MOSFETs as discussed in the previous chapter 2.4.1, which can be utilized. One example highlighted by the authors is the negligible leakage power for digital circuits, therefore recommending the usage of

Temp.	Technology	Year	Application	Function	Ref.
4 K	28 nm bulk CMOS	2019	QC control (Transmon)	4 GHz to 8 GHz pulse modulator for qubit manipulation.	[98]
4 K	22 nm FinFET CMOS	2020	QC control (Tansmon)	2 GHz to 20 GHz FDMA polar modulator for manipulation of multiple qubits.	[85]
4 K	40 nm bulk CMOS	2020	Digital signal processing	Cryogenic RISC-V processor.	[100]
100 mK	28 nm FDSOI CMOS	2019	QC control (GaAs spin)	Generate static and dynamic voltages for manipulation of multiple qubits.	[99]
100 mK	65 nm bulk CMOS	2019	QC biasing and control (GaAs spin)	Generate bias voltages and voltage pulses for qubit manipulation.	[101]*

Table 2.5: Overview of state of the art of cryogenic IC systems for qubits. *This work, full system yet to be characterized at targeted 100 mK.

low-threshold voltage (LVT) devices or in case of FDSOI the use of back-gate biasing, and a reduced thermal noise $P_{N,TH}$. A summary of the discussed blocks, cryogenic effects and their impact to the circuit are given in Table 2.6. The thermal lower limit of minimum switching energy $E_s(min) = \ln(2)k_BT$ is reasoned by J. D. Meindl and J. A. Davis [102]. Overall, all these effects and changes require that close attention is paid when designing ICs for deep cryogenic temperatures and accurate cryogenic models are necessary.

Block	Cryo change	Effect
Digital circuitry	Steeper SS	Negligible leakage currents (use LVT devices or back-biasing)
	Increased V_{TH}	Slower maximum speeds
	Increased I_{ON}/I_{OFF} ratio	Larger signal swing
	Reduced $P_{N,TH}$	Reduced noise margin needed
	Increased charge mobility μ	Higher maximum speeds (overmatched by V_{TH} increase for advanced nodes)
	Reduced minimum thermal switching energy limit $E_s(min)$	Operate at very low supply voltages
Voltage references	Freeze-out	BJTs lose exponential behavior and required base-emitter voltage is above 1 V
	Increased V_{TH}	Narrowed supply headroom
	Steeper SS	No advantage moving to weak inversion to increase headroom
	Increased mismatch	Avoid weak inversion (and usage of chopping and dynamic element matching)
	Increased flicker noise	Use of mitigation techniques (e.g. chopping)
DACs and ADCs	Freeze-out	Passive element values may vary significantly (use polysilicon resistors: temp. stability ±10 % and metal capacitors temp. stability <10 %)
	Increased V_{TH}	Increased resistivity of pass gates for mid-rail voltages (use boot-strapped switches or thick-oxide transistors with higher supply)
	Reduced $P_{N,TH}$	Less capacitance required k_BT/C, use of larger resistances possible $4k_BTR$, allows lower unit currents
	Increased mismatch	Larger device dimensions, use of calibration techniques
	Reduced interconnect resistance	Reduced IR-drop, reduced interconnect delay, relaxed routing constraints (e.g. timing errors in the clock tree)

Table 2.6: Cryogenic CMOS circuitry: challenges and opportunities. As discussed in [83].

Chapter 3

System Overview

This chapter gives a system and block level overview about the system proposed in this work and its application environment. First, the overall setup including the vision of scalable cryogenic control electronics inside a dilution refrigerator is presented. Second, the power budget inside a dilution refrigerator and the low noise that each signal connected to the qubit is required to have and the consequences arising for the system are discussed. In the following, the requirements for the Bias-DAC generating the voltages forming the potential well are derived and implementations that enable possible future scaling are presented.

3.1 Local Cryogenic Control Electronics

The general setup of a dilution refrigerator is divided into many temperature stages gradually reducing the temperature from ambient temperatures down to the base temperature of the mixing chamber which is in the range of 10 mK to 100 mK for spin-based qubits, see section 2.3.3. The inner setup of a dilution refrigerator is shown in Fig. 3.1. The 4 K stage, the intermediate stages and the mK sample space are marked. The intermediate stages are used to create the temperature gradient between the lowest temperature stage and the 4 K stage. A sample and its PCB are typically mounted vertically or horizontally inside the sample space. Typical PCB dimensions which can still be fitted inside the sample space of the dilution refrigerator of our project partners at RWTH Aachen University physics department are about 5 cm × 10 cm and are mounted vertically.

The joint paper of many solid-state qubit research groups by Vandersypen et al. [2] is focusing on possible ways for future qubit scaling. This is needed due to two arising challenges when the number of qubits are scaled towards the estimated required number of 10^6 to 10^8 physical qubits. The sheer number of DC and RF connections required for each individual qubit leads to a magnitude of cables required to be fed into the cryostat. Furthermore, the required bandwidth of multiple Tb/s appears unpractical and following example is calculated in the paper: “For example, if 108 qubits are repeatedly read out at 1 µs intervals and each qubit measurement provides one bit of information, the data flow amounts to 100 Tb/s” [2]. The paper also names two ingredients for overcoming these challenges:

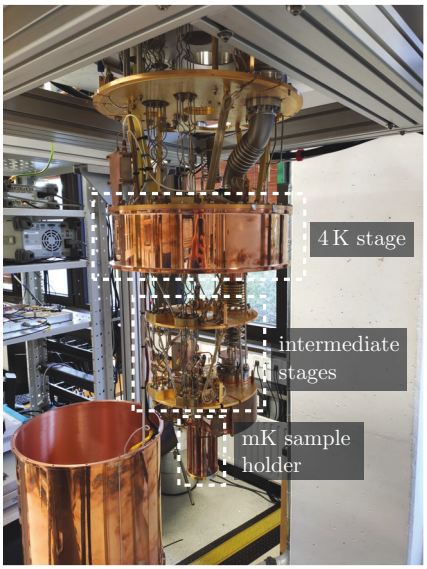


Figure 3.1: Inner setup of a dilution refrigerator.

1. Multiplexing strategies
2. A first layer of classical electronics residing next to the qubits and commensurate with the inter-qubit spacing

The paper further addresses the idea of successively placing layers of rising complexity of classical electronics on higher temperature stages, following a hierarchical setup approach. In this approach, where classical electronics may be placed on each temperature stage, processing more complex tasks and operations are feasible due to the increased power budget of higher temperature stages, while retaining an manageable interface complexity to the neighboring temperature and operating stage.

The aim of this work is to design a custom IC in a modern TSMC 65 nm CMOS process, which is then placed in close vicinity to the qubit inside the mixing chamber generating bias voltages. The IC also includes circuitry to generate pulsed control voltages, for a two electron spin based GaAs qubit, but this is not focus of this work. Naturally, this requires connections from room temperature to supply voltages and fed control signals into the chip. Figure 3.2 shows the concept of placing a CMOS chip next to the qubit chip in order to generate local control and biasing voltages. Additional classical electronics may be placed at the 4 K stage, utilizing lower thermal noise, reduced interconnects to room temperature and shorter signal paths to the mK sample stage.

This is done as a first step towards a vision of a fully scalable quantum computer. One could think of a connection of classical control electronics face-to-face with a qubit chip by through-silicon-vias (TSVs) as a solution to the interconnect issue in an universal quantum computer. However, there are still open questions to this approach as to which materials could be used to thermally decouple the classical control chip while having a good electrical connection and if superconducting materials could be a viable solution to

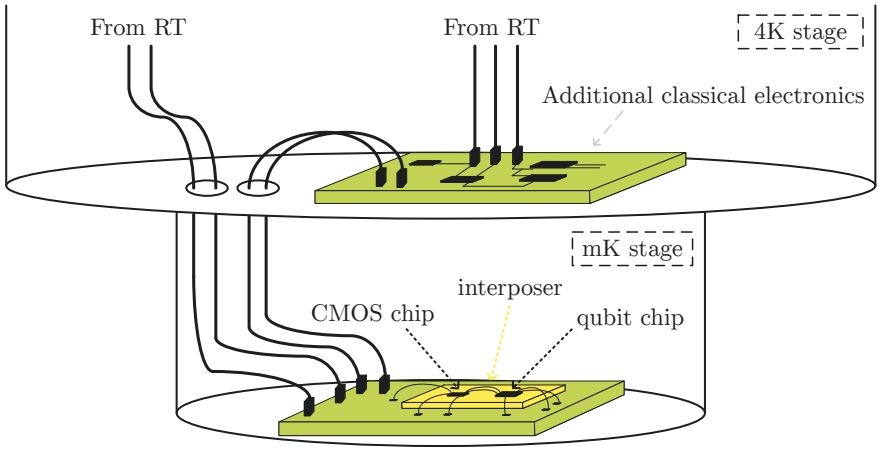


Figure 3.2: Schematic setup of classical cryogenic electronics and custom CMOS chip for qubit control. Both chips are placed on an interposer and connected via interconnect technologies like, e.g. wire bonding.

achieve that goal. Some of these questions have recently been addressed in published research articles and include prototype implementations, which are discussed in the following paragraph.

The vision of cryogenic superconducting TSV interconnects is also gaining attention and increased focus by other research groups like presented in [103] in May 2020:"Solid-state qubits integrated with superconducting through-silicon vias" [103]. The paper demonstrates integration of the electronics with superconducting qubits as a promising approach for 3D system integration. The authors showed baseband control and high fidelity read-out by high-aspect ratio TSVs in a two-chip bump-bonded architecture. The negative effects of using industry standard deposited inter-layer dielectrics (ILDs) materials like SiO_2 and Si_3N_4 are also described. Those materials deteriorate qubit lifetimes due to present defects and electric field interactions. The common material used for the TSV itself is metal, e.g. copper, which is a good electrical conductor but offers only a low thermal resistivity. One suggested approach by the authors is to make use of the cryogenic temperatures and employ superconducting materials, e.g. Niobium (Nb), which is used in various superconducting alloys like Niobium–titanium and exhibits a critical temperature of about 10 K [104]. These materials would allow for almost ideal electrical conduction while maintaining a low thermal conductivity. With a footprint of 10 µm × 20 µm for the superconducting titanium nitride (TiN) TSV and a pitch of 1 TSV per 100 µm, the authors conclude up to 10 000 TSV interconnects being possible for a 10 mm × 10 mm die [103]. A similar approach is taken by Alfaro-Barrantes et al. [105]. The main distinction is the change in TSV material to CMOS-compatible superconducting aluminum (Al) at temperatures below 1.28 K. Due to their CMOS-compatibility, Al TSVs are a promising candidate for "high-density 3D integration for Si-based quantum computing" [105]. Concluding, current research results support the idea of superconducting TSVs as a scalable mean to interface local cryogenic classical

electronics and the qubits layer. The superconducting properties allow for almost ideal electrical connectivity while minimizing thermal conduction and therefore disturbance to the qubit fidelities.

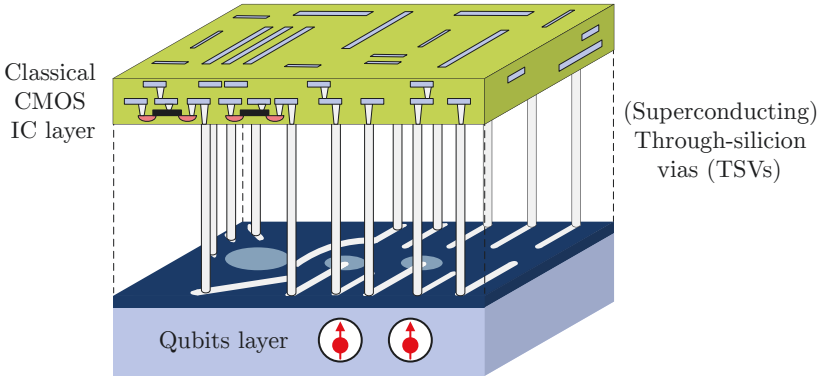


Figure 3.3: Vision of classical cryogenic electronics and custom CMOS chip for qubit control building a fully scalable general purpose quantum computer.

One of the circuitry being included in this local cryogenic control electronics is expected to be the qubit biasing. System level considerations about this Bias-DAC are presented in the following part of this chapter.

3.2 Bias-DAC Requirements

This section elaborates more detailed on system level design choices concerning the Bias-DAC supplying the voltages to form the potential well. For the generation of potential wells as described in section 2.3.3.1 multiple quasi-static DC voltages are required. The following table 3.1 sums up the requirements with impact on the Bias-DAC design. These requirements are originating from qubit characteristics and discussions with Prof. Hendrik Bluhm and his research group, see end of section 2.3.3.1. Noise requirements are specified as root mean square voltage v_{RMS} of the total integrated voltage noise spectral density v_n.

A voltage range of 1 V, i.e. from −1 V to 0 V, enables the formation of potential wells and thus the creation of quantum dots. The voltage range is mostly determined by the variability of the qubit samples and depends on the qubit type and implementation. A voltage step size of 250 µV allows for fine tuning of the quantum dots into (in most cases) single electron regime. This tuning is up to now and to the best of the author's knowledge done manually although there is ongoing effort to automate the tuning of the qubits, e.g. [53]. The output noise v_{RMS} should be minimized and kept below 20 µV in order to achieve high qubit fidelity rates, which are comparable to current state of the art qubit experiments ($\gtrapprox$ 99 %). The Bias-DAC is placed in close vicinity to the qubits and is therefore required to operate at the same cryogenic temperatures, i.e. $<$ 1 K and typically around 100 mK. The capacitance of a single metal electrode for the qubit structure (ref.

to Fig. 2.8) is about 100 fF and up to 8 electrodes per qubit have to be supplied by the Bias-DAC with uncorrelated bias voltages.

Characteristic	Specification
Output voltage range	−1 V to 0 V
Output noise v_{RMS}	≤ 20 µV
Output voltage step size	250 µV(≈ 12 bit)
Temperature	< 1 K
Total power budget at 100 mK	< 1 mW
Output load	100 fF
No. of bias voltages per qubit	≤ 8

Table 3.1: Bias DAC Specification obtained from discussions with RWTH Aachen University physics department.

For operation of the Bias-DAC a standardized interface is required to set registers, write and read data. From the most commonly used and quasi industry standard interface options like: JTAG, I^2C, SPI, LVDS etc. I^2C holds the best trade-off for the application, as only low speed and low bandwidth communication is required. Moreover, I^2C has the charm of being a 2-wire interface resulting in less interconnects from room temperature into the cryostat and thus reduced thermal load. Moreover, an I^2C interface in the same technology is already available in-house and has been validated to be operational with dipstick measurements at liquid helium temperature of 4.2 K.

3.3 Power Budget

The power budget inside nowadays dilution refrigerators at the lowest temperature stage is limited to about 1 mW [2] and thus also the power dissipation of any electronics placed on the same temperature stage are required to be operating below that limit or the qubit fidelity will deteriorate. Therefore, long-term scaling should be taken into considerations and only the minimum amount of electronics should be placed at cryogenic temperatures in the mixing chamber.

In the beginning of this section an example of a dilution refrigerator setup was shown, see Fig. 3.1. The different temperature stages differ notable in their cooling power. The cooling power of the 4 K stage, which is about 1 W to 2 W, is significantly higher than the cooling power of the mixing chamber [2]. Naturally, allowing for more and more complex circuitry and computational tasks. However, the following discussion is aimed mainly towards the lowest temperature stage.

In order to illustrate the challenge placed upon the power dissipation of the first layer electronics inside the mK stage following example can be calculated. Taking the lower end of the spectrum of the generally considered number of required qubits for a universal quantum computer, which is around 10^6 physical qubits, and 3 DC voltages per qubit

for creating the potential well, we end up with: $1\,\mathrm{mW}/(10^6 \cdot 3) \approx 0.3\,\mathrm{nW}$ per qubit per generated DC voltage.

The power consumption of a conventional D-flipflop in the used 65 nm CMOS technology with an estimated load of $C_{Load} = 20\,\mathrm{fF}$ for interconnects and capacitive load of the following circuitry and a clock frequency of 250 MHz has an internal power consumption of about $0.006\,\mu\mathrm{W/MHz} \cdot 250\,\mathrm{MHz} = 1.5\,\mu\mathrm{W}$. Discussions with the GaAs qubits research group of Prof. Hendrik Bluhm at RWTH Aachen University lead to 250 MS/s voltage pulses for qubit control, which defines the clock frequency of the IC. The dynamic power consumption due to charging of the load (worst case, change in the output signal each clock cycle: $\sigma = 0.5$) is:

$$P = \sigma \cdot f \cdot C_{Load} \cdot V_{DD}^2 = 0.5 \cdot 250\,\mathrm{MHz} \cdot 20\,\mathrm{fF} \cdot (1.2\,\mathrm{V})^2 = 3.6\,\mu\mathrm{W} \tag{3.1}$$

In consequence the power consumption for a single D-flipflop, which is a standard device used in almost all IC designs, is already exceeding the allowed power consumption by a factor of $(3.6\,\mu\mathrm{W} + 1.5\,\mu\mathrm{W})/0.3\,\mathrm{nW} = 17000$. A supply voltage reduction by a factor ≈ 100 seems possible for a dedicated croygenic CMOS technology to 10 mV [52], resulting in an decrease in power consumption by a factor $100^2 = 10000$ and therefore the power is $(3.6\,\mu\mathrm{W} + 1.5\,\mu\mathrm{W}) \div 10000 = 0.51\,\mathrm{nW}$. This would enable CMOS designs that could cope with the ultra-low power requirements inside a dilution refrigerators even for a larger number of qubits. Another option would be to move the qubits to higher temperatures to significantly increase the cooling power budget, e.g. this would result in a factor of 1000 to 2000 in cooling power when moving from 100 mK to 4 K. First ideas of this approach are discussed in [2], but show some additional challenges in qubit design. Both options are a field of ongoing research [52, 106–108].

With the prospect of a dedicated cryogenic CMOS technology with lowered supply voltage in combination with vanishing leakage currents due to the very steep sub-threshold slope, the power consumption of digital blocks can be greatly decreased. However, the supply voltage of analog blocks, e.g. digital-to-analog converter, cannot be reduced as the qubits require specific voltage ranges to operate, e.g. for the bias voltages –1 V to 0 V, see Table 3.1. Moreover, analog circuits cannot gain as much as digital blocks in terms of power reduction from the very steep sub-threshold slope. This places special emphasis on approaches to limit power consumption for analog blocks.

In summary, it is shown that meeting power consumption requirements enabling a universal computer consisting of one million or more physical qubits is a challenging endeavor. On the other hand, research in these areas is ongoing with increasing momentum as described previously. As a dedicated cryogenic CMOS technology appears to be indispensable in order to reduce power consumption of all digital blocks effectively for a fully scaled universal quantum computer, this work will lay special emphasis on ways to scale analog and mixed-signal circuitry and limit the power consumption of these.

3.4 Low Noise

Qubits are commonly very sensitive to noise due to their quantum mechanical nature of coherence and decoherence, see section 2.3.3. For utilization of the quantum mechanical features, like superposition and entanglement, in order to perform computation, a coherent quantum state is required, as described in more detail in the previous chapter 2. Therefore, qubits are always dealing with the challenge of operating between the following two poles. On the one hand, an as low as possible interaction with other particles is required in order to maintain a coherent state. On the other hand, the quantum state has to be manipulated, e.g. for initialization, in order to perform quantum gates (operations) or read-out, which requires interaction with the outside world. One important step for longer coherence and dephasing times of the qubits is to minimize noise presented to the qubit.

One benefit of going to deep cryogenic temperatures is the natural reduction in thermal noise. As shown in [2] noise on metal electrodes for semiconductor spin-based qubits should be aimed to be kept within a few µV of v_{RMS}. The mean-square $|\overline{v_n}|^2$ thermal noise is defined as the Johnson–Nyquist noise of the storage capacitor C_S also referred to as "kTC noise", see Fig. 3.6 and 3.7. This capacitor C_S stores the generated bias voltage for one qubit electrode and is independent of the later chosen Bias-DAC topology, because a permanent driving of the qubit electrodes seems misplaced in the presence of a purely capacitive output load and the previously described ultra-low power constraints, see section 3.3. The thermal noise of C_S can be calculated by [109]:

$$|\overline{v}_n|^2 = \frac{k_B T}{C_S} \tag{3.2}$$

$$|v_n| = v_{RMS,C} = \sqrt{\frac{k_B T}{C_S}} \tag{3.3}$$

This yields to a required capacitance value of $C_S = 1.38\,\text{pF}$ at 100 mK to limit the RMS noise to $v_{RMS,C} = 1\,\mu\text{V}$ when considering only the Johnson–Nyquist noise. Some additional noise will be added by reference voltages of the Bias-DAC as well as the Bias-DAC itself, which is discussed in the following.

What is expected to be of more concern in terms of introducing noise is the impact of leakage current draining the capacitance C_S and a required periodical refresh of the voltage level, depending on the present leakage current, which is expected to be significantly reduced (due to an increased sub-threshold slope at cryogenic temperatures) yet still present. The impact of this leakage is in principle shown in Fig. 3.4. Leading to a trade-off between power and area on the one side and noise on the other side. Area is also effected as a higher refresh rate leads to less number of channels a single Bias-DAC is able to supply, which will be discussed more deeply in section 3.5 considering challenges and opportunities for scaling up the number of supplied qubits.

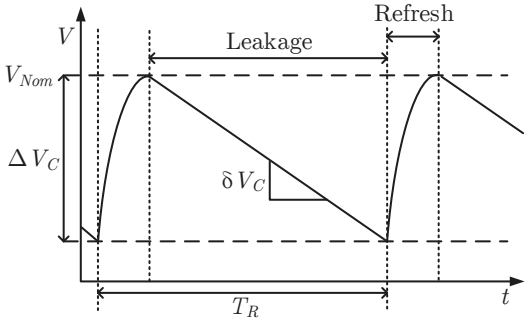


Figure 3.4: Leakage current I_L has to be compensated by a periodical refresh of the stored charge on a capacitor C_S. This example has a leakage to GND with a slope of $\delta V_C = \frac{\mathrm{d}V_C}{\mathrm{d}t} = I_L/C_S$.

When considering a constant total leakage current I_L either to V_{DD} or GND through an arbitrary number of leaking paths, the required refresh rate $f_R = \frac{1}{T_R}$ to limit the change in voltage on the storage capacitor to $\Delta V_C < v_{RMS}$ can be calculated by:

$$\Delta V_C = \frac{1}{C_S} \int_0^{T_R} I_L \, \mathrm{d}t \tag{3.4}$$

$$\Delta V_C = \frac{1}{C_S} \cdot T_R \cdot I_L \tag{3.5}$$

$$f_R = \frac{1}{T_R} = \frac{I_L}{C_S \cdot \Delta V_C} \tag{3.6}$$

In the following considerations, a value of 2 pF is chosen for the storage capacitor, resulting in a unit capacitor of 1 pF for the Bias-DAC implementation. With a leakage current of $I_L = 1\,\mathrm{pA}$ the refresh rate to reach $\Delta V_C \leq 1\,\mu\mathrm{V}$ on a 2 pF capacitor is $f_R = 500\,\mathrm{kHz}$. Considering the power constraints discussed in the previous chapter this is still a relatively high frequency with only $0.\bar{3}\,\mathrm{nW}$ per channel available. However, this is linearly depending on the present leakage currents, which are expected to be significantly reduced due to cryogenic effects like bulk freeze-out and an increased SS, see section 2.4.1. The size of the storage capacitor C_S of 2 pF seems to be on the edge of what can be considered reasonable, leading to a size of the storage capacitor of about $31\,\mu\mathrm{m} \times 31\,\mu\mathrm{m}$ considering a common capacitance density in modern CMOS processes of ca. $2\,\mathrm{fF}/\mu\mathrm{m}^2$ for linear metal capacitors.

When considering a periodical refresh one additional thing has to be avoided: The appearance of a significant spur at the present clock frequency on the output voltage. In section 3.3 a clock frequency of 250 MHz was reasoned as this is the pulse rate for controlling the qubit, which naturally results in the qubit being sensitive for signals at that specific frequency. Thus, a low pass filter is required to suppress the clock spur. This low pass can be constructed as a simple passive RC filter by adding a resistor to the storage capacitor. Additionally, a split storage capacitance C_S results in a second

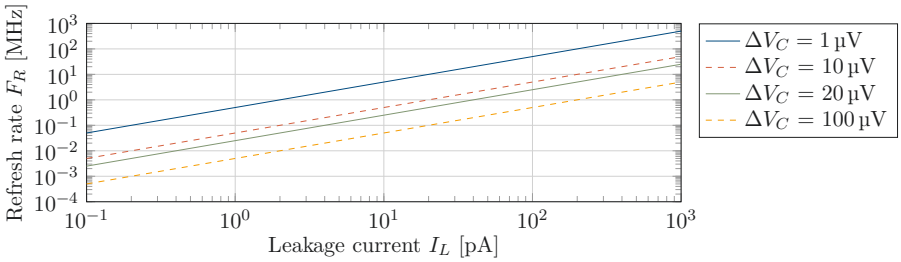


Figure 3.5: Refresh rate f_R required to limit the voltage ripple ΔV_C on the storage capacitor $C_S = 2\,\text{pF}$ due to a leakage current I_L

order RC filter for improved suppression of the clock spur. However, this will come at the cost of increased thermal noise on the output as the "kTC" noise rises, due to the halved capacitance of each individual capacitor $C_1 = C_2 = C_S/2 = 1\,\text{pF}$.

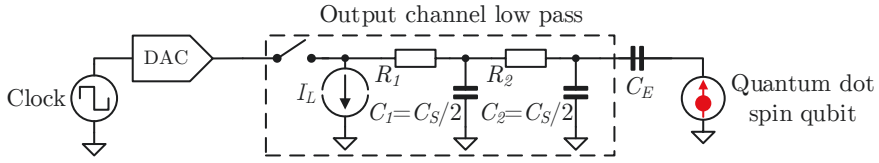


Figure 3.6: Low pass filtering each output stage to suppress clock spur.

Looking at Fig. 3.6 and a capacitor value set to $C_S/2 = 1\,\text{pF}$, values for R_1 and R_2 have to be chosen. In general, a value as big as possible seems best fitting the application, as the potential well voltages have to be changed only at the timescale of milliseconds or even up to seconds. However, some restrictions as to what seems feasible for an integrated resistance, e.g. required die area and cryogenic effects of different resistance types like polysilicon or N-well, implementations have to be considered. Furthermore, R_1 is designed to be smaller than R_2, as we want to charge the first capacitor faster with the Bias-DAC output for improved settling time. After disabling the output switch, the stored charge on the first capacitor C_1 can level gradually through the larger resistor R_2 onto C_2, which holds the output voltage as seen by the qubit. This is done as the duty cycle of output switch is expected to be rather low, i.e. the switch being open for the major part of a refresh cycle. The proposed values for this work are $R_1 = 25\,\text{k}\Omega$ and $R_2 = 150\,\text{k}\Omega$, thus the cut-off frequencies of the two poles are at: $f_1 = 1/(2\pi R_1 C_1) = 6.366\,\text{MHz}$ and $f_2 = 1/(2\pi R_2 C_2) = 1.06\,\text{MHz}$, respectively.

However, all the previous noise considerations were done disregarding the presence of already existing noise on supplies and references. This is further discussed in section 3.6.

3.5 Scaling Opportunities

In this section general considerations about possible ways to scale the number of generated voltages are given while power and area consumption increase is kept to a minimum. As it appears impractical to have an individual Bias-DAC with a minimum required resolution of 12 bit for each qubit electrode, a demultiplexing strategy appears natural to solve this issue. This is also reasoned by the quasi-static character of the bias voltages rendering high sample rates unnecessary. The concept is shown in Fig. 3.7. Each of these output channels can be realized by the low pass S&H structure discussed in section 3.4 and Fig. 3.6. In this work, the Bias-DAC is designed with demultiplexing to eight output channels, because this is the required number of bias voltages for one GaAs qubit, see Table 3.1.

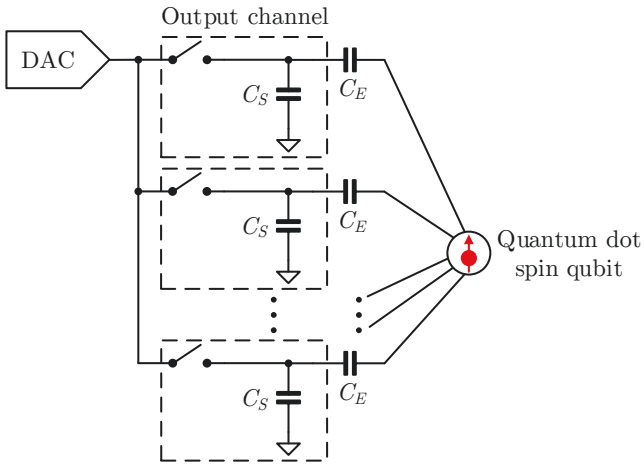


Figure 3.7: A single DAC supplying multiple channels by demultiplexing.

Another idea is to use synergies in the digital logic controlling the Bias-DAC, when using DAC topologies like ΣΔ, PWM or charge-redistribution, which require dynamical switching during operation. The concept would be to generate control signals centralized in one block and later distribute those to the individual Bias-DACs, each having a local memory to save the programmed DAC values. Fig. 3.8 shows the described concept together with the multiple output channels of each Bias-DAC generated by demultiplexing (ref. to Fig. 3.7) and a digital interface for configuration, data write and read.

3.6 Supply and Reference Voltage Noise

The ultra-low noise requirement of today's qubits, which has already been discussed in section 3.4 together with the consequences for the Bias-DAC design, is also placing constraints on the supply and reference voltages. Current setups, e.g. [3, 50], require heavy filtering of signals and bias voltages in order to reduce the noise to a sufficient

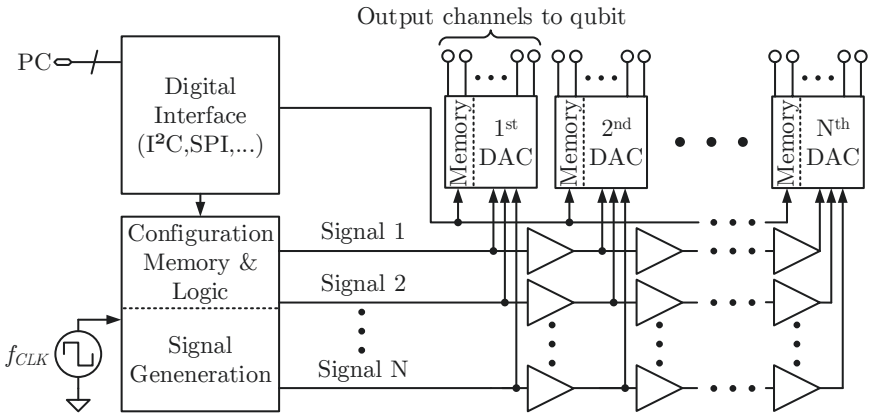


Figure 3.8: Distribution of signals to multiple DACs and their local memory.

level for the qubits. Therefore, in order to also reach a low noise level sufficient for the bias voltages generated by the Bias-DAC, it is required to filter the noise introduced by supply and reference voltages. For comparison, a commercially available low noise LDO like the Texas Instruments TPS7A91 "1-A, High-Accuracy,Low-Noise LDO Voltage Regulator" is barely reaching the noise constraints of $V_{N,RMS} \leq 20\,\mu V$ with an output noise specified as 4.7 µV for the frequency band of 10 Hz to 100 kHz. However, these results are achieved for output capacitors $\geq 10\,\mu F$, giving an idea of the stringent noise specifications one has to fulfill to not disturb a qubit state.

Nowadays the bias voltages required for spin qubit operation, as described in more detail in section 2.3.3, are fed through a cascade of filters anchored at every temperature stage in order to suppress noise [50]. In the current GaAs qubit setup at RWTH Aachen University, filtering is done at RT via switchable low pass filters in the breakout box of the DC lines, cut-off frequencies are at either 17 Hz, 1060 Hz or no filtering. In addition, voltage dividers with a ratio of 1:6 are available, the basic idea is to increase signal level to increase the SNR and later divide to the desired level, while maintaining a better SNR. This approach is feasible if the present noise level is above the thermal noise floor at RT. Following the switchable RC low pass filter and optional voltage divider, a fixed π-filter with 1.5 nF capacitance is in the signal path. A schematic of this switchable filter path inside the breakout box is shown in Fig. 3.9. No value is stated for the inductance of the π-filter by the authors [3].

Furthermore, the signals are not only filtered by the adjustable paths inside the breakbox, but also in the cryostat by additional filters. These filters are placed in a "cold RC filter box" [3] with a resistance of 1 kΩ and capacitance of 10 nF, thus the cut-off frequency is $f_c = 15.9\,kHz$. A second filter capacitor of 10 nF is placed on the PCB containing also the qubit sample.

Placement of a linear regulator (LR) inside the cryostat could help to suppress the noise coming from RT further. By operating the LR in cryogenic temperatures, the presence of thermal noise can be severely reduced. This calls also for a reference voltage generation, which is typically done by a bandgap. The necessity of reference voltages as a key

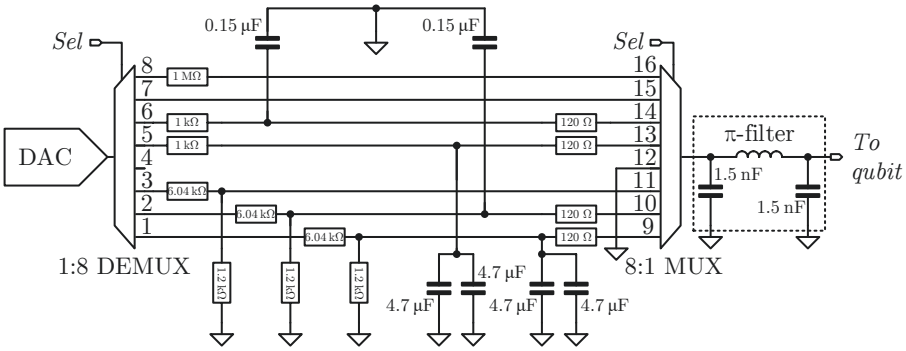


Figure 3.9: Filtering Setup for DC lines in the RT breakbox in the qubit experiment setup at RWTH Aachen University, as shown in [3, Fig. A.1.]

component for achieving high performance data converters and voltage regulators is also supported by van Dijk et. al. [83]. The following chapter 4 will show the design and implementation of a LR in combination with a bandgap for cryogenic temperatures. In order to minimize power dissipation in the lowest temperature chamber of the dilution refrigerator, the LR and bandgap are to be operated on the 4 K stage, also allowing for a higher power budget of ≈1 W. This approach is feasible as the number of required supply and reference voltages driving a classical control electronic IC is mostly fixed and not dependent on the number of qubits, allowing interfacing the LR on the 4 K with the control IC at 100 mK while maintaining scalability. This setup of LR and bandgap with control IC can be visualized by understanding the LR and bandgap as part of the "additional classical electronics" as depicted in Fig. 3.2.

Chapter 4

Bandgap and Linear Regulator

The previous chapter 3 ended with a description of the DC line filters employed in a current experiment setup as used by the research group of Prof. Hendrik Bluhm at RWTH Aachen University. Big effort is undertaken in order to suppress noise entering the fridge and is additionally filtered multiple times inside the fridge [3, 50]. This chapter is focusing on the design and implementation of a linear regulator (LR) including a bandgap reference (BG or short *bandgap*) implementation for reference voltage generation and supply voltage regulation.

A block level overview of the LR and BG is given in Fig. 4.1. The linear regulator converts and regulates an input voltage V_{IN} to an output voltage V_{OUT}. The reference voltage V_{REF} can be supplied via an R-string connected to V_{IN} and can be used as start-up circuitry, or can be generated by the depicted bandgap reference. The feedback voltage V_{FB} for the error amplifier is also generated via an R-string. The bandgap can be supplied either by V_{IN} or V_{OUT} and generates an adjustable reference voltage V_{BG}, which can be routed to the error amplifier and to the output voltage node V_{OUT} for bandgap measurement purposes. The node of V_{OUT} is connected to multiple on-chip capacitors with a total capacitance of 300 pF. The circuit blocks are discussed in the following sections, starting with the bandgap design.

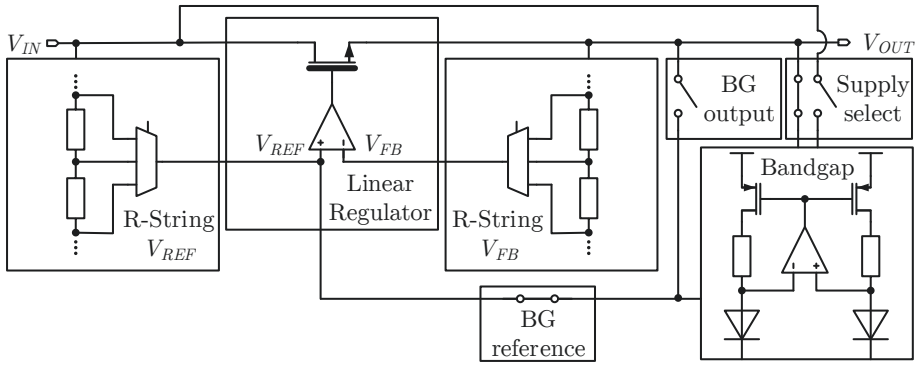


Figure 4.1: Block level overview of LR and bandgap.

4.1 Bandgap

For the topology of the bandgap, the well-known current-mode topology is used [110]. This topology was originally invented in order to operate bandgap references with supply voltages below the bandgap voltage of silicon of around $V_{BG,Si} \approx 1.25\,\mathrm{V}$. The nominal supply voltage for the 65 nm CMOS technology used in this work is $V_{DD,nom} = 1.2\,\mathrm{V}$ and therefore just below the bandgap voltage of silicon. Even if one considers the option to increase the supply voltage to levels above V_{BG_Si}, a topology, which is minimizing the required supply voltage, seems best fitting the application. Additionally, an increased threshold voltage for the diodes $V_{TH,D}$ employed in a bandgap is to be expected at decreasing temperatures, which can be seen looking at the Shockley diode equation [111, p. 12]:

$$I_D = I_S(T)\left(\mathrm{e}^{\frac{V_D}{nV_T}} - 1\right) \tag{4.1}$$

describing the diode current I_D by the temperature dependent reverse leakage current $I_S(T)$, the voltage across the diode V_D, ideality factor n and thermal voltage $V_T = k_B T/q$. Whereas the reduced V_T increases the value of the exponential function, the diode current I_D is still reduced for the same voltage V_D at lower temperatures. This is due to the change in $I_S(T)$

$$I_S(T) = I_S(T_0)\mathrm{e}^{\left(\frac{T}{T_0}-1\right)\frac{V_G(T)}{nV_T}}\left(\frac{T}{T_0}\right)^{\frac{\chi_{T,I}}{n}} \tag{4.2}$$

overcompensating the changes originating from a reduced V_T [111, p. 12]. Here, $V_G(T)$ is the bandgap voltage of silicon and its temperature dependence is typically negligible, T_0 is a reference temperature (usually 300 K) and $\chi_{T,I} \approx 3$. The diode threshold voltage $V_{TH,D}$ is able to increase up to the bandgap voltage of silicon $V_{BG,Si}$ at which point the diode would turn conducting.

This behavior was measured for a diode in the used 65 nm CMOS process technology via dipstick at liquid helium temperature (4.2 K) and is plotted in Fig. 4.2, showing a shifted threshold voltage from RT $V_{TH,D,RT} = \approx 0.55\,\mathrm{V}$ to 4.2 K $V_{TH,D,4.2\,\mathrm{K}} = \approx 1.25\,\mathrm{V}$. Therefore, diode operation is validated by measurement results at deep cryogenic temperatures and can be employed in bandgap designs for reference voltage generation, when taking the increased $V_{TH,D}$ into account. This will require a raised supply voltage, but the effect is minimized by choosing a current-mode topology for the bandgap.

Fig. 4.3 shows the designed current-mode bandgap for cryogenic operation. The start-up circuit can be programmed via the I^2C interface to be either self-starting (M1, M3, M5), which can be deactivated by disabling transistors M2 and M4, or start-up can be forced through M6. The bandgap itself can be disabled by pulling net V_B via the digital controlled M8 to V_{DD}. A common-mode (CM) select MUX allows for configuring the input voltages of the operational amplifier (OpAmp). This was included as previous measurements indicated that a misplaced CM could lead to clipping of the OpAmp output voltages, see 6.20. Two 8-bit binary weighted current mirror banks are implemented in order to generate two configurable reference currents, one of them being converted to a reference

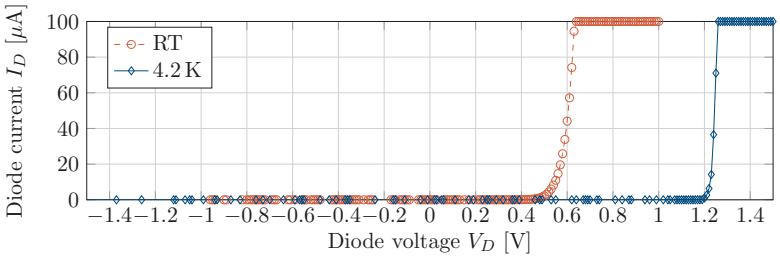


Figure 4.2: Measurement of 65 nm CMOS diode in liquid helium at 4.2 K.

voltage by $R_3 = 2\,\text{k}\Omega$. Both of these can be routed through transmission gates (TGs) TG1 to TG4, either to the pad connected to V_{OUT} or to the LR as reference voltage V_{BG} and bias current $I_{REF,BG}$, respectively. For allowing an LR independent measurement, switches to select either V_{IN} or V_{OUT} are build-in.

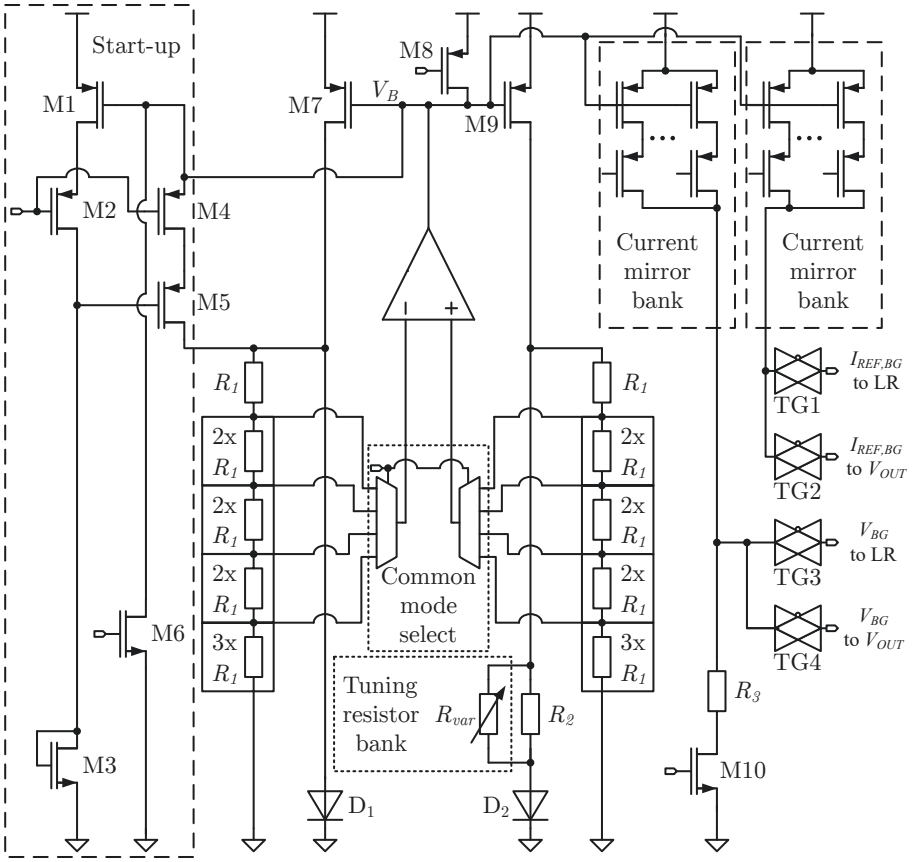


Figure 4.3: Bandgap design.

The adjustable resistor R_{var}, implemented as a digitally controlled resistor bank, can change the temperature behavior of the bandgap. Additionally, the resistor bank can be set to be high ohmic by disabling all transmission gates. This change was simulated and the bandgap output voltage V_{BG} is plotted in Fig. 4.4. The "tilt" towards lower temperatures alongside an overall shift to higher voltages is more pronounced for decreasing resistance values of R_{var}. Bandgap behavior was simulated with extrapolated PDK models for temperatures down to −180 °C, which is significant below the valid temperature range of the PDK of −40 °C to 120 °C and should be taken with increasing caution when moving further to cryogenic temperatures. For simulation temperatures < −180 °C convergence issues for the simulation were arising. Two additional voltage sources were added in series with the diodes D1 and D2 to account for the measured shift in $V_{TH,D}$, see Fig. 4.5a. Simulations showed an operational bandgap for supply voltage $V_{DD} > 1.8\,\text{V}$, see Fig.4.5b. The bandgap output voltage V_{BG} is again plotted for changing R_{var} values. The offset in output voltage V_{BG}, which is induced by V_{DD} increase can be tuned to the original target value of 0.9 V by changing the setting of the current mirror bank, see Fig. 4.3.

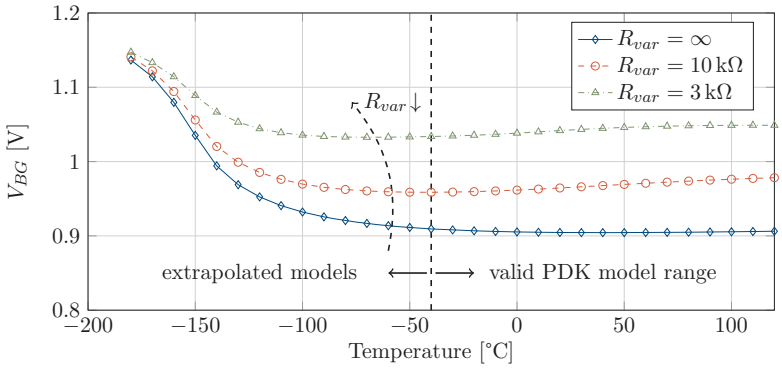
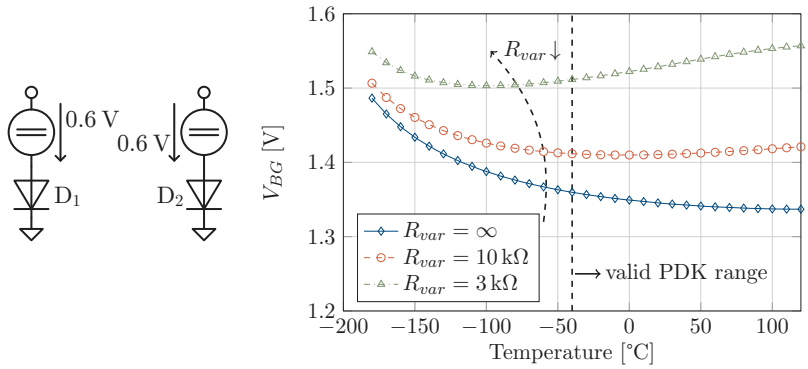


Figure 4.4: Bandgap simulated reference voltage V_{BG} tunable by R_{var}.

The OpAmp topology employed inside the bandgap is a folded-cascode configuration and is shown in Fig. 4.6. A folded-cascode is chosen in order to maximize the input common-mode range, which has been the priority design goal and is supported by the common-mode selection, see Fig. 4.3. Options for biasing are implemented either by self-biasing through resistor R_B, or by feeding the bandgap voltage V_B back into the OpAmp to a current-mirror bank. Transistors M1 and M5 are used for selecting the biasing option, M8 and M11 power off the OpAmp (ref to Fig. 4.6). A PMOS input stage design is chosen, due to the fact that CM selection is able to deliver voltages closer to GND than to V_{DD}. Due to the OpAmp consisting of a single stage, no stability problems are to be expected and simulations showed not instabilities regardless of OpAmp bias conditions.



(a) Added V_{DC} sources.

(b) Bandgap output V_{BG}.

Figure 4.5: Bandgap simulated with additional ideal voltage sources ($V_{DC} = 0.6\,\mathrm{V}$) to model cryogenic $V_{TH,D}$ shift (ref. to Fig. 4.2). Supply voltage increased from 1.2 V to $V_{DD} = 1.8\,\mathrm{V}$.

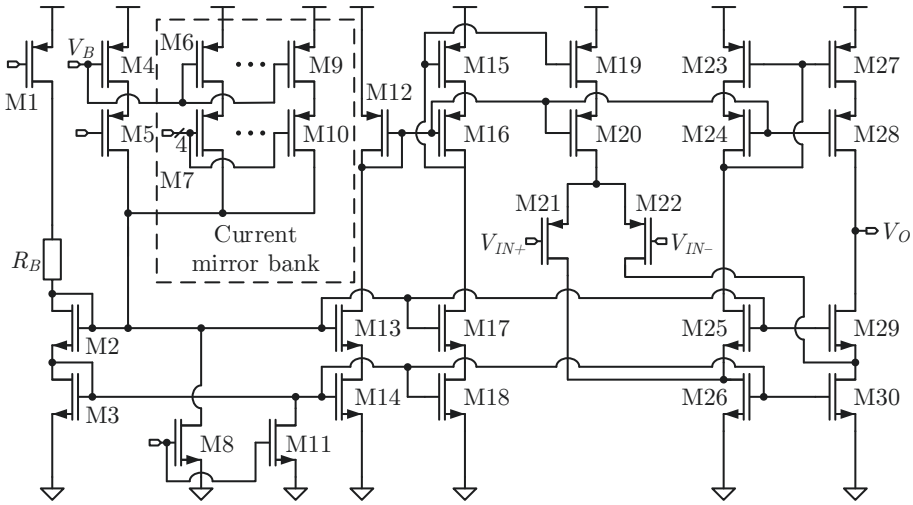


Figure 4.6: Folded cascode OpAmp design.

4.2 Linear Regulator

The LR is designed to convert voltages ranging from 2.2 V to 3.3 V down to core supply voltage level of 1.2 V. The specific levels can be tuned by changing the feedback voltage V_{FB} by the feedback R-string or by shifting the reference voltage V_{REF}, which is generated by either the reference voltage R-string or by the bandgap output, see Fig. 4.1. The typical start-up procedure is to enable both V_{REF} and V_{FB} R-strings first and subsequently power on the LR itself. After V_{OUT} is settled on a voltage level sufficient to supply the bandgap, the bandgap is powered on by either self-starting or by force start (see transistor M6 in Fig.4.3). Afterwards, the settled output voltage of the bandgap is used as a V_{REF} for the LR. This self-supplying setup of the bandgap being supplied by the output of the LR, but in turn also creating the reference for the LR, is proven to reliably work in [112].

The R-string design for the generation of the start-up reference voltage, which is connected to V_{REF}, and the R-string for the feedback voltage V_{FB} are shown in Fig. 4.7. Both of them being built by p-doped polysilicion unit resistors of $R = 7.2\,\text{k}\Omega$, which are reported to be stable for a wide temperature range and down to deep cryogenic temperatures, see section 2.4.2. Fig. 4.7 shows the usage of IO MOSFETs for M1 and M2 in the so-called "overdrive" modeling flavor suitable for operation with up to 3.3 V (regular IO voltage is 2.5 V), which are used for all designs supplied by the higher V_{IN} voltage. Due to the feedback R-string being connected with the lower V_{OUT} voltage, the usage of regular core devices is feasible for the transistor M3. Both R-Strings employ an 8 to 1 MUX for voltage level selection and allow for later tuning while in operation. One additional distinction of both R-string designs is the number of unit resistances R as well as the selectable voltage division levels, which enables the selection of voltages fitting for good error amplifier operation. The possible voltage tuning range for both R-strings is given in Table 4.1 depending on the available supply voltage. The error amplifier is designed with a nominal CM input level of 0.9 V and further discussed in the following paragraph. Therefore, it is possible to set a V_{REF} and V_{FB} of ≈0.9 V for all supply voltage combinations in order to assure operation even if the bandgap requires a supply voltage of $2.1\,\text{V} = 1.8\,\text{V} + 300\,\text{mV}$ beyond the simulated supply level of 1.8 V.

		V_{REF}		V_{FB}		
V_{DD}	[V]	2.2	3.3	1.2	1.8	2.1
V_{MAX}	[V]	1.51	2.27	1.2	1.8	2.1
V_{MIN}	[V]	0.55	0.83	0.5	0.75	0.88

Table 4.1: LR R-strings voltage tuning ranges.

The LR is consisting of an error amplifier including a biasing block for the amplifier, an NMOS pass transistor M1 and a transistor M2 in order to turn off the LR output by pulling the gate voltage of M1 to GND. An NMOS pass transistor is chosen to achieve better stability than by usage of a PMOS in a low-dropout regulator topology. This increases the required voltage drop over M1 and limits the achievable power efficiency. But due to the absence of reliable device models for cryogenic temperatures, a design aiming at robustness and stability appears more advantageous. The bias circuitry has

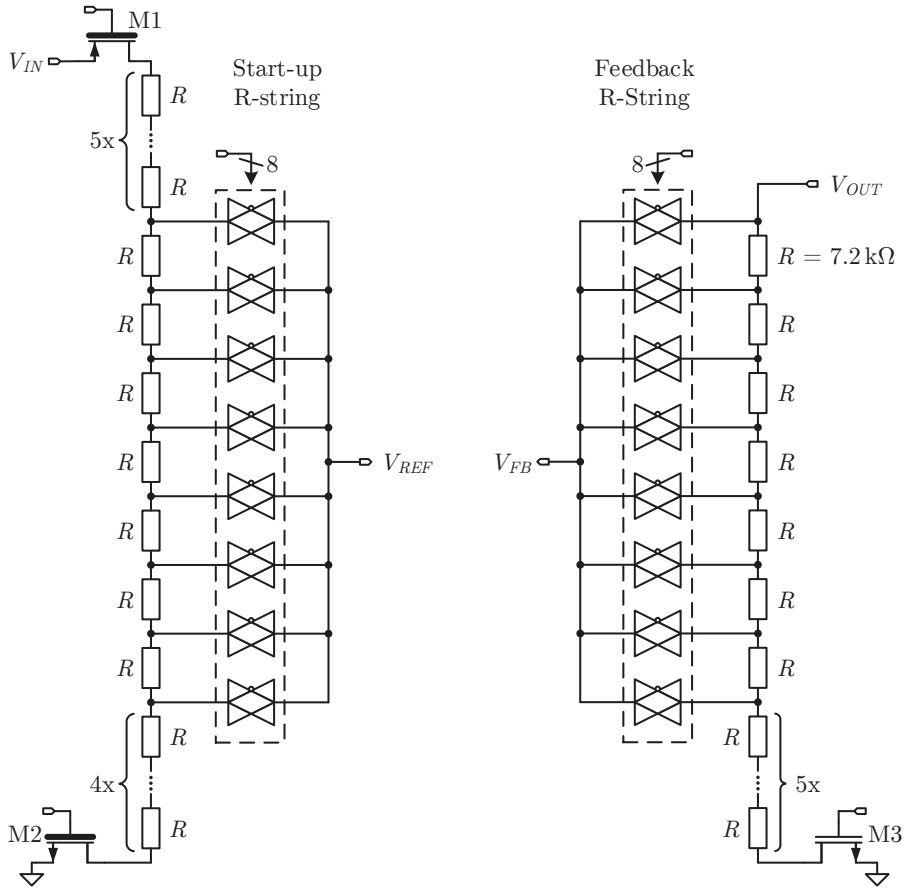


Figure 4.7: Start-up reference voltage R-String and feedback R-string design.

the option to generate the error amplifier bias current internally, as shown in Fig.4.10, or use a reference current from the bandgap $I_{REF,BG}$.

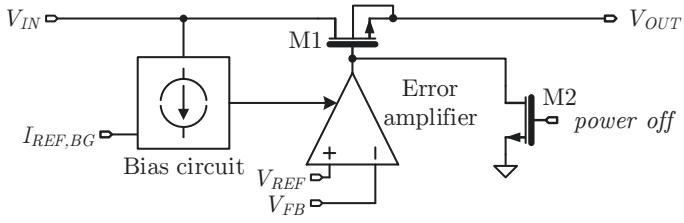


Figure 4.8: Linear regulator design.

The error amplifier is a 2-stage Miller-OpAmp and it is shown in Fig. 4.9. A wide swing current mirror (M1,M2) is used to increase output resistance and accurately mirror the either internally generated or bandgap generated reference bias current into the differential amplifier, while maintaining a maximum voltage headroom for operation of transistors M3 to M6. A current mirror load is used for the first stage for an improved amplification factor. The second stage consists of a Miller-compensated source amplifier M8 with active load M7, which is implemented as single transistor current mirror in order to maximize output voltage swing. Values for the Miller-compensation are $C_M = 800\,\text{fF}$ and $R_z = 6.4\,\text{k}\Omega$ yielding to a simulated minimum phase margin (PM) of about 40° when supplied with the internal biasing option. PM can be increased by adjusting the bias current, if cryogenic effects and temperatures require this. However, this is degrading the overall performance of the amplifier. The error amplifier simulated open loop DC gain is $A_{DC} = 70.83\,\text{dB}$ and the unity gain bandwidth (UGB) is 502 MHz. The UGB is simulated with the amplifier connected in unity gain configuration and is defined as the frequency at which the amplifier gain is reduced by −3 dB.

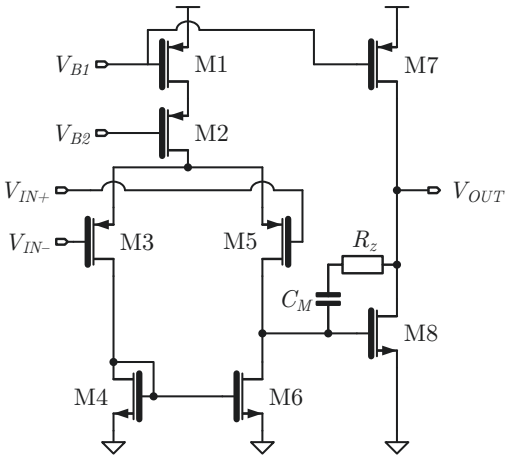


Figure 4.9: LR error amplifier design.

The error amplifier can be supplied in two ways, which are shown in Fig. 4.10. First, the biasing is provided internally which is susceptible to all process, voltage and temperature

(PVT) variations. Second, a 8-bit tunable reference current $I_{REF,BG}$ generated by the bandgap reference, see previous section 4.1, can be used to bias the error amplifier. Transistors M6 to M12 build up the wide swing current mirror generating the biasing voltages V_{B1} and V_{B2} for the error amplifier, see Fig. 4.9. The design pays attention to be fully controllable in terms of source selection and reliable in powering on and off certain parts of the biasing network without effecting other parts.

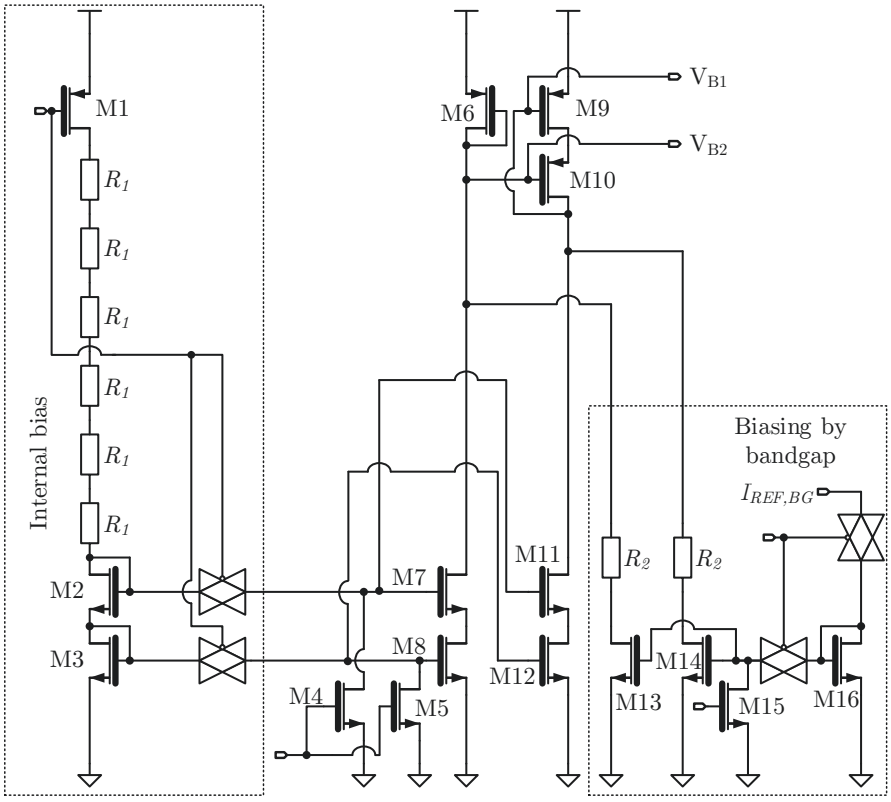


Figure 4.10: LR error amplifier biasing network.

Fig. 4.11 shows the simulated transient behavior of the whole system of LR and bandgap (ref. to Fig. 4.1) including start-up and rapid load changes, testing the stability. The bandgap is configured as described previously in section 4.1 with $R_{var} = 3\,\text{k}\Omega$ and additional ideal voltage sources of 0.6 V (ref. to Fig. 4.5a) to account for expected diode threshold shifts at cryogenic temperatures (ref. to Fig. 4.2). The LR output voltage is stabilized by an on-chip capacitor array with a total capacitance of 303 pF and an additional off-chip capacitor of 1 µF. The complete start-up behavior is simulated by setting a V_{REF} via the reference voltage R-string (ref to Fig. 4.7) to generate an initial output voltage fitting to start the internal bandgap reference. The point in time when switching to the bandgap generated reference voltage is marked in Fig. 4.11. V_{OUT} can always be adjusted by two degrees of freedom. The reference voltage V_{REF} can be tuned in the R-string and in the bandgap reference. Additionally, the feedback R-string can

be set to a different level, which is shifting the feedback voltage V_{FB}. This enables V_{OUT} to be set to similar levels in the start-up and operational phase. A zoom-in on the LR output V_{OUT} is given in Fig. 4.12 in order to make the effect of load variations visible. Voltage spikes are in the order 200 µV, but V_{OUT} is directly regulated back towards the nominal output voltage level.

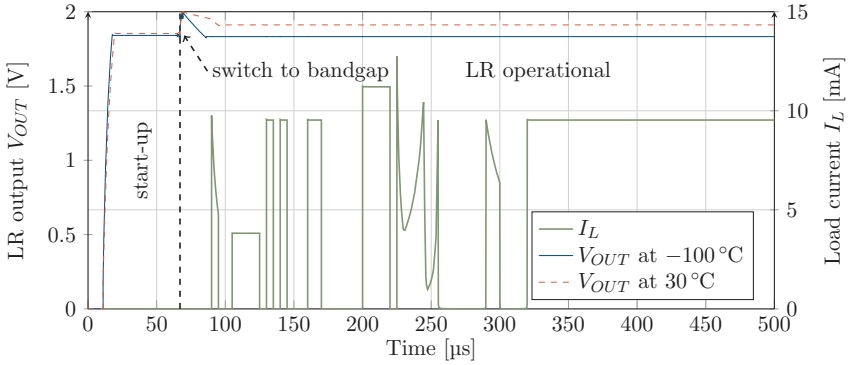


Figure 4.11: LR simulated with start-up and switch to internal bandgap supplying V_{REF} and $I_{REF,BG}$. Output voltage V_{OUT} is stable when simulating rapid varying load currents I_L.

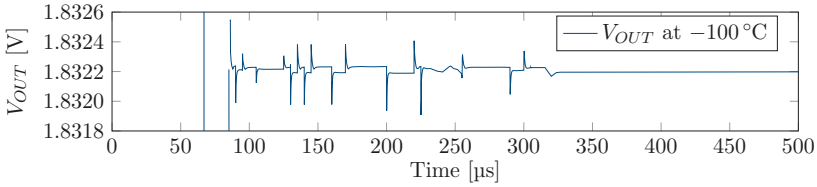


Figure 4.12: Zoom-in on simulated output voltage V_{OUT}.

The simulated power supply rejection-ratio (PSRR) is plotted in Fig. 4.13. The RT curve makes the BW of the LR apparent, which manages to regulate up to around 60 kHz and the output capacitor filtering frequencies >1 MHz. A degradation from −78 dB at RT to −60 dB at −100 °C for the LR regulator is shown. However, 60 dB would still be a satisfying result for a first prototype considering the absence of any valid models below −40 °C. Furthermore, one focus of the LR design is to enable tuning and being configurable by e.g. biasing, voltage levels, CM level, etc. This may be one option to enhance the PSRR further, if this is required. A benefit of lower operation temperatures is the increased regulation bandwidth of about 200 kHz to 300 kHz. Therefore, the reduced PSRR from −80 dB to −60 dB can be explained by the increase in bandwidth, which are both changing by a factor of 10. This behavior is typical for the design of every amplifier or regulator as a trade-off in bandwidth and gain.

This promising simulation results indicate a reasonable confidence to show operational behavior for a bandgap and LR design in the deep cryogenic temperatures of 4 K and overall challenging environment inside a dilution refrigerator. Measurement results are

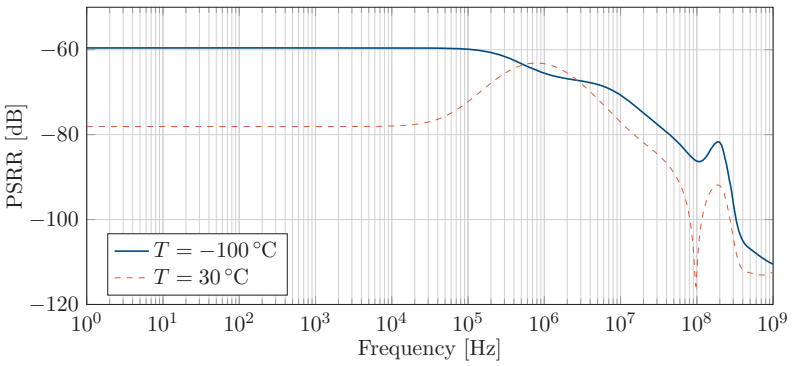


Figure 4.13: PSRR of LR simulated with operating point at the end of transient analysis, shown in Fig. 4.11.

shown and discussed in chapter 6 with bandgap results in section 6.2 and the LR in section 6.3.

Chapter 5

Bias-DAC

The Bias-DAC is designed to generate independent voltages for forming quantum dots required by solid-state spin-based qubits. System level considerations about noise and power have been discussed in chapter 3. The requirements for the Bias-DAC are summarized in Table 3.1. Furthermore, some Bias-DAC system level considerations with respect to scaling opportunities are presented in previous section 3.2.

5.1 Topology

In order to choose the DAC topology best fitting for the application and specific environmental challenges arising from placement inside a dilution refrigerator at the lowest temperature stage in close vicinity to the qubits, a comparison of DAC topologies including a discussion of pros and cons is given in this section. The following possible topologies are taken into consideration:

- Current steering DAC
- R-string DAC
- R-2R ladder DAC
- Pulse width modulation (PWM) DAC
- ΣΔ DAC
- Charge-redistribution DAC

Starting with the current steering DAC, which is mainly used for high-speed applications, multiple downsides for usage as a Bias-DAC are apparent. A constant current flow is required in order to generate an output voltage. The reported increase in transistor mismatch at cryogenic temperatures [80] renders the usage of current mirrors challenging and may require additional calibration structures, which can compensate this increased mismatch. Therefore, a current steering DAC does not appear to be natural choice for an ultra-low power 12 bit DAC without the need for a high sampling rate. However, one fitting use case could be in generating control pulses for GaAs qubits, which typically require a DAC with a 250 MS/s sample rate and ±4 mV dynamic range [101].

One major selling point of the R-string DAC is the guaranteed monotonicity of the generated output voltage, which is not mandatory required in this application but desirable.

However, this comes at the cost of a non-negligible disadvantage, i.e. an exponential increase in unit resistances and switches. Therefore, an R-string DAC with 12 bit resolution would require $2^{12} = 4096$ resistances and switches. While this may be a feasible approach for a single qubit, it is in doubt if a complex circuit with a topology that requires this large number of elements is the right choice to bias thousand or more qubits. A DAC relying on binary weighting and therefore a linear scaling with the number of bits is therefore favored for this application.

The R-2R ladder structure is a binary weighted DAC topology and therefore better scalable than the previously described R-string. This topology is relying on a voltage divider approach to generate a desired output voltage, like the R-String and the later discussed charge-redistribution DAC. The important differentiation compared to the charge-redistribution is that the R-2R ladder relies on a resistive voltage divider and as a result needs a constant current flow. This static current would create issues with the later in section 5.3 described DAC segmentation or coarse tuning as the amount of current flow is depending on the DAC input word. A changing current would lead to a varying voltage drop across the coarse tuning MUX and deteriorate the DAC output by simulated amounts of up to 2 mV to 3 mV, which is not in accordance to the specified 250 µV step size, see Table 3.1.

PWM and ΣΔ DACs can be considered jointly. Both share a digital output, which is either V_{DD} or GND. This results in the necessity of an analog low pass filter. The presence of such a filter is already reasoned in section 3.4 and Fig. 3.6 to minimize the impact of a required voltage level refresh in order to compensate for leakage currents. However, if one considers the required damping of the filter at the operation frequency of the PWM or ΣΔ DAC to reduce the full-swing output down to the required level of ≈20 µV, the required resistance or capacitance values are unreasonable for implementation in an IC. The output signal would need to be reduced by $20 \log\left(\frac{20\,\mu\text{V}}{1.2\,\text{V}}\right) = -95.6\,\text{dB}$. Another option to avoid unrealistic device values for resistances and capacitances in the output filter would be to increase the clock frequency of the DAC, which tampers the need for ultra-low power consumption. In case of a multi-level ΣΔ this problem can be relaxed, but not solved. Moreover, the very high precision of a ΣΔ, usually the topology of choice for >20 bit DACs, is not required in this application. Thus, the PWM and ΣΔ DAC topology are not as fitting as the following proposed charge-redistribution topology.

Charge-redistribution DACs are utilizing binary weighted capacitive voltage dividers to generate the desired output voltage. Multiple implementation forms are known today and the most common ones are either the conventional binary weighted charge-redistribution or the binary weighted with attenuation capacitor C_A, shown in Fig. 5.1 and Fig. 5.2, respectively [113, pp. 978–981].

One drawback of the conventional charge-redistribution DAC is the need for an exponential capacitance increase per bit, whether it be implemented by more unit capacitors in parallel or by a single capacitor with increased size, e.g. for K bit the MSB capacitor is sized $2^{K-1}C_0$. This problem can be avoided by a split array design, implementing the previous named attenuation capacitor C_A. Making the split array charge-redistribution DAC a popular choice due to its “simplicity and relatively good accuracy” [113, p. 980]. The split array is typically distributed evenly between the MSB and LSB side with $N = M = K/2$

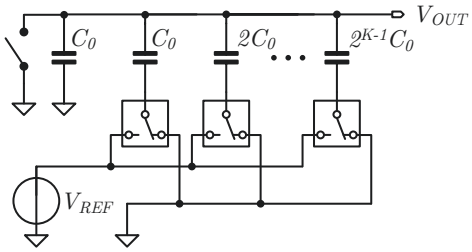


Figure 5.1: Conventional charge-redistribution DAC.

and $C_A = \frac{2^N}{2^M - 1}$, but also other distributions are possible. In this work an even weighted split-array design is implemented.

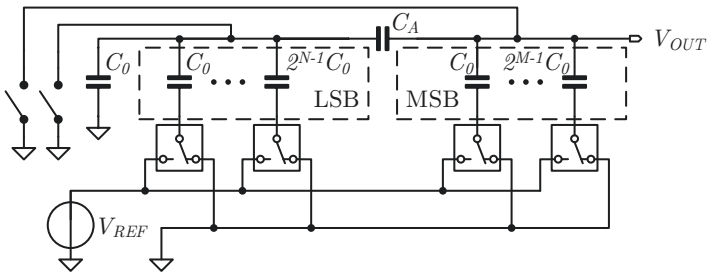


Figure 5.2: Charge-redistribution DAC with attenuation capacitor C_A.

One major advantage of capacitor based DACs for this application case is a zero quiescent current, which aids in designing for minimum power consumption. Additionally, in most technologies device mismatch and tolerances are greater for resistances than for capacitors [114]. This makes charge-redistribution an often-used DAC topology choice for implementation in CMOS technologies [113, 114]. Moreover, metal capacitors are reported with good temperature stability, i.e. <10 % change from RT to 4 K [77, 78, 83]. An additional benefit in implementing a capacitor-based DAC is the option to place active devices, such as transistors, diodes and resistors, below the capacitors and thus saving die area. This is possible due to the linear capacitors in CMOS technologies typically being fabricated in upper metal layers and may even include an shielding layer to block influence of the underneath circuitry. This enables an even denser design than any other DAC topology, because all metal layers can be utilized. A further advantage is the bandwidth independent Johnson–Nyquist noise of $\overline{v}_n^2 = \frac{k_B T}{C}$, which scales linearly with temperature.

Other possible capacitor-based topologies like the cyclic [115] or pipelined [116] DAC, which require either oversampling or higher digital effort and might suffer from charge injection due to more switching operations. This type of DACs could be considered for implementation in future chip designs. However, this work uses the split-array DAC for a first chip implementation due to its previous described advantages, robustness and being well established in CMOS designs. In the following part of this work, the split

array charge-redistribution DAC will be referred to as just charge-redistribution DAC or Bias-DAC.

5.2 Iterative Charging

As the operation of qubits with scalable local cryogenic ICs is demanding in terms of ultra-low power, noise and area requirements, proposal is to omit the typically present output buffer embedded in a charge-redistribution DAC design. In most use cases, a DAC is expected to drive a significant load. This requires the integration of a buffer in order to be able to drive the load and ensure an unloaded capacitive voltage divider of the DAC. However, as the qubit electrodes represent just a capacitive load of ≈100 fF and a nyquist rate conversion is not required for the quantum dot defining bias voltages, thus the buffer can be omitted in order to minimize noise, power and area consumption. The consequence is an iterative capacitive charging behavior (ref. to Fig. 5.6) present for the output voltage on storage capacitors C_S (ref. to Fig. 3.6), which hold the current voltage level to bias the qubit.

An equation to describe and model the charging behavior can be derived by redrawing the split array charge-redistribution DAC (of Fig. 5.2) in Fig. 5.3. This combines the individual capacitors depending on the digital DAC input words divided into LSBs $Z_L \in [0, 2^N-1]$ and MSBs $Z_M \in [0, 2^N-1]$ for an equal split array with both sides converting N bit of a total DAC bit word of $2N$ bit. The total capacitance connected to V_{REF} is therefore described by $Z_L \cdot C_0$ and $Z_M \cdot C_0$ and the remaining other capacitors are connected to GND by $\left(2^N - Z_L\right) C_0$ and $\left(2^N - 1 - Z_M\right) C_0$. The LSB side is increased by one unit capacitor C_0 due to the always grounded capacitor, see Fig. 5.2. The attenuation capacitor is $C_A = \frac{2^N}{2^N-1} C_0$.

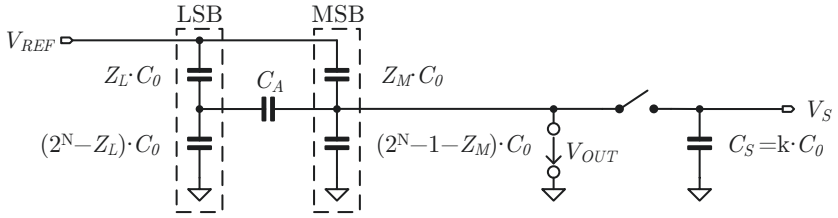


Figure 5.3: Charge-redistribution DAC redrawn to derive equation for iterative charging behavior.

The MSB and LSB side are considered separately for calculation of the voltage drop induced by the storage capacitor $C_S = k \cdot C_0$. The total voltage drop can be derived by superposition of the result for the MSB and LSB side $V_{Drop} = V_{D,L} + V_{D,M}$. This voltage drop should be reduced with each iteration step as the storage capacitor C_S is now pre-charged by the previous step. Therefore, the conversion step m is added to the index $V_{Drop,m} = V_{D,L,m} + V_{D,M,m}$.

Starting with the $V_{D,M,m}$ derivation for the MSBs side, we can set all LSB capacitors to GND as we want to superimpose both sides later. This leads to a setup as shown in Fig. 5.4.

The series of $C_A = \frac{2^N}{2^N-1}C_0$ and $2^N C_0$ can be substituted by a total capacitance of one unit capacitor $1 \cdot C_0$. Thus leaving the typical setup of a non-split charge redistribution DAC due to the addition of one C_0 to GND, depicted on the right side of Fig. 5.4.

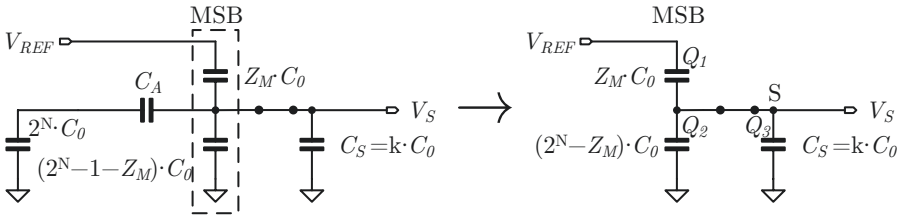


Figure 5.4: Charge-redistribution DAC schematic for MSBs part.

Considering that the storage capacitor $C_S = kC_0$ is holding a charge $Q_{m-1} = V_{S,m-1}kC_0$ from previous DAC conversion steps and all other capacitors are reset prior to every conversion step, the charge balance for the node S is:

$$Q_{m-1} = Q_2 + Q_3 - Q_1 \tag{5.1}$$

$$\begin{aligned} \Leftrightarrow kV_{S,m-1}\cancel{C_0} &= (2^N - Z_M)V_S\cancel{C_0} + kV_S\cancel{C_0} - Z_M(V_{REF} - V_S)\cancel{C_0} \\ &= (2^N + k)V_S - Z_M V_{REF} \end{aligned} \tag{5.2}$$

Next, the voltage V_S is rewritten as the difference of the desired ideal DAC output voltage $V_{N,M}$ as created by the MSBs alone and the voltage drop $V_{D,M,m}$ induced by the loaded capacitive votlage divider inside the DAC by the storage capacitor C_S. Substituting $V_S = V_{N,M} - V_{D,M,m}$ and for the previous conversion step that stored the charge Q_{m-1} it is substituted $V_{S,m-1} = V_{N,M} - V_{D,M,m-1}$ into (5.2):

$$k(V_{N,M} - V_{D,M,m-1}) = (2^N + k)(V_{N,M} - V_{D,M,m}) - Z_M V_{REF} \tag{5.3}$$

Solving (5.3) for the voltage drop of the current conversion step $V_{D,M,m}$ gives:

$$V_{D,M,m} = V_{N,M} - \frac{(V_{N,M} - V_{D,M,m-1})k + Z_M V_{REF}}{2^N + k} \tag{5.4}$$

Now the ideal MSB output voltage $V_{N,M}$ is depending on the input word Z_M, the bit count N and the reference voltage V_{REF} by $V_{N,M} = \frac{Z_M}{2^N} V_{REF}$.

$$\begin{aligned} V_{D,M,m} &= \frac{Z_M}{2^N} V_{REF} - \frac{(\frac{Z_M}{2^N} V_{REF} - V_{D,M,m-1})k + Z_M V_{REF}}{2^N + k} \\ &= \frac{Z_M}{2^N} V_{REF} \left[1 - \frac{k - \frac{V_{D,M,m-1} 2^N k}{Z_M V_{REF} + 2^N}}{2^N + k} \right] \\ &= \frac{Z_M}{2^N} V_{REF} \left[\cancel{1} - \frac{2^N + \cancel{k}}{\cancel{2^N} + k} + \frac{\frac{V_{D,M,m-1} 2^N k}{Z_M V_{REF}}}{2^N + k} \right] \\ &= \frac{Z_M}{\cancel{2^N}} \cancel{V_{REF}} \frac{\frac{V_{D,M,m-1} \cancel{2^N} k}{\cancel{Z_M} \cancel{V_{REF}}}}{2^N + k} \\ &= \frac{V_{D,M,m-1} k}{2^N + k} = V_{D,M,m-1} \frac{k}{2^N + k} \end{aligned} \tag{5.5}$$

The voltage drop for conversion step m can now be recursively calculated starting from an uncharged capacitor C_S with zero stored charge $Q_{m-1} = Q_0$ in the first DAC conversion step. $Q_0 = 0\,\mathrm{C}$ demands for a voltage $V_{S,m-1}$ and thus $V_{D,M,m-1} = V_{N,M}$ as initial condition. The voltage drop is following a logarithmic behavior, as each iteration step multiplies $V_{D,M,m-1}$ with a constant factor $\frac{k}{2^N+k}$, see (5.5).

Following the same approach, a formula for the voltage drop for the LSB side $V_{D,L,m}$ can be derived. Fig. 5.5 shows the setup for the LSB case and with the same reasoning as before we put all MSB capacitors to GND in order to calculate each side independently and superimpose the resulting voltages.

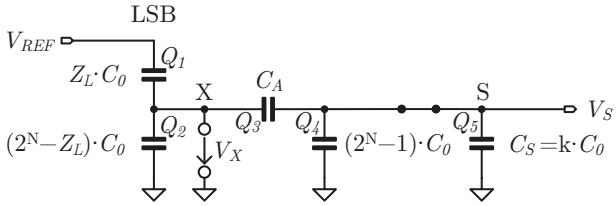


Figure 5.5: Charge-redistribution DAC schematic for LSBs part.

Again, a charge balance approach is taken, starting with node X. Because all capacitors except C_S are reset prior to each conversion iteration, the total charge sum for X is required to be zero:

$$0 = Q_2 + Q_3 - Q_1 \tag{5.6}$$

The total charge sum for node S is again the stored charge of the previous conversion step Q_{m-1}.

$$Q_{m-1} = Q_4 + Q_5 - Q_3 \tag{5.7}$$

Combining (5.6) and (5.7), it is:

$$Q_{m-1} = Q_4 + Q_5 - Q_2 + Q_1 \tag{5.8}$$

The previously stored charge Q_{m-1} is again defined by $Q_{m-1} = V_{S,m-1}kC_0$. After substitution of each charge definition by voltage and capacitor, the relation is:

$$\begin{aligned} kV_{S,m-1}\cancel{C_0} &= (2^N - 1)V_S\cancel{C_0} + kV_S\cancel{C_0} - (2^N - Z_L)V_X\cancel{C_0} + Z_L(V_{REF} - V_X)\cancel{C_0} \\ \Leftrightarrow kV_{S,m-1} &= 2^N V_X + (2^N - 1 + k)V_S - Z_L V_{REF} \end{aligned} \tag{5.9}$$

In order to substitute V_X the charge Q_3 is defined as follows and solving for V_X taking $Q_3 = Q_1 - Q_2$ into account, see (5.6), yields to:

$$Q_3 = \frac{2^N}{2^N - 1}(V_X - V_S)C_0 \tag{5.10}$$

$$\Leftrightarrow Q_1 - Q_2 = \frac{2^N}{2^N - 1}(V_X - V_S)C_0$$

$$\Leftrightarrow Z_L(V_{REF} - V_X)\cancel{C_0} - (2^N - Z_L)V_X\cancel{C_0} = \frac{2^N}{2^N - 1}(V_X - V_S)\cancel{C_0}$$

$$\Leftrightarrow V_X = \frac{2^N - 1}{2^{2N}}Z_L V_{REF} + \frac{V_S}{2^N} \tag{5.11}$$

Using (5.11) we can rewrite (5.9) to:

$$\begin{aligned} kV_{S,m-1} &= 2^N\left[\frac{2^N - 1}{2^{2N}}Z_L V_{REF} + \frac{V_S}{2^N}\right] + (2^N - 1 + k)V_S - Z_L V_{REF} \\ &= -\frac{Z_L}{2^N}V_{REF} + (2^N + k)V_S \end{aligned} \tag{5.12}$$

Then, V_S and $V_{S,m-1}$ are again substituted by the difference of ideal output voltage $V_{N,L}$ and the voltage drop created by the loaded capacitive divider inside the DAC $V_{D,L,m}$. Thus, $V_S = V_{N,L} - V_{D,L,m}$ and $V_{S,m-1} = V_{N,L} - V_{D,L,m-1}$. Solving the resulting equation for $V_{D,L,m}$, yields to:

$$k(V_{N,L} - V_{D,L,m-1}) = -\frac{Z_L}{2^N}V_{REF} + (2^N + k)(V_{N,L} - V_{D,L,m}) \tag{5.13}$$

$$\Leftrightarrow V_{D,L,m} = \frac{-\frac{Z_L}{2^N}V_{REF} - kV_{N,L} + kV_{D,L,m-1}}{2^N + k} + V_{N,L} \tag{5.14}$$

The unloaded output voltage for the LSB side is $V_{N,L} = \frac{Z_L}{2^{2N}} V_{REF}$.

$$\begin{aligned} V_{D,L,m} &= \frac{-\frac{Z_L}{2^N} V_{REF} - k\frac{Z_L}{2^{2N}} V_{REF} + k V_{D,L,m-1}}{2^N + k} + \frac{Z_L}{2^{2N}} V_{REF} \\ &= \frac{-\frac{Z_L}{2^N} V_{REF} - k\frac{Z_L}{2^{2N}} V_{REF} + k V_{D,L,m-1} + \left(\frac{Z_L}{2^{2N}} V_{REF}\right)(2^N + k)}{2^N + k} \\ &= \frac{\cancel{-\frac{Z_L}{2^N} V_{REF}} - \cancel{k\frac{Z_L}{2^{2N}} V_{REF}} + k V_{D,L,m-1} + \cancel{\frac{Z_L}{2^N} V_{REF}} + \cancel{k\frac{Z_L}{2^{2N}} V_{REF}}}{2^N + k} \\ &= V_{D,L,m-1} \frac{k}{2^N + k} \end{aligned} \tag{5.15}$$

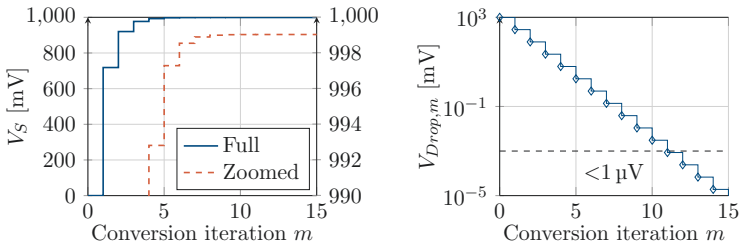
Comparing the MSB side voltage drop $V_{D,M,m}$ (5.5) and LSB side $V_{D,L,m}$ (5.15), each conversion iteration multiplies both with the same factor $\frac{k}{2^N+k}$. The total voltage drop $V_{Drop,m}$ for the loaded equal split-array charge-redistribution DAC in the conversion iteration $m \in \mathbb{N}^+$ is:

$$V_{Drop,m} = V_{D,M,m} + V_{D,L,m} = \left[V_{D,M,m-1} + V_{D,L,m-1}\right] \frac{k}{2^N + k} \tag{5.16}$$

with $V_{D,M,0} = V_{N,M} = \frac{Z_M}{2^N} V_{REF}$ and $V_{D,L,0} = V_{N,L} = \frac{Z_L}{2^{2N}} V_{REF}$. $V_{Drop,m}$ can also be calculated by substitution of the recursive $V_{D,M,m-1}$ and $V_{D,L,m-1}$, leading to:

$$V_{Drop,m} = \left[V_{D,M,0} + V_{D,L,0}\right] \prod_{i=1}^{m} \frac{k}{2^N + k} = \left[Z_M + \frac{Z_L}{2^N}\right] \frac{V_{REF}}{2^N} \left(\frac{k}{2^N + k}\right)^m \tag{5.17}$$

Using (5.17) the S&H voltage V_S and the corresponding $V_{Drop,m}$ were calculated for $N = 5$, $Z_M = Z_L = 2^5 - 1 = 31$, $k = 12.5$ and $V_{REF} = 1\,\mathrm{V}$ and are plotted in Fig. 5.6. The ideal output voltage of the DAC is for this case $V_N = \left[Z_M + \frac{Z_L}{2^N}\right] \frac{V_{REF}}{2^N} = \left[31 + \frac{31}{2^5}\right] \frac{1\,\mathrm{V}}{2^5} = 999.023\,\mathrm{mV}$ and is asymptotically approached with each conversion iteration m. These values are the worst case in terms of absolute voltage drop. Still, calculations show a sufficient small output voltage drop $V_{Drop,m} < 1\,\mu\mathrm{V}$ is reached after 11 conversion iterations, albeit saving the typical present output buffer of the DAC.



(a) Iterative charging of V_S.

(b) Voltage drop $V_{Drop,m}$.

Figure 5.6: Calculated effect of loading the charge-redistribution DAC with an S&H capacitor C_S.

5.3 Reference Voltage Coarse Tuning

Considering the possible bit resolution for a charge-redistribution DAC is reported in literature as 10 bit to 12 bit [113, p. 980] and no valid models for cryogenic temperatures exist, a conservative approach seems advisable. Therefore, the Bias-DAC is designed with a 10 bit resolution. In order to be able to meet the specified 12 bit resolution (ref. to Table 3.1) a segmented DAC approach can be taken. This is typically achieved by cascading two DACs with the second operating on the output voltage of the first one [117]. Instead of adding an additional DAC to the design, multiple reference voltages are fed into the chip from external sources. This minimizes area, noise and power consumption inside the constricted lowest temperature stage of the dilution refrigerator. The reference voltage sources can be placed at higher temperature stages, or even at RT.

The application requires a step size of 250 µV($\approx$ 12 bit) with an output voltage range of 1 V (see Table 3.1). Thus, additional 2 bit in resolution is required and therefore 2^2 coarse tuning voltages suffice. Later, the effect of parasitic capacitance is discussed and it is shown that for certain regions a loss of 1 bit accuracy is present. Therefore, the number of external reference voltages is increased from 2^2 to 2^3, which appears still reasonable with $2^3 = 8$ pads being required to operate the Bias-DAC. Those reference voltages are only fed into the chip once and are distributed to multiple Bias-DACs for later scaling the number of qubits. This can be combined with the scaling approach to generate digital timing and control signals centralized and route them to every DAC (ref. to section 3.5 and Fig. 3.8). Thus, a mere minimum of local memory of a few bytes, which is described in more detail in the following section 5.4, and the analog charge-redistribution core are required for each DAC, which in turn can supply multiple output channels, as depicted in Fig. 3.7.

Fig. 5.7 schematically shows such a setup schematically, the reference voltages are equally spaced at a step size of 125 mV from 0 V to 1 V, or when operating the DAC with the specified output voltage range from −1 V to 0 V. However, as this will require the GND potential of the chip to be shifted to −1 V. It is equivalent to consider the reference voltages to be set as shown in Fig. 5.7. With 3 bit for $V_{REF,U} \in [125\,\text{mV}, 1\,\text{V}]$ and $V_{REF,L} \in [0\,\text{V}, 875\,\text{mV}]$ each, it is possible to independently select the level for both reference voltages. This reference voltage coarse tuning allows selecting the operation range of the following DAC and is reducing the power consumption, because the capacitors are now charged with a reduced voltage swing. Coarse tuning the reference voltages results in a reduction from 1 V to 0.125 V charging the internal DAC capacitors and thus the dynamic power consumption of charging and uncharging the capacitors $P \propto V^2 \cdot f \cdot C$ is reduced to $\left(\frac{1\,\text{V}}{0.125\,\text{V}}\right)^2 = \frac{1}{64} = 1.5625\,\%$.

In the following, the reference voltage coarse tuning is considered part of the overall DAC input word Z_{IN} composed of the 6 bit for the reference voltage coarse tuning $V_{REF,U}$ and $V_{REF,L}$ and the 10 bit of the charge-redistribution inputs Z_M and Z_L, as shown in Fig. 5.8. However, in most cases the bits for $V_{REF,U}$ and $V_{REF,L}$ are set to the same level, which selects voltages so that the charge redistribution DAC is operated with a reference voltage swing of 125 mV. One exception to this mode of operation is to generate intermediate steps, which is discussed later in this section. Selection of unequal bit settings for $Z_{IN}[15:13]$ and $Z_{IN}[12:10]$ results in the charge-redistribution DAC being operated

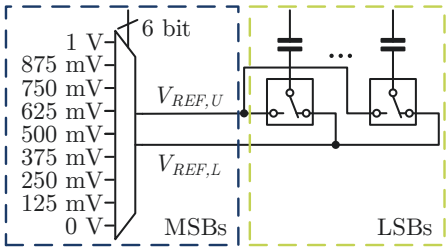


Figure 5.7: Coarse tuning upper $V_{REF,U}$ and lower $V_{REF,L}$ reference voltages of the Bias-DAC.

with voltages ranging from 250 mV up to 1 V. The step size of the Bias-DAC output voltage V_S is increasing corresponding to this higher reference voltage swing.

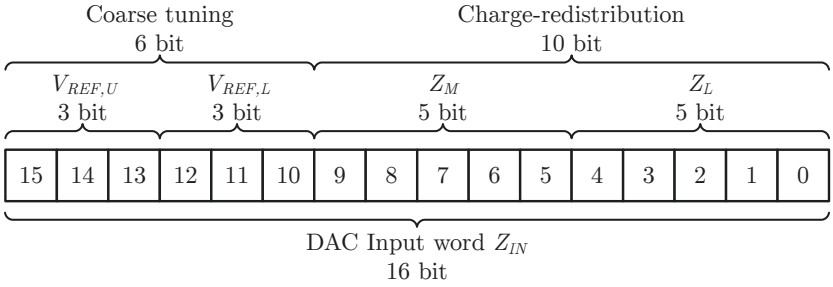


Figure 5.8: DAC input word Z_{IN} composition.

One drawback of implementing a coarse tuning is missing codes due to a nonideal DAC gain caused by parasitic capacitance in the charge-redistribution DAC itself. This effect is shown in Fig. 5.9. Every parasitic capacitance C_{P3} after the S&H switch can be viewed as merely increasing the storage capacitance C_S and will only affect the number of conversion cycles required to reach the desired output voltage, see previous section 5.2. The gain error caused by C_{P1} and C_{P2} leads to a voltage jump V_{jump} in the DAC output curve when crossing coarse tuning regions. The gain in region I is reduced and the DAC is not able to reach the full upper reference voltage $V_{REF,U}$ (ref. to Fig. 5.7). However, section II is still starting at the lower reference voltage $V_{REF,L}$ as a gain error has no impact if all DAC capacitors are reset and in the conversion set to GND ($Z_L = Z_M = 0$).

Two potential solutions to resolve this drawback are discussed in the following. A pair of two slightly shifted reference voltages $V_{REF,I}$ and $V_{REF,II}$ are provided at the coarse tuning crossing points. Fig. 5.10 shows the principle of starting the coarse tuning region II with the slightly lowered second reference voltage $V_{REF,II}$, e.g. $V_{REF,I} = 250\,\text{mV}$ and $V_{REF,II} = 240\,\text{mV}$. $V_{REF,II}$ can be set to exactly match the maximum output voltage of region I or could be set even lower to include some margin. This margin requires to calibrate the DAC at the start of region II not with the digital input word $Z_M = Z_L = 0$ but rather with an offset, e.g. $Z_L = 17$. This calibration requires additional effort but enables sharing the same reference voltages across all Bias-DACs when considering qubit scaling.

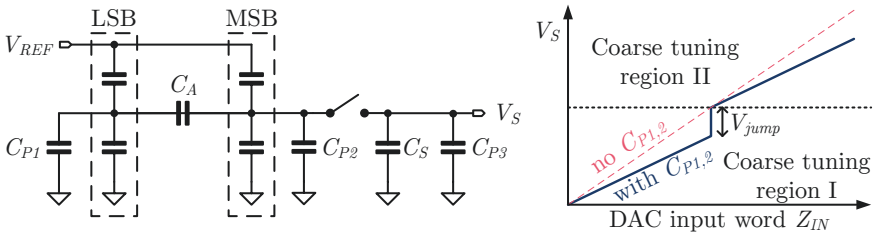


Figure 5.9: DAC gain error caused by parasitic capacitance C_{P1} and C_{P2} leading to a voltage jump V_{jump} at crossings of coarse tuning regions.

This is necessary as even multiple duplicated Bias-DACs have different mismatch and parasitic capacitances introducing a varying gain error. However, this solution approach comes at the cost of a doubled step size and a reduced DAC resolution of 1 bit. Fig. 5.10 shows this approach and how a linear DAC output behavior can be achieved.

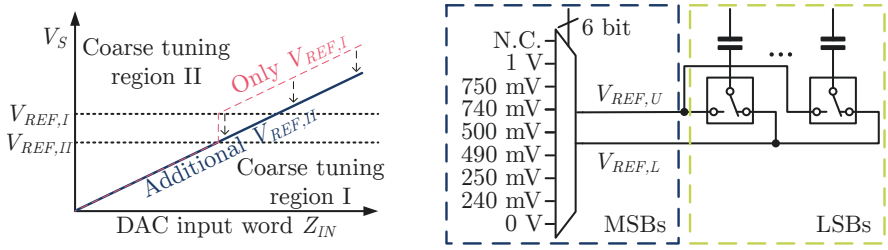


Figure 5.10: Avoid voltage jump V_{jump} by using two slightly shifted reference voltages $V_{REF,I}$ and $V_{REF,II}$ per coarse tuning crossing.

The second approach to avoid voltage jumps V_{jump} uses the regular reference voltages, as shown in Fig. 5.7. The missing voltage steps between the two regions I and II are filled with intermediate steps of double the step size. However, all other voltage steps remain unaffected and are operated with a step size of ≈125 µV corresponding to 13 bit resolution. Fig. 5.11 shows the principle of this solution. In order to generate intermediate steps filling the missing voltage range, the DAC operates with following coarse tuning setting. First, the end of region I is approached with regular coarse tuning settings, i.e. the DAC is being supplied with a reference voltage difference $\Delta V_{REF} = V_{REF,U} - V_{REF,L} = 125\,\text{mV}$. After reaching the last voltage step of region I, the lower reference voltage of region I $V_{REF_L} = V_{REF,L,I}$ is kept and the upper one of region II $V_{REF_U} = V_{REF,U,II}$ is set and thus a reference voltage difference of $\Delta V_{REF} = 250\,\text{mV}$ is applied to the DAC. This is the reason for the doubling in step size. Now, voltages of the previous missing voltage range V_{jump} can be generated while doing so the charge-redistribution DAC input is operated somewhere in the center of its digital input range, typically around $2^N \cdot Z_M + Z_L = 400$ to 600 for the 10 bit input word of the charge-redistribution DAC. Doing so adds some additional input words to the DAC input range, because we move away from the setting of $Z_{IN}[15:13] = Z_{IN}[12:10]$ and add some values where $Z_{IN}[15:13] = Z_{IN}[12:10]+1$. As with the first and previous discussed approach, voltage jumps V_{jump} in the DAC output characteristic can be avoided. In contrast to the previous approach, the overall resolution

of the DAC is not diminished and just the added intermediate steps doubled in step size.

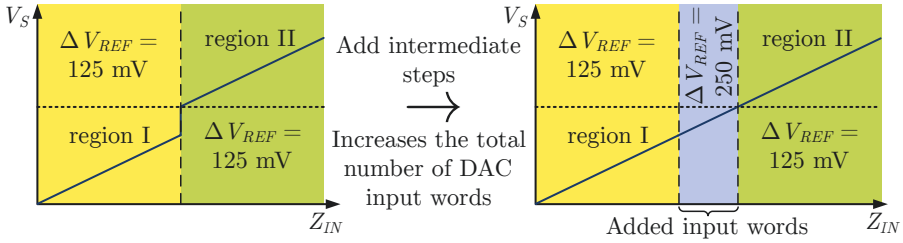


Figure 5.11: Avoid voltage jump V_{jump} by adding intermediate steps between region I and region II.

5.4 Digital control, timing and memory

This section focuses on the digital parts of the Bias-DAC. Section 3.2 introduced the idea of generating timing and control signals for multiple Bias-DACs in an independent block, as to facilitate qubit scaling. The central generated signals are then routed to each DAC. The local memory of the DAC is saving the output words in 8x 16 bit arrays and in which sequence the output channels are to be written into 9x 4 bit arrays, see Fig. 5.12. This totals to $8 \cdot 16\,\text{bit} + 9 \cdot 4\,\text{bit} = 164\,\text{bit} = 20.5\,\text{B}$ of local memory to generate 8 independent output voltages. The DAC then cycles through these memory arrays by utilizing an internal 4 bit counter until the next channel select value is programmed to 15, which selects the first array entry as the next. This enables us to select the order and number of active output channel and their corresponding input word freely. In order to operate the DAC with some output channels deactivated, the active ones are programmed starting from the beginning of the array, but not all array rows are used and the special channel select entry 15 is placed after the last memory entry. The memory can be reset, written and read out via the I^2C interface.

Additional to the local memory, the DAC only requires 4 digital signals: $D_{Discharge}$, $D_{Conversion}$, $D_{S\&H}$ and $D_{NextCoarse}$. $D_{Discharge}$ to discharge and reset the charge-redistribution DAC internal capacitors. $D_{Conversion}$ to start the conversion and apply the current entry input date from the input word memory, if signal is low all input dates are set to 0. Setting all input dates to 0 is needed in order to reset the DAC to the next lower reference voltage $V_{REF,L}$ that could be different to what was set in the previous conversion. $D_{NextCoarse}$ changes the coarse tuning setting to the next entry. Lastly, $D_{S\&H}$ toggles the switch of the S&H output channel of the current entry in the channel select memory. The following sequence is used to operate the Bias-DAC. Starting from the point in time where the DAC just completed the previous conversion and disabled the S&H switch: first, the coarse tuning is set to the next selected reference voltages by $D_{NextCoarse}$, so the following discharge is done to the correct $V_{REF,L}$. Then the DAC is discharged by $D_{Discharge}$. The DAC conversion is started by $D_{Conversion}$. After all capacitors are charged to the correct value and the DAC generates the desired output voltage, the S&H switch

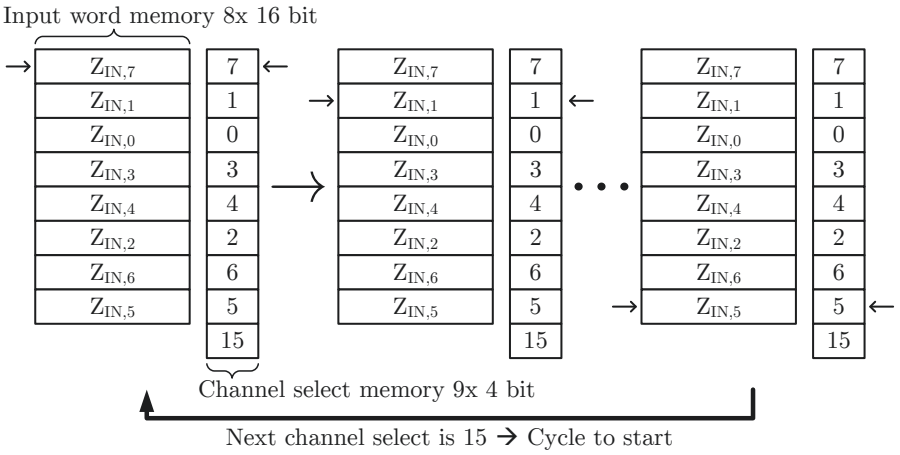


Figure 5.12: Local DAC memory saving up to 8 input words Z_{IN} and corresponding output channel. Memory is cycling if next channel select entry is 15.

of the corresponding output channel is opened and closed again after half a clock cycle. This is done to shift the refreshing of the output voltage to the highest possible frequency, so that the low pass shows most effect (ref. to Fig. 3.6). The conversion is finished by disabling $D_{Conversion}$ and the next conversion begins with changing the coarse tuning via $D_{NextCoarse}$. Each signal's rising and falling timing can be programmed via the I^2C interface. A 16 bit counter is continuously incrementing at each clock cycle and signals are changed to either high or low state if the counter is equal to the programmed dates. Each signal is therefore programmed with two dates one for rising and one for falling counter state, e.g. $D_{Discharge} \uparrow$ and $D_{Discharge} \downarrow$. This allows setting the timing and duty cycle of each signal fully configurable. Furthermore, the overflow of the counter can be set via I^2C to program a counter period date, if the counter reaches this value, it is starting from 0 again.

Every clocked digital block in this work is preceded by a clock select MUX and clock divider, see Fig. 5.13. The clock sources can be set to GND, which disables all following circuitry as a measure to manual clock gate. Other clock source are either the I^2C clock CK_{I2C}, an externally fed clock signal CK_{EXT} or an on-chip DCO generated clock CK_{DCO}. However, the DCO implementation is not part of this work. The following clock divider allows division by a factor 2^N and $N \in [0, 15]$. While operating a qubit a use case can arise where the Bias-DAC and the pulse-DAC, which is generating the control pulses for qubit manipulation, are required to share one of the clock sources. The clock divider is able to divide down the 250 MHz clock, as it is required by the pulse-DAC, and thus save power in the Bias-DAC

An overview of the just described digital circuitry combined the previously discussed analog part is given in Fig. 5.14. Some not previously elaborated design choices are the usage of IO NMOS transistors, which are preceded with level shifter (LS) to convert the core voltage (1.2 V) up to the IO voltage (1.8 V to 3.3 V). Those IO transistors are used in order to minimize leakage current on high-ohmic circuit nodes. Some additional dummy

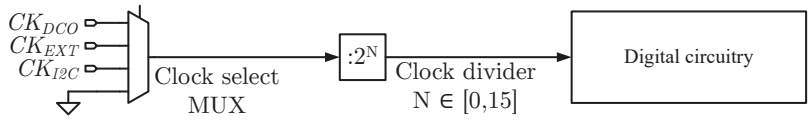


Figure 5.13: Clock select MUX and clock divider.

transistors are included to counteract the charge injection of the S&H switch. The signal D_{DacClk} is the clock of the Bias-DAC's local memory blocks and is triggered when either $D_{Discharge}$ or $D_{NextCoarse}$ is changed.

5.5 Auxiliary Measurement Circuitry

A challenge resulting from saving an output buffer in the Bias-DAC is a very low driving capability, only designed to counteract leakage current in the range of some pA, as the metal electrodes of the qubit represent a high-ohmic and purely capacitive load. This complicates direct measurement of the Bias-DAC and some auxiliary circuitry is added in order to guarantee measurement capability of the Bias-DAC. In order to avoid disturbance with the qubit operation, a duplicate of the Bias-DAC is included, whose output channels are wired to the on-chip measurement circuitry. Whereas power consumption plays a major role in the Bias-DAC design, the power constraints of the auxiliary measurement circuitry are more relaxed, because those blocks will only be needed for measurement purposes and are powered down when the Bias-DAC is in use with a qubit.

Fig. 5.15 shows the setup of the duplicated Bias-DAC and different output channels are connected to either one of the three amplifier configurations. These amplifiers are used to buffer or amplify the output voltage to enable measurements. In order to be able to convert the voltage on-chip into the digital domain, a ΣΔ modulator is designed and implemented. The on-chip analog-to-digital conversion via the ΣΔ modulator is included in case the cabling or other noise sources (e.g., crosstalk of the long twisted-pair cables inside the dilution refrigerator) impose a problem to measure via the amplifiers. Moreover, a direct on-chip analog-to-digital conversion seems useful as building block for future cryogenic ICs to come. One possible application could be in the automated tuning and calibration of DACs, but is not limited to this. The ΣΔ modulator measures the mean value of the Bias-DAC output voltage $V_{S,4}$. An input current into the ΣΔ modulator will be present. This is solved by adding a buffer amplifier between the DAC and the ΣΔ modulator in order to detect voltage drifts and fast changes in $V_{S,4}$, which are not visible via the ΣΔ modulator. A window comparator is included in the design to detect if $V_{S,4}$ is always between the two externally fed voltage limits $V_{WC,1}$ and $V_{WC,2}$.

5.5.1 Amplifier

The three amplifier configurations for buffering or amplification of $V_{S,1-3}$ as well as the used OpAmp design are shown in Fig. 5.16. For the OpAmp an existing and well-tested design of previous tapeouts is used. The OpAmp was designed for a high gain of

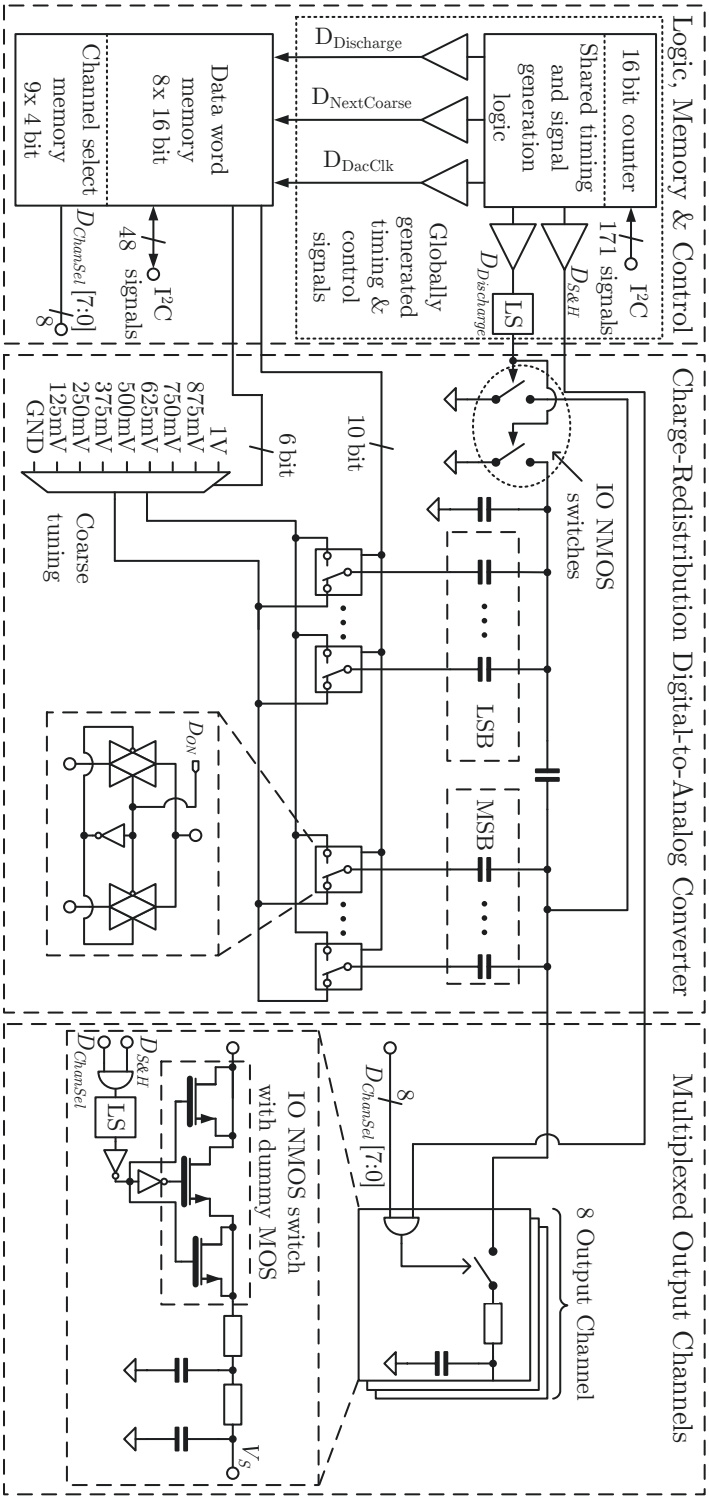


Figure 5.14: Overview of implemented Bias-DAC.

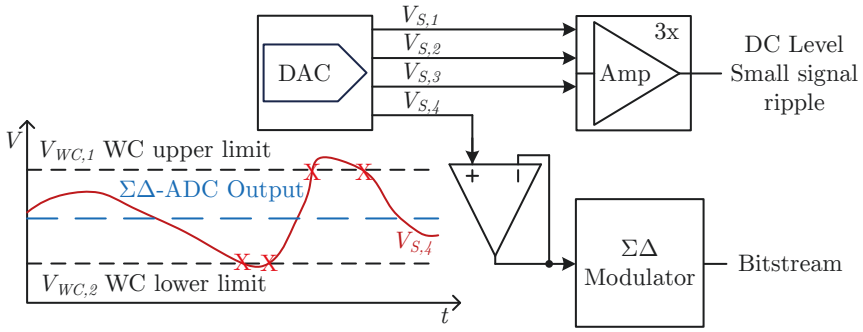


Figure 5.15: Dublicate of the Bias-DAC connected to auxiliary measurement circuitry.

70 dB, which is quite fitting to this use case. The OpAmp topology used for the three configurations is a Miller-OpAmp. M3 and M4 are used as a PMOS input differential stage and transistors M5–M7 are designed as a cascode current mirror load. M11 and M12 are used as a class A output stage. R_z and C_M generate a dominant pole for stabilization. Biasing is done via a wide swing current mirror maximizing the voltage headroom, which is important as an increase in transistor threshold voltage is expected at cryogenic temperatures (ref. to section 2.4.1).

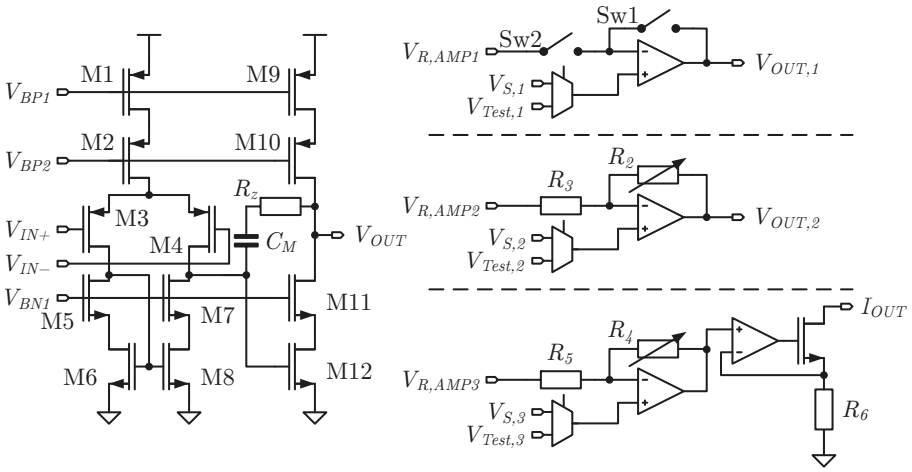
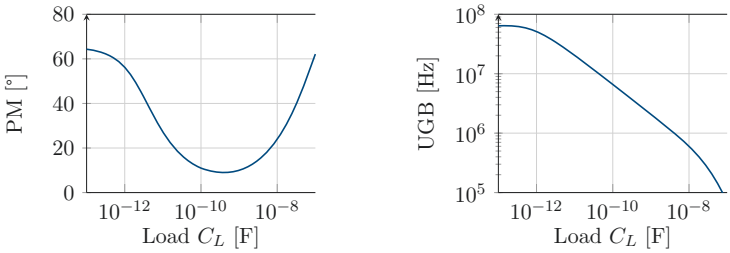


Figure 5.16: On-chip amplifier to buffer and amplify DAC output $V_{S,1-3}$.

Simulation of the OpAmp used with all three amplifiers results in an open loop gain of about 73 dB. With a load of 100 fF the PM is 65° and the UGB is at 80 MHz. As the load is not fixed and may vary depending on the measurement setup, the PM and UBG is simulated over a swept load capacitance C_L and results are shown in Fig. 5.17. The PM plotted in Fig. 5.17a, shows a reduced PM for rising C_L values down to 10.6° at 263 pF. For even greater load capacitance values, the dominant pole is the output node and therefore the PM is rising again. Simulations indicate OpAmp stability for all load conditions, because the PM is always greater zero. Additionally, the PM can be altered by changing

the bias current level as well as supply voltage. If this is still not sufficient in order to stabilize the OpAmp, a different load must be used in the measurement setup, e.g. by increasing/decreasing C_L or by installation of an additional off-chip buffer into the signal path. Each of the OpAmps shown in Fig. 5.15 and Fig. 5.16 are biased through a 3 bit binary weighted current mirror bank, which in turn is biased by one reference current I_{REF} fed in from external. This is done in order to allow for a multitude of configuration options to tune the amplifiers at cryogenic temperatures. With the nominal reference current of $I_{REF} = 25\,\mu A$ the current mirror banks can tune each bias current of the OpAmps in the range of 2 µA to 16 µA in 2 µA steps.



(a) OpAmp PM over load C_L.

(b) OpAmp UGB over load C_L

Figure 5.17: Simulated PM and UGB of used OpAmp in the auxiliary measurement amplifier.

The three different OpAmp configurations shown in Fig. 5.16 were included for test case purposes, enabling additional on-chip gain and optional voltage to current conversion. The first amplifier can be connected to either $V_{S,1}$ or $V_{Test,1}$ on its negative input port. The option to connect to an external test voltage $V_{Test,1}$ combined with the option to switch the OpAmp from unity-gain to open-loop configuration and supply a second voltage from external $V_{R,AMP1}$ enables us to characterize the OpAmp at cryogenic temperatures prior to using it for the Bias-DAC measurements. The same is done for the other two OpAmp configurations, i.e. non-inverting amplifier and non-inverting amplifier with following voltage-to-current conversion. The gain of the non-inverting amplifier can be set between 2 and 7 via digital configuration bits changing the value of R_2, which is implemented as a resistor bank, with $R_3 = R_5 = 10\,k\Omega$. One difference compared to the unity-gain buffer is that for the non-inverting amplifier to operate the reference voltage $V_{R,AMP2}$ is always required, it is therefore possible to select and MUX one of the 8 Bias-DAC reference voltages to $V_{R,AMP2}$. Being able to switch from one reference to another while in operation may be necessary to prevent the OpAmp output from reaching the rails and thus operating the OpAmp in compression, especially when higher gain levels are selected. The voltage-to-current conversion is designed to be able to drive a 50 Ω load of measurement equipment, e.g. a spectrum analyzer, and R_6 is also designed as 50 Ω resistor. The conversion is done by a NMOS transistor rather than PMOS for two reasons: it is offering a higher mobility and thus intrinsic gain and the GND of the measurement equipment can be used as a supply, when the GND level of the chip is shifted down to −1 V.

Primary focus of these amplifiers is the measurement of noise and the refresh ripple in the Bias-DAC output, see Fig. 3.4. However, one could also think about using them to

measure the DAC output curve and the unity-gain buffer appears as a natural choice in this case. Considering the Bias-DAC without added intermediate steps, 13 bit of resolution have to be measured. A finite open-loop gain of $A_{OL} = 70\,\text{dB}$ induces a maximum gain error at full-scale (1 V) of 2.5 LSB. The gain error at 1 V is $G_{Err} = 1 - \frac{A_{OL}}{A_{OL}+1}$ and has to be set in relation to the LSB step size $LSB_{Step} = 1/2^{13}$ and thus it is $G_{Err}/LSB_{Step} = \left[1 - \frac{A_{OL}}{A_{OL}+1}\right] \cdot 2^{13} = 2.5\,\text{LSB}$. However, there a few ways to circumvent this issue. If the Bias-DAC output can be measured directly, it gives the most trustworthy results possible. The ΣΔ modulator can be used, which will regulate the gain error inside the control loop. Measurement of only the charge-redistribution DAC without the coarse tuning requires only 10 bit resolution to be measured, resulting in a full-scale error of 0.3 LSB. This can be done as the shift of the input reference voltages is not affecting the capacitor mismatch and the present parasitic significantly. However, the last option will render it impossible to measure both techniques to mitigate voltage jumps V_{jump}, see section 5.3.

5.5.2 ΣΔ-Modulator

The ΣΔ modulator is implemented as a cascaded modulator or also called multistage noise shaping (MASH) modulator. Fig. 5.18 shows the designed third-order 2-1 MASH modulator. [118, pp. 277-280]

The choice of implementing a third-order 2-1 MASH ΣΔ for this application is discussed first. The Bias-DAC is expected to generate a stable output voltage. This DC input leads to a repeating pattern in the output of a ΣΔ and thus is visible as a noise spur in the spectrum. This can be avoided by using a dither source. However, also a second-order modulator utilizing two integrators is spreading the repeating pattern over a longer period. [113, pp. 241-242]

Additionally, the already increased noise shaping behavior of the second-order ΣΔ can be further emphasized by implementing a third-order ΣΔ modulator. The design is implemented in such a way that the modulator can be operated in either second or third-order mode. Whereas second-order ΣΔ modulators are always stable, there exists a risk that a third-order one can become unstable [113, p.267]. This can be prevented by changing to a feed forward structure, which is achieved by operating the second stage of the modulator on the quantization error of the first second-order stage. Therefore, the whole modulator is build with unconditionally stable first and second-order loops. We choose a 2-1 MASH instead of an also possible 1-1-1 MASH, which would cascade three first-order loops, because they are described by Baker as "[...] much more robust than the 1-1-1-based topology and can provide output signals free of unwanted tones." [113, pp. 275-279]. As all the criteria match the desired application, the overall structure of the ΣΔ modulator is then adopted from [113, Fig. 7.58]. For the comparators a 1 bit quantization was chosen, because this guarantees an inherent linearity [113, p.269]. The digital circuitry following both comparators is discussed later, after all the color indicated tuning options in Fig. 5.18 have been presented. The reference voltage V_{REF} can be demultiplexed from either the Bias-DAC reference voltages or generated in a ΣΔ modulator-internal R-string DAC, which is designed to output 0 V to 1.2 V in 100 mV steps, for a given supply voltage of $V_{DD} = 1.2\,\text{V}$.

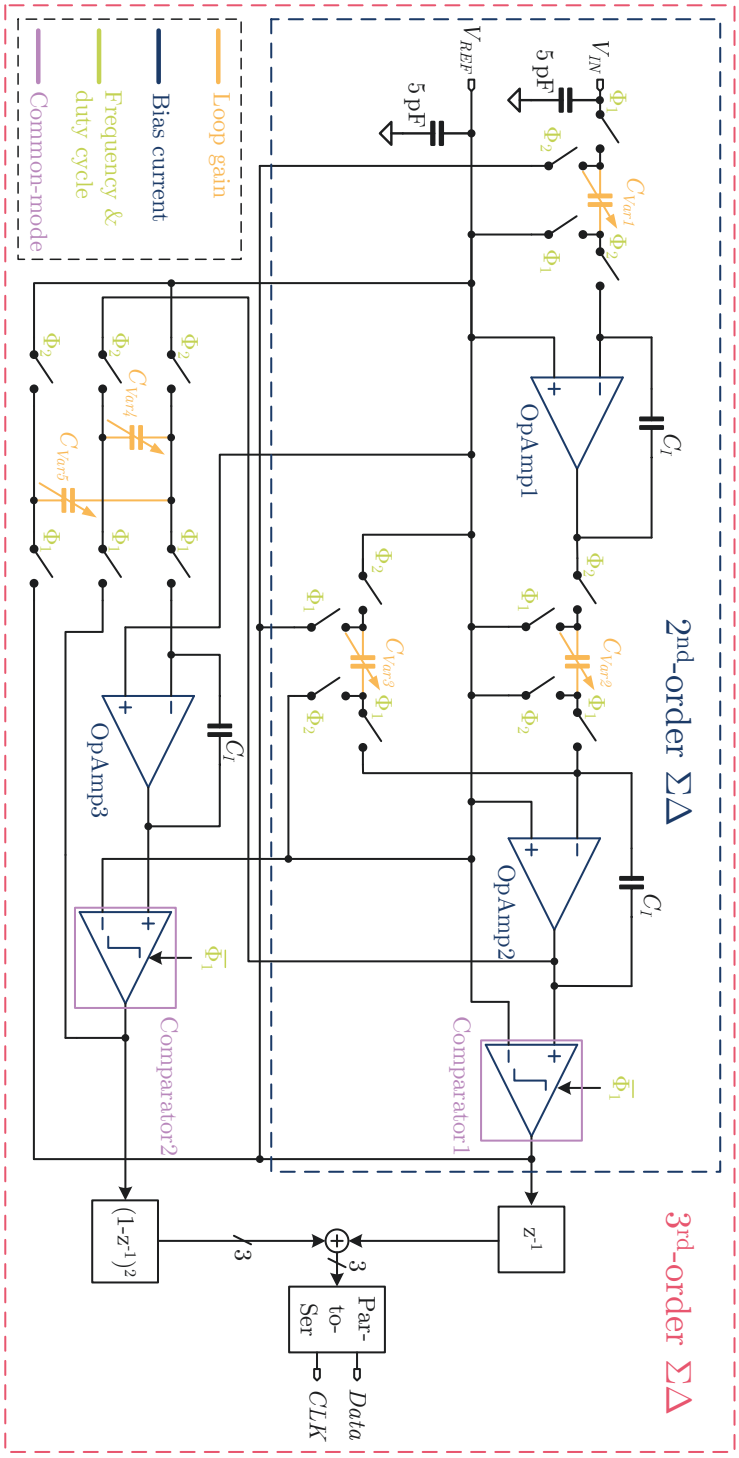


Figure 5.18: Third-order 2-1 MASH ΣΔ modulator.

Special emphasis is laid on incorporating many configuration and tuning options to cope with the device behavior changes at cryogenic temperatures. For later debugging, the same OpAmp as described in section 5.5.1 is used for the integrators OpAmp1-3. Thus, the same individual bias current tuning is implemented and is also done for the later presented comparator design. This is the first of the total of four ways to tune and configure the ΣΔ modulator. The two non-overlapping clocks Φ_1 and Φ_2 can be controlled in frequency and their duty-cycle can be individually set, see Fig. 5.19. Each high and low hold time of Φ_1 and Φ_2 can be individually set to $K, L, M, N \in [1, 254]$ clock cycles. The loop-gain is adjustable by changing settings of the 3 bit controlled capacitor banks C_{Var1-5}, going from 200 fF in 200 fF steps up to 1.6 pF. In combination with an integrator capacitance $C_I = 2\,\text{pF}$ the integrator gains can be adjusted independently in the range from 0.1 to 0.8 with 0.1 step size. On the one hand, this is done to assure that each integrator gain is low enough to assure the OpAmps are not reaching close to the supply rails (integrator saturation). On the other hand, a larger signal level is beneficial to the modulator's performance. Lastly, the CM feedback (CMFB) level of the comparators can be individually adjusted.

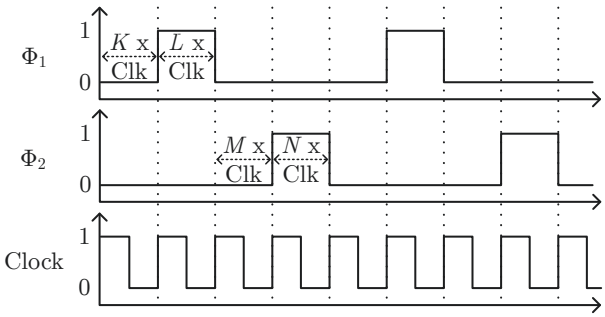


Figure 5.19: Generation of two configurable non-overlapping clocks Φ_1 and Φ_2.

Fig. 5.20 shows the comparator design, which consists of a preamplifier [119] with CMFB and a track & latch (T&L) comparator [119, 120]. The preamplifier boosts the input voltage difference and reduces metastability in the T&L comparator by increasing the gain. The preamplifier also reduces the input offset voltage. The bias current I_{REF} is generated with the same current mirror bank as implemented for all OpAmps. The internal CMFB OpAmp is the same as shown in Fig. 5.16 and used with the identical reasoning as for using it in the ΣΔ integrators. The CMFB resistors R_{CM} can be designed rather large, i.e. 200 kΩ each. In general, this would induce much thermal noise, but because the targeted temperature is in the deep cryogenic regime, the thermal noise is playing a vastly reduced role and transistor noise is expected to be the main source of noise, see Table 2.6. The CMFB voltage level $V_{REF,CM}$ can be set via a programmable R-string from 0 V to 1.2 V in 50 mV steps and is again depended on the supply voltage. The preamplifier achieves a simulated gain of 30 dB.

The comparator output is then digitally processed, i.e. multiplication with z^{-1} and $(1 - z^{-1})^2$ and summation. Depending on the selected order of the ΣΔ modulator, the MASH branch may be deactivated and only the second-order loop output is used. A parallel-to-serial conversion is included in order to transmit the 3 bit wide data word of

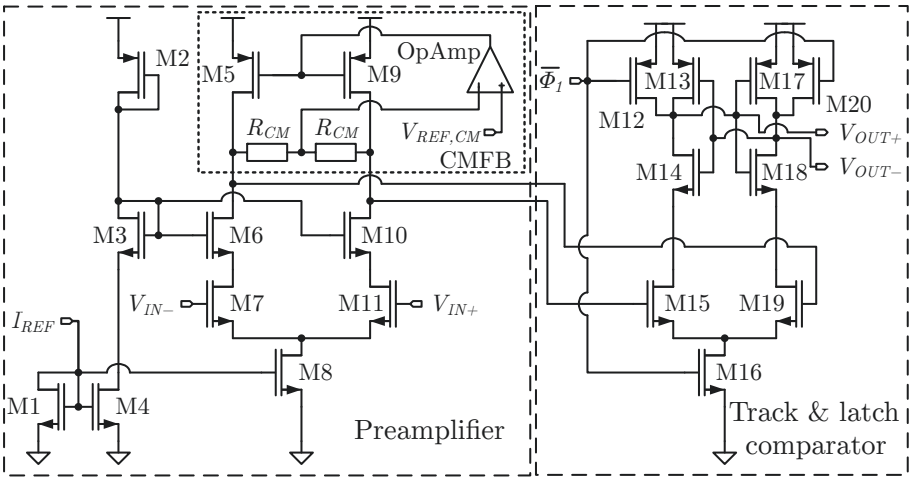


Figure 5.20: Track & latch comparator with pre-amplifier.

the third-order modulator over the single data wire. The data to be sent are also of 3 bit word size, because the third-order output is multiplied with $(1 - z^{-1})^2 = 1 - 2z^{-1} + z^{-2}$ and can therefore only be in the range of $[-2, +2]$. Adding the 1 bit of the second order loop the summed output word is in the range of $[-3, +3]$ which is well represented with 3 bit. If only the second-order loop is enabled, the data word has only 1 bit and can be transmitted over the data wire directly. The data as them will be received from the ΣΔ modulator is schematically depicted in Fig. 5.21. For the third-order modulator case the three bits of the data word are always followed by at least one missing clock cycle. This is implemented to be able to detect start and end of transmission packages and the missing clock cycle can be used to align the logic analyzer even when the transmission is read from an arbitrary point in time. Furthermore, the transmission clock rate can be calculated from the ΣΔ modulator clock and settings. With this encoding scheme, the modulator bitstream can be send in real-time for second and third-order noise shaping.

The required oversampling ratio (OSR) can be calculated by [121]:

$$OSR = \left[\frac{2}{3} \frac{DR^2}{2L+1} \frac{\pi^{2L}}{(2^{B-1})^2} \right]^{\frac{1}{2L+1}} \tag{5.18}$$

with L being the ΣΔ modulator order, DR is the dynamic range and B the quantization bit count. In our case the quantization bit count is fixed to $B = 1$. The ΣΔ is aimed at $N = 16$ bit resolution. Therefore, the dynamic range in dB is $DR = 6.02 \cdot N + 1.76 \approx 98$ dB. Consequently, the calculated OSR for the second-order modulation $L = 2$ is $OSR_{2nd} = 152.3$ and for third-order modulation $L = 3$ $OSR_{3rd} = 47.9$. F. Maloberti [122, p.270] derived that the OpAmp open loop gain A_{OL} should satisfy following relation to have an negligible impact on the modulator performance:

$$\pi(A_{OL} + 2) \gg OSR \tag{5.19}$$

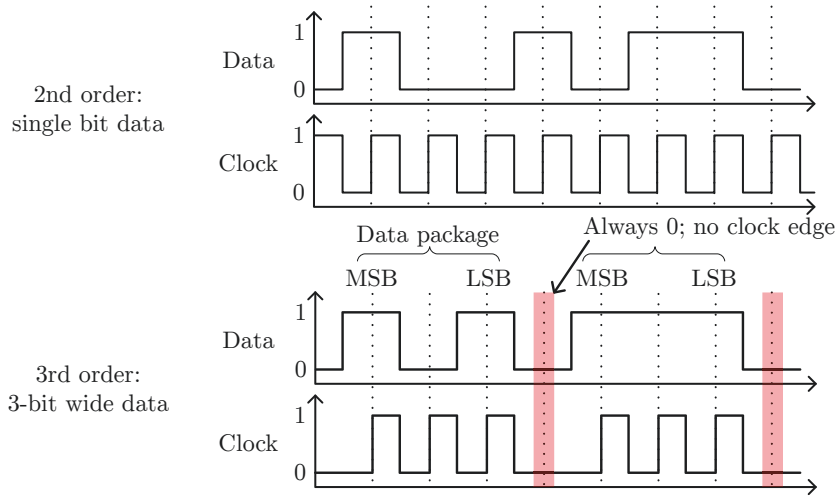


Figure 5.21: Second and third-order ΣΔ modulator bitstream data transmission.

With a simulated open loop gain of $A_{OL} = 70\,\text{dB} \approx 3160$ this condition is fulfilled for both second and third-order modulation.

5.5.2.1 Window Comparator

The beginning of section 5.5 presented the idea to use a window comparator to detect if the ΣΔ modulator input voltage stays within set voltage boundaries $V_{WC,1}$ and $V_{WC,2}$, see Fig. 5.15. Fig. 5.22 shows the implemented window comparator. The OpAmp is a duplicate of the one used in the amplifiers and ΣΔ modulator integrators, see Fig. 5.16. The T&L comparator of the ΣΔ is not used, because this could lead to missing a crossing when it appears in-between two clock cycles. With an open loop gain of ≈70 dB the OpAmp can be basically considered a mere comparator when operated in open loop configuration. It is therefore independent of the later applied clock frequency for the window comparator to detect crossings. Another benefit is the ability to characterize the OpAmp on its own via the unity gain buffer circuitry and be able to more conveniently debug the cryogenic window comparator behavior. The window comparator is also able to count upwards and downwards crossing of both voltages $V_{WC,1}$ and $V_{WC,2}$ and sum the number of events in four 8 bit counters. Detection of a crossing is only limited by the OpAmp bandwidth, but the counting of up and down crossings is limited by the applied clock frequency. However, detection of number and direction of crossings is just additional information. The important information is if any crossing event did happen at all and that is assured by using non-clocked OpAmps followed by four flip-flops (FFs) saving the event occurrence until the next clock cycle is happening and the counters save that event.

For testing purposes the input of the window comparator can be multiplexed to test voltages V_{Test1} and V_{Test2}, which are fed in from external sources. Furthermore, the

digitally buffered output of the OpAmps can be multiplexed to the two digital pads which are normally used for the ΣΔ data and clock.

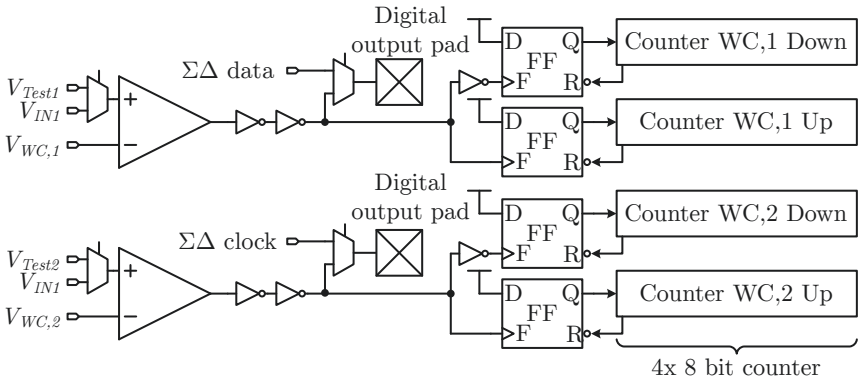


Figure 5.22: Window comparator used in combination with the ΣΔ modulator.

Chapter 6

Measurement

This chapter focuses on measurement results of the fabricated designs presented in the previous chapters 4 and 5. Designs presented in those chapters were realized as parts of two different tapeouts, but both ICs use the same TSMC 65 nm LP CMOS technology.

6.1 Measurement Setup

The general cryogenic measurement setup is presented in this section. All measurements were performed inside an Attocube attoDRY800 closed-cycle helium Gifford-McMahon (GM) cryostat, which can reach base temperatures of about 6 K. Fig. 6.1 shows the measurement setup.

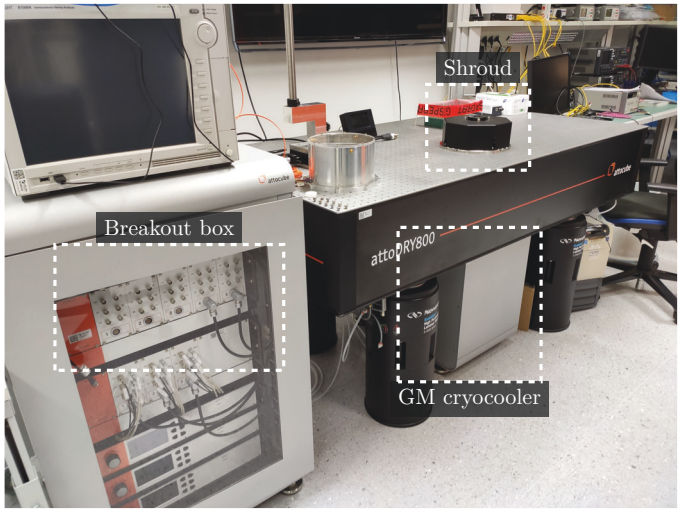


Figure 6.1: Attocube attoDRY800 closed-cycle helium cryostat.

The setup consists of an optical table with a shroud for sample placement on top of the table, whereas a GM cryocooler is mounted below the table. Up to 58 DC or low frequency lines can be connected to the cryostat sample space via the breakout box. The breakout box is holding 29 BNC connectors, whose signal and ground connections can be used to connect two individual signals to the inside of the cryostat. The signal is then routed

via Fischer connectors to the cryocooler and is finally wired via internal twisted pair cables up to the sample space. The shroud offers additional 3 SMA connectors to directly connect signals to the sample space, this is especially useful for high frequency RF signals, e.g. clock signals. A picture of the sample space in a typical measurement experiment is shown in Fig. 6.2, Fig. 6.17 and Fig. 6.28. The cryostat is equipped with a sample space heater inside its golden sample plate holder, which allows to set a controlled sample temperature. The lower temperature limit is set by the base temperature of the cryostat ≈6 K, which is determined by the available cooling power. The upper temperature limit is set by the maximum heating power of the sample heater, i.e. 5 W, the number of wires and mass inside the sample space. Typical maximum achievable temperatures $T_{S,Max}$ are in the range of 100 K > $T_{S,Max}$ > 50 K.

Two custom ICs were fabricated, one IC which includes the bandgap and LR, see chapter 4, and a second one including the Bias-DAC with auxiliary measurement circuitry, see chapter 5. The SMD capacitors used for all PCBs are of ceramic dielectric NP0/C0G type, which is reported to behave well at cryogenic temperatures down to liquid helium [123, 124].

6.2 Bandgap

The custom IC sample is mounted on a PCB, which is fabricated with a backplate of electroless nickel gold. This backplate is required for good thermal anchoring of the PCB to the 6 K temperature of the sample holder. Additional ground stitching vias guarantee a good thermal conduction through all the layers of the PCB and up to the big ground plane of the packaged IC sample, as device under test (DUT). The PCB is shown in Fig. 6.2. The PCB is mounted on top of a thick copper plate, which is used as a mechanical adapter for mounting the PCB inside the cryostat. The following bandgap measurements were done with either a Keysight 34465A digital multimeter or a 34470A digital multimeter.

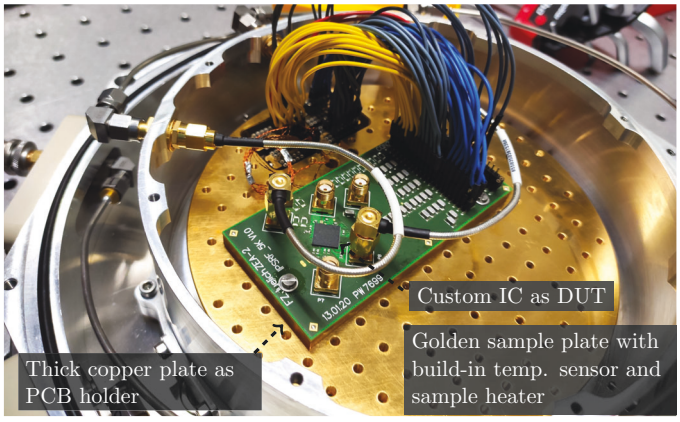


Figure 6.2: Bandgap and LR measurement setup inside the cryostat shroud.

The bandgap startup for various configuration settings was tested. This was done by sweeping through all CM and bias settings for various supply voltages. Afterwards, the bandgap was started by turning on transistor M6 (ref. to Fig. 4.3), which is discharging the node of the OpAmp output voltage V_B. After disabling of start-up transistor M6, the output voltage V_{REF} was measured through a pad by turning on transmission gate TG4. As the bandgap output is to be measured via the V_{OUT} pad (ref. to Fig 4.1), the bandgap is supplied by the pad connected to V_{IN} through the supply select switch. The bandgap functionality is then tested by sweeping through the output level of V_{REF} by changing its current mirror setting. An example of a functional and non-functional configuration of CM, bias level and supply voltage is shown in Fig. 6.3. Measurement is started 1 K above the base temperature of ≈6 K in order to achieve a regulated and settled sample temperature which is not dependent on the thermal power dissipation of the sample itself.

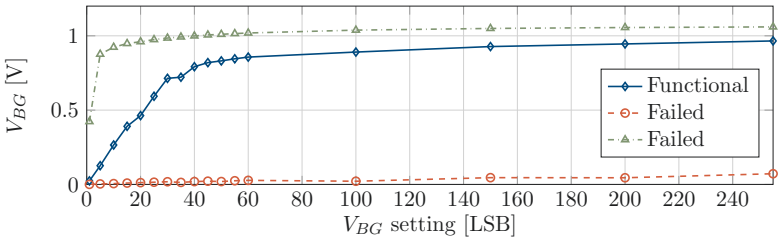


Figure 6.3: Example of bandgap being functional or failing depending on supply voltage, bias and CM settings at 7 K.

The results of this functionality test are summarized in Table 6.1. The bias current of the OpAmp inside the bandgap should be kept low in order to achieve a functional bandgap operation. Moreover, the CM level appears to be of less importance and can be set to all values. The internal bias current generation, which consists of transistor M1 enabling the current flow through resistor R_B, M2 and M3, which are connected as a cascode current mirror (ref. to Fig. 4.6), appears functional in order to operate the bandgap at 7 K. However, more extensive temperature sweep measurements show the instability and unreliability when using the latter biasing option.

		Min	Max
V_{DD}	[V]	1.2	> 2
CM level		1	4
Bias current mirror	[LSB]	1	9
Internal transistor diode bias		ok	ok

Table 6.1: First bandgap functionality test results.

After checking the bandgap functionality at 7 K, measurements in the temperature range of 7 K to 40 K were conducted. One of the results is the previously described instability of using the internal OpAmp biasing via diode connected transistors M2 and M3. Fig. 6.4 shows the corresponding bandgap output for a set output level setting of 25 and CM is set

to the lowest option, as higher CM settings were not working with the OpAmp internal biasing. The reason for this strong dependence on supply voltage and temperature is expected to be caused by temperature dependence of the internal biasing current itself. However, the measurement curve for $V_{DD} = 1.5\,\mathrm{V}$ indicates an internally self-biased OpAmp could possibly be used in further cryogenic bandgap designs. Valid cryogenic device models are required in order to design the OpAmp in such a way that it is able to operate with all variances in its bias current. The seemingly very stable output for $V_{DD} = 1.2\,\mathrm{V}$ at temperatures <20 K is discussed later in this section. For this work, the usage of a temperature dependent biasing via diode connected transistors appears not to be a valid choice.

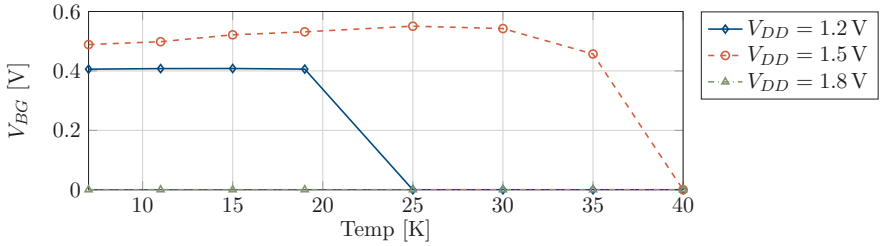


Figure 6.4: Bandgap operation for internal OpAmp bias configuration. Functionality is depending on V_{DD} and temperature.

The bandgap output voltage V_{BG} is shown in Fig. 6.5 for various values of the tuning resistance R_{var} (ref. to Fig. 4.3). As the bandgap OpAmp is not operational with its internal biasing, the reference current of the bandgap is used as bias current reference via V_B (ref. to Fig. 4.3 and Fig. 4.6). Detailed measurements for this biasing configuration are presented later in Fig. 6.8. Previous simulations, which are presented in Fig. 4.4 and Fig. 4.5b, showed a similar output voltage behavior with decreased R_{var} as the measurement results (ref. to Fig. 6.5), i.e. an overall increase in V_{BG} and tilt to lower temperatures. However, in contradiction to the simulated data an increase of R_2 would be required to shift the bandgap behavior towards a better temperature compensated state. The option to tune the bandgap in a wider tuning range even beyond what simulation results indicate should be included in future cryogenic bandgap designs. For this work, the best option is to disable bandgap resistor tuning and set $R_{var} \longrightarrow \infty\,\Omega$ high-ohmic.

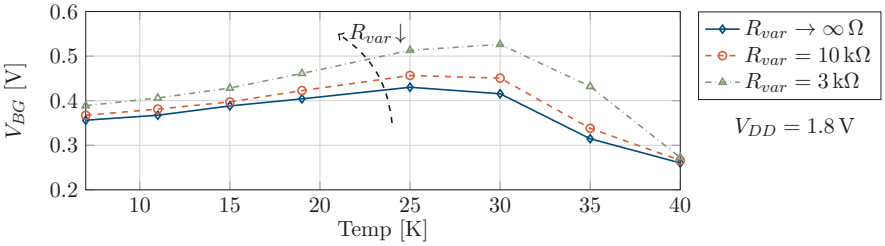


Figure 6.5: Effect of tuning R_{var} on bandgap output voltage V_{BG}. OpAmp biased by bandgap current.

After the measurement results of tuning the resistance R_{var} were discussed, a detailed look at the previously shown bandgap behavior for $V_{DD} = 1.2\,\text{V}$ is possible. As shown in Fig. 6.5, the decrease of R_{var} is visibly affecting the bandgap output V_{BG}. However, Fig. 6.6 shows no effect for varying R_{var} values for $V_{DD} = 1.2\,\text{V}$. This is a strong indication that the bandgap is not in a desirable operation state.

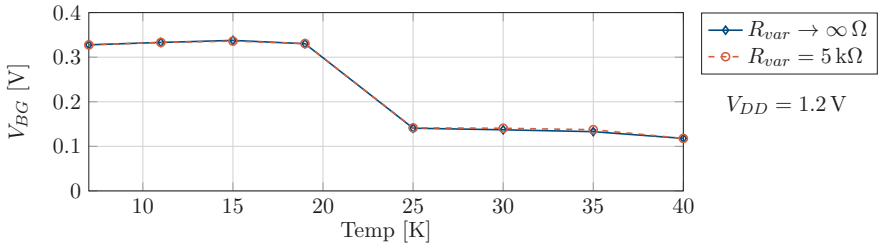


Figure 6.6: Tuning R_{var} with no effect for $V_{DD} = 1.2\,\text{V}$.

The next tuning option of the bandgap is the CM level and the impact of different CM level settings is measured, which is also depending on the supply voltage. The naming convention for describing the CM setting is for the lowest CM voltage option "1" and increasing to the highest CM voltage option "4", see Fig. 4.3. Fig. 6.7 shows three graphs for supply voltage levels of $V_{DD} = 1.5\,\text{V}$, $1.8\,\text{V}$ and $2.4\,\text{V}$. For $V_{DD} = 1.5\,\text{V}$ the output voltage V_{BG} is increasing with the CM level, but shows a drop when the CM level is increased from 3 to 4. This can be reasoned by the supply voltage not being high enough to allow for the highest CM level to operate the bandgap OpAmp as desired. This effect is similar to a different OpAmp measurement (ref. to Fig. 6.20), which is also requiring a CM input level to not exceed a certain threshold voltage. Further discussions to this effect are done in section 6.4. The CM setting of 4 is not inverting the trend of an increased bandgap output voltage V_{BG} for supply voltages $V_{DD} > 1.8\,\text{V}$, indicating enough voltage headroom for operation in the highest CM level setting. Furthermore, for $V_{DD} = 1.5\,\text{V}$ the CM level 2 and 3 are mostly identical in terms of V_{BG}, especially for temperatures $T < 15\,\text{K}$. This could be due to a larger voltage headroom requirement at colder temperatures. The overlapping curves for CM 2 and 3 can be viewed as indication for approaching the CM limit of the bandgap OpAmp. An increased supply voltage is shifting this CM limit upwards. Thus, when increasing the supply voltage to $V_{DD} = 1.8\,\text{V}$, the CM level 3 and 4 fall on top of each other, again indicating the CM limit. By increasing the supply further to $V_{DD} = 2.4\,\text{V}$, a separation of CM 3 and 4 curves is apparent and therefore supporting the assumption of an increased CM limit due to a larger voltage headroom at higher supply voltages. In terms of effect on the temperature stability, all CM settings appear to be of minor impact. A CM setting ≤ 2 would allow for safe operation of the bandgap, also for $V_{DD} = 1.5\,\text{V}$.

Changing the bias current is leading to a negligible effect as long as it is below a certain threshold. The bias level of the OpAmp is tuned via a current mirror bank (ref. to Fig 4.6), which is biased by the bandgap current mirror voltage V_B (ref. to Fig. 4.3). An increase of the bias level is leading to an output shift of the bandgap V_{BG}, see Fig. 6.8. However, the bias level is not noticeably impacting the temperature behavior of V_{BG} for small bias level settings of $\leq 5\,\text{LSB}$. A bias level setting of 6 LSB or above leads to a kink in the

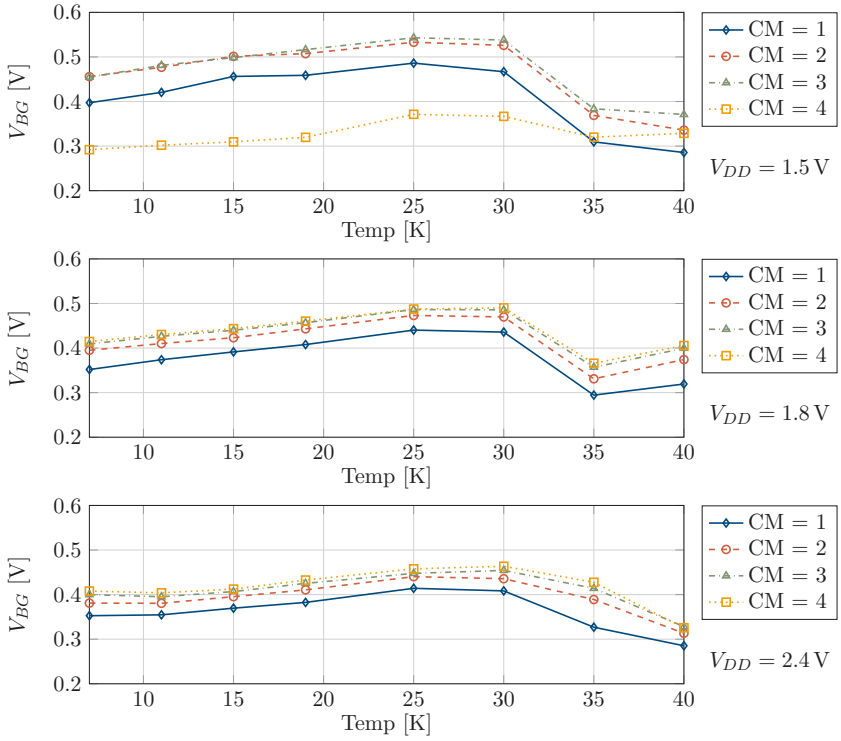


Figure 6.7: Effect of tuning CM level on bandgap output voltage V_{BG} for different supply voltages $V_{DD} = 1.5\,\mathrm{V}$, $1.8\,\mathrm{V}$ and $2.4\,\mathrm{V}$.

bandgap output voltage occurring between the two temperature measurement points at 19 K and 25 K. The same effect appears for all supply voltages in the range from 1.5 V to 2.4 V. In order to assure bandgap operation also for temperatures ≤ 19 K the bias level has to be kept below 5, adding margin the recommended setting is < 4.

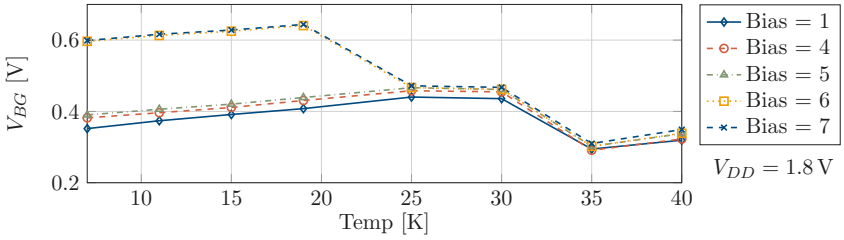


Figure 6.8: Effect of tuning bias level on bandgap output voltage V_{BG}.

Fig. 6.9 shows the bandgap output voltage for various supply voltages. Due to the previously presented results the CM and bias level are both set to 1. Although the bandgap can be regarded functional for V_{DD} = 1.5 V, the output voltage exhibits a visible offset to all the other tested supply voltages V_{DD} = 1.8 V, 2.0 V and 2.4 V. This can be interpreted as an indication that the voltage headroom is close to its minimum limit with an supply voltage of V_{DD} = 1.5 V. If one considers the previously discussed cryogenic shift in diode threshold voltage (ref. to Fig. 4.2) to about 1.2 V to 1.3 V, a supply voltage of 1.5 V allows for a drain-source voltage V_{DS} for the transistors M7 and M9 of the bandgap (ref. to Fig. 4.3) of about 0.2 V to 0.3 V. This V_{DS} voltage is just about the typical voltage that is required to operate transistors in saturation region in this technology node. This explains the difference in the output voltage between 1.5 V and the higher supply voltages.

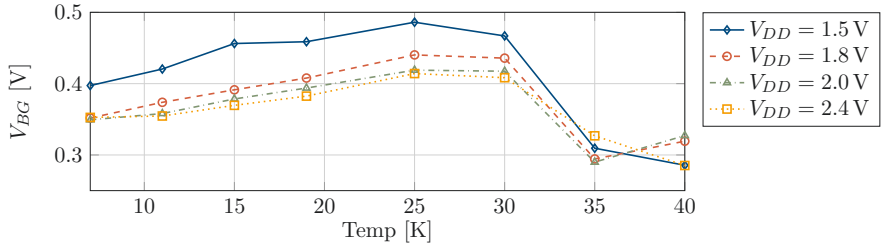


Figure 6.9: Bandgap output voltage V_{BG} vs. temperature for different supply voltage levels.

The corresponding power consumption for each supply voltage level is plotted in Fig. 6.10. For temperatures ≥ 35 K a correlation between bandgap output voltage V_{BG} and the current drawn is visible. However, this correlations is lessened for V_{DD} = 1.8 V and not observable for V_{DD} = 2.4 V. Another interesting point is the similar power consumption for V_{DD} = 1.5 V and 1.8 V at temperatures ≤ 15 K, which is about 220 µW to 300 µW. In order to characterize the cryogenic properties of the 65 nm CMOS technology used, a chip with single test devices like transistors, passive elements and also diodes was designed. This chip enables individual measurement of the diode type embedded inside

the bandgap. The following diode measurements can be used to investigate some of the cryogenic effects appearing for the bandgap.

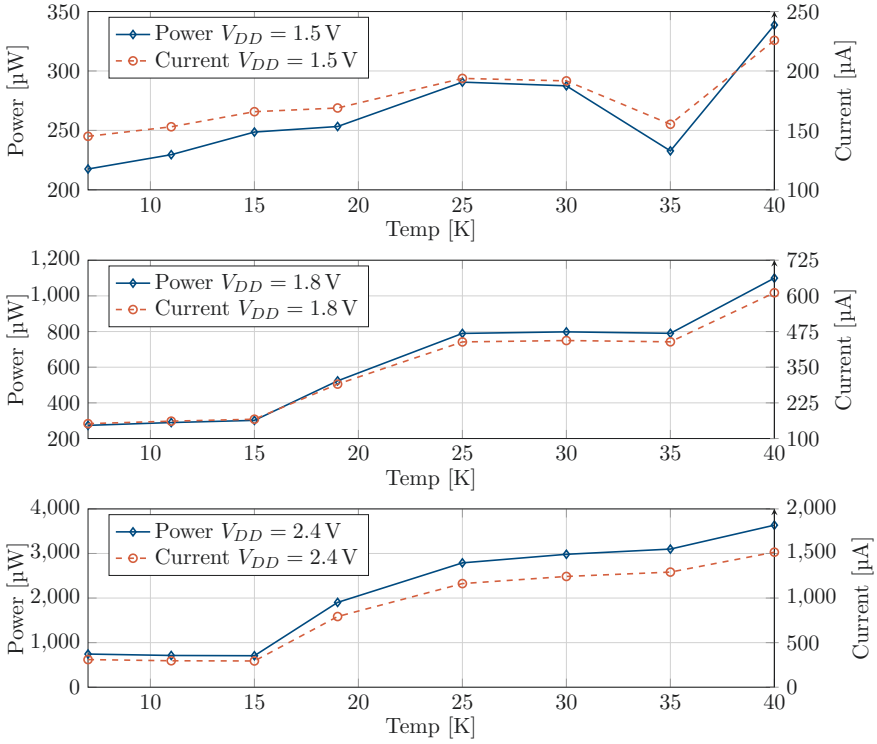


Figure 6.10: Bandgap power consumption vs. temperature for different supply voltages $V_{DD} = 1.5\,\mathrm{V}$, $1.8\,\mathrm{V}$ and $2.4\,\mathrm{V}$.

Fig. 6.11 shows results of I-V sweeps for the diode current I_D vs. the diode voltage V_D at cryogenic temperatures in the range of 7.5 K to 120 K, which were measured by a Keysight B1500A semiconductor device analyzer shown in the top left corner of Fig. 6.1. Furthermore, the typical range of interest for IC circuitry (bandgap design) is depicted, which would be from a few nA to ≈100 µA. The same threshold voltage shift towards higher voltages for lower temperatures is present as measured previously for a different diode, see Fig. 4.2. The diode shows a classical characteristic at 120 K with one continuous transition following the expected exponential curve, which can be described by (4.1). Additionally to the shifted threshold voltage, the slope is steeper at lowered temperatures as described in section 4.1. However, an additional cryogenic effect is appearing at $T \lessapprox 40\,\mathrm{K}$, which is changing the increase of slope to a rapid flattening and adds additional kinks to the I-V curve. These kinks remind of the cryogenic kink effect appearing for older CMOS technology ($\gtrapprox 350\,\mu\mathrm{m}$) transistors, see section 2.4.1 and Fig. 2.12a. Furthermore, these kinks and the flat slope give an indication to the change in the bandgap output voltage V_{BG} as well as power consumption at $\approx 30\,\mathrm{K}$. The flat I-V curve at 7.5 K is approaching a similar slope as the diode exhibits at RT. The kinks are likely to cause unexpected circuit behavior if not considered and future cryogenic device

models need to include these effects. This holds especially true when designing dedicated cryogenic bandgaps and circuitry aiming for optimum performance. However, the focus of this work is not single device characterization and modeling. Further investigation of this topic is therefore skipped with the remark that parallel research with the aim of development of comprehensive cryogenic device models is undertaken.

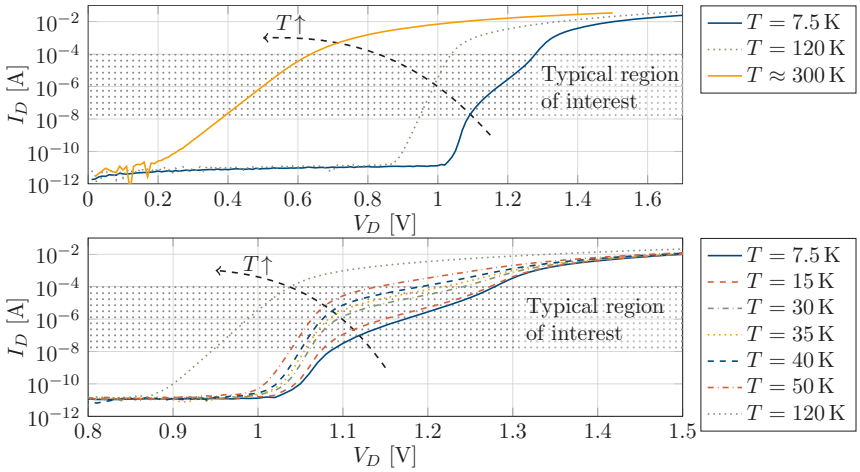


Figure 6.11: Cryogenic I-V measurements of diode type used in the bandgap.

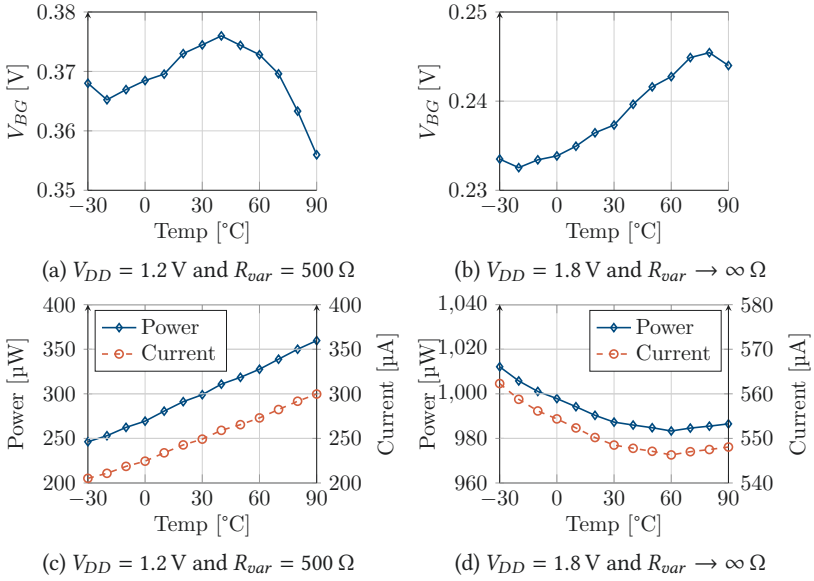
After discussion of each tuning option and its impact on the overall bandgap performance, the most suitable settings for the bandgap operation are summarized in Table 6.2. Additionally, also the minimum and maximum bandgap settings and supply values are given, as they have been derived and discussed previously.

		Min	Max	Proposed
V_{DD}	[V]	1.5	2.4	1.8
CM level		1	2	1
Bias current mirror	[LSB]	1	4	1
Internal transistor diode bias				no

Table 6.2: Summary of bandgap results for operation.

Fig. 6.12 presents RT measurement results of the bandgap. CM and bias level are set identical to the proposed cryo measurement ones, i.e. the CM level is set to 1 and bias level is set to 1 LSB. The current mirror bank setting for the output voltage V_{BG} (ref. to Fig. 6.3) is also set to its cryogenic measurement value, i.e. 25 LSB. The nominal supply voltage for the bandgap is $V_{DD} = 1.2\,\mathrm{V}$ and for the best temperature compensation the tunable resistor bank R_{var} is set to 500 Ω, see Fig. 6.12a. Because the proposed cryogenic supply voltage is set higher at 1.8 V, the bandgap is also measured at RT with $V_{DD} = 1.8\,\mathrm{V}$. For optimum temperature compensation with $V_{DD} = 1.8\,\mathrm{V}$ the tuning resistor is switched high-ohmic, i.e. $R_{var} \longrightarrow \infty\,\Omega$, see Fig. 6.12b. Fig. 6.12c and 6.12d are showing the current

flow and power consumption for both cases. The offset in bandgap output voltage V_{BG} between $V_{DD} = 1.2\,\text{V}$ and $1.8\,\text{V}$ is mainly caused by the change of R_{var} in order to achieve best temperature compensation for both supply voltages. This effect is discussed in section 4.1.



(a) $V_{DD} = 1.2\,\text{V}$ and $R_{var} = 500\,\Omega$

(b) $V_{DD} = 1.8\,\text{V}$ and $R_{var} \to \infty\,\Omega$

(c) $V_{DD} = 1.2\,\text{V}$ and $R_{var} = 500\,\Omega$

(d) $V_{DD} = 1.8\,\text{V}$ and $R_{var} \to \infty\,\Omega$

Figure 6.12: Bandgap measurement results in the range from −30 °C to 90 °C.

Table 6.3 summarizes the bandgap measurement results and compares cryogenic and RT performance. As the bandgap is aimed to be operated at deep cryogenic temperatures of ≈4 K and research to investigate the physical mechanisms leading to the kink at 35 K are currently ongoing (ref to Fig.6.11), parameters for the bandgap are calculated in the range of 7 K to 30 K. The large ΔV_{BG} at cryogenic temperatures originates from the lack of possibility to increase R_2, see previous discussions about Fig. 6.5, which is in strong contradiction to simulation results, due to the absence of valid cryogenic devices models (ref. to Fig. 4.4 and 4.5b). Future cryogenic bandgaps can be designed with this effect in mind and are expected to greatly improve on the temperature stability. This work is the first one to show a bandgap at deep cryogenic temperatures, which is not relying on bipolar [86, 88], MOS threshold [87, 88] or DTMOS devices [86], but is using P-N junction diodes for operation to the best of the author's knowledge.

6.3 Linear Regulator

The LR is planned to be operated in combination with the previously presented bandgap, see Fig. 4.1. The start-up procedure is described in detail in section 4.2 and the results of a start-up simulation are shown in Fig. 4.11. Using the proposed bandgap settings given in Table 6.2, the LR start-up is tested at 7 K. This setup requires the bandgap to be

		Cryo	RT	
Temp. range		7 K to 30 K	−30 °C to +90 °C	
V_{DD}	[V]	1.8	1.2	1.8
$\overline{V}_{BG}$	[mV]	400.2	369.1	238.5
ΔV_{BG}	[mV]	88.5	20.0	12.9
$\Delta V_{BG}/\Delta K$	[mV/K]	3.85	0.17	0.11
$\Delta V_{BG}/\Delta K/\overline{V}_{BG} \cdot 1 \times 10^6$	[ppm/K]	9620	460.6	461.2
Mean current $\overline{I}_{DD}$	[µA]	275.5	250.4	551.2
Mean power $\overline{P}_{DD}$	[µW]	496.1	300.6	992.2
Area	[mm^2]		0.010	

Table 6.3: Summary of bandgap measurement results.

powered by the output of the LR and therefore the supply select switch of the bandgap is set to the inverted state as for the bandgap only measurement case (ref. to Fig. 4.1). The input and supply voltage of the LR V_{IN} is set to 3 V.

The LR output is stabilized with an off-chip capacitance $C_{S,off} = 3.3\,\mu F$. The start-up procedure is measured with a Keysight MSOX4154A oscilloscope. Corresponding data for the LR output voltage V_{OUT} is plotted in Fig. 6.13. Compared to the simulated start-up (ref. to Fig. 4.11), timescales are much larger, which is solely caused by the limited speed of the digital SPI interface of the chip. First, the LR pull-down transistor M2, shown in Fig. 4.8, is in disabled configuration. This leads to a random voltage output and fluctuation until the LR is supplied with a defined reference voltage V_{REF}, which is generated by the V_{REF} R-string, shown in Fig. 4.7. Thus, the voltage is regulated and settles to $V_{OUT} = 1.72\,V$, which is a sufficient supply voltage level to start the bandgap. After the bandgap is started, the reference voltage V_{REF} is driven by the R-string and the bandgap simultaneously. This is done in order to avoid an undefined reference voltage level when switching from the R-string to the bandgap defined reference voltage. At last, the R-string is disabled and thus V_{REF} is only set by the bandgap reference. Additionally, the bias current for the LR error amplifier is also switched to the bandgap generated reference current $I_{REF,BG}$ (ref. to Fig. 4.8). The LR is biased in voltage and current domain solely by the internal bandgap reference for $t > 380\,ms$.

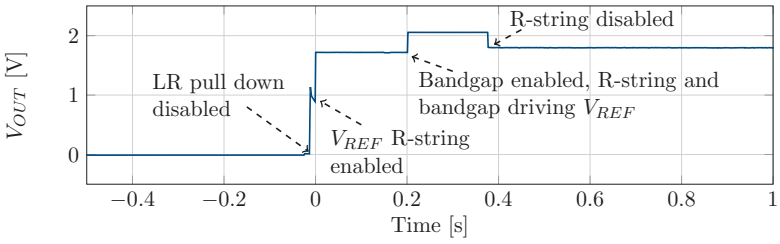


Figure 6.13: LR start-up at 7 K.

After the start-up sequence completed, the output voltage of the LR V_{OUT} can be controlled via the 8 bit bandgap reference setting register for the voltage V_{BG}, which is tuned by the current mirror bank as shown in Fig. 4.3. The measurement results of a V_{BG} sweep are plotted in Fig. 6.14. A lower limit for the output voltage exists at about 1.27 V, because the bandgap is supplied by V_{OUT} and will stop operating below that voltage, leading to V_{OUT} dropping to ≈0.8 V. The LR can only be recovered from that state by performing the start-up sequence again. Measurement is performed without any external load connected to V_{OUT}. However, a significant current flow I_{IN} was measured into the 3 V supplied input pad of the LR, which is additionally plotted in Fig. 6.14. A linear voltage dependence of I_{IN} to V_{OUT} is visible.

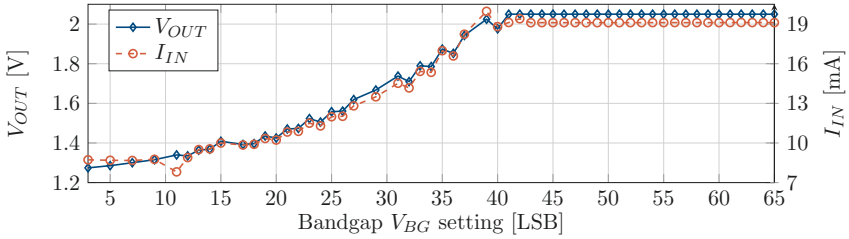


Figure 6.14: LR output voltage V_{OUT} and input current I_{IN} depending on bandgap reference voltage V_{BG} setting at 7 K.

In order to locate the cause for this voltage dependent current I_{IN}, both the LR and the bandgap are turned off. By disabling the LR and forcing the pass transistor M1 shut by pulling its gate to ground via M2 (ref. to Fig. 4.8), the nets of V_{IN} and V_{OUT} can be isolated from each other. Tested nodes are named according to Fig. 4.1. An external test voltage V_{Test} is swept on both nets individually, as well as shorted together, and the corresponding current flow I_{Test} is measured, see Fig. 6.15. Additionally, the digital supply voltage V_{DIG} is raised from nominal 1.2 V to 1.7 V in order to check for dependencies to the digital domain. This results in a unchanged current flow I_{Test} for all cases, negating any impact of the digital domain. For this test all connected blocks are always powered down. Connecting or disconnecting the bandgap is also possible via the supply select switch, which can be set to open for both possible supplies (ref. to Fig. 4.1). This gives an option to determine if an undesired current flow, even in powered down state, is occurring inside the bandgap. Measurement results show no indication of such an undesired current existing, as disconnecting the bandgap supply does not lead to a noticeable change in I_{Test}. Thus, the bandgap reference can be ruled out as cause for the significant current flow seen in Fig. 6.14. Furthermore, the LR with its biasing network and error amplifier can be excluded as possible origin, because the measured current flow of ≈3 µA at the V_{IN} node is well below the measured current flow I_{IN}. If the level shifters at the interface to the digital domain are the reason for the large current flow of I_{IN}, a change in digital supply voltage should lead to an altered current flow. This is not the case. The good agreement of the test current I_{Test} at the V_{OUT} node compared to I_{IN} as well as the output voltage dependency of I_{IN} strongly indicate the cause of the large current flow, as seen in Fig. 6.14, to be originating on the V_{OUT} node side of the LR.

The bandgap as current sink is already excluded and also the feedback R-String with its total resistance of $12 \cdot 7\,\text{k}\Omega = 84\,\text{k}\Omega$ will not explain a current in the mA range. The

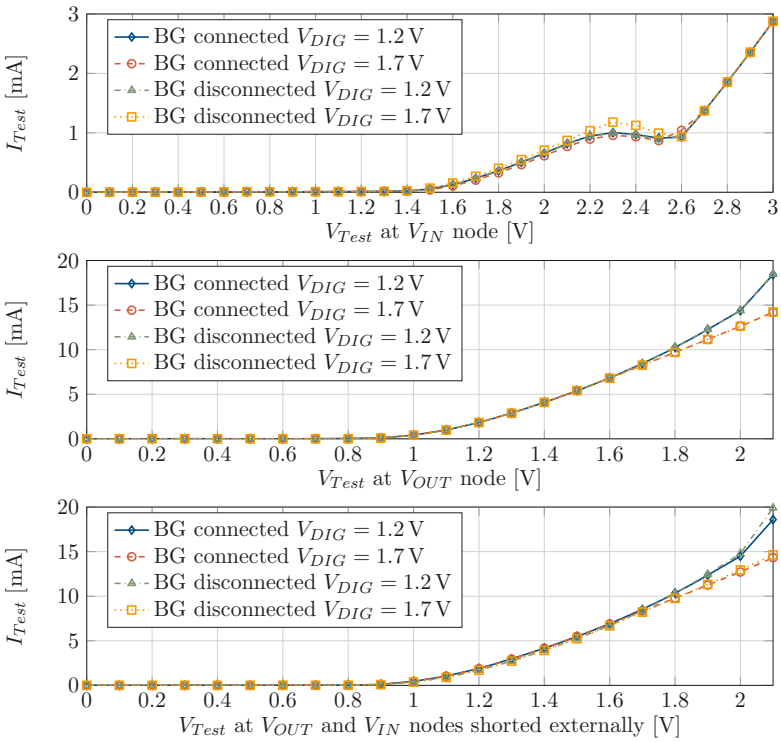


Figure 6.15: Measured current flow I_{Test} for applied test voltage V_{Test} at 7 K.

linear dependence of the current I_{IN} to V_{OUT} cannot be explained by an ESD diode, e.g. of a pad, and can be excluded as well. In order to exclude current flows occurring between both nodes of V_{IN} and V_{OUT}, those were shorted externally, but revealed no change in current flow compared to applying V_{Test} to the V_{OUT} node alone. Thus, currents between both nodes can also be ruled out as possible cause. Therefore, it is concluded that the cause for the most part of the current flow seen for I_{IN} is most likely into one of the on-chip circuit blocks (excluding the bandgap) following the LR, which are also powered by V_{OUT} as supply voltage. In the following, the current as measured in Fig. 6.15 for the V_{OUT} node is assumed as load current I_L for the LR.

A transient test of the LR for varying load currents and output voltages has been performed. Results for the output voltage V_{OUT} of the LR and the calculated corresponding load current I_L are plotted in Fig. 6.16, assuming a correlation of V_{OUT} and I_L as described in the previous paragraph. Load current I_L is calculated by linear interpolation of the V_{OUT} node data (middle graph) shown in Fig. 6.15 for a disconnected bandgap reference and digital supply V_{DIG} at nominal 1.2 V. The LR is able to generate output voltages V_{OUT} in the range of about 1.27 V to 2.05 V and corresponding load currents I_L of 2.6 mA to 16.5 mA while being biased solely by the bandgap reference, i.e. reference voltage V_{REF} and bias current I_{BIAS}, at a cryogenic temperature of 7 K.

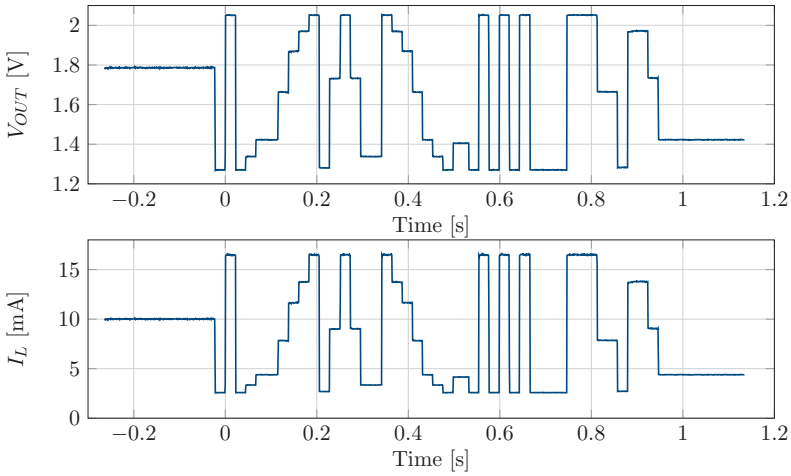


Figure 6.16: LR measurement of varied load current I_L and output voltage V_{OUT} at 7 K.

6.4 OpAmp and Unity Gain Buffer

For measurement of the Bias-DAC and the auxiliary measurement circuitry, a second PCB for the cryogenic measurements has been designed, which differs to the prior one used for the characterization of the LR and bandgap, see Fig. 6.2. The backplate of the PCB is again manufactured with electroless nickel gold and ground via stitching, in order to achieve a good thermal anchoring of the sample. Fig. 6.17 depicts the setup with this PCB and the second IC as DUT. The new PCB is designed with the same dimensions as

the previous one, in order to fit on the same mechanical copper plate PCB holder. The prototype chip is named “SQuBiC1”, which is an IC designed for *Scalable QUbit Control* research activities at the ZEA-2 institute.

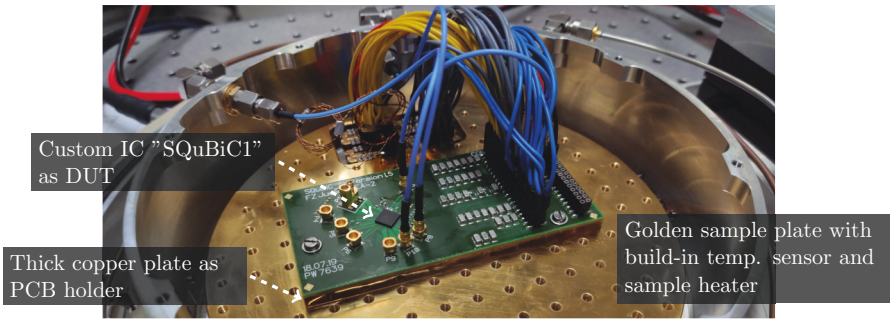


Figure 6.17: Amplifier measurement setup inside the cryostat.

Looking at the die photograph presented in Fig. 6.18, the three amplifiers are placed at the top left corner of the chip and take up a total area of 0.032 mm^2. The current mirror banks, which set individual bias currents for each OpAmp in the amplifiers, ΣΔ modulator and window comparator, are all gathered in one place: near the input pad of the single external fed bias current for better matching properties. This placement is leading to a distribution of currents rather than voltages over the chip, which is less susceptible to parasitic effects. Fig. 6.18 also shows all other blocks, which are measured (with the exception of the I^{2}C) and are presented later in this chapter.

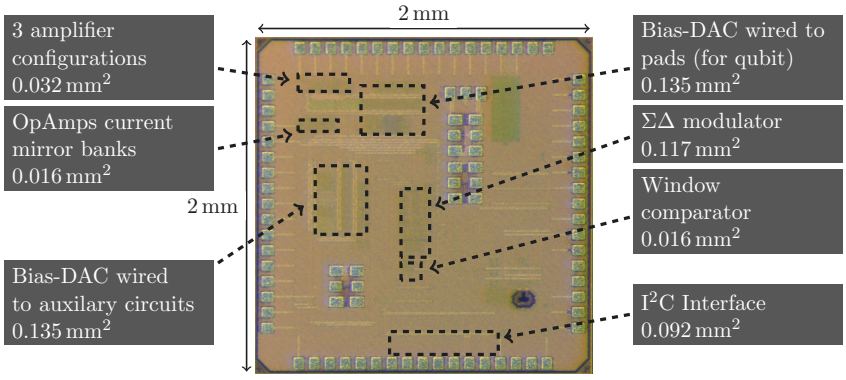


Figure 6.18: Die photograph of prototype chip SQuBiC1.

The open loop gain for the amplifier is measured at RT and at 6 K. Typically, open-loop gain is measured by usage of an auxiliary OpAmp. This setup is complicated in the scenario of a cryostat measurement, which requires long cabling or cryogenic OpAmps with a high gain. Therefore, the OpAmp gain is measured by sweeping the input voltage of the OpAmp while maintaining a stable reference voltage and deriving the slope of the output transition from low to high. The measured gain of 70 dB is in good accordance with simulation results (ref. to section 5.5.1) and multiple steps are measured in the OpAmp

transition, providing a reliable measurement of the transition slope. Measurement results are plotted in Fig. 6.19. The open-loop gain is then calculated by the slope $S = \frac{\Delta V_{OUT}}{\Delta V_{IN}}$ and converted to dB by $A_{OL} = 20 \cdot \log(S)$.

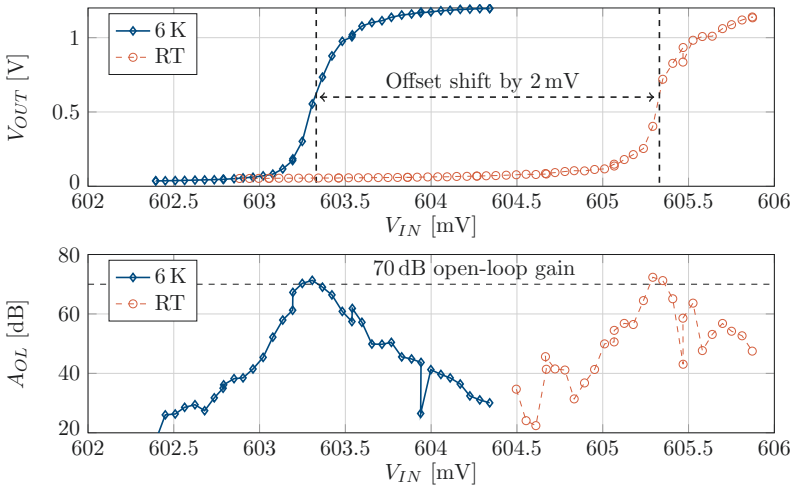


Figure 6.19: Measurement of amplifier output voltage V_{OUT} and open-loop gain A_{OL} for swept input voltage V_{IN} and $V_{REF} = 600\,\text{mV}$.

The maximum measured gain for RT and 6 K is 71.31 dB and 72.34 dB, respectively. The measured offset voltage shift of about 2 mV is still in the range of process and mismatch variations. However, when operating the OpAmp in unity gain buffer configuration, a clipping is apparent for input voltages $\gtrapprox 700\,\text{mV}$. Corresponding measurement results are plotted in Fig. 6.20. This behavior is explained by the input CM voltage of the OpAmp increasing above the threshold voltage of the input PMOS pair M3 and M4 in Fig. 5.16 and by the steep subthreshold slope at cryogenic temperatures, which is rendering an operation in moderate or weak inversion unfeasible. A supply voltage increase by ΔV_{DD} shifts the point of clipping voltage level by the same upwards. Thus, a supply voltage increase of ΔV_{DD} enables OpAmp functionality in the desired voltage range of 0 V to 1.2 V. This is validated by a measurement, which is also plotted in Fig. 6.20. A functional operation of the OpAmp in the input voltage range of 0 V to 1.2 V is guaranteed if the supply voltage is increased by 500 mV to 1.7 V.

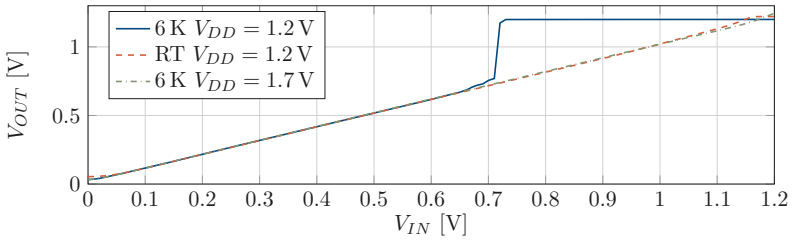


Figure 6.20: Unity gain buffer output clipping to V_{DD} for input CM > 0.7 V at 6 K.

The measured UGB, which is defined as the frequency with a unity gain A_{Unity} reduction of −3 dB, is plotted in Fig. 6.21. Measurements are done by applying a 100 mV peak-to-peak sinusoidal voltage with a swept input frequency f_{IN}. The DC input level is set to 500 mV. Reference current input is set to nominal 25 µA and the current mirror bank is programmed to output 10 µA bias current for the OpAmp, which is the nominal bias current for the OpAmp design. In order to force the same external reference current flow into the diode connected MOSFET of the current mirror bank, the required voltage shifted from 650 mV at RT up to 800 mV at 6 K. This effect is matching the expected threshold voltage increase.

If the nominal supply voltage $V_{DD} = 1.2$ V is applied, a slight degradation in UGB from RT to 6 K of about 375 kHz − 410 kHz = −35 kHz is noticeable. However, a supply voltage increase is yielding to an overcompensation effect at 6 K of 525 kHz − 375 kHz = +150 kHz compared to RT, which only increases by 460 kHz − 410 kHz = +50 kHz at $V_{DD} = 1.7$ V. On the one hand, this indicates the potential gain in performance at cryogenic temperatures due to the higher carrier mobility, see section 2.4.1. On the other hand, in order to revert the initial performance loss of −35 kHz to a performance gain of 525 kHz − 460 kHz = +65 kHz a higher supply voltage is required in order to compensate for the threshold voltage increase at cryogenic temperatures. The UGB is low due to large capacitive load of the long cabling to and inside the cryostat. No oscillation for the OpAmp is detected in any measurement and is also indicated by the flat A_{Unity} curve. The curve does not cross above 0 dB before the UGB is reached and A_{Unity} starts to decrease.

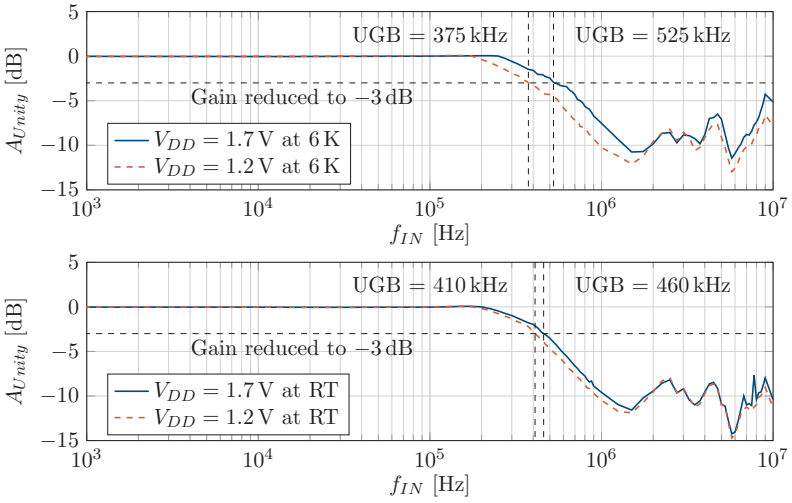
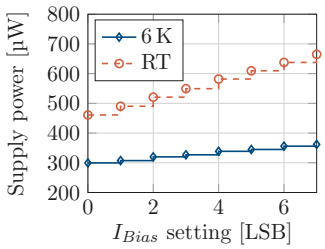


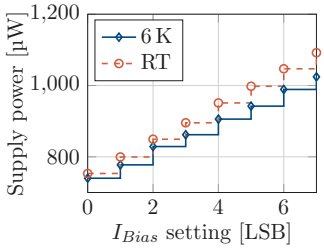
Figure 6.21: UGB measured for $V_{DD} = 1.2$ V and $V_{DD} = 1.7$ V at 6 K and at RT.

As pad number limitations do not allow for a separate OpAmp supply connection, it is not possible to measure the individual OpAmp power consumption directly. Fig. 6.22 shows the total supply net power consumption for each bias current setting of the current mirror bank for the amplifier under test. This also includes power consumption of multiple other blocks, which are tied to the same supply net and draw additional power. Fig. 6.22a shows the supply net power consumption for $V_{DD} = 1.2$ V. A decrease of power at 6 K

compared to RT is visible, which can be explained by a decrease in leakage currents and circuits being operated with less voltage headroom due to an increased threshold voltage. The increase in power consumption for consecutive bias current settings is reduced at 6 K at $V_{DD} = 1.2\,\text{V}$, which can also be reasoned by the reduced voltage headroom. However, by giving the circuitry enough headroom to operate as desired even with an increased threshold voltage, i.e. by raising the supply voltage to $V_{DD} = 1.7\,\text{V}$, the power consumption and the increase for each bias setting step at 6 K is leveling again with the RT one. The difference in power consumption increase for bigger I_{Bias} settings indicates again a correlation to reduced voltage headroom at cryogenic temperatures. A deterioration of transistor mismatch, as described in section 2.4.1, imposes less of an issue for the OpAmp biasing.



(a) Supply power for $V_{DD} = 1.2\,\text{V}$.



(b) Supply power for $V_{DD} = 1.7\,\text{V}$.

Figure 6.22: Measured power consumption for the complete supply net connected to the amplifier under test.

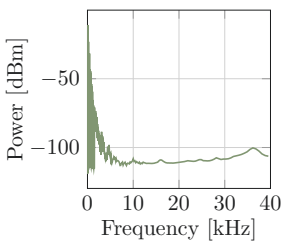
From the changes in the power consumption at different bias current settings, the power consumption of the individual amplifier block, i.e. one OpAmp, can be deducted. One assumption to be made here is the power consumption of the unity gain buffer for its always-on bias current of 2 µA, which is present for I_{Bias} setting = 0. Each bias level increase results in a 2 µA larger bias current, thus it is assumed that the first always-on current power consumption can be approximated by the mean value of all power jumps. The calculated power consumption at the highest biasing setting, alongside other characteristics, of the unity gain buffer is given in Table 6.4.

		6 K		≈300 K	
V_{DD}	[V]	1.2	1.7	1.2	1.7
Power	[µW]	71	325	233	387
A_{OL}	[dB]	≈ 71		≈ 72	
UGB	[kHz]	375	525	410	460
Max. output voltage	[V]	0.7	1.2	1.2	1.7
Area	[mm^2]	0.005			

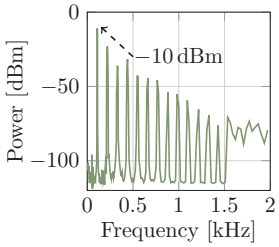
Table 6.4: Summary of unity gain buffer measurement results.

6.5 ΣΔ Modulator

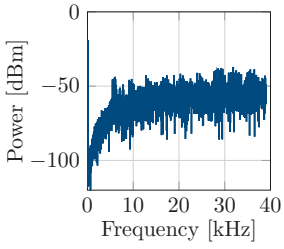
The second part of the auxiliary measurement is the ΣΔ modulator, which includes the window comparator (WC). Measurement results of the WC are given in section 6.5.1. Fig. 6.23 shows the unfiltered ΣΔ modulator output spectrum for second and third-order modulation at cryogenic temperatures of 6 K. Because the ΣΔ modulator integrator stages and comparators are build with the same OpAmp as is used for the unity gain buffer, the supply voltage is increased for all of the following measurements to 1.7 V in order to mitigate cryogenic effects (ref. to Fig. 6.20). The input signal is a 110 Hz sinusoidal voltage with an amplitude of 500 mV and a DC offset of +600 mV, which is generated by a Keysight 33600A waveform generator. The input voltage noise is measured with a Keysight signal source analyzer E5052B (SSA). The typical noise shaping behavior is visible for all plotted spectrums.



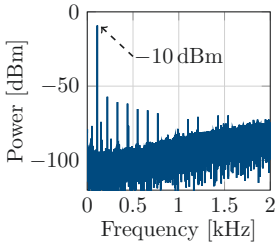
(a) Spectrum of input voltage.



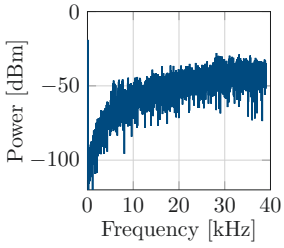
(b) Zoom-in of Fig. 6.23a.



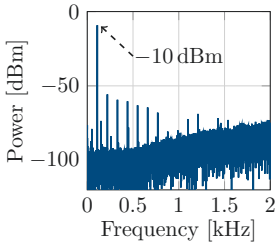
(c) 2nd-order ΣΔ modulator spectrum.



(d) Zoom-in of Fig. 6.23c.



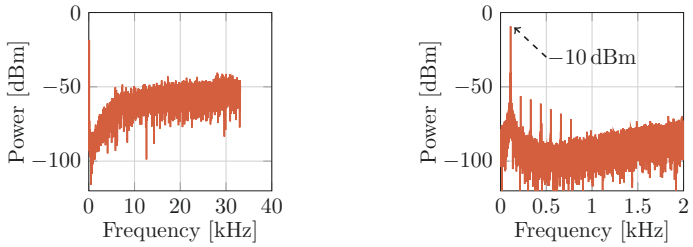
(e) 3rd-order ΣΔ modulator spectrum.



(f) Zoom-in of Fig. 6.23e.

Figure 6.23: Spectrum of input voltage and unfiltered ΣΔ modulator output at 6 K.

Comparing these cryogenic measurement results to RT results, which are plotted in Fig. 6.24, a better noise performance at 6 K becomes apparent, especially around the signal frequency of 110 Hz.



(a) 2nd-order ΣΔ modulator spectrum.

(b) Zoom-in of Fig. 6.24a.

Figure 6.24: Unfiltered ΣΔ modulator output spectrum at RT.

The ΣΔ modulator has been designed to measure the DC output level of the Bias-DAC and provides on-chip digital-to-analog conversion. The modulator output bitstream is digitally filtered at RT, by averaging all bitstream values over the period of 5 s and multiplying with the supply voltage value. A sweep of the input voltage $V_{IN,\Sigma\Delta}$ shows stable operation for the whole desired input range with the exception of voltages $\lessapprox 50$ mV, which is due to OpAmp limitations, see Fig. 6.20. This issue can be circumvented by starting the Bias-DAC output voltage at 50 mV instead of 0 V and is a valid approach for the Bias-DAC measurement. This approach will be discussed later in section 6.6 for the Bias-DAC measurement via the on-chip unity gain buffer. Results of the input voltage sweep of the ΣΔ modulator are plotted in Fig. 6.25

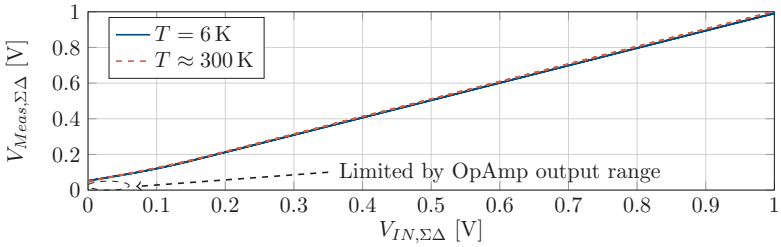


Figure 6.25: DC input voltage sweep $V_{IN,\Sigma\Delta}$ measured via ΣΔ modulator at 6 K.

A zoom into Fig. 6.25 is given in Fig. 6.26. The input voltage $V_{IN,\Sigma\Delta}$ source (Keysight N6761A precision autoranging power module) is programmed to output equal steps of 100 µV, which appears to be close to the limit of the device in terms of accuracy as some voltage steps are visibly larger or smaller. A 50 µV step of $V_{IN,\Sigma\Delta}$ is marked in Fig. 6.26, which is still detectable via the ΣΔ modulator at RT and cryogenic temperatures of 6 K. Some signals are shifted by +x mV x $\in \{0, 5, 12\}$ numerically in order to fit all curves into the same plot. The added numerical shift is about equal to the offset between the curves. Thus, the ΣΔ modulator exhibits an offset of 12 mV at RT which reduces to 5 mV at 6 K. However, constant offsets can be easily subtracted and pose no issue to the performance of the ΣΔ modulator.

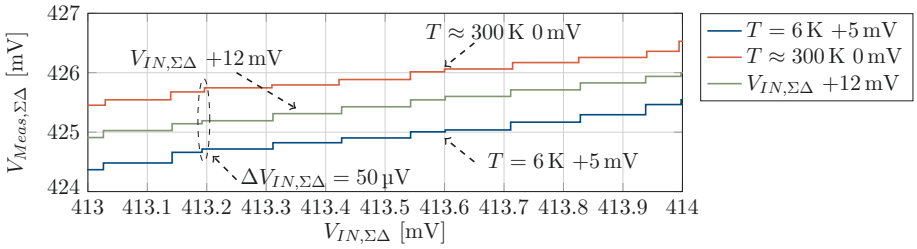


Figure 6.26: Zoom-in on measurements of Fig. 6.25 at 6 K. Signals are shifted by +x mV x ∈ {0, 5, 12} to fit inside the plot.

Power consumption is in the range of about 1 mW. This measurement results show that a ΣΔ modulator, which is to be operated at deep croygenic temperatures, is a promising candidate for later Bias-DAC calibration, which is discussed in more detail in chapter 7.

6.5.1 Window Comparator

The window comparator is verified to be functional at 6 K. The external reference voltages $V_{WC,1}$ and $V_{WC,2}$ were set to 620 mV and 600 mV, respectively. The changing input voltage V_{IN} is crossing both voltages, as is shown in Fig. 6.27. After the measurement finished, all 4 on-chip counters are read-out via the I^2C interface, see Table 6.5. The correct number of crossing for each window limit and the corresponding crossing direction has been counted. This allows to check if the ΣΔ modulator input voltage is drifting while an analog-to-digital conversion is taking place, even at deep cryogenic temperatures.

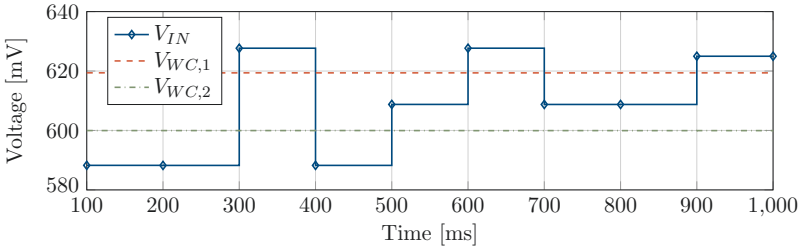


Figure 6.27: Window comparator functional at 6 K.

	No. of detected upwards crossings	No. of detected downwards crossings
Counter WC,1	3	2
Counter WC,2	2	1

Table 6.5: Read counter values after measurement (Fig 6.27).

6.6 Bias-DAC

The Bias-DAC is the one block in this work that is designed to be operated at the lowest temperature stage of a dilution refrigerator alongside and simultaneously with a qubit. Therefore, the Bias-DAC is required to strictly abide by the power limit of $< 1\,\text{mW}$ in order to avoid disturbance of the qubit operation. Other blocks are not so tightly bound to the power limit, because they are planned to be either placed on a higher temperature stage (LR and bandgap) or are only used for verification use cases (amplifier and $\Sigma\Delta$ modulator). At best, the Bias-DAC power consumption is kept below $400\,\mu\text{W}$, which is the typical cooling power of contemporary commercially available dilution refrigerators at 100 mK [125].

For noise measurements the exact voltage amplitude of the refresh ripple is to be measured (ref. to Fig. 3.4). Due to an unknown load, it is not valid to measure the noise power and calculate the corresponding voltage from that result. In order to drive the $50\,\Omega$ impedance of the measurement equipment a commercially available cryogenic buffer amplifier is placed inside the cryostat, i.e. a Stahl-Electronics Cryogenic CMOS Buffer Amplifier BUF 0.12 [126]. Fig. 6.28 shows the setup inside the cryostat with the already known PCB (ref. to Fig. 6.4) alongside the BUF 0.12. The BUF 0.12 will become relevant later in this section.

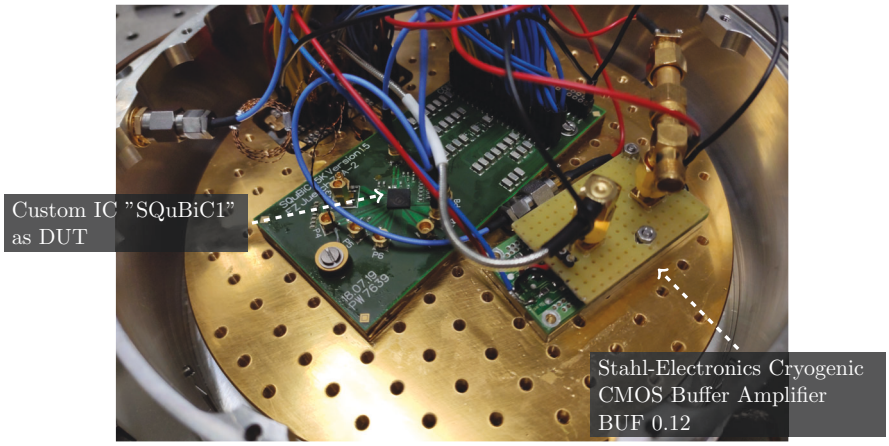


Figure 6.28: Bias-DAC measurement setup inside cryostat.

The Bias-DAC is verified by usage of the on-chip unity gain buffer amplifier, see section 6.4. The BUF 0.12 is not used in this measurement. The input word Z_{IN} (ref. to Fig. 5.8) is here described by the removal of the 3 MSBs, which select the $V_{REF,U}$ level, as those are all always equal to the next lesser 3 bit, which select the $V_{REF,L}$ level. This leads to a constant reference voltage difference of $\Delta V_{REF} = 125\,\text{mV}$ (ref. to Fig. 5.7). Results are plotted in Fig. 6.29. The measurement is limited by the finite output voltage range of the unity gain buffer for voltages $< 30\,\text{mV}$ (ref. to Fig. 6.20). In section 5.3 the voltage jumps V_{jump} (ref to Fig. 5.9) induced by the voltage coarse tuning in the presence of parasitic capacitance have been discussed. V_{jump} is visible in Fig. 6.29 at all points where the 125 mV reference voltage coarse tuning is changing and is about $V_{jump} \approx 7\,\text{mV}$.

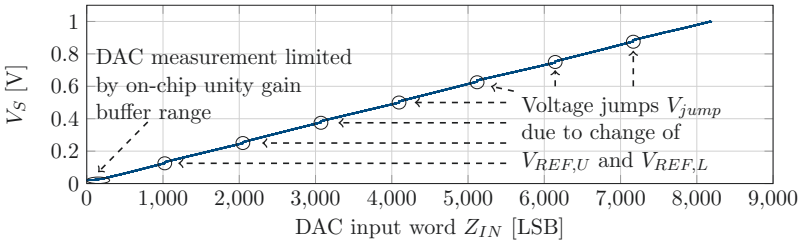


Figure 6.29: Bias-DAC measured via on-chip unity gain buffer at 6 K.

A zoomed plot of a coarse tuning switch is given in Fig. 6.30. The usage of a mitigation technique is verified by measurement, i.e. adding intermediate steps between two coarse tuning regions, which is presented in Fig. 5.11. Upon closer inspection, also the doubled step size for the intermediate steps range are noticeable. The calibration algorithm is described in section 5.3 and depicted in Fig. 5.11. Once the calibration is finished, the according start and end values of each intermediate step ranges are saved in an off-chip lookup table. This lookup table is implemented in such a way that the additional intermediate steps from the calibration are added to the original $Z_{IN} = 2^{13} = 8192$ in a continues matter.

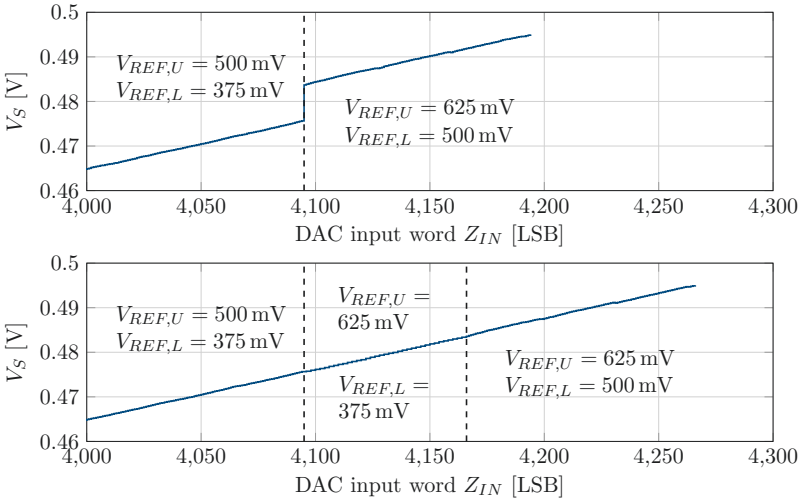


Figure 6.30: Introduction of intermediate steps between two coarse tuning regions by operating the Bias-DAC with a doubled reference voltage difference ΔV_{REF} = 250 mV at 6 K.

The lookup table for Z_{IN} with intermediate steps is visualized in Fig. 6.31 and shows the corresponding bits which are programmed into SQuBiC1, i.e. 3 bit for V_{REF_U}, 3 bit for V_{REF_L} and 10 bit for the charge-redistribution DAC. Z_{IN} is increased continuously, but for the intermediate steps range the Bias-DAC configuration bits are repeated twice. This is done in order to correct the DAC slope in the intermediate steps range, which is due to the doubled step size of the intermediate steps.

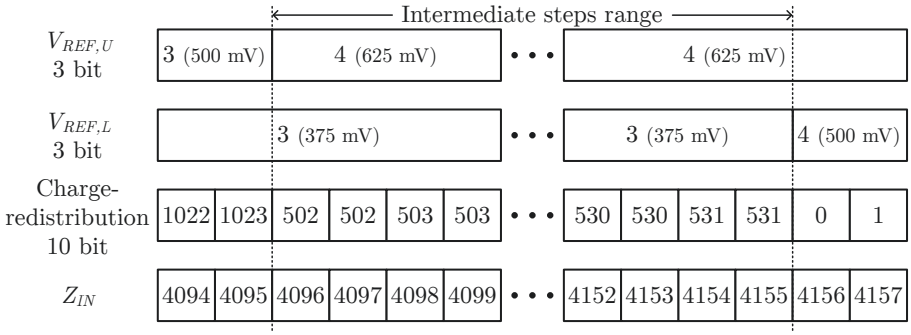


Figure 6.31: Added intermediate steps in lookup table.

With the intermediate steps added for all coarse tuning transitions, all voltage jumps V_{jumps} can be removed, see Fig. 6.32. Also the maximum number of Z_{IN} increased from 8191 to 8618, because of the added intermediate steps.

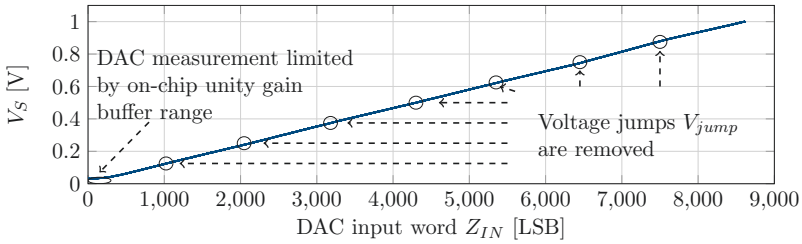


Figure 6.32: All V_{jump} occurrences removed by addition of intermediate steps between coarse tuning transitions at 6 K.

The limited OpAmp output range can be circumvented by raising all reference voltages of the Bias-DAC by 50 mV, see Fig. 6.33. This allows for a measurement of the differential non-linearity (DNL) of the Bias-DAC, because the whole DAC output range can be measured. The Bias-DAC output and its corresponding DNL is measured at 6 K and RT. The RT DNL is comparable or slightly worse than at 6 K. The difference between RT and cryogenic Bias-DAC output for voltages $\gtrapprox 0.8$ V is attributed to the Bias-DAC as the unity gain buffer transfer characteristic is well behaved at cryogenic temperatures and at RT, see Fig. 6.33. A change in the resistivity of the MOSFET switches due to temperature difference is a possible explanation for this behavior.

For measurement of the voltage ripple of the Bias-DAC (ref. to Fig. 3.4), the need for a cryogenic buffer amplifier (ref. to Fig. 6.28), which is able to drive the 50 Ω input of measurement equipment is indicated at the beginning of this section 6.6. Table 6.6 summarizes the most important characteristics of the used BUF 0.12 device. One important characteristic is the output impedance of the BUF 0.12 being 150 Ω instead of the typical 50 Ω used for measurement equipment. Thus, a voltage division by 4 is expected when using the BUF 0.12 to drive the SSA AC coupled baseband noise input port, which is used to measure the Bias-DAC ripple in the frequency range of 10 Hz to 100 MHz.

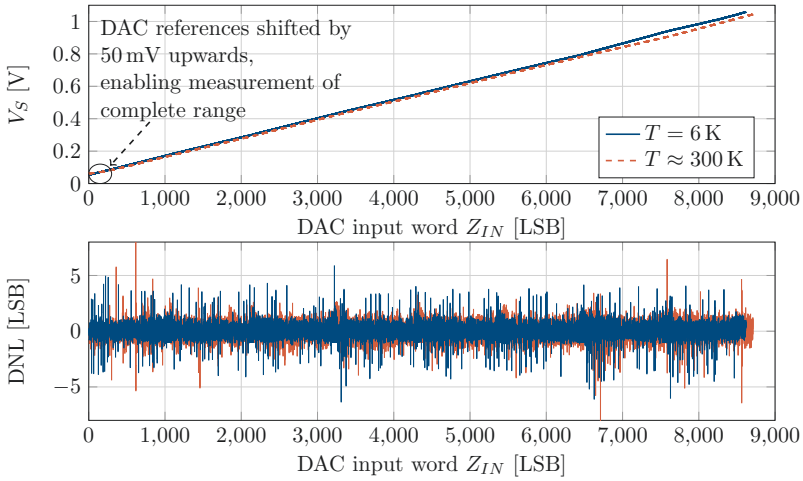


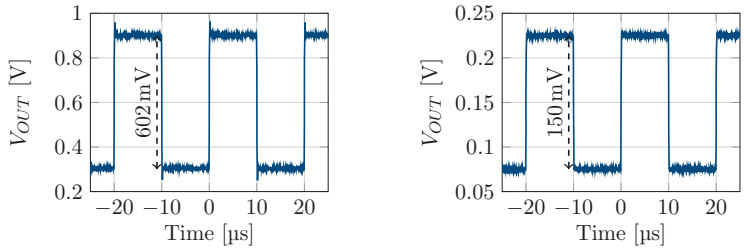
Figure 6.33: Bias-DAC DNL (output via unity gain buffer) at 6 K. Legend applies to both graphs.

	Min	Max
Temp	4.2 K	300 K
Power	29 mW	
Freq.	DC	120 kHz
Freq. 6 dB roll-off	10 MHz	
Offset	typ. ±200 µV	±500 µV
Input impedance	> 100 MΩ	
Input capacitance	12 pF	
Input noise	10 nV/$\sqrt{\mathrm{Hz}}$	
Output impedance	150 Ω	

Table 6.6: Characteristics of Stahl-Electronics Cryogenic CMOS Buffer Amplifier BUF 0.12 [126].

The division-by-4 factor is checked by applying a 50 kHz square wave to the input of the BUF 0.12 and measuring its output voltage V_{OUT} by a Keysight MSOX4154A oscilloscope. The input resistance $R_{IN,OSC}$ of the oscilloscope is switched between 1 MΩ and 50 Ω. Results are shown in Fig. 6.34. The expected division by 4 is visible by comparing the amplitudes for the two $R_{IN,OSC}$ values. The amplitude is reduced from 602 mV to 150 mV. Moreover, the upper and lower voltage of the square wave decrease from 902 mV to 225 mV and from 300 mV to 75 mV, respectively. This verifies the effect of the voltage divider as it is expected from the BUF 0.12 data sheet.

Considering the previously discussed voltage divider between the BUF 0.12 output and the 50 Ω SSA input, the Bias-DAC ripple is measured and results are presented in the



(a) $R_{IN,OSC} = 1\,\mathrm{M\Omega}$. (b) $R_{IN,OSC} = 50\,\Omega$.

Figure 6.34: Measured effect of BUF 0.12 150 Ω output impedance.

following part. Directly connecting the Bias-DAC output to the BUF 0.12 is not possible, because the Bias-DAC is designed to counteract leakage currents of pA. Thus, the Bias-DAC cannot drive the BUF 0.12 input resistance reliable. Therefore, a chain of two buffer amplifier is required to gradually increase the driving capability to the the required 50 Ω of the SSA. Fig. 6.35 depicts this measurement setup and indicates the corresponding maximum output current range below each block. Starting from the Bias-DAC, which is designed to drive pA, the signal is applied to the on-chip unity gain buffer, increasing the driving capability to the range of µA. Sequentially, the on-chip buffer is driving the input of the BUF 0.12 buffer, which is able to source the signal into the SSA.

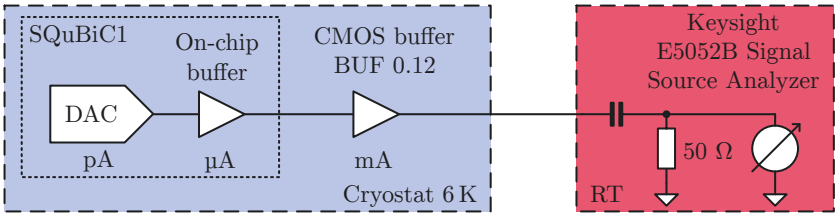


Figure 6.35: Buffer chain enabling Bias-DAC measurement into 50 Ω port.

In order to account for the voltage divider, the measured voltage noise spectral density v_n must be multiplied by a factor 4 for all signals passing the BUF 0.12 device. Results are plotted in Fig. 6.36. Naturally, the noise power increases for each added buffer stage. The roll-off is happening for the on-chip buffer at ≈2 MHz.

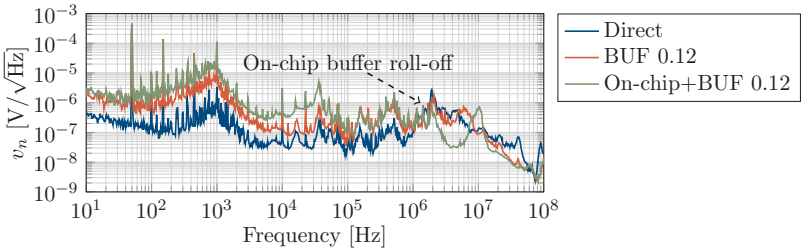


Figure 6.36: Noise measurement of buffer chain at 6 K.

For all following results of Bias-DAC measurements, all eight output channels are operating simultaneously and set to random voltage levels across the DAC range, although only one DAC channel is being measured. The voltage levels are unchanged while a measurement is running, because this is according to the use case of generating constant bias voltages for the qubit. The Bias-DAC performance operating at a high channel refresh rate $f_R = 765\,\text{kHz}$, see (3.6), is measured via the BC and is plotted in Fig. 6.37. The lower frequency noise $< 3\,\text{kHz}$ is dominated by the BC noise. The reference voltage V_{REF} noise is suppressed at higher frequencies by the 220 nF capacitance placed on the PCB for each supply and reference voltage. The refresh spur of f_R is visible in the spectrum and is marked.

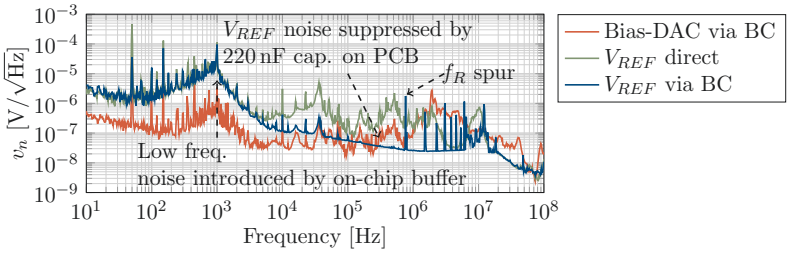


Figure 6.37: Noise spectral density of Bias-DAC with $f_R = 765\,\text{kHz}$ at 6 K.

In order to find the optimum refresh frequency f_R in terms of noise and power, the voltage noise spectral density v_n is squared and integrated over the whole measured frequency range of 10 Hz to 100 MHz. The root mean square voltage v_{RMS} is calculated by taking the square root of the integral:

$$v_{RMS} = \sqrt{\int_{10\,\text{Hz}}^{100\,\text{MHz}} v_n^2(f)\,\mathrm{d}f} \tag{6.1}$$

This is done for the charge-redistribution DAC being set to its LSB value $Z_{CR} = 1$, its MSB value $Z_{CR} = 512$ and a random value $Z_{CR} = 928$, in order to check for dependencies to the input word. However, all three DAC input words behave similar and show only negligible differences.

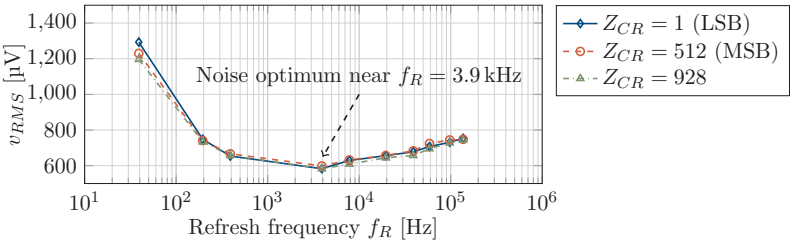


Figure 6.38: Total integrated noise of whole spectrum from 10 Hz to 100 MHz depending on refresh frequency f_R.

The total power consumption of the Bias-DAC including clock buffer is presented in Fig. 6.39. The power at the optimum noise point is about 26 µW and reduces to ≈8 µW

at f_R = 39 Hz, but this comes at the cost of an increased noise level. As a total power consumption of 26 µW is already well below the power limit of 400 µW, which is the cooling budget of a contemporary commercially available cryostat at 100 mK, we propose operating the Bias-DAC in the optimum noise point. This also fulfills the power requirements as they have been concluded from discussions with the qubit research group of Prof. Bluhm at RWTH Aachen University, which set a power limit of < 1 mW (ref. to Table 3.1). The optimum noise point in Fig. 6.39 is found to be at f_R = 3.9 kHz.

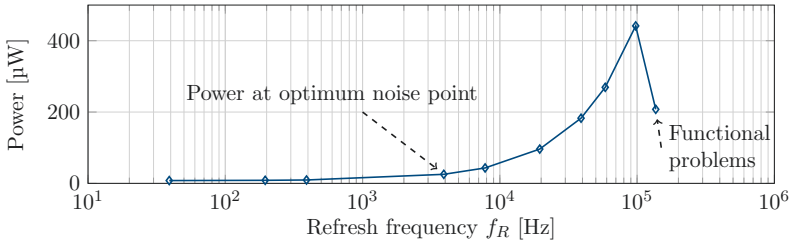


Figure 6.39: Total Bias-DAC power consumption depending on refresh frequency f_R.

The Bias-DAC voltage noise spectral density at the optimum noise point f_R = 3.9 kHz is plotted alongside one reference voltage V_{REF} in Fig. 6.40. The channel refresh spur is visible at f_R = 3.9 kHz, spurs at frequencies > 7.8 kHz are considered harmonics of the refresh spur.

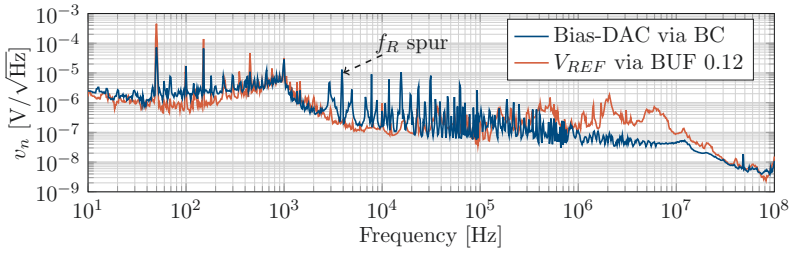


Figure 6.40: Noise measurement of Bias-DAC with f_R = 3.9 kHz at 6 K.

In order to understand which noise is contributing the most to v_{RMS}, the voltage noise spectral density v_n is integrated between f_{min} and f_{max}:

$$v_{RMS,fmax} = \sqrt{\int_{f_{min}}^{f_{max}} v_n^2(f)\,\mathrm{d}f} \tag{6.2}$$

Setting the lower frequency limit to f_{min} = 10 Hz, $v_{RMS,fmax}$ can be plotted depending on f_{max}, see Fig. 6.41. Because the noise above 10 MHz is far off the refresh spur and its harmonics, f_{max} is swept from f_{min} to 10 MHz. Furthermore, measurements results of the BC bandwidth reveal a roll-off at ≈2 MHz (ref. to Fig. 6.36).

Fig. 6.41 shows a significant impact of the 50 Hz power grid spur and its harmonics to the overall noise v_{RMS}. Furthermore, a spur at 1 kHz is present for both the Bias-DAC and the reference voltage. Therefore, a reasonable lower frequency limit for the region

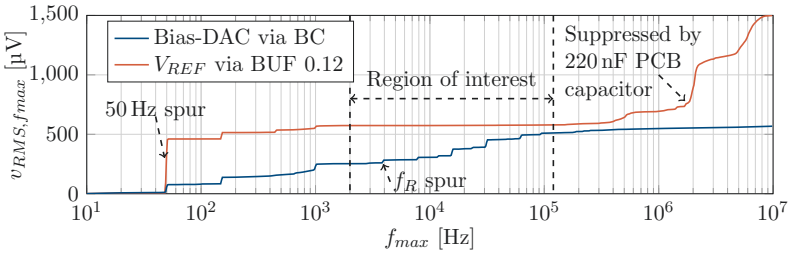


Figure 6.41: Cumulative summed noise of Bias-DAC with f_R = 3.9 kHz at 6 K.

of interest is set to 2 kHz. For higher frequencies the 220 nF capacitance on the PCB removes the reference voltage noise and has little impact to the Bias-DAC noise. Thus, an upper frequency limit to the region of interest is set to 120 kHz, which is also the upper frequency limit for the BUF 0.12 (ref. to Table 6.6). $v_{RMS,fmax}$ in the region of interest can be calculated from v_n by setting f_{min} = 2 kHz, which is presented in Fig. 6.42.

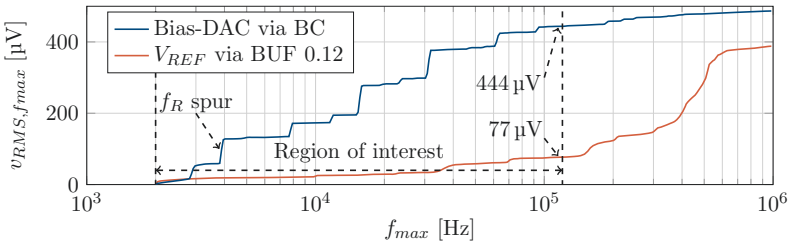


Figure 6.42: Cumulative summed noise of Bias-DAC with f_R = 3.9 kHz and f_{min} = 2 kHz at 6 K.

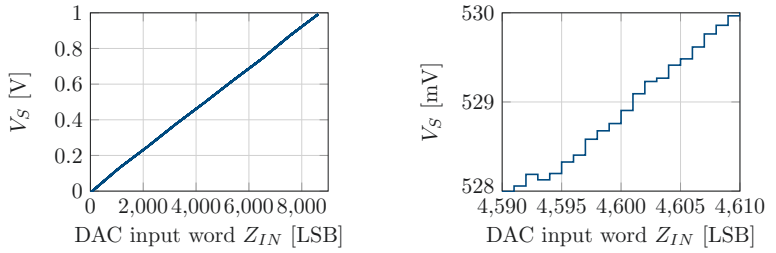
The total integrated noise $v_{RMS,fmax}$ for the reference voltage and Bias-DAC at f_{max} = 120 kHz is 77 µV and 444 µV, respectively. Assuming the reference voltage noise is also present in the Bias-DAC output voltage and the Bias-DAC noise is added as uncorrelated noise, the Bias-DAC adds a total noise of

$$v_{RMS,DAC} = \sqrt{(444\,\mu V)^2 - (77\,\mu V)^2} = 437\,\mu V \tag{6.3}$$

The assumption of uncorrelated noise is valid, because the Bias-DAC noise is dominated by the refresh ripple (ref. to Fig. 3.4) and its corresponding harmonics, which are independent of any reference voltage noise. Further experiments will show the impact of the Bias-DAC generated noise to qubit fidelity rates. Effort is currently undertaken to perform such an experiment and an outlook to this is given in chapter 7. However, even with diminished qubit fidelity rates a locally generated qubit biasing is valuable in order to pave the way for future scalable control electronics.

The Bias-DAC is verified working at the lowered refresh frequency f_R = 3.9 kHz by measuring its output voltage V_S over the complete range of Z_{IN}. The Bias-DAC can be measured directly without the need for any buffer by setting the Keysight 34470A digital multimeter to a high-z input resistance of > 10 GΩ. Fig. 6.43 shows the results

of this measurement. The Bias-DAC behaves well over the whole output range, see Fig. 6.43a. Upon closer inspection of the output voltage, some single non-monotonic steps are noticeable. However, as the Bias-DAC is for the vast majority monotonic and non-monotonic steps are singular, no downside for the qubit operation will arise as they are detectable when fine-tuning the quantum dot of GaAs qubits. This has been reviewed and checked together with the qubit research group of Prof. Bluhm at RWTH Aachen University.



(a) Bias-DAC output.

(b) Zoom-in of Bias-DAC output.

Figure 6.43: Bias-DAC output voltage V_S over whole range for refresh frequency f_R = 3.9 kHz at 6 K.

The corresponding DNL and integral non-linearity (INL) to Fig. 6.43 is given in Fig. 6.44. The y-axis range of the DNL plot can be halved from ±8 to ±4 LSB compared to previous DNL plot, which has been measured via the unity gain buffer (ref. to Fig. 6.33). This implies a non-negligible influence of the unity gain buffer to the Bias-DAC measurements. The intermediate steps range is now visible in the DNL plot due to its doubling of step size. The INL is dominated by the effect of coarse tuning ranges, which is arising due to offsets in the external reference voltages. The reference voltages are generated on a RT PCB by various commercially available low drop-out (LDO) voltage regulators (Texas Instruments TPS7A91) and their output voltages are defined by discrete components, i.e. resistors with different resistivity. These resistors are subject to mismatch and thus a reference voltage that should ideally be e.g. 500 mV is measured to 497.1 mV. This effect can be mitigated by tuning the reference voltages to their correct value if this is required for qubit operation.

The Bias-DAC power consumption at cryogenic temperatures is given in Table 6.7. 99.5 % of the Bias-DAC power is dissipated in digital circuitry and scales well with CMOS technology node. Moreover, the structure of the Bias-DAC was planned to be scalable at system level and digital control and timing signals are only generated once and can be distributed to multiple Bias-DACs (ref. to Fig. 3.8).

The DAC is compared with other cryogenic DACs in Table 6.8 and is filling the gap of an ultra-low power multi-channel DAC operating at cryogenic temperatures down to 6 K and will be tested in the lowest temperature stage of a dilution refrigerator, see section 7. This DAC enables a scalable solution for qubit biasing with an output voltage range of 1 V, consuming about 2.7 µW per channel. A larger output voltage range can be realized when all MOSFETs in the design are replaced with IO type MOSFETs, which will only require a minor design change. A total chip power consumption of well below 400 µW

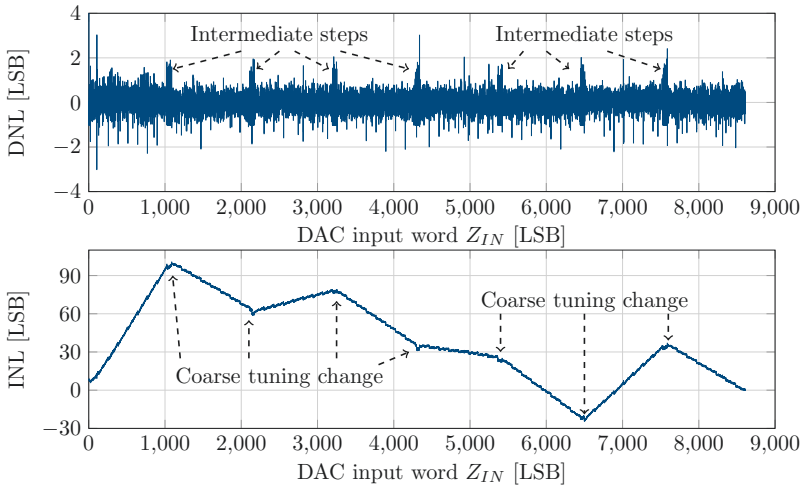


Figure 6.44: Bias-DAC DNL and INL for refresh frequency f_R = 3.9 kHz at 6 K.

Block	Power consumption
Charge-redistribution DAC & multiplexed output channel (ref. to Fig. 5.14)	77 nW
DAC reference voltages, all 8 summed (ref. to Fig. 5.14)	3 nW
DAC digital logic, memory & control (ref. to Fig. 5.14)	21 µW
Bias-DAC total	21.1 µW (2.63 µW per channel)
Clock buffer	4.3 µW
Total	25.4 µW (3.18 µW per channel)

Table 6.7: Bias-DAC power consumption for f_R = 3.9 kHz at 6 K. Adopted from [97].

(including I2C, and other non-active blocks on the chip) allows for placement of the Bias-DAC inside the mixing-chamber of a dilution refrigerator and directly bondwire to the qubit chip, thus bringing the bias voltage generation to the same temperature level.

	[94]	[95]	[96]	this work
Technology	0.5 µm SiGe BiCMOS	0.5 µm SiGe BiCMOS	0.5 µm SOS BiCMOS	65 nm CMOS
Temperature	93.15 K	93.15 K	4.2 K	6 K
Type	Current steering	Current steering	Current steering	Charge-redistribution
Resolution	12 bit	8 bit	10 bit	13 bit
Channel	1	1	1	8
Power	39.6 mW	3 mW	32.18 mW	21.1 µW
Supply	3.3 V	3.3 V	3 V	1.2 V & 2.5 V
Area	6.3 mm^2	0.25 mm^2	1.1 mm^2	0.14 mm^2

Table 6.8: Comparison of cryogenic DACs. Adopted from [97].

Chapter 7

Discussion and Outlook

Due to the ultra-low power consumption of $< 3\,\mu W$ per channel (ref. to Table 6.7), the SQuBiC1 IC can be placed at the lowest temperature stage of a dilution refrigerator. The Bias-DAC would provide locally generated bias voltages to the qubit in order to form the potential well and tune the qubit, as described in section 2.3.3.1. Preparations for such an experiment are currently ongoing and Fig. 7.1 shows the SQuBiC1 IC on the same interposer and wired to a qubit sample. The PCB is mounted to the mK sample holder of a dilution refrigerator and can be placed at the mK stage, see Fig. 3.1. Results of those experiments will show if the heavy filtering as it is currently applied to the biasing voltages of a qubit (ref. to Fig. 3.9), is reducing the output noise of the Bias-DAC enough to achieve good qubit fidelity rates. However, even for an increased noise level local qubit biasing could be demonstrated with a deteriorated gate fidelity.

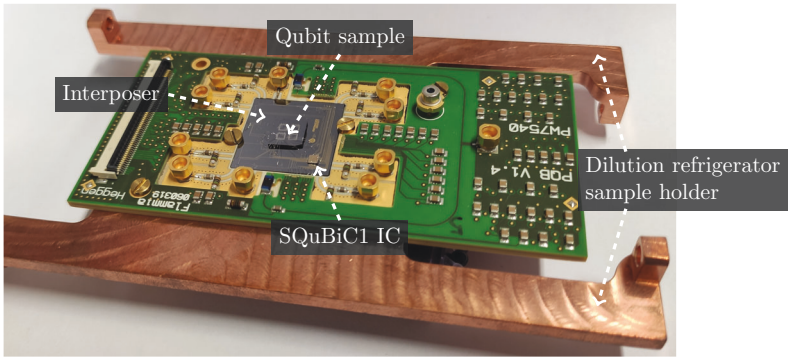


Figure 7.1: SQuBiC1 mounted on interposer and wired to a qubit.

Measurement results of the Bias-DAC revealed some singular non-monotonic steps in the DAC transfer characteristic (ref. to Fig. 6.43). Calibration is required in order to mitigate voltage jumps V_{jump} caused by voltage coarse tuning (ref. to Fig. 6.30). 99.5 % of the Bias-DAC power is being consumed in digital circuitry (ref. to Table 6.7). By incorporating on-chip digital assistance circuitry for calibration and moving towards a more advanced CMOS technology node, e.g. 22 nm FDSOI, all of the previously stated issues can be improved upon. Making it a natural choice for the next iteration of a Bias-DAC design. Additionally, the digital-assistance circuitry itself will also benefit from the implementation in an advanced CMOS technology. The general setup for calibration by digital-assistance is shown in Fig. 7.2. Although this is already included in

this work by calibration of the Bias-DAC with intermediate steps, which are stored in an off-chip look-up table (ref. to Fig. 6.31), current effort is undertaken to evaluate what the trade-offs of integrating more blocks into the IC are. This includes improvements or alternatives to the presented ΣΔ modulator as part of the analog-to-digital converter (ADC). First simulations of a multi-step binary-weighted capacitive digital-to-analog converter (MBDAC) with a subradix architecture and ordered element matching are showing promising results and implementation work is ongoing.

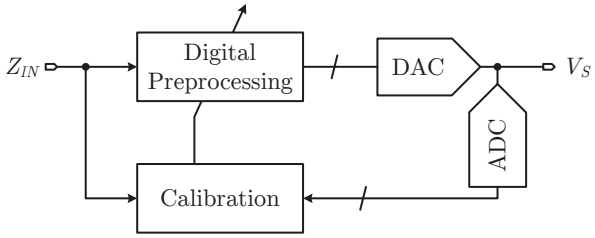


Figure 7.2: Using digital assistance circuitry to improve Bias-DAC performance.

The implemented bandgap could not be tuned into a good temperature compensated state of operation, due to the lack of tuning options. This behavior is contradicting all previous simulation results due to missing valid cryogenic device models. Future designs will include this option and are going to rely on better cryogenic device models, which are currently being developed in parallel conducted research.

Although operation of a linear regulator (LR) at cryogenic temperatures of 7 K with self-biasing via the bandgap (ref. to Fig. 4.1 and Fig. 6.16) has been proven, the undesired current flow seen for the LR output is rendering in-depth measurement and evaluation difficult. Therefore, an improved bandgap and LR design is being implemented at the moment, which is making use of the experience gained from this work.

Chapter 8

Summary

In this work the modeling, implementation and measurement of an ultra-low power digital-to-analog converter for qubit biasing (Bias-DAC), a bandgap reference, a linear regulator, an operational amplifier configured as unity gain buffer and an analog-to-digital ΣΔ modulator in a TSMC 65 nm technology operating at cryogenic temperatures from 6 K to 7 K are presented.

All circuit blocks are verified functional at these cryogenic temperatures. The bandgap reference is able to generate a tunable reference voltage and current at temperatures down to 7 K. This is the first demonstration of a PN-junction diode being used inside a cryogenic bandgap reference at such low temperatures, to the best of the author's knowledge. The bandgap reference is used to bias a linear regulator in voltage and current domain. The linear regulator itself is able to generate output voltages in the range from 1.3 V to 2 V from a 3 V supply and is able to drive a current of up to 16 mA at 7 K. This is a crucial building block for future cryogenic supply and reference voltage regulation inside of a dilution refrigerator.

The unity gain buffer and ΣΔ modulator are designed to enable measurement of the Bias-DAC. The unity gain buffer required an increase of supply voltage in order to operate over the full input range of 1 V, due to cryogenic effects arising at the measurement temperature of 6 K. Afterwards, the unity gain buffer is successfully used as element of a cryogenic buffer chain and enabled noise measurements of the Bias-DAC at cryogenic temperatures of 6 K. The ΣΔ modulator was also verified operational at 6 K and proposes a means of cryogenic on-chip analog-to-digital conversion. Future on-chip calibration of the Bias-DAC can make use of this modulator as part of a required ADC.

Focus of this work is the Bias-DAC, designed to operate simultaneously with a qubit and generate up to eight individually programmable biasing voltages within a 1 V output voltage range. Special emphasis is placed on systematic scalability of the Bias-DAC in order to bias an increasing number of qubits. An ultra-low power consumption of $< 3\,\mu W$ per channel is achieved and allows for placement at the lowest temperature stage of a dilution refrigerator in close proximity to the qubit at 100 mK. The proposed coarse tuning of reference voltages lowered the power consumption and increased the DAC resolution from 10 bit to 13 bit. A mitigation technique is implemented to avoid arising voltage jumps in the DAC transfer characteristic, i.e. adding intermediate DAC steps. This was verified by measurement at a cryogenic temperature of 6 K.

The Bias-DAC constitutes a scalable solution to locally bias an increasing number of qubits, while staying within the power budget of a dilution refrigerator, i.e. < 1 mW.

Bibliography

[1] Frank Arute et al. “Quantum supremacy using a programmable superconducting processor”. In: *Nature* 574.7779 (Oct. 2019), pp. 505–510. DOI: 10.1038/s41586-019-1666-5.

[2] L. M. K. Vandersypen et al. “Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent”. In: *npj Quantum Information* 3.1 (July 2017). DOI: 10.1038/s41534-017-0038-y.

[3] Pascal Cerfontaine. “High-fidelity single- and two-qubit gates for two-electron spin qubits”. en. PhD thesis. 2019, pp. 2019–. DOI: 10.18154/RWTH-2019-09348.

[4] Heinrich Klar and Tobias Noll. *Integrierte Digitale Schaltungen*. Springer Berlin Heidelberg, 2015. DOI: 10.1007/978-3-540-69017-7.

[5] Prof. Rainer Waser. *Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices*. Ed. by Prof. Rainer Waser. Third edition. Wiley-VCH, 2012. ISBN: 978-3-527-40927-3.

[6] Ramamurti Shankar. *Principles of Quantum Mechanics*. Second Edition. Springer Science+Business Media, 1994. ISBN: 978-0-306-44790-7.

[7] M. Nielsen and I. Chuang. *Quantum Computation and Quantum Information*. 10th Anniversary edition. Cambridge University Press, 2010. ISBN: 978-1-107-00217-3.

[8] N. D. Mermin. *Quantum Computer Science An Introduction*. Cambridge University Press, 2007. ISBN: 978-0-511-34258-5.

[9] David P. DiVincenzo. “The Physical Implementation of Quantum Computation”. In: *Fortschritte der Physik* 48.9-11 (July 2000), pp. 771–783. DOI: 10.1002/1521-3978(200009)48:9/11<771::aid-prop771>3.0.co;2-e.

[10] Colin D. Bruzewicz et al. “Trapped-ion quantum computing: Progress and challenges”. In: *Applied Physics Reviews* 6.2 (June 2019), p. 021314. DOI: 10.1063/1.5088164.

[11] Richard Jozsa. “Fidelity for Mixed Quantum States”. In: *Journal of Modern Optics* 41.12 (Dec. 1994), pp. 2315–2323. DOI: 10.1080/09500349414552171.

[12] Benjamin Schumacher. “Quantum coding”. In: *Physical Review A* 51.4 (Apr. 1995), pp. 2738–2747. DOI: 10.1103/physreva.51.2738.

[13] A. Uhlmann. “The "transition probability" in the state space of a $*$-algebra”. In: *Reports on Mathematical Physics* 9.2 (Apr. 1976), pp. 273–279. DOI: 10.1016/0034-4877(76)90060-4.

[14] Yeong-Cherng Liang et al. “Quantum fidelity measures for mixed states”. In: *Reports on Progress in Physics* 82.7 (June 2019), p. 076001. DOI: 10.1088/1361-6633/ab1ca4.

[15] Matthias Hübner. "Explicit computation of the Bures distance for density matrices". In: *Physics Letters A* 163.4 (Mar. 1992), pp. 239–242. DOI: 10.1016/0375-9601(92)91004-b.

[16] Dorit Aharonov, Michael Ben-Or, and Elad Eban. "Interactive Proofs For Quantum Computations". In: (Oct. 30, 2008). arXiv: 0810.5375v2 [quant-ph].

[17] Earl T. Campbell, Barbara M. Terhal, and Christophe Vuillot. "Roads towards fault-tolerant universal quantum computation". In: *Nature* 549.7671 (Sept. 2017), pp. 172–179. DOI: 10.1038/nature23460.

[18] Joseph Emerson, Robert Alicki, and Karol Życzkowski. "Scalable noise estimation with random unitary operators". In: *Journal of Optics B: Quantum and Semiclassical Optics* 7.10 (Sept. 2005), S347–S352. DOI: 10.1088/1464-4266/7/10/021.

[19] Lars R. Schreiber and Hendrik Bluhm. "Silicon comes back". In: *Nature Nanotechnology* 9.12 (Oct. 2014), pp. 966–968. DOI: 10.1038/nnano.2014.249.

[20] Ady Stern. "Anyons and the quantum Hall effect—A pedagogical review". In: *Annals of Physics* 323.1 (Jan. 2008), pp. 204–249. DOI: 10.1016/j.aop.2007.10.008.

[21] Ananda Roy and David P. DiVincenzo. "Topological Quantum Computing". In: *Topological Quantum Computing* (Jan. 18, 2017). arXiv: 1701.05052v1 [quant-ph].

[22] Chetan Nayak et al. "Non-Abelian Anyons and Topological Quantum Computation". In: *Rev. Mod. Phys. 80, 1083 (2008).* (July 12, 2007). DOI: 10.1103/RevModPhys.80.1083. arXiv: http://arxiv.org/abs/0707.1889v2 [cond-mat.str-el].

[23] Sophia Chen. *The Hunt For the Elusive Majorana Qubit.* Ed. by David Voss. 2018. URL: https://www.aps.org/publications/apsnews/201804/hunt.cfm (visited on 11/25/2019).

[24] Brian Wang. *Microsoft's Hunt for a Topological Quantum Computer Qubit.* 2019. URL: https://www.nextbigfuture.com/2019/11/microsofts-hunt-for-a-topological-quantum-computer-qubit.html (visited on 11/25/2019).

[25] W. Neuhauser et al. "Localized visible Ba^+ mono-ion oscillator". In: *Physical Review A* 22.3 (July 1980), pp. 1137–1140. DOI: 10.1103/physreva.22.1137.

[26] T. P. Harty et al. "High-Fidelity Preparation, Gates, Memory, and Readout of a Trapped-Ion Quantum Bit". In: *Physical Review Letters* 113.22 (Nov. 2014). DOI: 10.1103/physrevlett.113.220501.

[27] T. P. Harty et al. "High-Fidelity Trapped-Ion Quantum Logic Using Near-Field Microwaves". In: *Physical Review Letters* 117.14 (Sept. 2016). DOI: 10.1103/physrevlett.117.140501.

[28] C. J. Ballance et al. "High-Fidelity Quantum Logic Gates Using Trapped-Ion Hyperfine Qubits". In: *Physical Review Letters* 117.6 (Aug. 2016). DOI: 10.1103/physrevlett.117.060504.

[29] M. Brownnutt et al. "Ion-trap measurements of electric-field noise near surfaces". In: *Reviews of Modern Physics* 87.4 (Dec. 2015), pp. 1419–1482. DOI: 10.1103/revmodphys.87.1419.

[30] Philip Krantz et al. "A Quantum Engineer's Guide to Superconducting Qubits". In: *Applied Physics Reviews 6, 021318 (2019)* (Apr. 13, 2019). DOI: 10.1063/1.5089550.

[31] Morten Kjaergaard et al. "Superconducting Qubits: Current State of Play". In: *Annual Reviews of Condensed Matter Physics 11, 369-395 (2020)* (May 31, 2019). DOI: 10.1146/annurev-conmatphys-031119-050605. arXiv: 1905.13641v3 [quant-ph].

[32] B.D. Josephson. "Possible new effects in superconductive tunnelling". In: *Physics Letters* 1.7 (July 1962), pp. 251–253. DOI: 10.1016/0031-9163(62)91369-0.

[33] Ivar Giaever. "Electron Tunneling and Superconductivity". In: *Nobel Lecture* (Dec. 12, 1973).

[34] M. Fernando Gonzalez-Zalba. "Solid-state qubits". In: *Revista Espanola de Fisica, Vol 31, No 3, 4-8 (2017)* (Jan. 20, 2018). arXiv: 1801.06722v1 [cond-mat.mes-hall].

[35] Anasua Chatterjee et al. "Semiconductor Qubits In Practice". In: (May 13, 2020). arXiv: 2005.06564v1 [cond-mat.mes-hall].

[36] Juan P Dehollain et al. "Optimization of a solid-state electron spin qubit using gate set tomography". In: *New Journal of Physics* 18.10 (Oct. 2016), p. 103018. DOI: 10.1088/1367-2630/18/10/103018.

[37] C. H. Yang et al. "Silicon qubit fidelities approaching incoherent noise limits via pulse engineering". In: *Nature Electronics* 2.4 (Apr. 2019), pp. 151–158. DOI: 10.1038/s41928-019-0234-1.

[38] Jun Yoneda et al. "A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%". In: *Nature Nanotechnology* 13.2 (Dec. 2017), pp. 102–106. DOI: 10.1038/s41565-017-0014-x.

[39] Pascal Cerfontaine et al. "Closed-loop control of a GaAs-based singlet-triplet spin qubit with 99.5% gate fidelity and low leakage". In: (June 12, 2019). arXiv: 1906.06169v2 [cond-mat.mes-hall].

[40] Pascal Cerfontaine et al. "High-fidelity gate set for exchange-coupled singlet-triplet qubits". In: *Physical Review B* 101.15 (Apr. 2020). DOI: 10.1103/physrevb.101.155311.

[41] J. M. Elzerman et al. "Single-shot read-out of an individual electron spin in a quantum dot". In: *Nature* 430.6998 (July 2004), pp. 431–435. DOI: 10.1038/nature02693.

[42] J. R. Petta. "Coherent Manipulation of Coupled Electron Spins in Semiconductor Quantum Dots". In: *Science* 309.5744 (Sept. 2005), pp. 2180–2184. DOI: 10.1126/science.1116955.

[43] R. Hanson et al. "Spins in few-electron quantum dots". In: *Reviews of Modern Physics* 79.4 (Oct. 2007), pp. 1217–1265. DOI: 10.1103/revmodphys.79.1217.

[44] Hendrik Bluhm and Lars R. Schreiber. "Semiconductor Spin Qubits — A Scalable Platform for Quantum Computing?" In: *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, May 2019. DOI: 10.1109/iscas.2019.8702477.

[45] Alexander V. Khaetskii, Daniel Loss, and Leonid Glazman. "Electron Spin Decoherence in Quantum Dots due to Interaction with Nuclei". In: *Physical Review Letters* 88.18 (Apr. 2002). DOI: 10.1103/physrevlett.88.186802.

[46] Wenxian Zhang et al. "Hyperfine interaction induced decoherence of electron spins in quantum dots". In: *Physical Review B* 74.20 (Nov. 2006). DOI: 10.1103/physrevb.74.205313.

[47] Sandra Foletti et al. "Universal quantum control of two-electron spin quantum bits using dynamic nuclear polarization". In: *Nature Physics* 5.12 (Oct. 2009), pp. 903–908. DOI: 10.1038/nphys1424.

[48] Hendrik Bluhm et al. "Enhancing the Coherence of a Spin Qubit by Operating it as a Feedback Loop That Controls its Nuclear Spin Bath". In: *Physical Review Letters* 105.21 (Nov. 2010). DOI: 10.1103/physrevlett.105.216803.

[49] Jeremy Levy. "Universal Quantum Computation with Spin-1/2Pairs and Heisenberg Exchange". In: *Physical Review Letters* 89.14 (Sept. 2002). DOI: 10.1103/physrevlett.89.147902.

[50] Tim Botzem. "Kohärenz und hochpräzise Kontrolle von Zweielektronen-Spinqubits in GaAs Quantenpunkten". en. PhD thesis. 2017, pp. 2017–. DOI: 10.18154/RWTH-2017-04410.

[51] Pascal Cerfontaine et al. "High-Fidelity Single-Qubit Gates for Two-Electron Spin Qubits in GaAs". In: *Physical Review Letters* 113.15 (Oct. 2014). DOI: 10.1103/physrevlett.113.150501.

[52] C. G. Almudever et al. "The engineering challenges in quantum computing". In: *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2017*. IEEE, Mar. 2017. DOI: 10.23919/date.2017.7927104.

[53] Julian D. Teske et al. "A machine learning approach for automated fine-tuning of semiconductor spin qubits". In: *Applied Physics Letters* 114.13 (Apr. 2019), p. 133102. DOI: 10.1063/1.5088412.

[54] T. F. Watson et al. "A programmable two-qubit quantum processor in silicon". In: *Nature* 555.7698 (Feb. 2018), pp. 633–637. DOI: 10.1038/nature25766.

[55] M. Veldhorst et al. "A two-qubit logic gate in silicon". In: *Nature* 526.7573 (Oct. 2015), pp. 410–414. DOI: 10.1038/nature15263.

[56] W. Huang et al. "Fidelity benchmarks for two-qubit gates in silicon". In: *Nature* 569.7757 (May 2019), pp. 532–536. DOI: 10.1038/s41586-019-1197-0.

[57] Daniel Loss and David P. DiVincenzo. "Quantum computation with quantum dots". In: *Physical Review A* 57.1 (Jan. 1998), pp. 120–126. DOI: 10.1103/physreva.57.120.

[58] D. M. Zajac et al. "Scalable Gate Architecture for a One-Dimensional Array of Semiconductor Spin Qubits". In: *Physical Review Applied* 6.5 (Nov. 2016). DOI: 10.1103/physrevapplied.6.054013.

[59] Tom Struck et al. "Low-frequency spin qubit energy splitting noise in highly purified 28Si/SiGe". In: *npj Quantum Information* 6.1 (May 2020). DOI: 10.1038/s41534-020-0276-2.

[60] Rodney Van Meter and Clare Horsman. "A blueprint for building a quantum computer". In: *Communications of the ACM* 56.10 (Oct. 2013), p. 84. DOI: 10.1145/2494568.

[61] Rosario M. Incandela et al. "Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures". In: *IEEE Journal of the Electron Devices Society* 6 (2018), pp. 996–1006. DOI: 10.1109/jeds.2018.2821763.

[62] Arnout Beckers, Farzan Jazaeri, and Christian Enz. "Cryogenic MOSFET Threshold Voltage Model". In: *ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC)*. IEEE, Sept. 2019. DOI: 10.1109/essderc.2019.8901806.

[63] Ybe Creten et al. "An 8-Bit Flash Analog-to-Digital Converter in Standard CMOS Technology Functional From 4.2 K to 300 K". In: *IEEE Journal of Solid-State Circuits* 44.7 (July 2009), pp. 2019–2025. DOI: 10.1109/jssc.2009.2021918.

[64] G. Ghibaudo and F. Balestra. "Low temperature characterization of silicon CMOS devices". In: *Microelectronics Reliability* 37.9 (Sept. 1997), pp. 1353–1366. DOI: 10.1016/s0026-2714(97)00007-3.

[65] F. Balestra and G. Ghibaudo. "Brief review of the MOS device physics for low temperature electronics". In: *Solid-State Electronics* 37.12 (Dec. 1994), pp. 1967–1975. DOI: 10.1016/0038-1101(94)90064-7.

[66] Arnout Beckers et al. "Physical Model of Low-Temperature to Cryogenic Threshold Voltage in MOSFETs". In: *IEEE Journal of the Electron Devices Society* (2020), pp. 1–1. DOI: 10.1109/jeds.2020.2989629.

[67] Arnout Beckers, Farzan Jazaeri, and Christian Enz. "Characterization and Modeling of 28-nm Bulk CMOS Technology Down to 4.2 K". In: *IEEE Journal of the Electron Devices Society* 6 (2018), pp. 1007–1018. DOI: 10.1109/jeds.2018.2817458.

[68] T.-Y. Yang et al. "Quantum Transport in 40-nm MOSFETs at Deep-Cryogenic Temperatures". In: *IEEE Electron Device Letters* (2020), pp. 1–1. DOI: 10.1109/led.2020.2995645.

[69] B. Cretu et al. "Assessment of DC and low-frequency noise performances of triple-gate FinFETs at cryogenic temperatures". In: *Semiconductor Science and Technology* 31.12 (Nov. 2016), p. 124006. DOI: 10.1088/0268-1242/31/12/124006.

[70] P. Galy et al. "Cryogenic Temperature Characterization of a 28-nm FD-SOI Dedicated Structure for Advanced CMOS and Quantum Technologies Co-Integration". In: *IEEE Journal of the Electron Devices Society* 6 (2018), pp. 594–600. DOI: 10.1109/jeds.2018.2828465.

[71] Arnout Beckers et al. "Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures". In: *Solid-State Electronics* 159 (Sept. 2019), pp. 106–115. DOI: 10.1016/j.sse.2019.03.033.

[72] Bruna Cardoso Paz et al. "Integrated Variability Measurements of 28 nm FDSOI MOSFETs down to 4.2 K for Cryogenic CMOS Applications". In: *2020 IEEE 33rd International Conference on Microelectronic Test Structures (ICMTS)*. IEEE, May 2020. DOI: 10.1109/icmts48187.2020.9107906.

[73] S. Bonen et al. "Cryogenic Characterization of 22nm FDSOI CMOS Technology for Quantum Computing ICs". In: *IEEE Electron Device Letters* (2018), pp. 1–1. DOI: 10.1109/led.2018.2880303.

[74] Omar López-L et al. "Electrical and Thermal Characterization for SOI p-type FinFET down to Sub-Kelvin Temperatures". In: *2020 IEEE Latin America Electron Devices Conference (LAEDC)*. IEEE, Feb. 2020. DOI: 10.1109/laedc49063.2020.9072950.

[75] D. Boudier et al. "On quantum effects and low frequency noise spectroscopy in Si Gate-All-Around Nanowire MOSFETs at cryogenic temperatures". In: *2017 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*. IEEE, Apr. 2017. DOI: 10.1109/ulis.2017.7962578.

[76] H. Bohuslavskyi et al. "28nm Fully-depleted SOI technology: Cryogenic control electronics for quantum computing". In: *2017 Silicon Nanoelectronics Workshop (SNW)*. IEEE, June 2017. DOI: 10.23919/snw.2017.8242338.

[77] Bishnu Patra et al. "Characterization and Analysis of On-Chip Microwave Passive Components at Cryogenic Temperatures". In: *IEEE Journal of the Electron Devices Society* 8 (2020), pp. 448–456. DOI: 10.1109/jeds.2020.2986722.

[78] Bishnu Patra et al. "Cryo-CMOS Circuits and Systems for Quantum Computing Applications". In: *IEEE Journal of Solid-State Circuits* 53.1 (Jan. 2018), pp. 309–321. DOI: 10.1109/jssc.2017.2737549.

[79] Torsten Lehmann. "Cryogenic Support Circuits and Systems for Silicon Quantum Computers". In: *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, May 2019. DOI: 10.1109/iscas.2019.8702413.

[80] P. A. 'T Hart et al. "Characterization and Modeling of Mismatch in Cryo-CMOS". In: *IEEE Journal of the Electron Devices Society* 8 (2020), pp. 263–273. DOI: 10.1109/jeds.2020.2976546.

[81] M.J.M. Pelgrom, A.C.J. Duinmaijer, and A.P.G. Welbers. "Matching properties of MOS transistors". In: *IEEE Journal of Solid-State Circuits* 24.5 (Oct. 1989), pp. 1433–1439. DOI: 10.1109/jssc.1989.572629.

[82] Farzan Jazaeri et al. "A Review on Quantum Computing: From Qubits to Front-end Electronics and Cryogenic MOSFET Physics". In: *2019 MIXDES - 26th International Conference "Mixed Design of Integrated Circuits and Systems"*. IEEE, June 2019. DOI: 10.23919/mixdes.2019.8787164.

[83] Jeroen van Dijk et al. "Cryo-CMOS for Analog/Mixed-Signal Circuits and Systems". In: *2020 IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, Mar. 2020. DOI: 10.1109/cicc48029.2020.9075882.

[84] Harald Homulle and Edoardo Charbon. "Performance characterization of Altera and Xilinx 28 nm FPGAs at cryogenic temperatures". In: *2017 International Conference on Field Programmable Technology (ICFPT)*. IEEE, Dec. 2017. DOI: 10.1109/fpt.2017.8280117.

[85] Bishnu Patra et al. "19.1 A Scalable Cryo-CMOS 2-to-20GHz Digitally Intensive Controller for 4×32 Frequency Multiplexed Spin Qubits/Transmons in 22nm FinFET Technology for Quantum Computers". In: *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*. IEEE, Feb. 2020. DOI: 10.1109/isscc19947.2020.9063109.

[86] Harald Homulle, Fabio Sebastiano, and Edoardo Charbon. "Deep-Cryogenic Voltage References in 40-nm CMOS". In: *IEEE Solid-State Circuits Letters* 1.5 (May 2018), pp. 110–113. DOI: 10.1109/lssc.2018.2875821.

[87] J. van Staveren et al. "Voltage References for the Ultra-Wide Temperature Range from 4.2K to 300K in 40-nm CMOS". In: *ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC)*. IEEE, Sept. 2019. DOI: 10.1109/esscirc.2019.8902861.

[88] Yuanyuan Yang et al. "Cryo-CMOS Band-gap Reference Circuits for Quantum Computing". In: (Oct. 2, 2019). arXiv: 1910.01217v1 [physics.ins-det].

[89] Kushal Das, Torsten Lehmann, and Andrew S. Dzurak. "Sub-Nanoampere One-Shot Single Electron Transistor Readout Electrometry Below 10 Kelvin". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 61.10 (Oct. 2014), pp. 2816–2824. DOI: 10.1109/tcsi.2014.2321196.

[90] Burak Okcan et al. "A cryogenic analog to digital converter operating from 300 K down to 4.4 K". In: *Review of Scientific Instruments* 81.2 (Feb. 2010), p. 024702. DOI: 10.1063/1.3309825.

[91] Hongliang Zhao and Xinghui Liu. "A low-power cryogenic analog to digital converter in standard CMOS technology". In: *Cryogenics* 55-56 (May 2013), pp. 79–83. DOI: 10.1016/j.cryogenics.2013.03.005.

[92] Ahmet Suna, Ismail Cevik, and Mustafa Berke Yelten. "A High Speed 180 NM CMOS Cryogenic SAR ADC". In: *2018 18th Mediterranean Microwave Symposium (MMS)*. IEEE, Oct. 2018. DOI: 10.1109/mms.2018.8611968.

[93] Burak Okcan, Georges Gielen, and Chris Van Hoof. "A third-order complementary metal–oxide–semiconductor sigma-delta modulator operating between 4.2 K and 300 K". In: *Review of Scientific Instruments* 83.2 (Feb. 2012), p. 024708. DOI: 10.1063/1.3681781.

[94] Yuan Yao et al. "A 12-Bit Cryogenic and Radiation-Tolerant Digital-to-Analog Converter for Aerospace Extreme Environment Applications". In: *IEEE Transactions on Industrial Electronics* 55.7 (July 2008), pp. 2810–2819. DOI: 10.1109/tie.2008.924174.

[95] Zhenqi Chen and Fa Foster Dai. "A 3mW 8-Bit radiation-hardened-by-design DAC for ultra-wide temperature range from −180 °C to 120 °C". In: *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*. IEEE, May 2011. DOI: 10.1109/iscas.2011.5937736.

[96] M.T. Rahman and T. Lehmann. "A cryogenic DAC operating down to 4.2 K". In: *Cryogenics* 75 (Apr. 2016), pp. 47–55. DOI: 10.1016/j.cryogenics.2016.02.003.

[97] P. Vliex et al. "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications". In: *IEEE Solid-State Circuits Letters* 3 (2020), pp. 218–221. DOI: 10.1109/lssc.2020.3011576.

[98] Joseph C. Bardin et al. "29.1 A 28nm Bulk-CMOS 4-to-8GHz ¡2mW Cryogenic Pulse Modulator for Scalable Quantum Computing". In: *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*. IEEE, Feb. 2019. DOI: 10.1109/isscc.2019.8662480.

[99] S. J. Pauka et al. "A Cryogenic Interface for Controlling Many Qubits". In: (Dec. 3, 2019). arXiv: 1912.01299v1 [quant-ph].

[100] E. Schriek, F. Sebastiano, and E. Charbon. "A Cryo-CMOS Digital Cell Library for Quantum Computing Applications". In: *IEEE Solid-State Circuits Letters* (2020), pp. 1–1. DOI: 10.1109/lssc.2020.3017705.

[101] C. Degenhardt et al. "Systems Engineering of Cryogenic CMOS Electronics for Scalable Quantum Computers". In: *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, May 2019. DOI: 10.1109/iscas.2019.8702442.

[102] J.D. Meindl and J.A. Davis. "The fundamental limit on binary switching energy for terascale integration (TSI)". In: *IEEE Journal of Solid-State Circuits* 35.10 (Oct. 2000), pp. 1515–1516. DOI: 10.1109/4.871332.

[103] D. R. W. Yost et al. "Solid-state qubits integrated with superconducting through-silicon vias". In: *npj Quantum Information* 6.1 (July 2020). DOI: 10.1038/s41534-020-00289-8.

[104] Z. Charifoulline. "Residual Resistivity Ratio (RRR) Measurements of LHC Superconducting NbTi Cable Strands". In: *IEEE Transactions on Applied Superconductivity* 16.2 (June 2006), pp. 1188–1191. DOI: 10.1109/tasc.2006.873322.

[105] J. A. Alfaro-Barrantes et al. "Superconducting High-Aspect Ratio Through-Silicon Vias with DC-Sputtered Al for Quantum 3D integration". In: *IEEE Electron Device Letters* (2020), pp. 1–1. DOI: 10.1109/led.2020.2994862.

[106] C. H. Yang et al. "Operation of a silicon quantum processor unit cell above one kelvin". In: *Nature* 580.7803 (Apr. 2020), pp. 350–354. DOI: 10.1038/s41586-020-2171-6.

[107] L. Petit et al. "Universal quantum logic in hot silicon qubits". In: *Nature* 580.7803 (Apr. 2020), pp. 355–359. DOI: 10.1038/s41586-020-2170-7.

[108] L. Petit et al. "High-fidelity two-qubit gates in silicon above one Kelvin". In: (July 17, 2020). arXiv: 2007.09034 [cond-mat.mes-hall].

[109] R. Sarpeshkar, T. Delbruck, and C.A. Mead. "White noise in MOS transistors and resistors". In: *IEEE Circuits and Devices Magazine* 9.6 (Nov. 1993), pp. 23–29. DOI: 10.1109/101.261888.

[110] H. Banba et al. "A CMOS bandgap reference circuit with sub-1-V operation". In: *IEEE Journal of Solid-State Circuits* 34.5 (May 1999), pp. 670–674. DOI: 10.1109/4.760378.

[111] Ulrich Tietze. *Halbleiter-Schaltungstechnik*. Berlin Heidelberg: Springer Vieweg, 2016. ISBN: 9783662483541.

[112] Leo Rolff et al. "An Integrated Low Drop Out Regulator with Independent Self Biasing Start Up Circuit". In: *2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. IEEE, Dec. 2018. DOI: 10.1109/icecs.2018.8618043.

[113] R. Jacob Baker. *CMOS : circuit design, layout, and simulation*. Hoboken, N.J: IEEE Press/Wiley, 2010. ISBN: 0470881321.

[114] Mehdi Saberi et al. "Analysis of Power Consumption and Linearity in Capacitive Digital-to-Analog Converters Used in Successive Approximation ADCs". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 58.8 (Aug. 2011), pp. 1736–1748. DOI: 10.1109/tcsi.2011.2107214.

[115] R.E. Suarez, P.R. Gray, and D.A. Hodges. "All-MOS charge-redistribution analog-to-digital conversion techniques. II". In: *IEEE Journal of Solid-State Circuits* 10.6 (Dec. 1975), pp. 379–385. DOI: 10.1109/jssc.1975.1050630.

[116] F.-J. Wang, G.C. Temes, and S. Law. "A quasi-passive CMOS pipeline D/A converter". In: *IEEE Journal of Solid-State Circuits* 24.6 (1989), pp. 1752–1755. DOI: 10.1109/4.45017.

[117] J.A. Schoeff. "An inherently monotonic 12 bit DAC". In: *IEEE Journal of Solid-State Circuits* 14.6 (Dec. 1979), pp. 904–911. DOI: 10.1109/jssc.1979.1051296.

[118] R. Jacob Baker. *CMOS Mixed-Signal Circuit Design, Second Edition*. Unpublished, 2008. DOI: 10.13140/RG.2.1.5146.6005.

[119] Phillip E. Allen. *LECTURE 32–IMPROVED OPEN-LOOP COMPARATORS AND LATCHES*. 2016. URL: https://aicdesign.org/wp-content/uploads/2018/08/lecture32-150604.pdf (visited on 10/28/2020).

[120] Fernando Paixao Cortes, Alessandro Girardi, and Sergio Bampi. "Track-and-Latch Comparator Design Using Associations of MOS Transistors and Characterization". In: *2006 13th IEEE International Conference on Electronics, Circuits and Systems*. IEEE, Dec. 2006. DOI: 10.1109/icecs.2006.379647.

[121] Phillip E. Allen. *LECTURE 39–OVERSAMPLING ADCS –PART I*. 2016. URL: https://aicdesign.org/wp-content/uploads/2018/08/lecture39-140626.pdf (visited on 10/28/2020).

[122] Franco Maloberti. *Data Converters*. Springer-Verlag GmbH, May 15, 2007. ISBN: 9780387324869.

[123] Harald Homulle et al. "A reconfigurable cryogenic platform for the classical control of quantum processors". In: *Review of Scientific Instruments* 88.4 (Apr. 2017), p. 045103. DOI: 10.1063/1.4979611.

[124] F. Teyssandier and D. Prêle. “Commercially Available Capacitors at Cryogenic Temperatures”. In: *Ninth International Workshop on Low Temperature Electronics - WOLTE9*. Guaruja, Brazil, June 2010.

[125] ICEoxford. *Eden DRY ICE 10mK Dilution Cryostat*. Nov. 24, 2020. URL: https://www.iceoxford.com/a-DRY-ICE-10mK-Dilution-Cryostat.htm (visited on 11/24/2020).

[126] Stahl-Electronics. *BUF 0.12 Cryogenic CMOS Buffer Amplifier*. Ed. by Dr. Stefan Stahl. Jan. 1, 2019. URL: https://www.stahl-electronics.com/bilder/Datasheet_CryoAmp_BUF_V2-1.pdf (visited on 11/25/2020).

Curriculum Vitae

Patrick N. Vliex

Academic Degree	Master of Science in Electrical Engineering
Date of Birth	12.01.1992
Place of Birth	Aachen

Professional Experience

since 01/2021	Postdoc at Central Institute of Engineering, Electronics and Analytics, Electronic Systems (ZEA-2) – Forschungzentrum Jülich GmbH, Jülich, Germany
01/2017 - 12/2020	Doctoral Researcher at Central Institute of Engineering, Electronics and Analytics, Electronic Systems (ZEA-2) – Forschungzentrum Jülich GmbH, Jülich, Germany
06/2016 - 10/2016	Internship at Intel Deutschland GmbH – RF Design Department, Duisburg, Germany
12/2014 - 05/2016	Research Assistant at Chair of Integrated Analog Circuits and RF Systems – RWTH Aachen University, Aachen, Germany

Education

10/2014 - 11/2016	Master of Science in Electrical Engineering, RWTH Aachen University, Aachen, Germany
10/2011 - 09/2014	Bachelor of Science in Electrical Engineering, RWTH Aachen University, Aachen, Germany
12/2014 - 05/2016	General Qualification for University Entrance (Allgemeine Hochschulreife), Inda-Gymnasium, Aachen, Germany

Publications and Conferences

IEEE Journal

P. Vliex et al., "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications," in IEEE Solid-State Circuits Letters, vol. 3, pp. 218-221, 2020, doi: 10.1109/LSSC.2020.3011576.

IEEE Proceedings

C. Degenhardt et al., "Systems Engineering of Cryogenic CMOS Electronics for Scalable Quantum Computers," 2019 IEEE International Symposium on Circuits and Systems (ISCAS), 2019, pp. 1-5, doi: 10.1109/ISCAS.2019.8702442.

C. Degenhardt, L. Geck, A. Kruth, P. Vliex and S. van Waasen, "CMOS Based Scalable Cryogenic Control Electronics for Qubits," 2017 IEEE International Conference on Rebooting Computing (ICRC), 2017, pp. 1-4, doi: 10.1109/ICRC.2017.8123682.

Invited Speaker

P. Vliex et al., "Scalable Quantum Bit Control (SQuBiC1) Cryogenic CMOS IC for Spin Qubit Control," IEEE 14th Workshop on Low Temperature Electronics (Wolte14), Virtual, Italy, April 2021

Speaker

P. Vliex et al., "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications," IEEE 47th European Solid-State Circuits Conference (ESSCIRC), Virtual, Grenoble, France, September 2021

P. Vliex et al., "Scalable Cryogenic CMOS Electronics for Spin Qubit Control," Silicon Quantum Electronics Workshop 2019, San Sebastián, Spain, October 2019

Conference Contribution

A. Artanov, D. Nielinger, P. Vliex et al. "Scalable Cryogenic CMOS Electronics for Spin Qubit Control," 695. WE-Heraeus-Seminar: Engineering a Scalable Quantum Information Processor, Bad Honnef, Germany, April 2019

P. Vliex et al., "Investigating CMOS Based Local Bias Voltage Generation for Solid-State Qubit Potential Well Creation," International Workshop on Silicon Quantum Electronics, Hillsboro, USA, August 2017

L. Geck, P. Vliex et al., "Investigating CMOS Based Local Control Electronics for Qubit Operation," Symposium zu Quantum Information, Aachen, Germany, July 2017

Master Thesis Supervision

P. Döll, „Modelling and design of CMOS digital assistance circuits for cryogenic DACs in quantum computing applications“. Master thesis, Integrated Analog Circuit and RF Systems, RWTH Aachen University, Aachen, Germany, March 2021

Band / Volume 61
Digital Signal Processing and Mixed Signal Control of Receiver Circuitry for Large-Scale Particle Detectors
P. Muralidharan (2020), xv, 109 pp
ISBN: 978-3-95806-489-8

Band / Volume 62
Development of Electromagnetic Induction Measurement and Inversion Methods for Soil Electrical Conductivity Investigations
X. Tan (2020), ix, 124 pp
ISBN: 978-3-95806-490-4

Band / Volume 63
Novel System Approach for a mm-range Precision Indoor Positioning System
R. Xiong (2020), xi, 144 pp
ISBN: 978-3-95806-517-8

Band / Volume 64
Quantitative investigation of group III-nitride interfaces by a combination of scanning tunneling microscopy and off-axis electron holography
Y. Wang (2021), 102 pp
ISBN: 978-3-95806-534-5

Band / Volume 65
Scalable Control Electronics for a Spin Based Quantum Computer
L. Geck (2021), xiv, 114, xv-xxxiii
ISBN: 978-3-95806-540-6

Band / Volume 66
DNA-capped silver nanoparticles for stochastic nanoparticle impact electrochemistry
L. Nörbel (2021), VI, 142 pp
ISBN: 978-3-95806-541-3

Band / Volume 67
Development, characterization, and application of intraretinal implants
V. Rincón Montes (2021), XII, 173 pp
ISBN: 978-3-95806-553-6

Band / Volume 68
Optogenetic and electrical investigation of network dynamics in patterned neuronal cultures
T. J. J. Hondrich (2021), x, 177 pp
ISBN: 978-3-95806-555-0

Band / Volume 69
Disentangling parallel conduction channels by charge transport measurements on surfaces with a multi-tip scanning tunneling microscope
S. Just (2021), xii, 225 pp
ISBN: 978-3-95806-574-1

Band / Volume 70
Nanoscale four-point charge transport measurements in topological insulator thin films
A. Leis (2021), ix, 153 pp
ISBN: 978-3-95806-580-2

Band / Volume 71
Investigating the Interaction between π-Conjugated Organic Molecules and Metal Surfaces with Photoemission Tomography
X. Yang (2021), xviii, 173 pp
ISBN: 978-3-95806-584-0

Band / Volume 72
Three-Dimensional Polymeric Topographies for Neural Interfaces
F. Milos (2021), 133 pp
ISBN: 978-3-95806-586-4

Band / Volume 73
Development, characterization, and application of compliant intracortical implants
K. Srikantharajah (2021), xiv, 155, xv-xvii pp
ISBN: 978-3-95806-587-1

Band / Volume 74
Modelling, implementation and characterization of a Bias-DAC in CMOS as a building block for scalable cryogenic control electronics for future quantum computers
P. N. Vliex (2021), xiv, 107, xv-xxviii pp
ISBN: 978-3-95806-588-8

Information
Band / Volume 74
ISBN 978-3-95806-588-8

Mitglied der Helmholtz-Gemeinschaft

JÜLICH
Forschungszentrum