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QSOLID

Quantum Computer in the Solid State

Scalable Cryogenic Qubit Control with Optimized CMOS Technologies

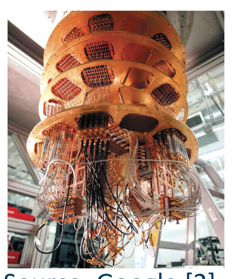
Motivation

Current approaches

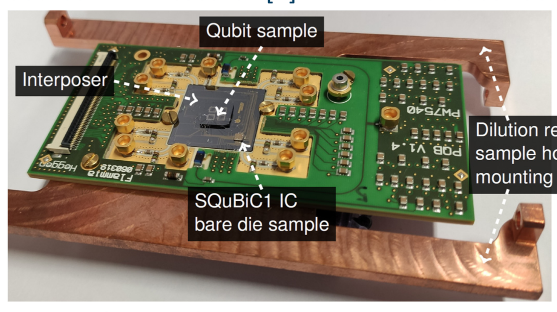
- 'Brute force' scaling to operate up to 50-100 qubits
- Further scaling very difficult

→ **Solution: INTEGRATED CIRCUITS (ICs)**

Source: IBM Research [1]



Source: Google [2]



Developed cryogenic IC at ZEA-2 [3]

Source: Forschungszentrum Jülich GmbH, ZEA-2

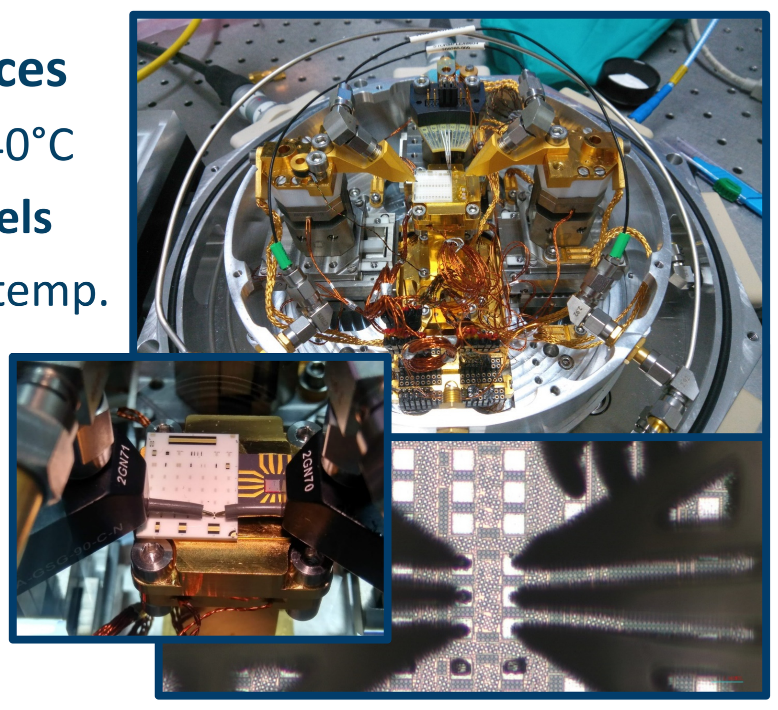
Scalable local cryogenic electronics

- Unique and **extreme operating challenges**
- Novel technology and circuit approaches
- **Scalability** is key performance indicator

Cryogenic Characterization at ZEA-2

Characterize commercial CMOS devices

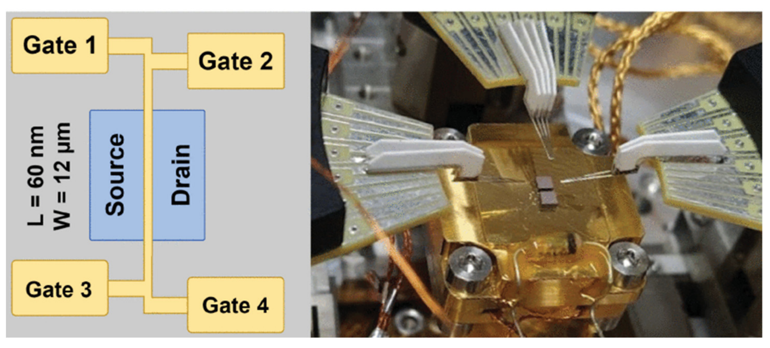
- Current device model range down to -40°C
- Enable development of **cryogenic models**
- **Setup for cryogenic measurement** for temp. down to 6 K (-267°C) of:
  - Transfer characteristic
  - RF performance (up to 20GHz)
  - Noise performance



Source: Forschungszentrum Jülich, ZEA-2

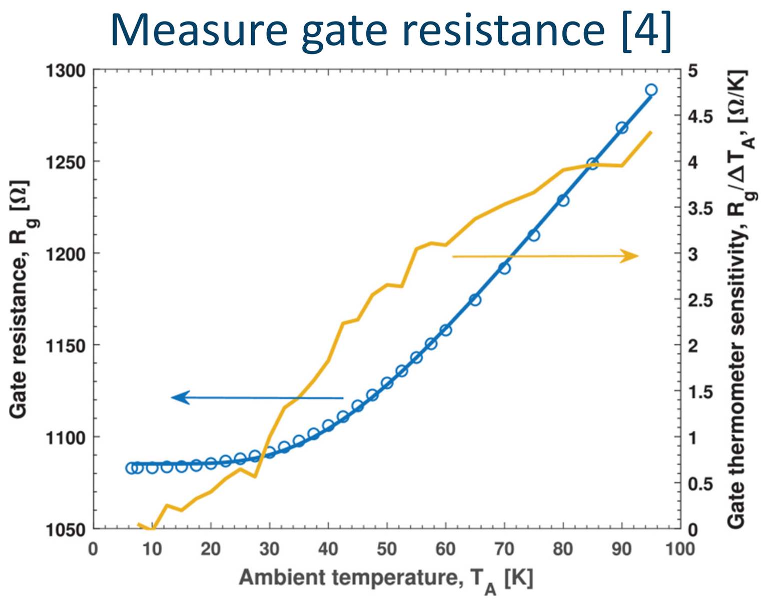
Self-heating effects in 65nm CMOS [4]

- Investigate real local temperature at CMOS device
- 4-point measurement of temperature-dependent gate resistance
- **Significant local heating is visible**

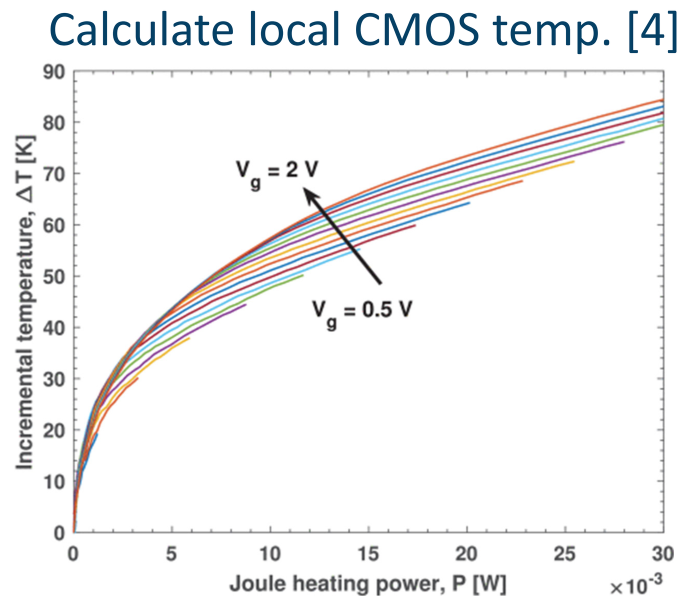


Source: Forschungszentrum Jülich, ZEA-2 [4]

Measure gate resistance [4]



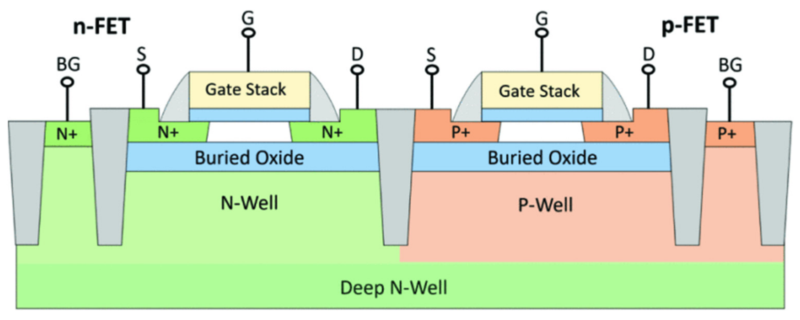
Calculate local CMOS temp. [4]



T5-2 Optimized Cryogenic Electronics

Tasks and partners of subproject T5-2

- Racyics, GF, ZEA-2 (FZJ) – **Test chip development**
- GF – **Wafer fabrication**
- IPMS, ZEA-2 (FZJ) – **Measure cryogenic device performance** by cryogenic needle probing setups
- AdMOS, Racyics – **Cryogenic device modeling** + PDK development



Source: IEEE (Authors: IPMS, GF) [6]

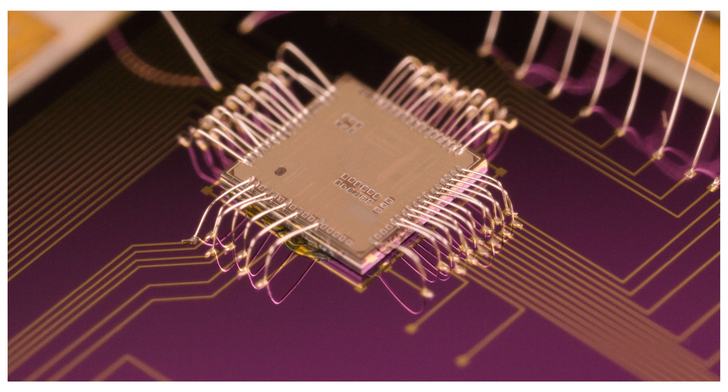
Improvements for state-of-the-art cryogenic electronics

- Create a **cryogenic** PDK library for GF 22nm FDSOI
  - Enable **cryogenic optimized** design and special circuit concepts
  - **Best performance** with **lowest power consumption**
- Improve **GF 22nm FDSOI technology for cryogenic operation**
  - Advance adaptive back-biasing technique of Racyics for cryogenic temp.
  - Develop cryogenic specific technology modifications
  - Decreased supply voltages and Ultra-Low-Voltage (ULV) circuitry

T5-4 Demonstrator Cryogenic Control

Tasks and partners of subproject T5-4

- PGI-11 (FZJ) – **Requirements**
- ZEA-2 (FZJ) – Concept and **design of an IC for qubit control** able to be operated locally **inside a dilution refrigerator** (previous designed IC shown right)
- GF – **IC fabrication**
- ZEA-2 (FZJ) – Measurement and **characterization of designed IC** at cryogenic temperatures
- PHI, IPE (KIT) – Integration and **test of designed IC with qubit**. Evaluation of qubit performance by cryogenic IC



Bonded IC (2x2mm²) of ZEA-2 [3] inside dilution refrigerator

Source: Forschungszentrum Jülich, Rene Otten & Paul Surrey

Scientific progress by cryogenic demonstrator IC

- Pave the way for fully scalable qubit control
- **Showcase cryogenic optimized design and special circuit concepts**
- **Demonstrate (technology) advancements achieved in T5-2**
  - Utilize the full potential of GF 22nm FDSOI in cryogenic environments

[1] IBM Research, "Inside an IBM Dilution Refrigerator", 4 Dec. 2015, URL: https://www.flickr.com/photos/ibm_research_zurich/26093909563/in/album-72157720168496793/ (visited on 14 April 2022)

[2] Mohseni, M., Read, P., Neven, H. *et al.* Commercialize quantum technologies in five years. *Nature* **543**, 171–174 (2017). https://doi.org/10.1038/543171a

[3] P. Vliex, "Modelling, implementation and characterization of a Bias-DAC in CMOS as a building block for scalable cryogenic control electronics for future quantum computers," Dissertation, Forschungszentrum Jülich GmbH, Zentralbibliothek, Verlag, Jülich, 2021. ISBN: 978-3-95806-588-8, doi: 10.18154/RWTH-2022-00302

[4] A. A. Artanov et al., "Self-Heating Effect in a 65 nm MOSFET at Cryogenic Temperatures," in IEEE Transactions on Electron Devices, vol. 69, no. 3, pp. 900-904, March 2022, doi: 10.1109/TED.2021.3139563.

[5] B. Cardoso Paz et al., "Performance and Low-Frequency Noise of 22-nm FDSOI Down to 4.2 K for Cryogenic Applications," in IEEE Transactions on Electron Devices, vol. 67, no. 11, pp. 4563-4567, Nov. 2020, doi: 10.1109/TED.2020.3021999.

[6] Q. H. Le et al., "W-Band Noise Characterization with Back-Gate Effects for Advanced 22nm FDSOI mm-Wave MOSFETs," 2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2020, pp. 131-134, doi: 10.1109/RFIC49505.2020.9218369.

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