Concept of mass-characterization for spin qubit devices on Si/SiGe

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Summary

Motivation:

- CMOS fabrication techniques enable large scale fabrication of semiconductor spin qubit devices [1]
- The number of fabricated devices necessitates a fast and efficient initial characterization of these devices.

Goals:

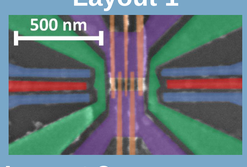
- Establish an automated characterization routine at 4 K
- Avoid gate hysteresis due to charge trapping [2]
- Use aggregated data to analyse fabrication and material

Devices

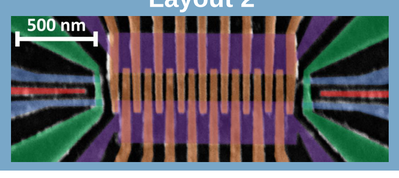
Device layout:

- Si/SiGe heterostructure creates a QW in the strained Si layer
- QuBus structure [3,4]:
  - 2 screening gates forming a 1D channel
  - finger gates perpendicular to the channel for control along the channel
- Sensing dot at each end of the QuBus
- Layout 1: 30 nm $Si_{0.7}Ge_{0.3}$
- Layout 2: 45 nm $Si_{0.7}Ge_{0.3}$

Layout 1

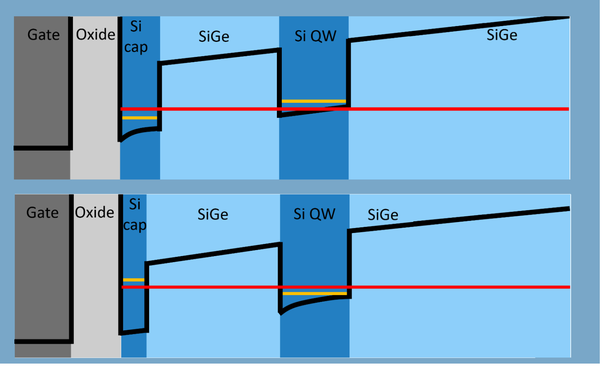


Layout 2

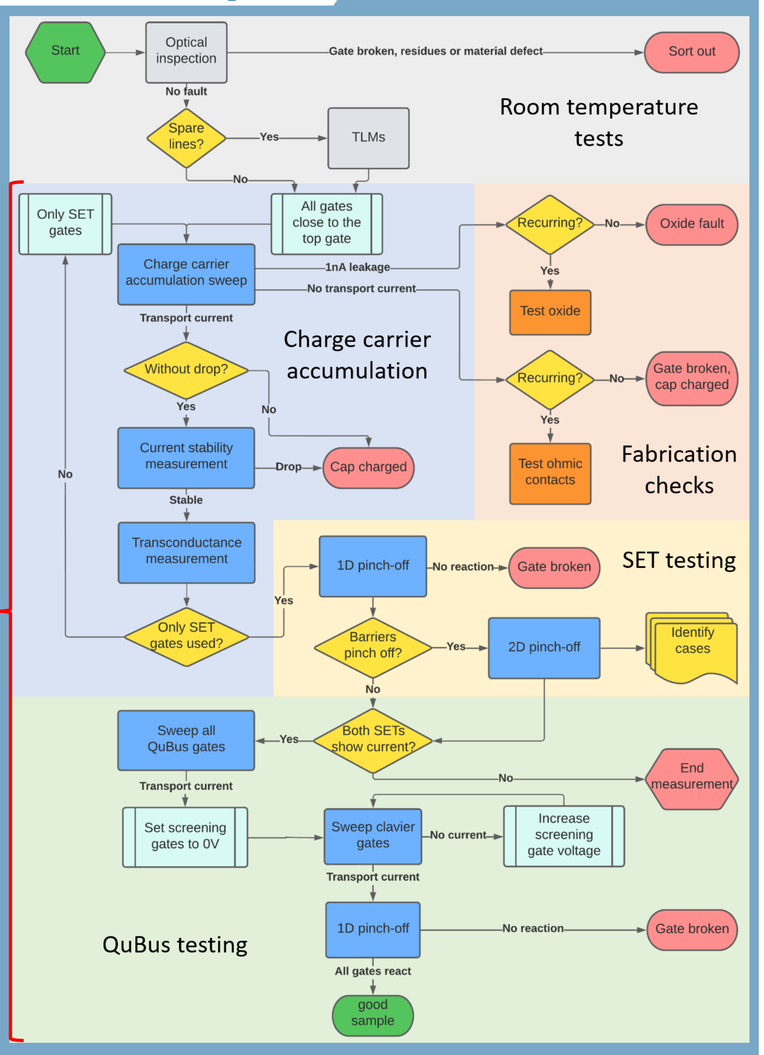


Charge trapping:

- Si cap layer creates a secondary QW
- Charges get trapped due to local cap thickness variation or high voltages



Concept



Room temperature:

- Inspection via an optical microscope

Charge carrier accumulation:

- Checking contact to QW
- Formation of conductive path under top gate without charge trapping

SET testing:

- Checking function of SET gates
- Obtainig pinch-off voltages for further measurements

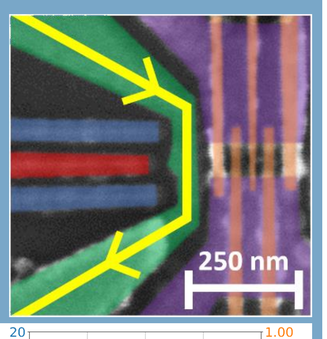
QuBus testing:

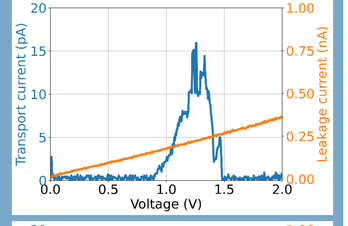
- Formation of the 1D channel
- Checking addressability of QuBus gates

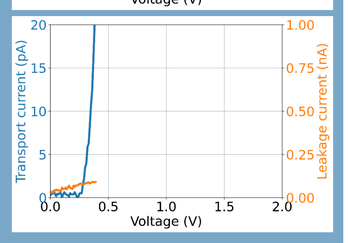
Accumulation

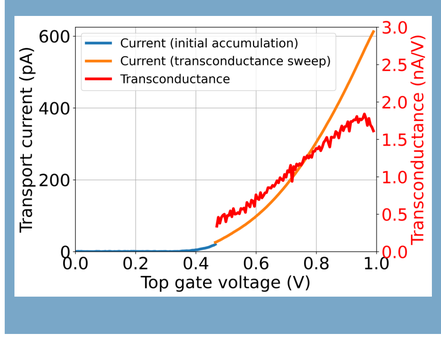
Initial accumulation:

- All gates close to the top gate are swept to form conductive path
- The sweep is terminated at a small transport current to prevent charge trapping
- Leakage through top gate is recorded to check oxide
- No transport current or a breakdown are signatures of charge trapping
- If normal accumulation occurs, the transport and leakage current are measured for 1 min to check stability of the conductive path









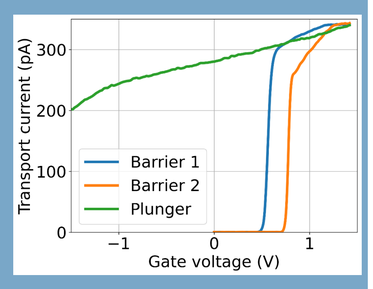
Transconductance:

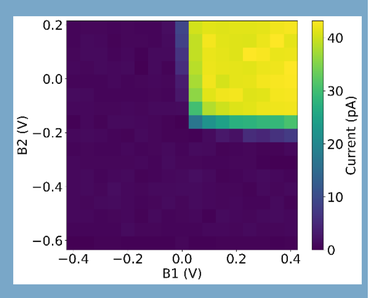
- $g_m = \frac{\Delta I}{\Delta V}$
- Current inflection point coincides with max. transconductance
- Max. voltage without charge trapping

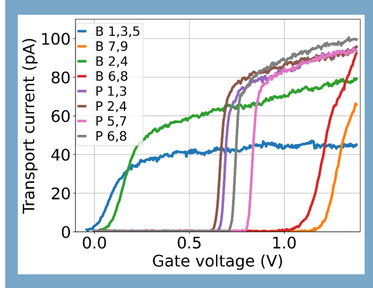
Gate testing

SET testing:

- Barrier and plunger gates are swept individually to check their addressability
- Cross coupling of barriers and their pinch-off voltage is investigated by a simultaneous sweep

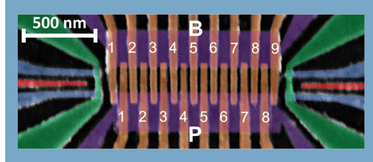






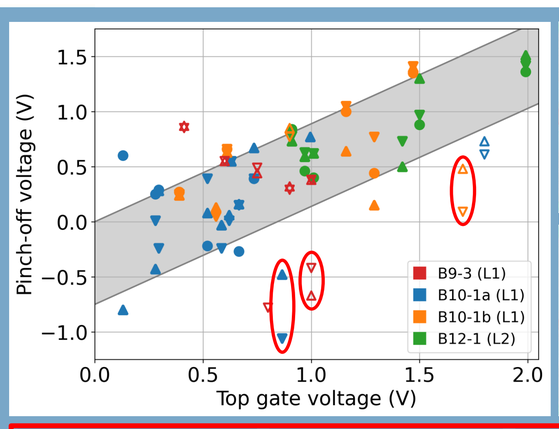
QuBus testing:

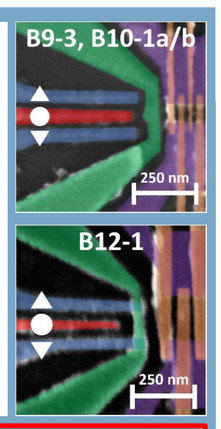
- The 1D channel is formed by the screening and finger gates (low as possible voltage on screening gates)
- Each finger gate is swept down individually to check if it pinches off the channel

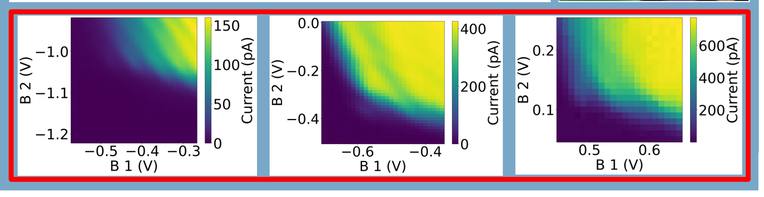


SET pinch-offs

- Linear dependence of the pinch-off voltages to the top gate voltage is observed
  - ➢ SET gates actively contribute to forming the conductive path
  - ➢ Top gate is not sufficient in this layout at the employed voltages
- 3 outliers were detected
  - ➢ SET gates only serve to pinch-off the transport current
  - ➢ The conductive path is mainly established by the top gate.
  - ➢ A deep quantum dot is formed and Coulomb oscillations are observed.







Conclusion

- The presented concept allows for an efficient and automated initial characterization at 4 K.
- Charge trapping is avoided as seen by an improvement of stable transport current from **30%** to **72%** of all devices compared to an older characterization routine
- The aggregated data can be used to evaluate the device design as seen in the pinch-off vs. top gate analysis.
- Next steps: Testing the concept on devices with different layout and materials to test its robustness

References

[1] A.M.J. Zwerver et al., Nat. Electronics **5.3**, 184 (2022).
[2] A. Wild et al., APL **100**, 143110 (2012).
[3] I. Seidler et al., arXiv:2108.00879 (2021).
[4] V. Langrock et al., arXiv:2202.11793 (2022).